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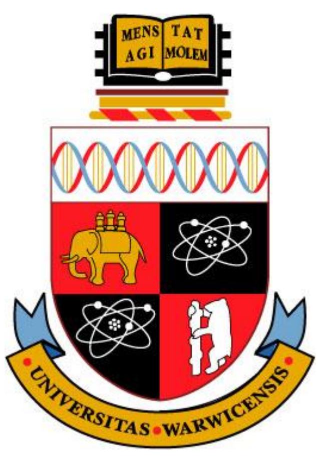

Strain-relaxed, high Ge content, SiGe layers grown on Si (100) substrate by Reduced Pressure- Chemical Vapour Deposition (RP-CVD)

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Submitted to the University of Warwick
in fulfilment of the requirements
for admission to the degree of
MSc by Research (in Physics)

September 26, 2012

Abstract

A different approach was taken to relieve strain from a high Germanium (Ge) content, Silicon-Germanium (SiGe) layers on a Silicon (Si) (100) substrate by growing a thin Ge under-layer between substrate and layer. The Ge under-layer acts as a strain reliving platform for further growth of a high Ge content SiGe layer to improve the structural quality of the sample by reducing the Root Mean Squared Roughness (R_{RMS}) and threading dislocation density (*TDD*).

The proposed structure involves the growth of thin $Si_{0.3}Ge_{0.7}$ and $Si_{0.5}Ge_{0.95}$ buffer layers of an average thickness of 350 nm grown on a Si (100) substrate and their structural qualities assessed. Experimental techniques include High Resolution X-Ray Diffraction, Atomic Force Microscopy, Transmission Electron Microscopy, and Defect Etching. All samples were shown to be fully relaxed and have a surface roughness between 1-8 nm. However, a threading dislocation density of 10^9 cm^{-2} was witnessed. Although these results are the first of their kind, further research into improving structural qualities is to be investigated in the future.

Table of Contents

1. Semiconductors 1
1.1 Semiconductor Industry 2
1.2 Silicon and Germanium – Properties 4
1.2.1 Miller Indices 7
1.3 Scope of Work 7
2 Epitaxial Growth 9
2.1 Reduced Pressure-Chemical Vapour Deposition (RP-CVD) 9
2.1.1 Growth Modes 12
2.1.2 Chemical Mechanical Polishing (CMP) 13
2.2 Strain Relaxation in Epitaxial Layers 14
2.2.1 Defects 14
2.2.2 Critical Thickness, h_c 17
2.3 Literature Review 20
2.3.1 Thick SiGe buffers 20
2.3.1.1 Wafer Bending 21
2.3.1.2 Constant Germanium Composition 21
2.3.1.3 Graded Composition 22
2.3.1.4 Linear Germanium Grading 24
2.3.2 Thin SiGe buffers 25
2.3.3 Annealing 27
3 Experimental Techniques 28
3.1 High Resolution X-Ray Diffraction (HR-XRD) 28
3.2 Atomic Force Microscopy (AFM) 31
3.3 Transmission Electron Microscopy (TEM) 33
3.3.1 Sample Preparation 34
3.4 Defect Etching (DE) 36
3.4.1 Determining Etch Depth 38
3.4.2 Modified Schimmel Reactivity 39
3.4.3 Sample Preparation 40
3.5 Scanning Electron Microscopy 41
4 Results and Discussion 44
4.1 $Si_{0.05}Ge_{0.95}$ 45

4.2 $Si_{0.3}Ge_{0.7}$ 49
4.3 Discussion of Samples being tested 52
5 Conclusion and Future Work 55
References 57

List of Figures

Figure 1: Over the years, TDD has declined gradually over the years for SiGe on Si layers by varying recipes and methods. Figure reproduced from ref. [5] without permission 4

Figure 2: Arrangement of atoms in a face- centred cubic structure. Figure modified from ref. [12] with permission 5

Figure 3: Band structure of Si at 300K 6

Figure 4: For the same cubic structure, (a) the ABCD plane intersects 5 atoms while (b) the ABEF plane intersects 6 atoms for the same crystal structure 7

Figure 5: All values are nominal and were measured to a calculated error by TEM 8

Figure 6: Path taken by precursors and dopants to obtain desired deposition. Figure reproduced from ref. [12] with permission. 9

Figure 7: Growth process of epitaxial layer on substrate by CVD. Figure reproduced from ref. [14] without permission 11

Figure 8: Exponential growth rates versus inverse temperatures by the use of dichlorosilane and Germane. Figure reproduced from ref. [17] without permission 11

Figure 9: Varying growth modes: (a) Volmer-Weber growth mode, (b) Frank-van der Merwe growth mode, and (c) Stranski-Krastanov growth mode. Figure reproduced from ref. [22] without permission 12

Figure 10: After drawing a closed loop along ABCD, points A and E are not equal and hence the burgers vector is the vector that equates the two points. Figure reproduced from ref. [26] without permission 15

Figure 11: (a) a foreign interstitial, (b) a line defect, (c)a self-interstitial, (d) a volume defect, (e) and a stacking fault. Figure reproduced from ref [28] without permission 16

Figure 12: Result of Dismukes et al. research. Figure reproduced from ref. [31] without permission 18

Figure 13: A network of misfit dislocations at interface. Image taken from sample 11-442 19

Figure 14: Determining the critical thickness for SiGe on Si. Figure reproduced from ref. [33] without permission 20

Figure 15: The bowing effect witnessed when growing thick SiGe layers on a Si Substrate. To view details of a patented process to reduce the bending effect, see ref. [34]. Figure reproduced from ref. [34] without permission 21

Figure 16: TEM image of the Si0.75Ge0.15 layer on a Si (100) substrate sample showing high value for TDD. Figure reproduced from ref. [52] without permission 22

Figure 17: Structure grown for Peng and Zhao et al. [35] 23

Figure 18: Forward graded SiGe on Si sample 24

Figure 19: (a) Network of TDs extending to the SiGe/Ge interface. (b) An increased magnification image of the SiGe/Ge interface. The interface shows the creation of MDs to relieve induced stress. Figure reproduced from ref. [37] without permission 26

Figure 20: Schematic setup of the HR- XRD kit. Figure reproduced from ref. [12] with permission .. 28

Figure 21: Reciprocal Space Mapping of Ge on Si sample. Figure obtained from ref. [12] with permission 30

Figure 22: An exaggerated tilt in a grown layer. Figure obtained from ref. [42] with permission 31

Figure 23: (a) raw data obtained from AFM. After collecting the raw data image, the sample was levelled giving (b). Finally, the background inaccuracy caused by a non-linear moving sample stage is removed by the subtraction of a 3rd degree polynomial from the image 32

Figure 24: Typical setup of the TEM used for sample imaging. Figure reproduced from ref. [43] without permission 34

Figure 25: Shows a strained Si layer with a TD. As time progresses the entire layer loses its thickness and the etchant eventually produces an etch pit at the TD. Figure reproduced from ref. [44] without permission 36

Figure 26: both Wright and Secco etchants reveal TDs better. However the "Cold" etchant was found to be "the most effective in obtaining unambiguous and uniform etch pit density figures..." Figure reproduced from ref. [46] without permission 38

Figure 27: Image of sample 11-439 showing 2 TDs combining to form 1 TD 39

Figure 28: A linearly declining relationship is observed for 20ml of the modified Schimmel etchant. 40

Figure 29: Basic setup of an SEM. Figure reproduced from ref. [47] without permission 41

Figure 30: (a) An SEM image showing the TD's after etching of a sample. (b) Shows the conversion of the SEM image into dots using the ImageJ program 42

Figure 31: (a) an unetched $Si_{0.05}Ge_{0.95}$ *and (b) an etched* $Si_{0.05}Ge_{0.95}$ 43

Figure 32: (a) the (004) and (b) (224) Miller planes for the 11-438 sample viewed in RSM shows the SiGe and Si peaks. The (004) peaks are vertically aligned indicating no tilt in the sample grown...... 46

Figure 33: % Relaxation of the top SiGe layer increases gradually for Si0.05Ge0.95. Error margins negligable........ 47

Figure 34: 10µm × 10µm AFM images for Si0.05Ge0.95: (a) without Ge under-layer (b) with 45nm Ge under-layer (c) with 87 nm Ge under-layer 48

Figure 35: R_{RMS} *and TDD vales show a similar relationship with increasing Ge seed layer thickness for* $Si_{0.05}Ge_{0.95}$ 48

Figure 36: the RSM of the 11-443 sample clearly shows the Ge seed layer as a faint, sky-blue line in the (a) (004) plane and (b) just below the SiGe over-layer in the (224) RSM 50

Figure 37: Increasing the Ge seed layer thickness causes an increase in relaxation for Si0.3Ge0.7. Error margins considered negligible 50

Figure 38: 10µm × 10µm AFM images for $Si_{0.3}Ge_{0.7}$*: (a) without Ge under-layer (b) with 52nm Ge under-layer (c) with 102 nm Ge under-layer* 51

Figure 39: the R_{RMS} *and TDD show a relatively similar trend similar trend for* $Si_{0.3}Ge_{0.7}$........ 52

Figure 40: (a) The Si0.3Ge0.7 structure is in registry with a substrate. While (b) a larger lattice constant layer grown on a similarly sized substrate would yield a higher TDD value due to a larger number of misfit dislocations 53

Acknowledgments

Special thanks to Dr. Maksym Myronov (for growth of all samples and all the help in data interpretation), Prof. David Leadley, John Halpin (for HR-XRD, TEM training and AFM), Dr. Vishal Shah (for Defect Etching), Dr. Neil Wilson (for AFM training), Dr. Richard Beanland (for TEM training), Steve York (for SEM training), Dr. Stephen Rhead, Catarina Casteleiro, Amna Hassan, "Ti" Van-Huy Nguyen.

1. Semiconductors

By definition, a semiconductor has an electrical conductivity somewhere between that of an insulator and a conductor. Quantitatively speaking however, semiconductors have a conductivity value between 10^{-8} to 10^{3} S/cm, which is a measure of how readily the semiconductor can conduct electricity.

The conductivity or insulation like property of a semiconducting material is dependent upon the doping levels of that material. *Doping* is the process of adding impurities to give a semiconducting material an increase in conductivity or insulation. An excess of electrons in the conduction band after doping means the material is an *n-type* material as it has more *negatively charged particles*, however the material is still considered charge neutral. A deficiency of electrons means that the material is a *p-type* material as it has fewer *negatively charged particles* and hence conduction is by positively charged holes. Temperature also plays a role in the conductivity of semiconductors.

Semiconductors have been the platform for the development of the electronics industry. The invention of the transistor is one example of this. Used to amplify or switch input signals, the transistor, which is widely used in modern circuit boards today, is made entirely of semiconducting materials, and recent advancement in SiGe technology enhanced transistor performance.

There is little doubt in saying that semiconductors are the main building block for all modern electronics. Whether the device is as sophisticated as an iPad or as simple as a traffic light signal, chances are it has a semiconductor built in it.

1.1 Semiconductor Industry

Consisting of 28% of the earth's crust, and the second most abundant element on earth, only after oxygen [1], it is little wonder that silicon is so widely used by the semiconductor industry. However, the history of semiconductors was greatly advanced, not by silicon, rather by the creation of the first transistor in germanium.

Although the first transistor ever to be built was made out of germanium in 1947, it was only 7 years later, when in 1954, Texas Instruments (TI) was the first company to ever produce pure silicon transistors. This transformed TI from an obscure start-up company to the giant it has become. By 2010 the semiconductor industry had grown to the tune of $298.3 Billion [2]. Table 1 shows the leading companies worldwide, jostling for position to obtain a bigger portion of that wealth:

Rank 2010	Rank 2011	Company	Country of Origin	2011 Revenue (million $ USD)	% changes from 2010	Market Share
1	1	Intel	USA	49,685	23.0%	15.9%
2	2	Samsung Electronics	South Korea	29,242	3.0%	9.3%
4	3	Texas Instruments	USA	14,081	8.4%	4.5%
3	4	Toshiba	Japan	13,362	2.7%	4.3%
5	5	Renesas Electronics Corporation	Japan	11,153	-6.2%	3.6%
9	6	Qualcomm	USA	10,080	39.9%	3.2%
7	7	STMicroelectronics	France & Italy	9,792	-5.4%	3.1%
6	8	Hynix	South Korea	8,911	-14.2%	2.8%
8	9	Micron Technology	USA	7,344	-17.3%	2.3%
10	10	Broadcom	USA	7,153	7.0%	2.3%
12	11	Advanced Micro Devices (AMD)	USA	6,483	2.2%	2.1%
13	12	Infineon Technologies	Germany	5,403	-14.5%	1.7%
14	13	Sony	Japan	5,153	-1.4%	1.6%
16	14	Freescale Semiconductor	USA	4,465	2.5%	1.4%
11	15	Elpida Memory	Japan	3,854	-40.2%	1.2%
17	16	NXP	Netherlands	3,838	-4.7%	1.2%
20	17	nVidia	USA	3,672	14.9%	1.2%
18	18	Marvell Technology Group	USA	3,488	-4.4%	1.1%
26	19	ON Semiconductor	USA	3,423	49.4%	1.1%
15	20	Panasonic Corporation	Japan	3,365	-32.0%	1.1%
Top 20				**203,907**	**3.5%**	**65.2%**
All other companies				**108,882**	**-1.1%**	**34.8%**
Total				**312,789**	**1.9%**	**100.0%**

Table 1: Top 20 Semiconductor Companies Worldwide, based on 2011 revenue [3].

Enhancing the electrical properties of transistors is not the only concern for the semiconductor industry. Gordon Moore, the co-founder of Intel Corporation, predicted that the number of transistors

on a circuit board would double every 2 years, this famous prediction is now known as Moore's Law. The prediction was found to be true as history has shown that transistors are in fact doubling in numbers approximately every 2 years on circuit boards. Therefore to satisfy Moore's Law the semiconductor industry is always looking for ways not only to add more transistors onto a circuit board, but also to reduce their size while maintaining, or preferably advancing, the electrical properties of the transistor.

Further research into fabricating better quality semiconductors by growing silicon-germanium (SiGe) on a silicon (Si) substrate was investigated around the time of the first transistor. However, the idea of actually growing SiGe on Si never materialised as it required a complex growth technique, or what is now known as *epitaxial growth*. It was not until 1975 that Erich Kasper, Jans-Horst Herzog and H. Kibbel managed to demonstrate the growth of SiGe on a Si substrate with a Ge content ranging from 0 to 15% by Molecular Beam Epitaxy (MBE) [4]. Their research was the starting point for future development into epitaxial growth.

Nowadays, fabricating thick buffer layers (roughly 1-12 μm in thickness) are being used to obtain a low *Root Mean Squared Roughness* (R_{RMS}), which is a measure of the surface roughness, and a low *threading dislocations density* (TDD) value, which is a measure of the abundance of defects within the structure. A buffer layer is a growth technique which involves growing a layer between the SiGe layer and the Si substrate. The basic concept behind having a buffer layer in the structure is to facilitate the difference in crystalline dimensions between the two layers grown, otherwise known as the *lattice mismatch* (see section 2.5) of the layers. Having a low lattice mismatch will lead to a low R_{RMS} and a low *TDD* value. Research over the past years was focused on the reduction of *TDD* by varying growth methods, such as linear [53] and step grading [18] techniques (see chapter 2) as shown in figure 2. Further on in time, research performed by Hollander et al. and Bucca et al. looked at varying growth conditions by adding helium ion implantation and varying annealing temperatures [19][25].

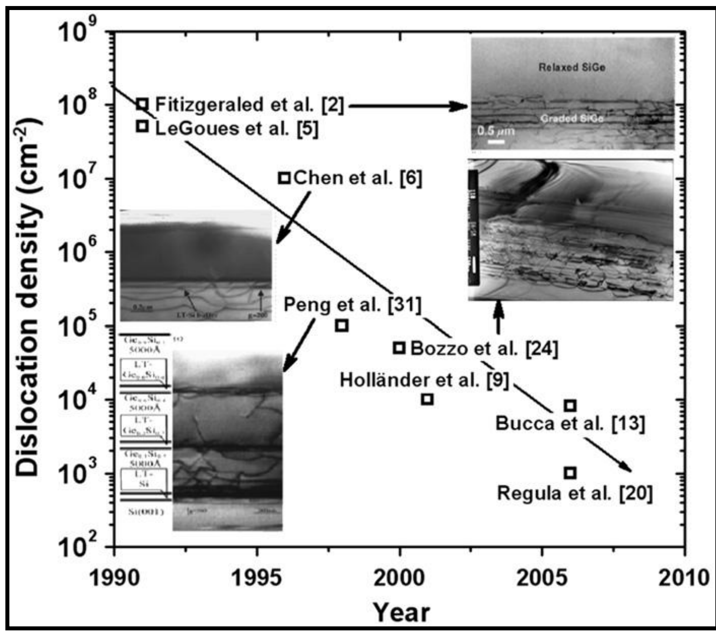


Figure 1: Over the years, TDD has declined gradually over the years for SiGe on Si layers by varying recipes and methods. Figure reproduced from ref. [5] without permission

Researchers are now starting to focus on the growth of thin buffer layers, less than 100 nanometers (nm) in thickness that look to have great potential in reducing the *TDD* to roughly 10^4 and the R_{RMS} to less than 1 nm. It is important to have a low R_{RMS} because a low R_{RMS} leads to lesser scattering of carriers which leads to greater mobility, a measure of electrical conductivity.

The application of SiGe buffer layers are far reaching. Recent research has shown how SiGe has been used as a platform to fabricate phototransistors which were up to 250% efficient and have a bandwidth of up to 5.3 GHz [8]. In addition, SiGe buffer layers can be used as a strain tuning tool that would lead to an increase in electron and hole mobilities [9].

1.2 Silicon and Germanium – Properties

Silicon and Germanium are crystalline materials which mean that the atoms are arranged periodically throughout the structure. The arrangement of atoms in silicon and germanium is a face-centred cubic

structure (see figure 3). Silicon and germanium both have 4 valence electrons and each of these electrons is covalently bonded with 4 adjacent electrons.

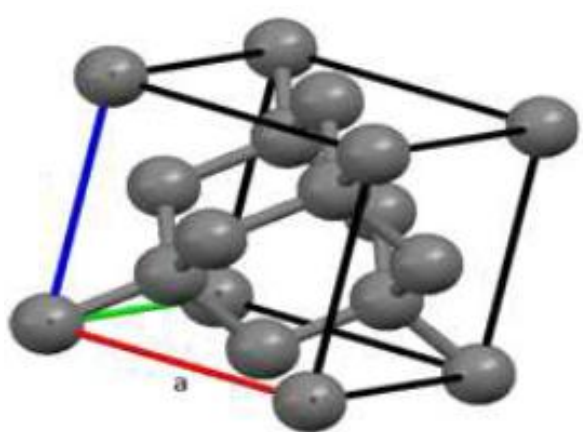


Figure 2: Arrangement of atoms in a face- centred cubic structure. Figure modified from ref. [12] with permission

The lattice constants, denoted *a*, is an important parameter as it gives the dimensions of the cubic structure. Silicon and germanium have a lattice constant of (a_{si}) 5.431 Å and (a_{ge}) 5.658 Å [6] respectively for room temperature. The atomic arrangement of Si and Ge consists of a 2 face-centred cubic (fcc) configuration in addition to a diagonal displacement of a ¼ of the cubic unit cell.

For epitaxial growth purposes, it is vital to know the lattice mismatch (l_m) between Si and Ge as this parameter is the foundation for the reduction of the *TDD* and R_{RMS}. Taking the values for lattice constants stated earlier, from equation 1 the lattice mismatch (l_m) between silicon and germanium is roughly 4.2%.

$$l_m = \frac{|a_{Si} - a_{Ge}|}{a_{Si}} \quad (1)$$

Both Si and Ge are *indirect bandgap materials*. This means that, unlike *direct bandgap materials*, electrons not only need the absorption of a photon of energy (E_G) for an electron to travel from the maximum valence band to the minimum of the conduction band, thereby allowing for the conduction

of electricity of the material, but also require a change in momentum (*k*). Figure 4 shows the band structure of Si.

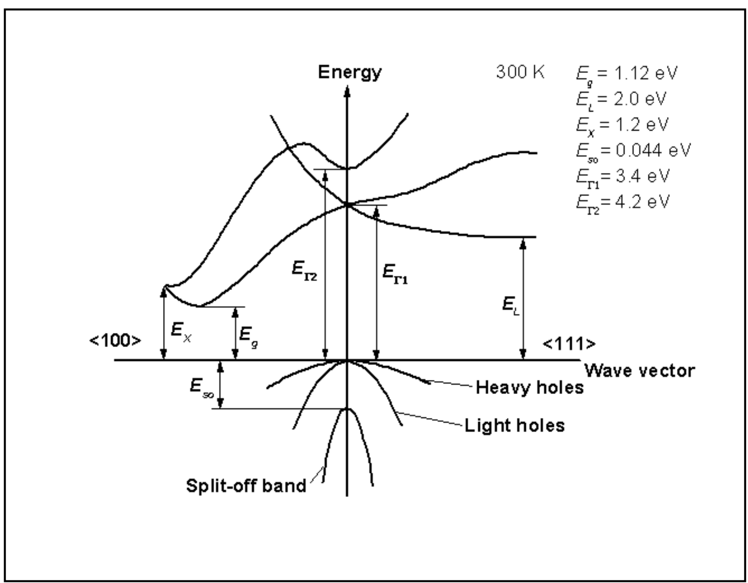


Figure 3: Band structure of Si at 300K

Other parameters such as material temperature and doping levels alter the bandgap energy of the material and hence can be engineered to perform specific tasks. Table 2 provides additional information for Si and Ge:

Element	Melting Point (°C)	Boiling Point (°C)	Density (g/cm^3)	Lattice Constant [6] (Å)	Carrier Mobilities (cm^2/V.s) [7]	
					Electron	Hole
Si	1410	2355	2.3	5.431	1350	480
Ge	938	2830	5.3	5.658	3900	1900

Table 2: Basic properties of Si and Ge [1]

1.2.1 Miller Indices

The Miller indices are a standard notation for representing planes intersecting a crystal structure. The indices are determined by: (1) Finding where the plane intercepts the x, y, & z axis, (2) taking the reciprocal of the 3 intercepts and then reducing these values to the smallest integer with the same ratio. And finally, to complete the notation, the direction of a plane is denoted in the form (hkl). Therefore, figure 5a has a (100) Miller index while figure 5b has a (110) Miller index.

Determining the crystal quality is directly dependent on the intersecting plane of the crystal. Figure 5 shows how 2 different planes on a face- centred cubic structure leads to a different understanding of the crystal's properties. It is therefore expected that comparing SiGe on Si substrates which have been grown on differently orientated substrates will lead to varying *TDD* and R_{RMS} values.

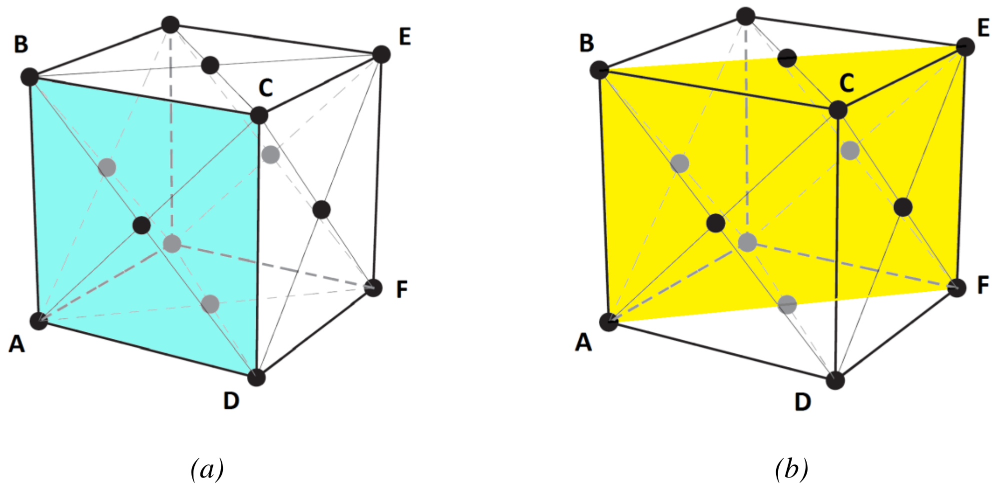


Figure 4: For the same cubic structure, (a) the ABCD plane intersects 5 atoms while (b) the ABEF plane intersects 6 atoms for the same crystal structure

1.3 Scope of Work

The research proposed was to investigate the structural quality of a batch of high Ge content, fully relaxed, thin SiGe buffer layers grown by Reduced Pressure-Chemical Vapour Deposition (RP-CVD).

Figure 6 shows the structure of the samples to be tested, along with the desired thickness of each layer.

Layer	Thickness
$Si_{0.05}Ge_{0.95}$	≈ 200 nm
Anneal	5 min. @ 800 ºC
$Si_{0.05}Ge_{0.95}$	≈ 100 nm
Ge	≈ (0,10,20,50,100) nm
p- -Si (1 0 0)	

Layer	Thickness
$Si_{0.3}Ge_{0.7}$	≈ 200 nm
Anneal	5 min. @ 800 ºC
$Si_{0.3}Ge_{0.7}$	≈ 100 nm
Ge	≈ (0,10,20,50,100) nm
p- -Si (1 0 0)	

Figure 5: All values are nominal and were measured to a calculated error by TEM

The sample recipe involves epitaxially growing a varying amount of Ge under-layer on a Si substrate. Subsequently, a 300 nm layer of SiGe is grown with an annealing process after 100 nm of the 300 nm SiGe layer. The samples to be tested were divided into 2 batches of 5 samples. The first batch contains a 95% Ge constant composition content in the SiGe layer; the second batch contains 70% Ge constant composition content. Both batches had a Ge under-layer of 0, 10, 20, 50, and 100 nm thick. There were a total of 10 samples to conduct the investigation.

The investigation will seek to verify whether thin SiGe buffer layers can live up to the structural qualities of thick SiGe buffer layers. Computing Strain Relaxation, *TDD* and R_{RMS} are the main parameters to be tested in determining the structural quality of the grown samples in this investigation. Additional research was done to determine layer characteristics by Transmission Electron Microscopy (TEM), and defect etching.

2 Epitaxial Growth

Epitaxial growth is the process in which a crystal structure is deposited on top of another crystalline structure. There are two main kinds of epitaxial growth, homoepitaxy and heteroepitaxy. Homoepitaxy is the growth of a crystal structure on a substrate structure of the same material, while in heteroepitaxy the crystal structures are different, as is the case in this research with the growth of SiGe on Si with a Ge under-layer.

There are mainly two methods used for epitaxial growth and they are by Reduced Pressure-Chemical Vapour Deposition (RP-CVD) or by Molecular Beam Epitaxy (MBE). All samples for this study were grown by RP-CVD.

2.1 Reduced Pressure-Chemical Vapour Deposition (RP-CVD)

First reported in 1957 by Sangster [10], RP-CVD is a process used to deposit an epitaxial layer on a substrate. The process works by passing gaseous precursors into a reduced pressure chamber, between 700-1 Torr [11], which reacts with a heated substrate to produce the desired layer deposition. Figure 7 shows the setup of the system.

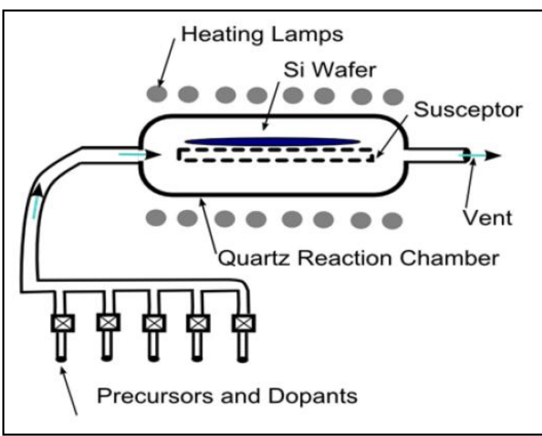


Figure 6: Path taken by precursors and dopants to obtain desired deposition. Figure reproduced from ref. [12] with permission.

Silane (Si_1H_4), Disilane (Si_2H_6) and Germane (GeH_4) are widely used precursors for CVD growth. While silane is used for high temperature growth, disilane is used for low temperature growth. During the chemical reaction of the precursors, by-products are produced and removed from the chamber to avoid the build-up of unnecessary compounds that can interfere with growth. Equations 2[13] and 3 show the decomposition of disilane and germane which were both used as precursors for the growth of all the samples in this research. During the final stage of decomposition, SiH breaks down to Si which is then deposited onto the substrate.

$$\begin{aligned} Si_2H_6(g) + - &\rightarrow \underline{Si}H_2 + SiH_4(g) \;** \\ SiH_4(g) + - &\rightarrow \underline{Si}H_2 + H_2(g) \;** \\ \underline{Si}H_2 + - &\rightarrow \underline{Si}H + \underline{H} \;** \end{aligned} \tag{2}$$

** *The sign '__' is referred to as the 'dangling bond', which means that the atom will covalently bond to neighbouring atoms to fill their valence shells.*

$$GeH_4 \rightarrow Ge + 2H_2 \tag{3}$$

The growth of the film is determined by surface diffusion and nucleation processes on the substrate interface. These parameters are dependent upon the Si substrate temperature, reactor pressure, and gas phase composition [14]. Figure 8 shows a schematic look into epitaxial growth by RP-CVD.

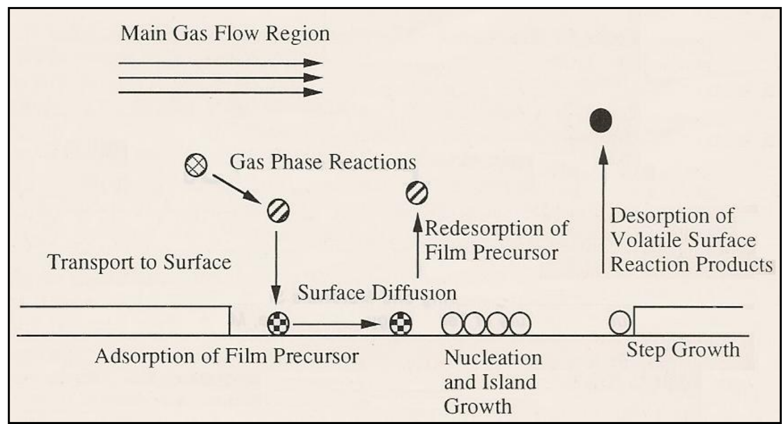


Figure 7: Growth process of epitaxial layer on substrate by CVD. Figure reproduced from ref. [14] without permission

Previous research has shown conformity in demonstrating a relationship between growth rates and substrate temperature with varying precursors such as silane (SiH_4), germane (GeH_4), and dichlorosilane ($SiCl_2H_2$) [15] [16] [17]. For the growth of thin SiGe layers, all samples in this investigation were grown at 450 °C (≈723K) to obtain a desirable growth rate. Samples were also annealed at 800°C but discussion on annealing will be delayed until later chapters.

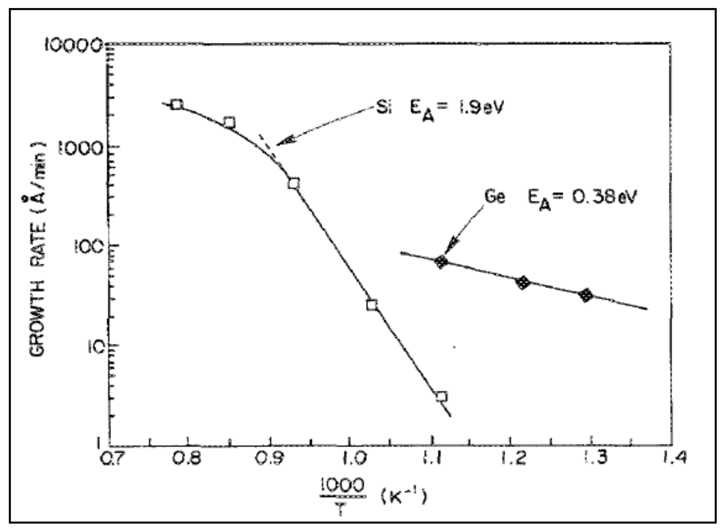


Figure 8: Exponential growth rates versus inverse temperatures by the use of dichlorosilane and Germane. Figure reproduced from ref. [17] without permission

2.1.1 Growth Modes

For epitaxial growth, much experimental work has shown that the growth of thin films on a substrate can proceed by 3 types of growth modes [21]. The first type, known as Volmer-Weber growth, involves the growth of 3D islands that eventually combine and form layered growth. The second growth mode is known as Frank-van der Merwe which involves the ordered growth of layer after layer. Finally, the Stranski-Krastanov growth mode is a mixture of the initial two techniques, where both ordered layer growth and 3D islanding is observed. Figure 10 shows all three growth modes.

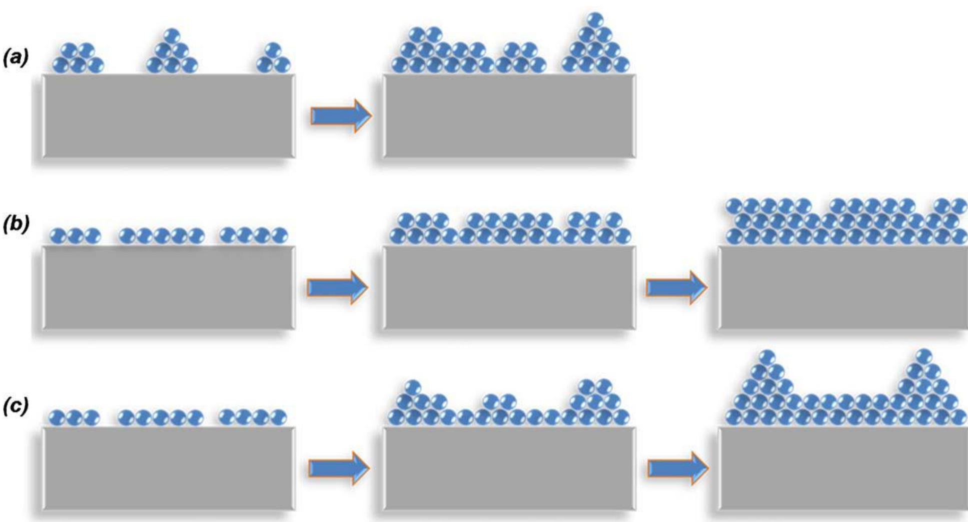


Figure 9: Varying growth modes: (a) Volmer-Weber growth mode, (b) Frank-van der Merwe growth mode, and (c) Stranski-Krastanov growth mode. Figure reproduced from ref. [22] without permission

Research has suggested that the favoured growth mode depends on the bonding energy of the deposited atoms with the substrate [22]. If the bonding energy is greater in atom-to-atom bonding than with atom-to-substrate, then Volmer-Weber growth mode is favoured. However a stronger bonding in atom-to-substrate will lead to Frank-van der Merwe growth. Stanski-Krastanov growth occurs after the bonding energy shifts favourably in the direction of atom-to-atom bonding when it was initially

favourable for atom-to-substrate bonding, and hence Stanski-Krastanov is a mixture of both growth modes.

2.1.2 Chemical Mechanical Polishing (CMP)

Before epitaxial growth can begin, Si wafers need to go through a long process of Chemical and Mechanical Polishing (CMP). This process starts after raw polysilicon is converted to Si wafers. For a detailed description for this conversion, see [23]. According to [24], Wafer processing involves slicing, lapping, etching, and wafer polishing (CMP), respectively. Below is a description of each technique:

Slicing: Si wafers in the shape of an ingot are sawed into circular discs. The wafer is then placed in a number of chemical baths to remove any unwanted stains on the wafer.

Lapping: During slicing, saw damage is prevalent in the wafer. Hence the wafer is placed in a lapping device which uses an abrasive on both sides of the wafer to remove any dirt and increase smoothness of the wafer.

Etching: During lapping, surface damage is probable and hence the wafers are placed in etching baths to remove any damage on the wafer surface. This process also promotes smoother and stronger wafer surfaces.

Wafer Polishing [23]: A polishing agent on a soft pad is pressed against a rotating Si wafer. The process not only acts as a simple mechanical interaction between the pad and wafer, but also a chemical reaction is induced into this process to create a suitable wafer surface.

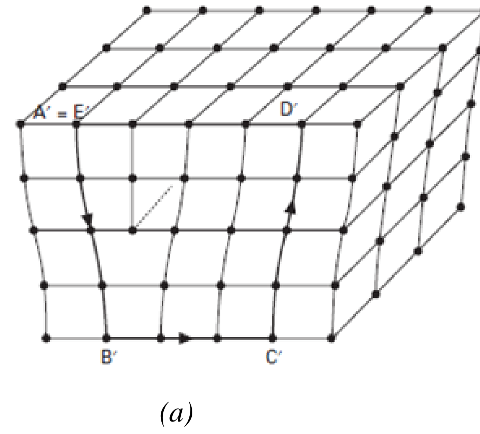
2.2 Strain Relaxation in Epitaxial Layers

2.2.1 Defects

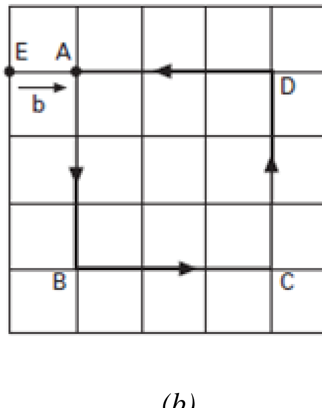
During crystal growth, defects form within the crystalline material. These defects locally interrupt the regular arrangement of atoms and alter the quality of the crystal. It is therefore necessary to reduce these defects to obtain better quality structures. Defects can generally be categorized into 4 main groups:

i) Line defects: Also referred to as threading dislocations (TDs) in this study, line defects are a result of misfit dislocations (MDs). When two dissimilar materials form an interface, MDs form to relive the induced stress caused by the lattice mismatch of the two materials. TDs are therefore an extension of a MD unless it reaches a surface. For a (100) material, TDs tend to travel towards the material surface at a 60° angle to relieve the induced stress.

The Dutch Physicist, Jan Burgers came up with a novel way of quantifying a line defect. The vector, known as the *Burgers vector*, denoted $\vec{b}$, determines the magnitude and direction of the line defect. Figure 13 explains how the vector is observed.



(a)



(b)

Figure 10: After drawing a closed loop along ABCD, points A and E are not equal and hence the burgers vector is the vector that equates the two points. Figure reproduced from ref. [26] without permission

ii) Point defects: There are two types of point defects. The first is when an atom is missing from the ordered arrangement of neighbouring atoms. This absence is known as a *vacancy*. The second is when an atom exists between the ordered arrangements of neighbouring atoms and is called a *self-interstitial*.

iii) Stacking faults: Occurs when the stacking order is interrupted. This happens when a layer is removed or added to the regular order of the layers which causes both the top and bottom layers to readjust their position to be in registry with the irregularly grown layer [27].

iv) Volume defects: Are caused by the introduction of excess impurities or dopants which exceeds the solubility of the impurity in the host element. This excess is precipitated from the host element which then leads to dislocations. Figure 14 shows all the different types of defects which occur during crystal growth.

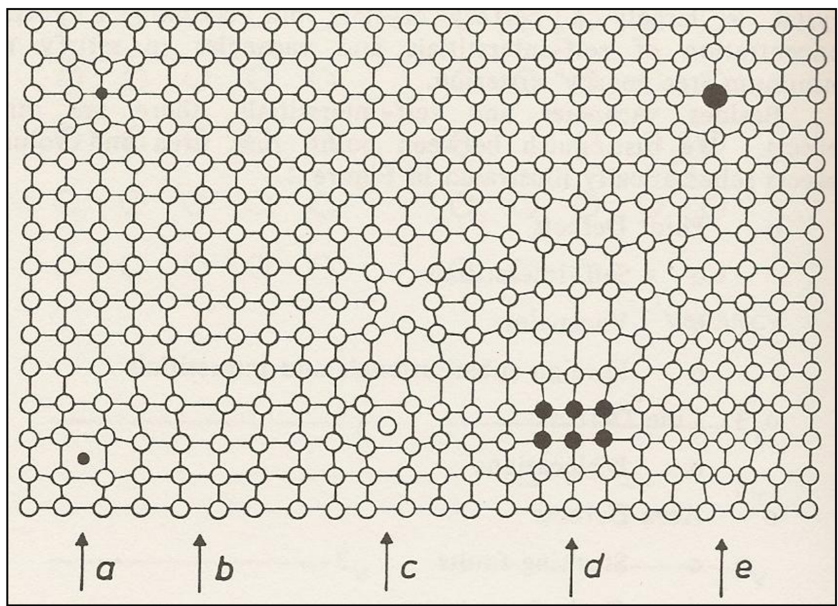


Figure 11: (a) a foreign interstitial, (b) a line defect, (c)a self-interstitial, (d) a volume defect, (e) and a stacking fault. Figure reproduced from ref [28] without permission

To obtain a better understanding of a crystal structure, it would be greatly advantageous to view the defects and calculate their abundance. According to D Hull and D J Bacon [29], defects can be viewed by 5 techniques:

1. Revealing dislocations at the sample's surface, known as *defect etching* (see section 3.5). This process involves revealing TDs by etching a sample to a certain depth and using a microscope to view and count the TDs.

2. By *Transmission Electron Microscopy* (see section 3.3) which involves using a high magnification microscope to view TDs.

3. By analysing diffracted x-rays incident on a sample surface which gives an understanding of defect location and abundance.

4. The use of field ion microscopy which images atoms at the surface of a sample and therefore reveals dislocations, in the sample structure.

5. The last technique is by decoration, which involves ‘decorating’ the sample with precipitate particles to see the network of dislocations.

Viewing defects in this study was confined to the first, two techniques.

2.2.2 Critical Thickness, h_c

To understand defect formation, an understanding of why misfit dislocations form needs to be discussed. The focus now turns to the lattice constant of a SiGe epitaxial layer. Equation 4 shows Vegard’s Law which says that there is a liner relationship between the lattice constant of an alloy (a_x) and alloy compositions (x).

$$a_x = x \cdot a_{si} + (1 - x)a_{Ge} \tag{4}$$

Recently however, there has been research which suggests that Vegard’s Law should be treated as an approximation, albeit a very good one [30]. Also et al. showed that the lattice constant of SiGe does not greatly deviate from Vegard’s Law [31].

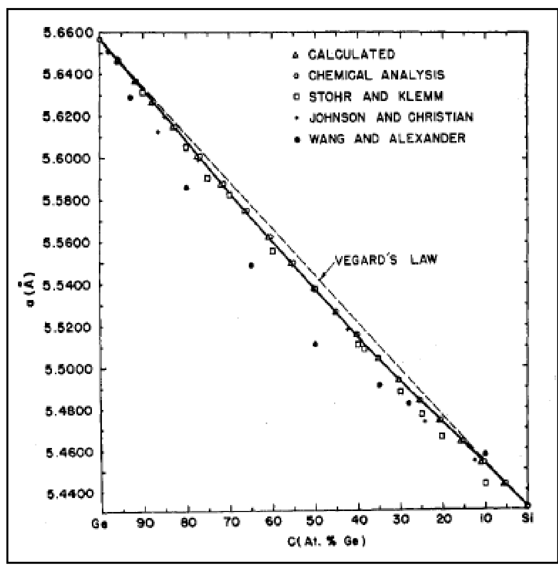


Figure 12: Result of Dismukes et al. research. Figure reproduced from ref. [31] without permission

Ignoring the negligible discrepancy in Vegard's Law and using the information provided in table 2 and equation 4, it can therefore be said that the growth of high Ge content SiGe layers, grown on a Si substrate, cannot be in perfect registry with the substrate as the SiGe layer has a larger lattice constant.

This would mean that the growth of a SiGe layer is initially psuedomorphic, meaning it is partially lattice-matched with the substrate, but eventually the induced strain energy due to the lattice mismatch gives way to the energy associated with relieving that strain by the creation of misfit dislocations. Figure 16 shows a network of misfit dislocations at the interface of a SiGe layer grown on a Ge seed layer, on top of a Si substrate.

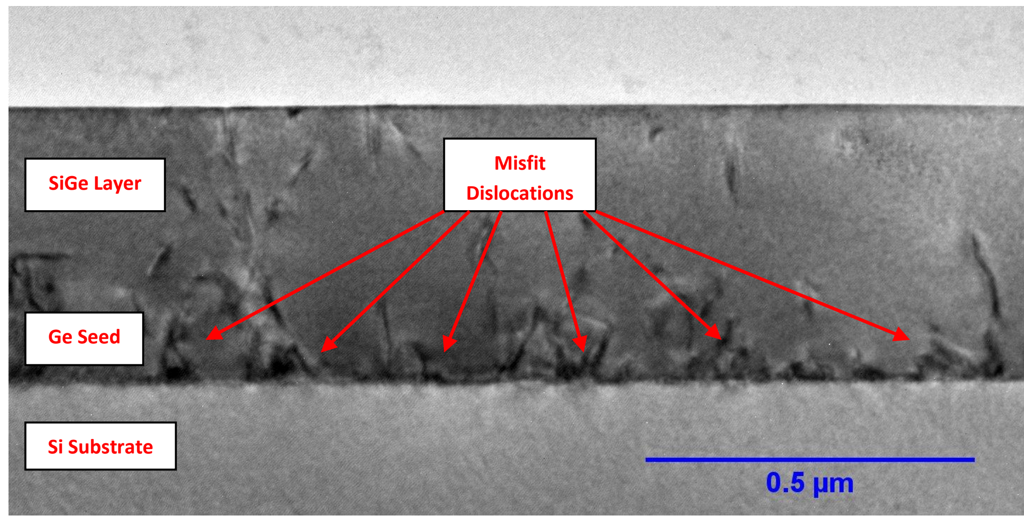


Figure 13: A network of misfit dislocations at interface. Image taken from sample 11-442

Since it is expected that misfit dislocations will exist at the interface, research was focused on better understanding when misfit dislocations start to form to obtain better quality structures. This led to the concept of *critical thickness*. Defined as:

> *"...the thickness above which a grown layer will partially or completely relax to its freestanding lattice constant by the creation of misfit dislocations...at the interface with the original substrate."* [32]

Much work has gone into determining the critical thickness of SiGe layers. A comprehensive study was performed by Bean et al. to determine the boundaries of the critical thickness for SiGe on Si substrates. Figure 17 below summarises the results obtained.

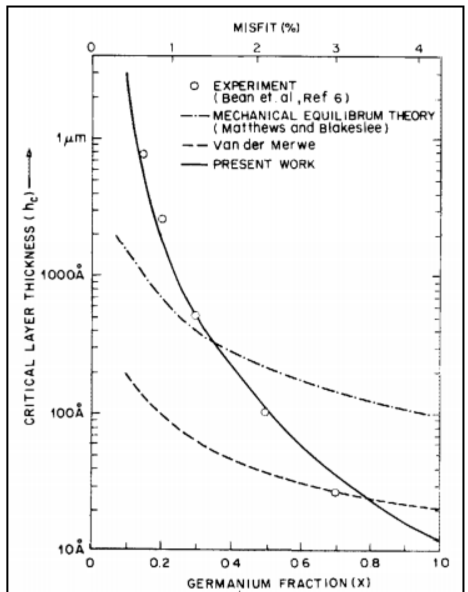


Figure 14: Determining the critical thickness for SiGe on Si. Figure reproduced from ref. [33] without permission

Equation 5 shows the People and Bean energy balance for relaxed SiGe with defects.

$$x = 2.01\sqrt{\frac{b}{h}\ln\left(\frac{h}{b}\right)} \tag{5}$$

Where x is the Ge composition, b is the Burger vector equalling 0.38 nm, and h is the critical thickness. From the study, thin buffer layers (≈100 nm thickness) will relax when the germanium fraction is roughly above 40%. It is therefore expected that high Ge content, thin SiGe buffer layers will have a network of misfit dislocations, unless the thickness is reduced even further.

2.3 Literature Review

2.3.1 Thick SiGe buffers

In general, the study of thick SiGe buffers is defined as a layer with a thickness between 1-12 μm. Hence all research shown in this section deals with structures with a thickness of that order of

magnitude. However, before presenting details of published work, a quick explanation of *wafer bending* is discussed as it was prevalent in the growth of the samples under investigation.

2.3.1.1 Wafer Bending

Experimental work has shown that there is an issue when growing high Ge content SiGe layers on Si substrates [34]. The issue is that when growth on a Si substrate is on only one side of the wafer, the wafer starts to bend and thereby causes difficulties for wafer handling and bonding [34]. Figure 18 shows the type of wafer bending depending on % Ge content composition.

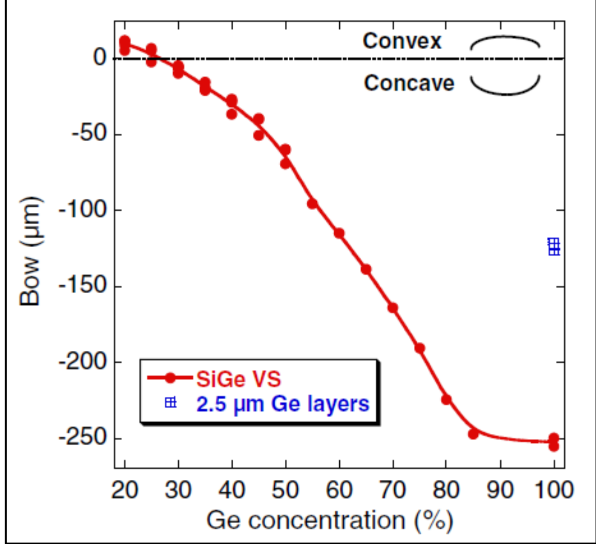


Figure 15: The bowing effect witnessed when growing thick SiGe layers on a Si Substrate. To view details of a patented process to reduce the bending effect, see ref. [34]. Figure reproduced from ref. [34] without permission

2.3.1.2 Constant Germanium Composition

Constant Ge composition is a process in which an unchanged % Ge composition is epitaxially grown on a Si substrate. Research performed in 1981 by Tsaur et al. involved growing a $Si_{0.85}Ge_{0.15}$ layer on a Si (100) substrate.

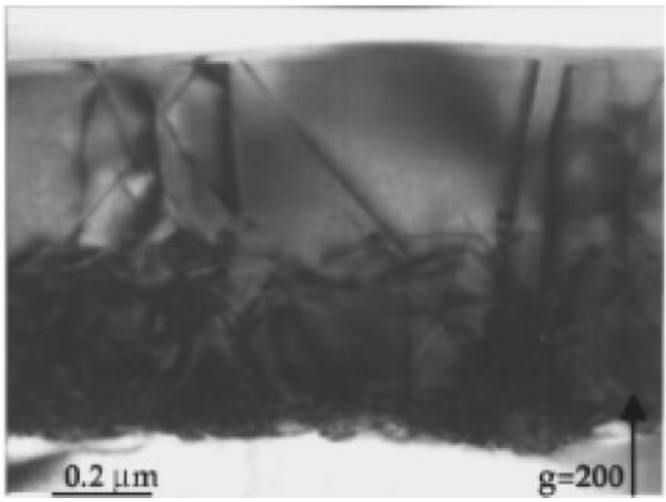


Figure 16: TEM image of the Si0.75Ge0.15 layer on a Si (100) substrate sample showing high value for TDD. Figure reproduced from ref. [52] without permission

Figure 19 shows a network of TDs from a SiGe on Si substrate. The reason for the high *TDD* value is because of a high lattice mismatch between the Si substrate and a large Ge content composition $SiGe_x$ layer. A summary of the results for this technique are [51]:

- High *TDD* (7×10^9 cm^{-2})
- High R_{RMS} (> 50nm)
- Low % Relaxation (R < 70%)
- Thick layers

2.3.1.3 Graded Composition

Graded composition involves growing an initial SiGe layer with a low % Ge content composition. This layer is then followed by the growth of a greater % Ge content composition until the desired Ge composition is reached. Some techniques end this structure with a capping layer though that is not always the case.

Research performed by Peng and Zhao et al. involved growing a graded structure of SiGe with increasing % Ge content composition. Figure 20 shows the structure in question, with *t* representing thickness.

$Si_{0.1}Ge_{0.9}$, t = 500 nm
LT- $Si_{0.4}Ge_{0.6}$, t = 50 nm
$Si_{0.4}Ge_{0.6}$, t = 500 nm
LT- $Si_{0.7}Ge_{0.3}$, t = 50 nm
$Si_{0.7}Ge_{0.3}$, t = 500 nm
LT-Si, t =50 nm
Si (001)

Figure 17: Structure grown for Peng and Zhao et al. [35]

The drawback of this procedure is that graded layers are usually thick. However, the gradual step wise increase in % Ge composition facilitates the structures increase in relaxation as the lattice mismatch between layers is relatively low compared to an abrupt change in Ge composition, as is evident in a constant germanium growth technique. Table 3 summarises the results obtained for this study.

% Relaxation	R_{RMS} (nm)	*TDD* (TD/cm^2)	Residual Strain (%)		
			$Si_{0.7}Ge_{0.3}$	$Si_{0.4}Ge_{0.6}$	$Si_{0.1}Ge_{0.9}$
"Fully Relaxed"	5.78	3.2×10^6	5	9	13

Table 3: Peng and Zhao et al. graded composition results [35]

2.3.1.4 Linear Germanium Grading

Linear grading involves gradually increasing the Ge composition from an initial percent composition, up to the desired percent composition. The rate at which the Ge composition increases is known as the *grading rate*. This is then usually followed by a thick capping layer to reduce *TDD*. Figure 21 shows a sample of a linearly graded SiGe layer on a Si substrate.

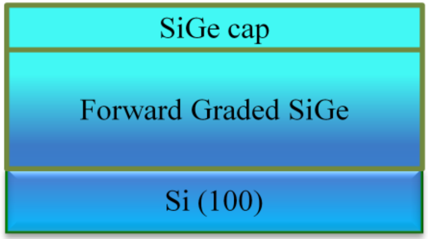


Figure 18: Forward graded SiGe on Si sample

Research by Destefanis and Hartmann et al. [36] involved growing linearly graded, low Ge content, SiGe samples on Si substrates. The sample recipe involved growing SiGe on a Si substrate starting with a 0% Ge content and gradually increasing the Ge content to a desired composition of 18%. The samples were then capped with an almost 1-µm thick constant Ge composition SiGe layer.

Higher Ge content samples were grown by Fitzgerald et al [53] which involved growing $Si_{0.47}Ge_{0.53}$ on Si substrates. The research also made an interesting hypothesis and that is that when step-graded structures are grown at conventional temperatures of 550 °C, the initial layer is elastically strained and hence the lattice mismatch is based almost entirely on the second grown layer and the substrate [53] which therefore creates an increase in TDs.

Finally, additional research performed by Hartmann et al. [34] involved growing a linearly terrace graded virtual substrate with a final Ge % composition of 85% and a 2-step CMP process. Terrace

grading is similar to linear grading except Ge content increases a fixed amount in each grown layer, or what is sometimes referred to as step-wise growth.

The sample structure involves the growth of a 0% -50% Ge content SiGe layer with roughly an 8% Ge/µm grading rate on a Si (001) substrate. This was followed by a 0.8 µm SiGe layer, and the first CMP process. The same growth conditions were repeated again however the Ge contents were from 50% to 85%. It is worth noting that the growth of these samples was done on 3 separate wafers. Table 4 summarises all the results:

Samples grown on Si substrate	Thickness (t)	Grading Rate (% GE/µm^1)	% Relaxation	R_{RMS} (nm)	*TDD*
$Si_{0.83}Ge_{0.17}$	t > 3.5 µm	≈ 5.9	96-104	3-11	10^5
$Si_{0.47}Ge_{0.53}$	t > 4 µm	≈ 10	"Fully relaxed"	-	3×10^6
$Si_{0.15}Ge_{0.85}$	t > 10 µm	≈ 8	102.8	15 nm	1.3×10^5

Table 4: A higher grading rate yields a greater TDD value, however the best result seems to come from a high Ge & Si samples. Summary of data from [34], [36], and [53]

From the results obtained for linear grading, the samples show high relaxation, and low *TDD* values. However the samples do show a relatively high R_{RMS} and are very thick in structure to facilitate the lattice mismatch.

2.3.2 Thin SiGe buffers

Research has generally been confined to the study of thick SiGe layers on Si substrates over the years. However research performed by Capellini and De Seta et al. [37] dealt with the growth of high Ge content, SiGe layers on Si substrates.

The research involved growing an 80 nm thick Ge seed under-layer by a two step process. The initial step involves deposition of Ge at low temperature (LT) of 350 ºC, followed by a high temperature (HT) deposition at 550 °C. This is then followed by the deposition of a SiGe layer. Table 5 summarizes the results obtained for this research.

Sample	Sample Thickness (t)	% Relaxation	Z_{RANGE} (nm) (See section 3.2)	*TDD*
$Si_{0.12}Ge_{78}$ on Si (100)	t < 600 nm	≈ 100%	45 & 25	≈10^7 cm^{-2}

Table 5: Summary of data from [37]

The study concluded that the *TDD* value before the growth of Ge at LT was 2 order of magnitude larger than at HT growth. Figure 22 shows how TDs reduce in number as they reach the SiGe/Ge interface.

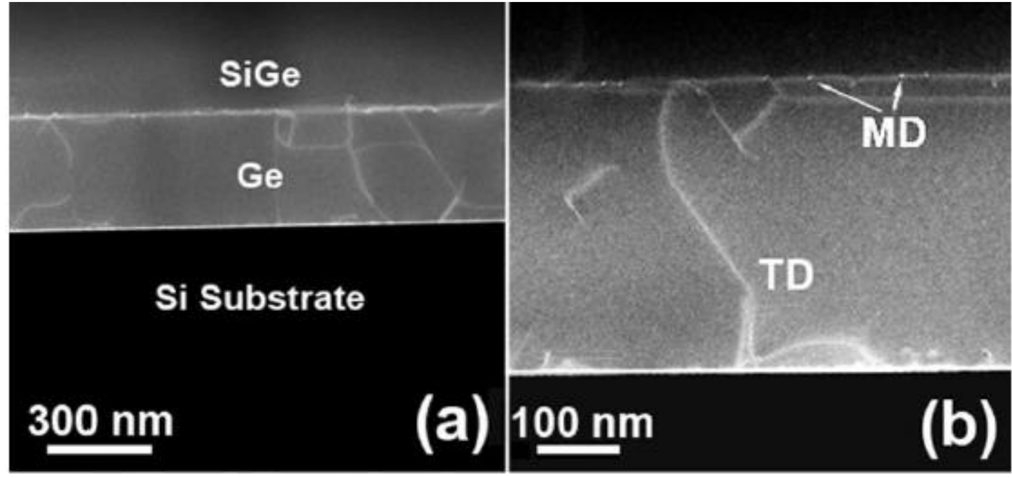


Figure 19: (a) Network of TDs extending to the SiGe/Ge interface. (b) An increased magnification image of the SiGe/Ge interface. The interface shows the creation of MDs to relieve induced stress. Figure reproduced from ref. [37] without permission

2.3.3 Annealing

Annealing is a process in which samples are exposed to high temperatures to increase relaxation and reduce *TDD*. Research performed by Fitzgerald et al. showed that annealing samples with high *TDD* values will cause TDs to annihilate, reducing the *TDD* value [38]. Besides annealing, ion implantation is also a way of increasing relaxation. The process involves adding certain dosages of an ion and witnessing the effects on the sample. Table 6 shows the effect of annealing and He^+ ion implantation doses on a 100 nm thick $Si0._7Ge_{0.3}$ layer on Si (100) substrate.

Implantation dose (10^6 cm^{-2})	Annealing temp./time (°C)/(s)	Degree of Relaxation (%)	*TDD* (10^7 cm^{-2})
0	750/600	7	
0	800/600	14	
0	850/600	34	
0	1000/30	34	
1.2	850/600	70	4.5 ± 1.8
2.0	750/600	66	3.7 ± 1.8
2.0	800/600	68	4.4 ± 1.6
2.0	850/600	68	1.62 ± 0.8
2.0	1000/30		102 ± 39
2.8	850/600	83	181 ± 1
3.0	850/600	80	7900 ± 140
3.0	1000/30	80	

Table 6: Effects of annealing and He^+ implantation dose for SiGe on Si (100) [49].

3 Experimental Techniques

3.1 High Resolution X-Ray Diffraction (HR-XRD)

HR-XRD is a tool used for characterizing material properties such as lattice mismatch, percent composition in alloys, and percent relaxation. Figure 24 shows the setup of the XRD system. All HR-XRD in this study was carried out using a Panalytical X'Pert PRO Materials Research Diffractometer.

The system has 3 main parts. The first part, the x-ray source, is where a high power copper source operated at 40 keV and 40 mA, was used to produce an incident CuKα_1 source with a 1.5406Å wavelength. The second part, the sample stage, is where the sample is mounted using regular scotch tape to hold it in place. To satisfy Bragg's Law of diffraction the HR-XRD needs to have a high degree of precision. For this reason, the sample stage has a total of 5 degrees of freedom which align the X-ray source, sample to be tested, and the detector. The sample's degrees of freedom are: the positions x, y, and z, and the rotation phi (φ) and tilt of the sample stage psi (ψ). The last part, the detector, is where the diffracted x-rays are collected and counted.

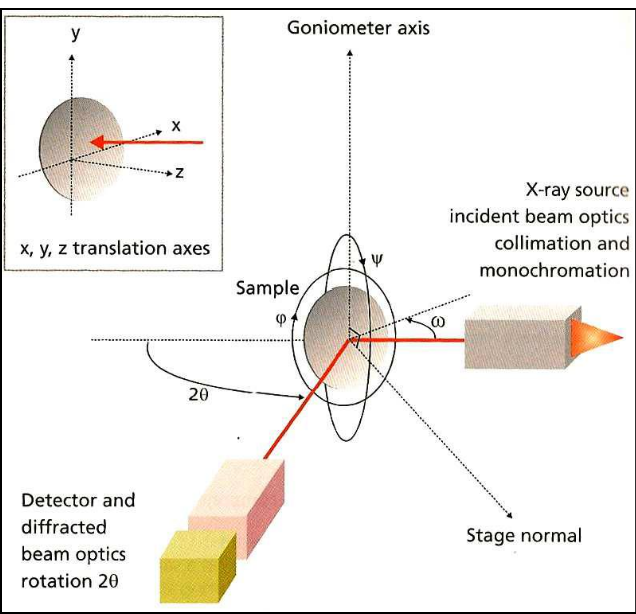


Figure 20: Schematic setup of the HR- XRD kit. Figure reproduced from ref. [12] with permission

A reciprocal space map (*RSM*) is produced to obtain a comprehensive picture of the sample to be tested. A *RSM* is a collection of rocking-curves which is when the incident x-ray angle (ω) is fixed and the detector angle (ω-2θ) scans over a range of angles to determine the Bragg Peaks. Hence a *RSM* is produced when multiple rocking-curves (varying ω) scan over the sample.

To obtain information about a sample, the symmetric (004) and asymmetric (224) Miller planes are usually used. For a detailed derivation into why these planes are used see [12].The degree of relaxation is obtained by comparing the lateral lattice parameter of the layer with the substrate. If the parameter is in perfect registry with the substrate then the layer is considered to be fully strained and therefore 0% relaxed. However, if the lateral lattice parameter of the layer is the same as its bulk value then no distortion has taken place and hence the layer is 100% relaxed. A relaxation value greater than 100% means the sample is under tensile strain (see eqn. 8). Equation 6 shows how the % relaxation (*R*) is determined from calculated lattice parameters. To determine the a_{lay} Vegard's law (eqn. 3) was used.

$$R = \frac{a_{sub} - a_{lay}}{a_{sub} - a_{lay(bulk)}} \tag{6}$$

All SiGe lattice parameter calculations were obtained using a program called X'Pert Epitaxy. The program calculates SiGe composition by applying Dismukes [31] corrected Vegard's Law. Equation 7 gives the relationship.

$$a_{Si_{x-1}Ge_x} = x \cdot a_{Ge} + \quad (1-x) \cdot a_{Si} + \quad 0.028 \cdot x \cdot (x-1) \tag{7}$$

For an example of a relaxed layer, figure 25 shows a *RSM* of an (004) and (224) Miller planes of a Ge layer grown on a Si substrate. The Q_y and Q_z axis represent the location, in *RSM*, of the layer and substrate peak that satisfy Bragg's condition.

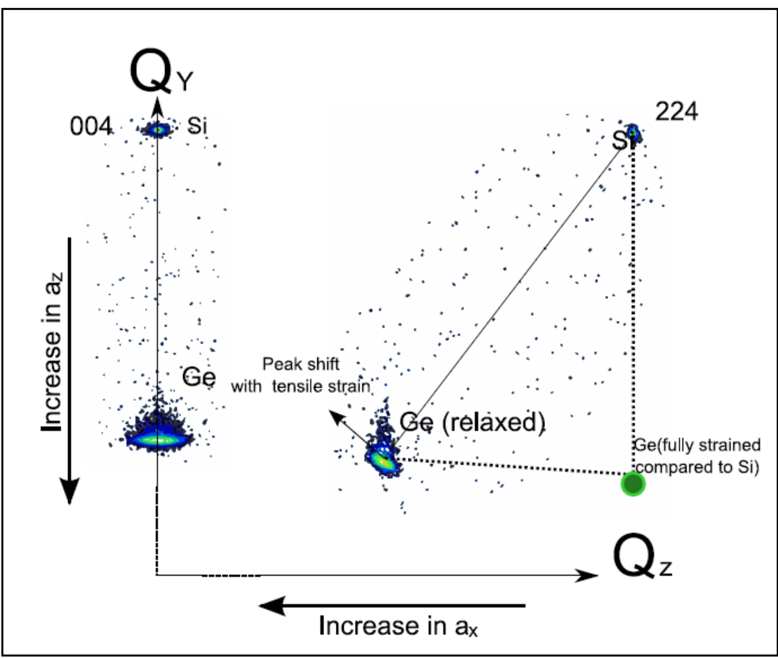


Figure 21: Reciprocal Space Mapping of Ge on Si sample. Figure obtained from ref. [12] with permission

From figure 25, the (224) plane shows how a decrease in the a_x direction of the lattice parameter leads to an increase in the a_z direction and hence the layer is said to be strained when compared to the Si substrate. Therefore, determining the % relaxation is confined within the a_x and a_z values of a grown layer. To determine these values equation 8 gives the distance between planes for a cubic lattice denoted d_{hkl}, obtained from an *RSM* scan.

$$d_{hkl} = \frac{a_{x,z}}{\sqrt{h^2 + k^2 + l^2}} \tag{8}$$

Tilting is another issue which needs to be addressed when determining structural properties of a crystal. Due to graded layers being grown on miscut substrates [39] or varying growth conditions [40],

grown layers are prone to tilting thereby distorting calculated data. Figure 26 shows an example of a tilted layer.

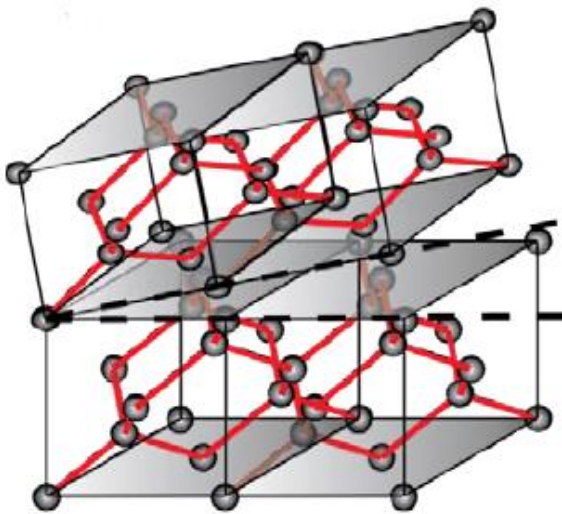


Figure 22: An exaggerated tilt in a grown layer. Figure obtained from ref. [42] with permission

Tilting in grown samples can be witnessed by viewing the substrate and layer peaks in the symmetric (004) scans. If the samples do exhibit tilting, the peaks are not vertically aligned, and an angle between substrate and layer peaks is observed. The amount of tilting is therefore represented by the angle created between the peaks.

3.2 Atomic Force Microscopy (AFM)

Created in 1986 by Binning et al. an AFM is used to provide a detailed description of a sample's topography. All samples obtained from AFM were done using a Veeco Multimode AFM with a Nanoscope IIIa controller.

An AFM has 2 settings, contact mode and tapping mode. For the purposes of the samples being tested the AFM was set to contact mode as the samples *Root Mean Squared Roughness* (R_{RMS}) is not less than 1 nm. Figure 28 shows the setup of the system for contact mode. In contact mode a tip is made to

scan the surface of a sample which is held by a cantilever that is free to bend based on the tips deflection. This deflection is what provides a detailed description of the sample's topography. To record this deflection, a Photodetector will register a shift in the lasers position and output the difference as a change in the samples height profile.

However due to an unevenly moving stage, which the sample sits on, and an unevenly scanning tip, the image needs to go through a few image processing steps. Figure 25 shows the 3 different image processing stages before the R_{RMS} value is calculated. The areas with a brighter contrast represent peaks, which increases the R_{RMS} value, while darker areas represents a trough which decreases the R_{RMS} value.

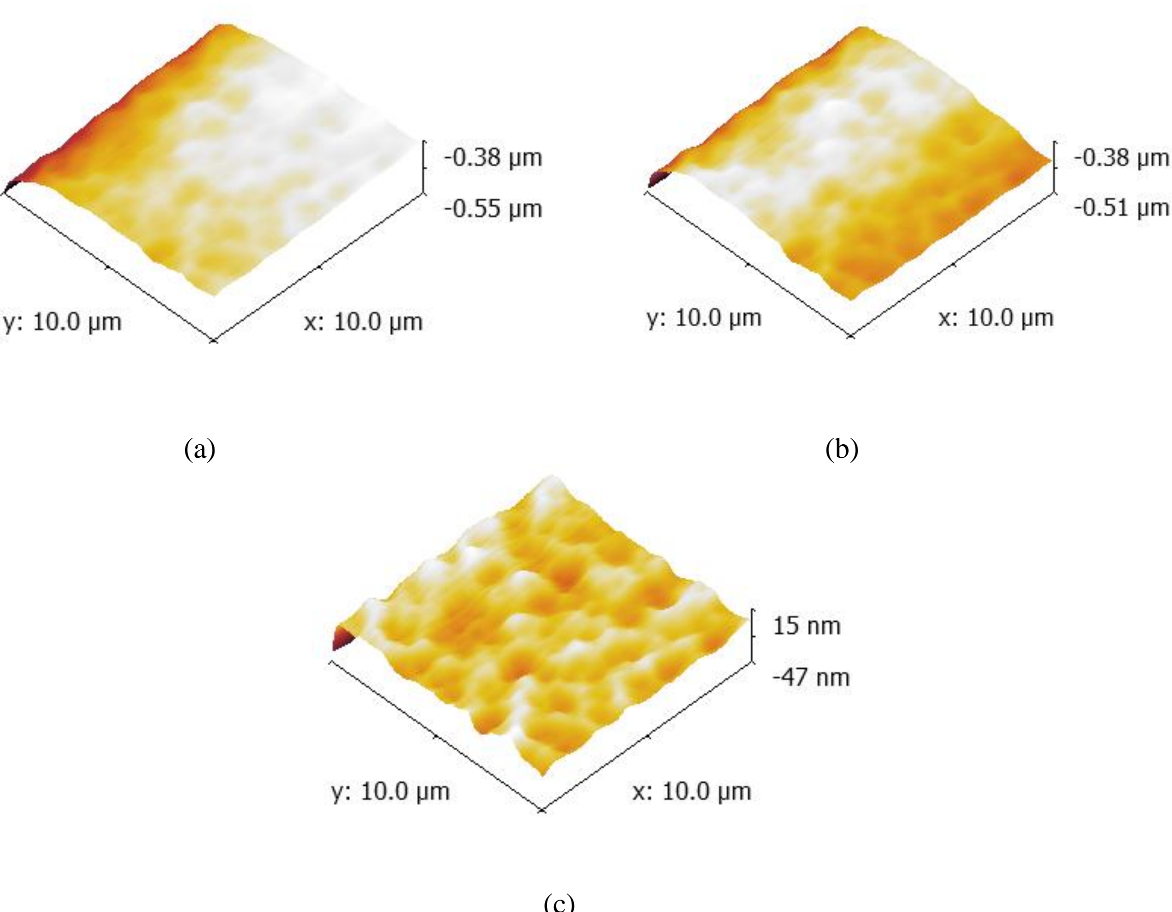


Figure 23: (a) raw data obtained from AFM. After collecting the raw data image, the sample was levelled giving (b). Finally, the background inaccuracy caused by a non-linear moving sample stage is removed by the subtraction of a 3rd degree polynomial from the image

When data from the AFM had been gathered, the R_{RMS} is calculated by measuring the height fluctuations (y_i) taken from the mean line (eqn. 9). However in some cases the *Z range* (eqn. 10) is either used with, or instead of the R_{RMS}.

$$R_{RMS} = \sqrt{\left(\frac{1}{n}\sum_{i=1}^{n} y_i^2\right)} \quad (9)$$

$$Z_{Range} = Z_{\max} - Z_{\min} \quad (10)$$

Finally, it is worth noting that the R_{RMS} of any sample varies depending on the size of each image because a smaller sized image might give the false impression that the R_{RMS} throughout the sample is high, when in actual fact the R_{RMS} of the entire sample is relatively low compared to a small region with a high R_{RMS}. To correct for this inaccuracy, all samples had 3 images taken of them at 3 different locations. Each image was 10 µm × 10 µm and an average value for the R_{RMS} was computed, error was also incorporated into the R_{RMS}.

3.3 Transmission Electron Microscopy (TEM)

TEM is used to view the crystal structure of a sample. Finer details such as viewing dislocations, amount of strain, and thickness of the sample can be viewed clearly. The TEM which was used in this study was a JEOL JEM-2000FX. Figure 29 shows the setup of the TEM.

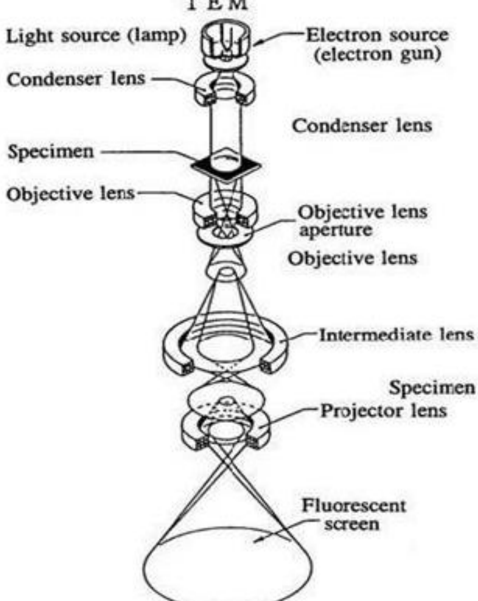


Figure 24: Typical setup of the TEM used for sample imaging. Figure reproduced from ref. [43] without permission

The TEM works by heating a tungsten filament which produces a stream of electrons. The electrons are released because the thermal energy surpasses the work function of the tungsten metal. These electrons are then accelerated by the application of a 200 keV voltage. The beam of electrons then passes through a condenser lens which acts to create a thin and even beam to pass through the sample. After passing the sample, the beam goes through the objective lenses to increase contrast. Finally, the image is projected onto a CCD camera. The entire TEM system is placed in vacuum (below 10^{-7} mbar) to eliminate the possibility of the electron beam interacting with other matter, thereby distorting the image. Interestingly, the TEM has a resolution of 0.32nm Point / 0.14nm Lattice.

3.3.1 Sample Preparation

Before putting a sample into the TEM, an arduous amount of work needs to be done to prepare the sample for imaging. For a TEM to form an image, the sample needs to be electron transparent and hence have to be 10 - 200 nm in thickness. The preparation work can be divided into 2 parts. The first

part involves creating the structure to be placed in the milling machine and the second part involves milling the sample.

Part 1 involves cleaving roughly two, $1.5 \times 0.5\ cm^2$ of the sample to be tested. Also, 2 similarly sized gash wafers, which will act as supports, need to be cleaved. The samples were then glued together facing one another with the gash wafers glued on both sides facing the sample. The sample was then left for 3 hours for the glue to set, which was then followed by a grinding process. The grinding process involves holding the sample to a rotating grinding paper. Slowly, the sample starts to lose thickness until a reasonably low thickness is reached. Then a very soft grinding paper, which acts as a polisher, is used on the sample. This procedure is done for the opposite side of the sample so that the sample is as thin as possible. The grinding process is completed when the sample is electron transparent, or to be more quantitative, is roughly 15-20 micrometers thick. Next, copper rings are glued onto the sample and left to dry for 3 hours. Finally, a scalpel is used to scrap away the area around the copper rings and then the rings are placed in a hot acetone both to remove any dirt or unwanted wax from the sample.

Part 2 involves milling the sample. A precision ion polishing system (known as Gatan-PIPS) was used. The system mills away the sample by firing charged argon ions at the sample which have been accelerated by the application of 4.5 keV. This results in the gradual removal of the sample surface to the desired thickness. After which, the sample is polished by lowering the ion beam energy to 2.5 keV for roughly 15 minutes. Now the sample is ready to be used for TEM.

3.4 Defect Etching (DE)

An important parameter which determines the quality of crystalline structures is the *threading dislocation density* (*TDD*). It is therefore necessary to reveal the threading dislocations by defect etching to determine the quality of the crystal grown.

To expose TDs, a selective wet chemical etchant is used to determine their location, but more importantly their abundance. The summation of all the TDs created per cm^2 of a sample's surface is what is referred to as the etch pit density (EPD), or can be synonymous with the Threading Dislocation Density (*TDD*). The selective wet chemical etchant works by etching away a layer at a constant rate, known as the etch rate, but in the presence of a TD the chemical etches faster at that location thereby creating a pit as depicted in figure 30.

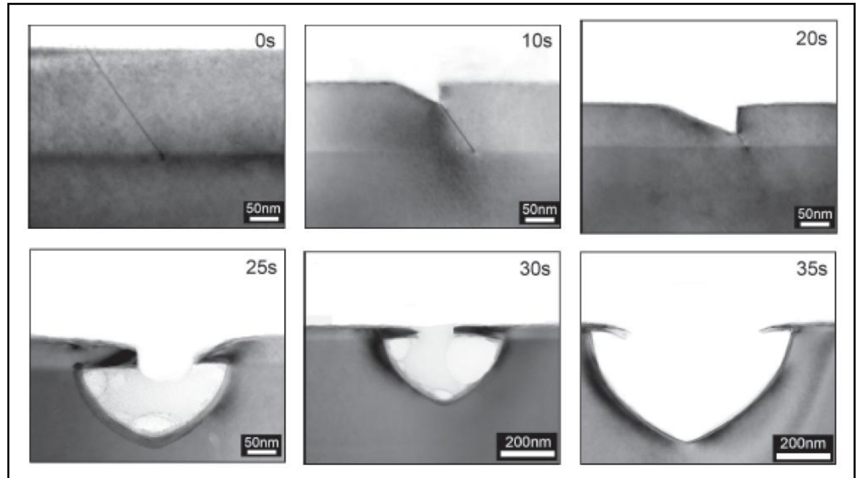


Figure 25: Shows a strained Si layer with a TD. As time progresses the entire layer loses its thickness and the etchant eventually produces an etch pit at the TD. Figure reproduced from ref. [44] without permission

Etchants have two main components, the first is an oxidizing agent and the second is an oxidizer removal agent [45]. Varying the ratio between the two components and/or diluting the sample dictates

the etch rate of the etchant. This is a vital parameter for any etchant as it gives the researcher a desirable etch rate depending on how much the sample is to be etched.

However the etchant might not reveal TDs at all. To understand why, it would be convenient to categorize the etch rate into 2 categories. The *bulk etch rate*, and the etch rate along the TD, or simply the *TD etch rate*. If the bulk etch rate is low, and the TD etch rate is high, then TDs would be revealed as depicted in figure 30. The entire structure is etched, but not as fast as in the TD location, and therefore a pit is created. However, if the bulk etch rate is greater or relatively equal to the TD etch rate, then the etchant will not reveal any TDs as the sample is being etched too fast for the etchant to create a pit at a TD.

All DE was carried out using a modified Schimmel etchant consisting of 7.5 grams of chromium trioxide, hydrofluoric acid, and water (CrO_3 <2 parts>: HF (50%) <4 parts>: H_2O <3 parts>). The etchant was created by mixing, 7.5 grams of the chromium trioxide with 100 ml of Deionised (DI) water. 150 ml of DI water was then added to the mixture which was then followed by the addition of 200 ml of HF (50%). The mixture was then left to stand for a week while being mixed by the use of a magnetic stirrer.

The etchant has been found to etch rather slowly with an etch rate of roughly 2 $nm.s^{-1}$ and 0.2 $nm.s^{-1}$ for 70% and 95% Ge content, respectively. The reason for using this etchant over others is because the samples were to be etched roughly 100 nm (see section 3.5.1). With such a slow etch rate, this gives ample time to place the sample in the etchant and remove it after a depth of 100 nm has been reached thereby guaranteeing reproducibility of the etch depth. Compare that with an iodine-based etchant that has an etch rate of roughly 280 $nm.s^{-1}$ and 50 $nm.s^{-1}$ for 70% and 95% Ge content, respectively [42].

A comprehensive study of 4 typical etchants was performed by S. Marchionna et al, which provides a detailed *TDD* analysis for Ge composition between 20% - 90%. Figure 31 below shows the results of their research.

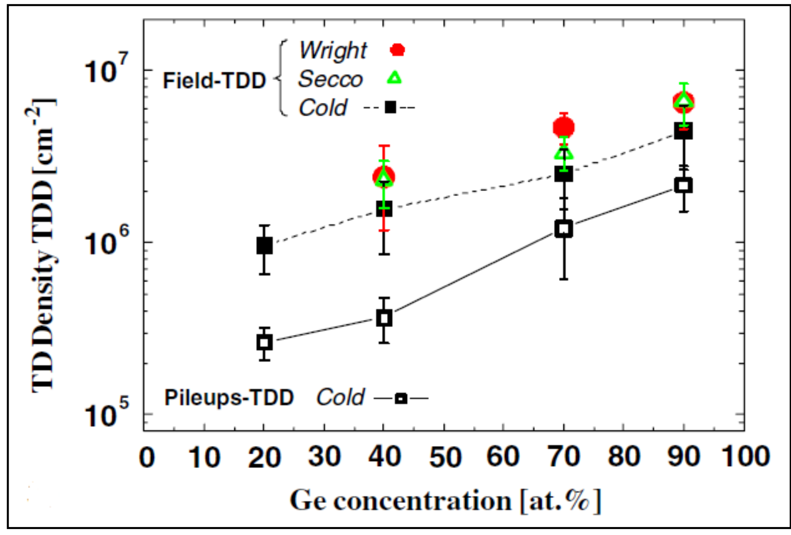


Figure 26: both Wright and Secco etchants reveal TDs better. However the "Cold" etchant was found to be "the most effective in obtaining unambiguous and uniform etch pit density figures..." Figure reproduced from ref. [46] without permission

3.4.1 Determining Etch Depth

A point of discussion arose when the value of 100 nm etch depth was determined. The question was at what etch depth should the *TDD* be determined? The reason for asking this question was because TDs have been found to combine in the area between the substrate and the sample surface, as shown in figure 32. Etching until, before or after the point of two intersecting TDs can be misleading because two TDs will be counted as one, or vice versa. Although the margin of error when taking this into consideration should not exceed one order of magnitude to the actual *TDD* value, it will however provide a more accurate description between *TDD* values of the same order of magnitude.

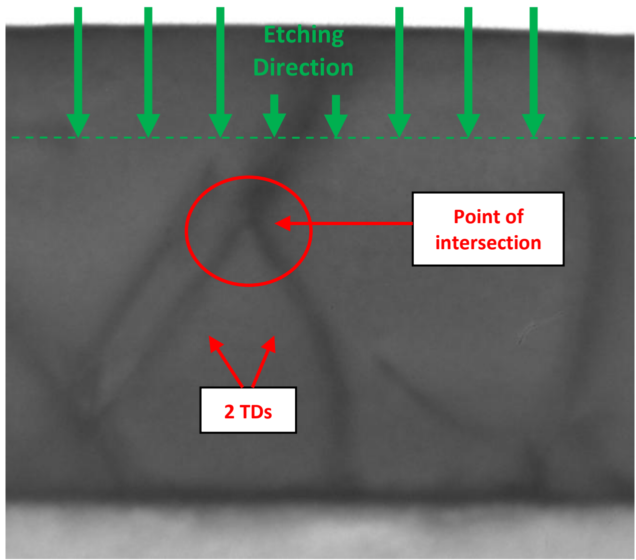


Figure 27: Image of sample 11-439 showing 2 TDs combining to form 1 TD

3.4.2 Modified Schimmel Reactivity

When using an etchant to etch a sample, as time passes the etchants loses its reactivity and therefore the etch rate naturally decreases. For etching thin buffer layers, this is an important concept which needs to be addressed. It was therefore necessary to determine the reactivity of the etchant, especially when etching a layer less than 200 nm to obtain a precise, and more importantly, repeatable etch depths to maintain similar comparisons between samples.

For the etchant used in this study, the reactivity was determined by cleaving 6 samples of $Si_{0.05}Ge_{0.95}$. The samples were then placed in the etchant one after the other for 10 minutes each (600 seconds). Earlier calculations showed that 10 minutes of etching should give an etch depth of 100 nm for all the samples, but due to loss of reactivity this was not the case. Figure 33 shows a plot of etch depth versus time.

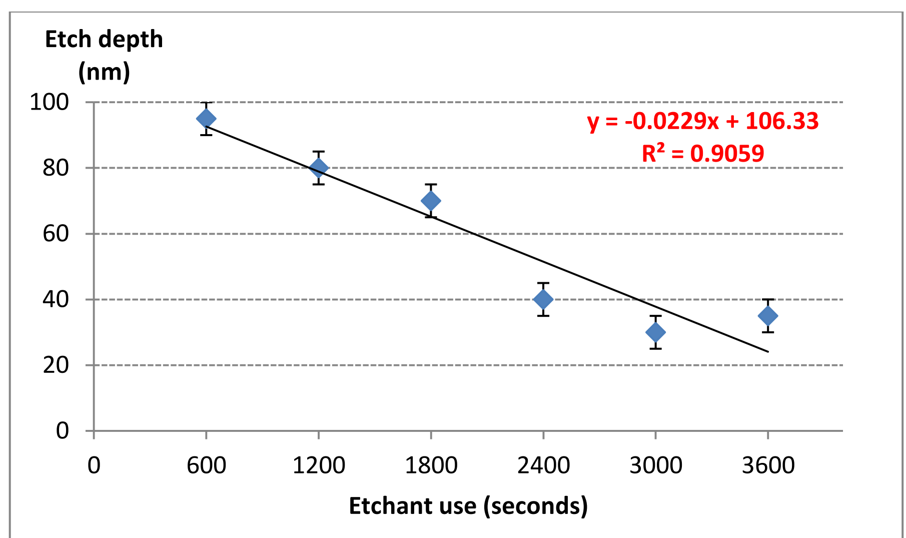


Figure 28: A linearly declining relationship is observed for 20ml of the modified Schimmel etchant

A similar linear relationship was observed when the same experiment was repeated for $Si_{0.3}Ge_{0.7}$. However, the difference was that the etching time was less than $Si_{0.05}Ge_{0.95}$ due to a difference in % Ge content composition.

From this result, it was now possible to obtain a 100 nm etch depth for all samples by etching an initial sample for 10 minutes, and then gradually increasing the etch time beyond 10 minutes for the following samples to obtain a consistent etch depth of 100 nm. Equation 11 shows the relationship between etch depth, etch time, and etch rate for the etchant used.

$$\text{etch rate (nm.s}^{-1}\text{)} = \frac{\text{etch depth (nm)}}{\text{etched time (s)}} \tag{11}$$

3.4.3 Sample Preparation

Each sample was initially cleaved to an area of roughly 1 cm^2. Next, a small area of the sample was covered with a layer of Apiezon, or simply 'black wax'. The wax's main role is to protect the sample from etching and thereby leaving an area of the sample unetched. The reason for this is to measure the etch depth by comparing the height difference of the etched and unetched regions. After etching, the

sample is placed in two toluene baths, one course and one fine, to remove the black wax. A nitrogen gun is then used to remove any trace of toluene and dirt on the sample.

The next part is to measure the etch depth. This was done using a Talystep machine which somewhat works the same way as an AFM. Initially, a pin is dragged across the sample's etched surface and when it reaches the *island* (unetched region) the pin moves vertically upwards and records the height difference. By knowing the etch time and etch depth, the etch rate is determined. The final step is to use SEM to view and count the etch pits.

3.5 Scanning Electron Microscopy

After a sample was etched, an SEM was used to view TDs and compute the *TDD*. The SEM which was used in this study was a ZEISS SUPRA 55-VP. Figure 34 shows the setup of the SEM.

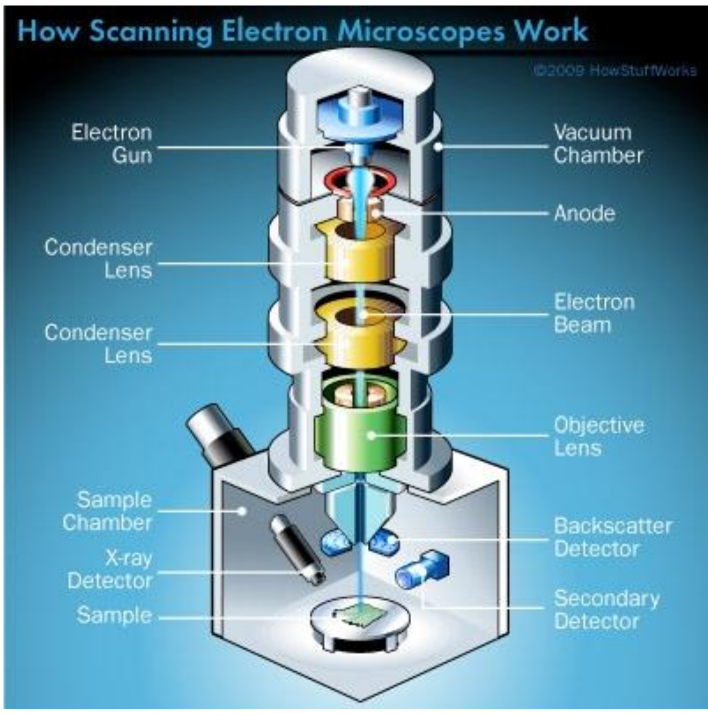
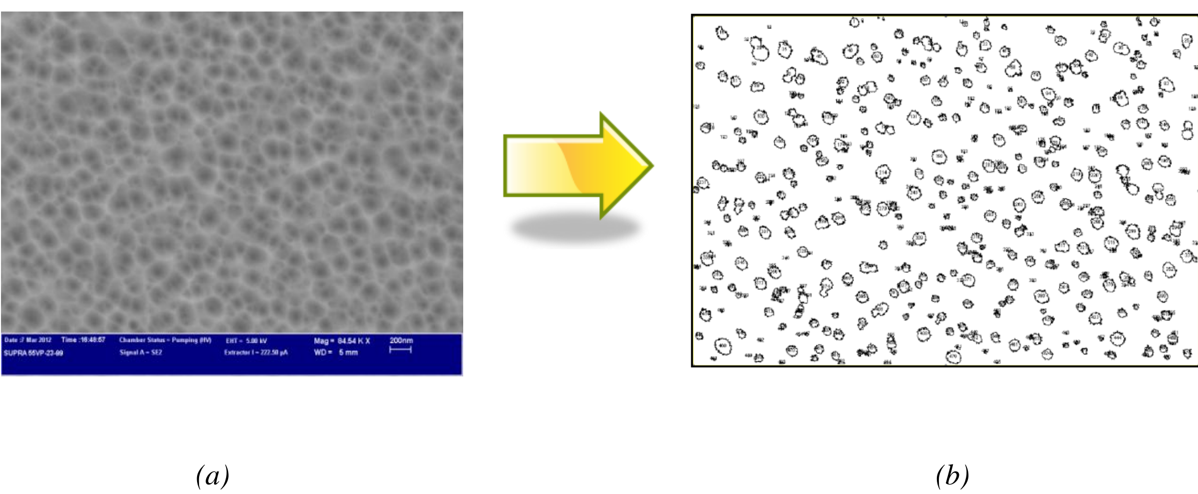


Figure 29: Basic setup of an SEM. Figure reproduced from ref. [47] without permission

An SEM works by accelerating electrons from an electron gun positioned at the top of the SEM towards the sample, which is positioned at the bottom. The electron beam travels through a series of lenses to direct and stabilise the beam. Once the beam of electrons hits the sample, x-rays and loosely bound electrons are dislodged from the sample. The ejected electrons are then collected in a secondary-electron (*SE*) detector to form an image on a computer screen. The image obtained in the *SE* detector is mainly used to determine topography of the sample. A 10 keV accelerator voltage is usually used to obtain maximum contrast.

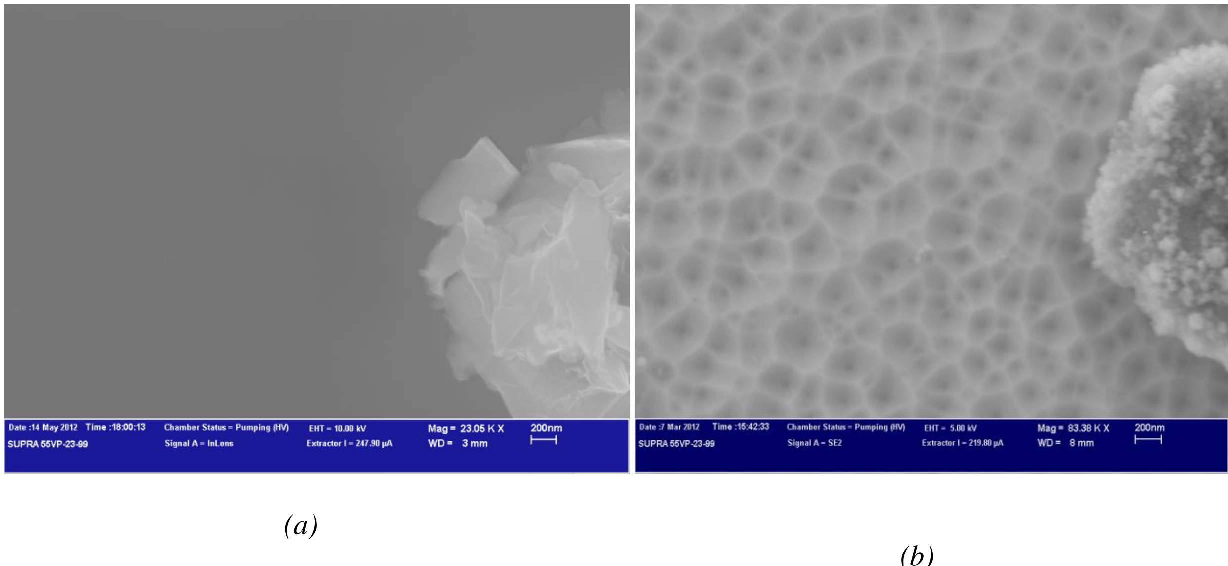
Once an image has been obtained of the etched samples, the next step was to count how many TDs were in a cm^2 of a sample and obtain a *TDD* value. This was done by downloading the free online software called *ImageJ* [20]. Among other functions, the software can be used to manipulate images. Once an image is opened, the dark spots, which represent TDs (see figure 35(a)) were converted into black dots on a white background. These dots were then summed over a single image, which were roughly 1 μm in size, and then multiplied by a calculated factor to convert the value obtained to a final *TDD* (TDs/cm^2). The error incorporated by this method is that the TD value per image is the same throughout the sample which is not the case. Hence, 5 SEM images of each sample were taken at different locations on the sample to reduce the error margin and the standard deviation was calculated to provide a clearer picture of the *TDD* value.



(a) *(b)*

Figure 30: (a) An SEM image showing the TD's after etching of a sample. (b) Shows the conversion of the SEM image into dots using the ImageJ program

Before determining the *TDD* of each sample, it had to be verified that what was seen on the SEM was in fact TDs which were revealed by wet chemical etching. To prove this, a $Si_{0.05}Ge_{0.95}$ sample was etched to obtain an etch depth of 90 nm and then placed in a SEM, a similar unetched sample was also placed in the SEM and the images compared.



(a)

(b)

Figure 31: (a) an unetched $Si_{0.05}Ge_{0.95}$ and (b) an etched $Si_{0.05}Ge_{0.95}$

From figure 36, both images show a foreign object on the right of each image, probably dust particles, which were used for focusing the SEM on the sample surface. The images clearly show the effect of etching on the $Si_{0.05}Ge_{0.95}$ sample by revealing TDs thereby verifying that the etchant does work.

4 Results and Discussion

The samples grown for this investigation were ten in total. Each sample had a SiGe layer grown on a Si (100) substrate, with a varying amount of Ge under-layer. All samples were grown by RP-CVD. The samples 11-435 to 11-439 consisted of 95% Ge content while the samples 11-440 to 11-444 were 70% Ge content.

The sample recipe involved growing a varying amount of a Ge seed layer on a Si substrate at 450 ºC. The reason for growing the samples at 450 ºC was because research has shown that temperatures of 450 ºC and below avoids the formation of islanding which is a favourable outcome for crystal quality [48]. The seed layers main role is to act as a relaxing platform for further growth.

On top of the seed layer was a 100 nm layer of SiGe with a 70% and 95% Ge content composition. After the 100 nm layer, the structure was annealed for 5 minutes at 800 ºC. Annealing has been proven to enhance relaxation and reduce TDs to improve crystal quality in grown layers [42]. A final 200 nm SiGe layer with the same composition as the layer underneath is then grown to obtain a smooth, high quality finish

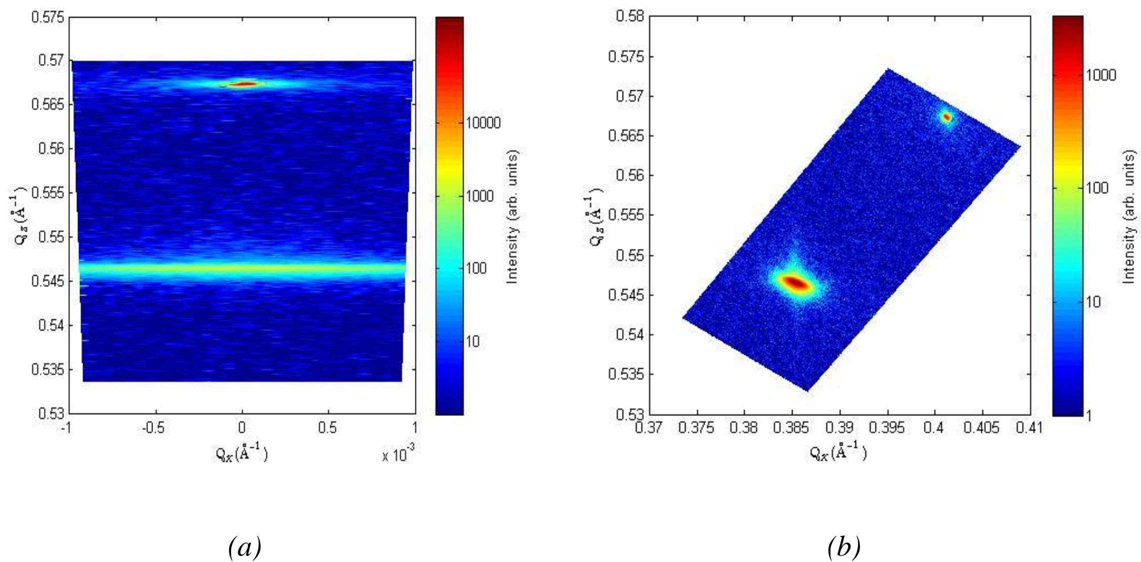
Table 7 gives a detailed description of the samples grown. Sample thicknesses were determined by cross sectional TEM imaging. Each image was opened in ImageJ, which was also used for counting TDs, and thickness measured using a measuring tool within the program. % Ge composition was computed using equation 7 which the Epitaxy program utilizes for calculation. Further sample properties can be found in the following sections.

Sample ID	Variable Parameters		
	$SiGe_x$ composition via HR-XRD	T_{SiGe} (ºC)	Ge Thickness (nm) via cross-sectional TEM (Error: ± 2nm)
11-435	0.948	450	9
11-436	0.941	450	17
11-437	0.943	450	45
11-438	0.946	450	87
11-439	0.942	450	0
11-440	0.714	450	10
11-441	0.720	450	21
11-442	0.720	450	52
11-443	0.724	450	102
11-444	0.721	450	0

Table 7: Sample recipes in initial investigation

4.1 $Si_{0.05}Ge_{0.95}$

All samples were initially assessed by HR-XRD to measure alloy composition, relaxation, and possible tilt between layer and substrate peaks. Tilt was measured by looking at the (004) Miller plane and verifying whether the layer and substrate peaks vertically align themselves with one another. Figure 32 shows the *RSM* for the 11-438 sample.



(a) *(b)*

Figure 32: (a) the (004) and (b) (224) Miller planes for the 11-438 sample viewed in RSM shows the SiGe and Si peaks. The (004) peaks are vertically aligned indicating no tilt in the sample grown

From the (004) and (224) Miller planes, the Si substrate and the SiGe layer are clearly visible. However the Ge seed layer does not appear to be very visible. Upon further inspection, it can be noticed that from the (224) plane, the SiGe peak is much broader when compared to samples with a thinner Ge seed layer. Hence the Ge seed layer seems to be incorporated within the SiGe peak.

Tilt was non-existent in all samples grown and hence no alteration to calculated data was made due to the mis-growth of the Ge or SiGe layers. Figure 33 shows a plot of % Relaxation of $Si_{0.05}Ge_{0.95}$ against Ge seed layer thicknesses.

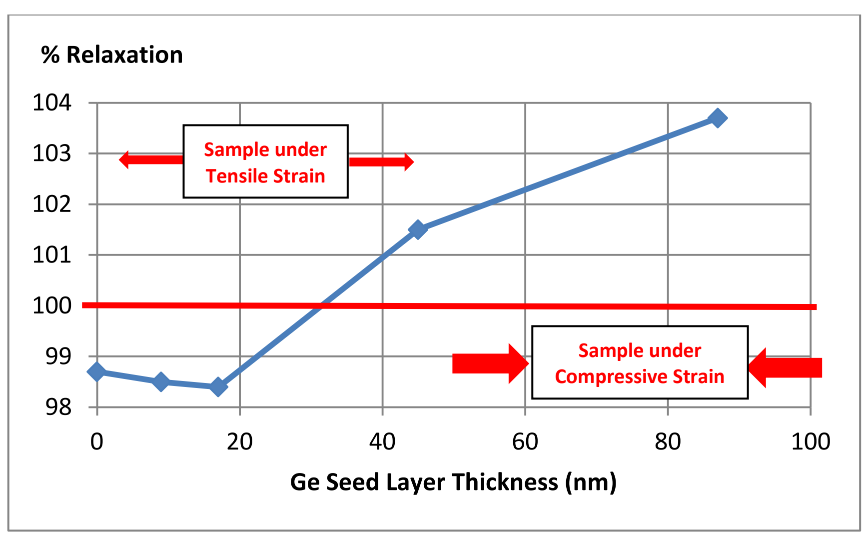


Figure 33: % Relaxation of the top SiGe layer increases gradually for Si0.05Ge0.95. Error margins negligible

The graph shows that as the Ge seed layer increases thickness, the SiGe top layer relaxes further. This increased relaxation will cause the expected generation of misfit dislocations to relieve the induced stresses and hence increase the *TDD* value.

Following HR-XRD assessment, the samples were placed in AFM to determine the surface morphology. Figure 34 shows the results for three samples having different thickness of Ge under-layer. Note that in each case this is an AFM profile of the final top alloy surface after the full sample has been grown.

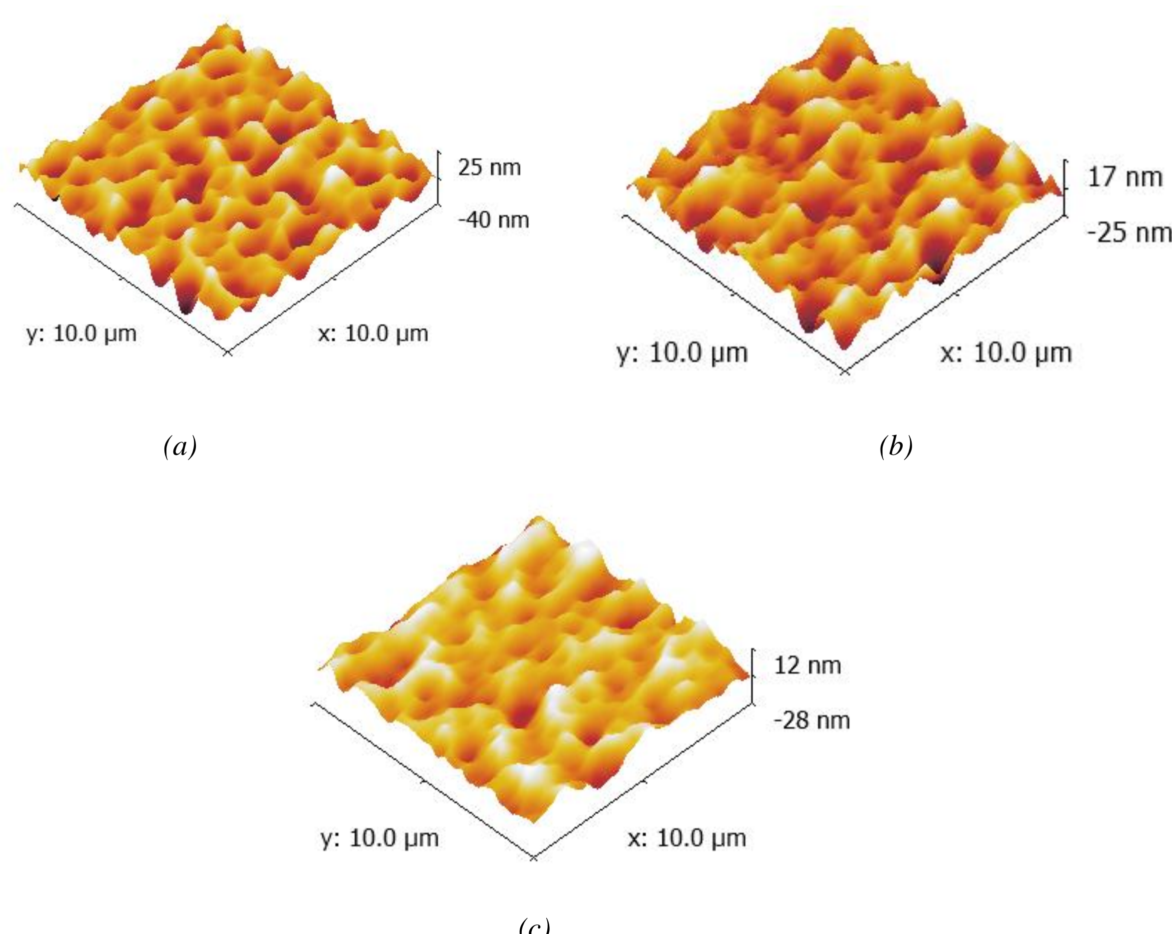


Figure 34: 10µm × 10µm AFM images for Si0.05Ge0.95: (a) without Ge under-layer (b) with 45nm Ge under-layer (c) with 87 nm Ge under-layer

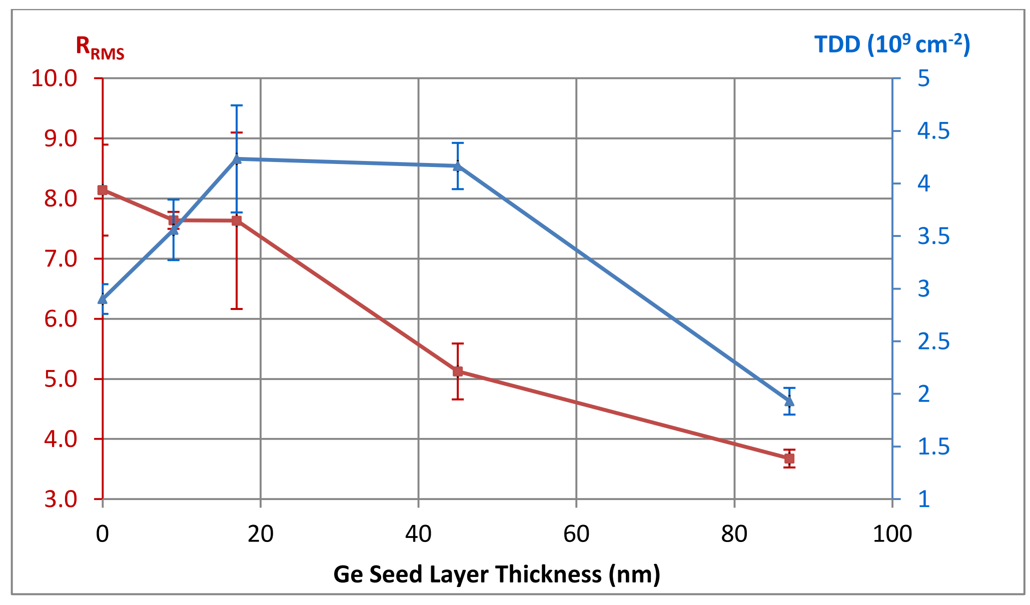


Figure 35: R_{RMS} and TDD vales show a similar relationship with increasing Ge seed layer thickness for $Si_{0.05}Ge_{0.95}$

Figure 35 summarizes the key features of the as-grown $Si_{0.05}Ge_{0.95}$ samples. The results show that as the Ge seed layer increases thickness and the sample relaxes to a value just above 100%, the R_{RMS} dramatically decreases to a value of 3.67 nm. The reason for this is because as the structure becomes more relaxed, and exceeds 100% relaxation, it starts to stretch horizontally, or what is technically known as *tensile strain*, thereby flattening the surface even further. This therefore causes a decrease in the sample's R_{RMS} value.

The *TDD* values exhibited by the samples show a different trend. The samples show that as the Ge seed layer thickness increases from 0-20 nm the *TDD* value increases gradually. This is the same region where the sample is under a compressive state. The *TDD* value then remains constant for Ge thickness values from 20-50 nm, at roughly 4.2×10^9 cm^{-2}. For a Ge thickness value greater than 50 nm, a drastic drop in *TDD* to roughly 2×10^9 cm^{-2} is observed. A possible reason for this is because as the Ge seed layer thickens, TDs have a greater likelihood of combining together, as discussed in section 3.4.1, thereby exhibiting a reduced *TDD* value than a lower Ge thickness layer. From this observation, samples under tensile strain exhibit a lower *TDD* value.

4.2 $Si_{0.3}Ge_{0.7}$

Once again, initial assessment of the samples was done in HR-XRD. Figure 36 shows the *RSM* for sample 11-443. With a Ge seed layer thickness of 102 nm, the seed layer can be clearly seen on both the (004) and (224) Miller planes.

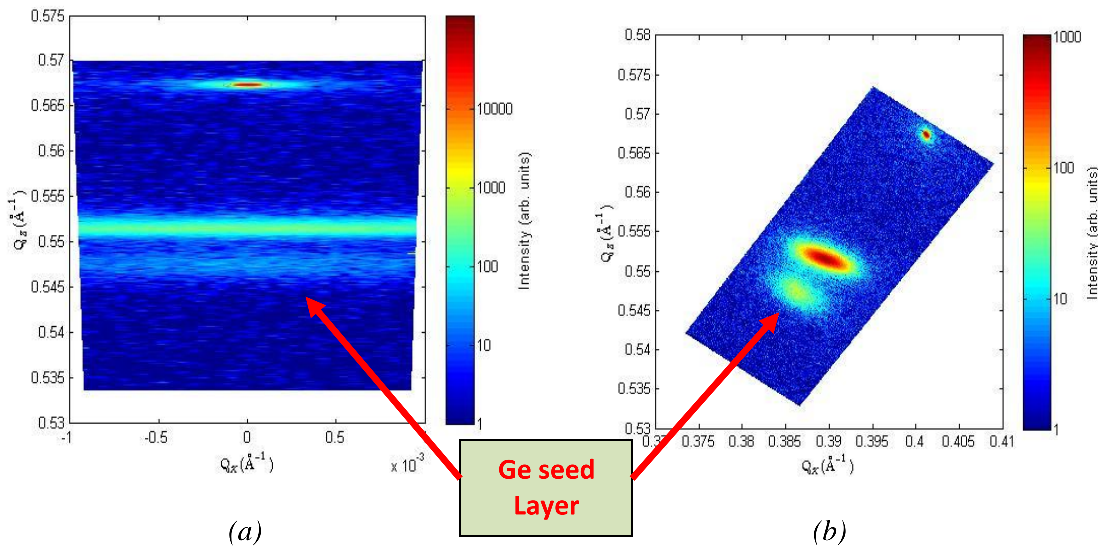


Figure 36: the RSM of the 11-443 sample clearly shows the Ge seed layer as a faint, sky-blue line in the (a) (004) plane and (b) just below the SiGe over-layer in the (224) RSM

From Figure 36, it is clear to see that all grown layers do not exhibit any tilting and are fully relaxed. This was prevalent in all the samples grown. A detailed description of relaxation values was plotted in figure 37.

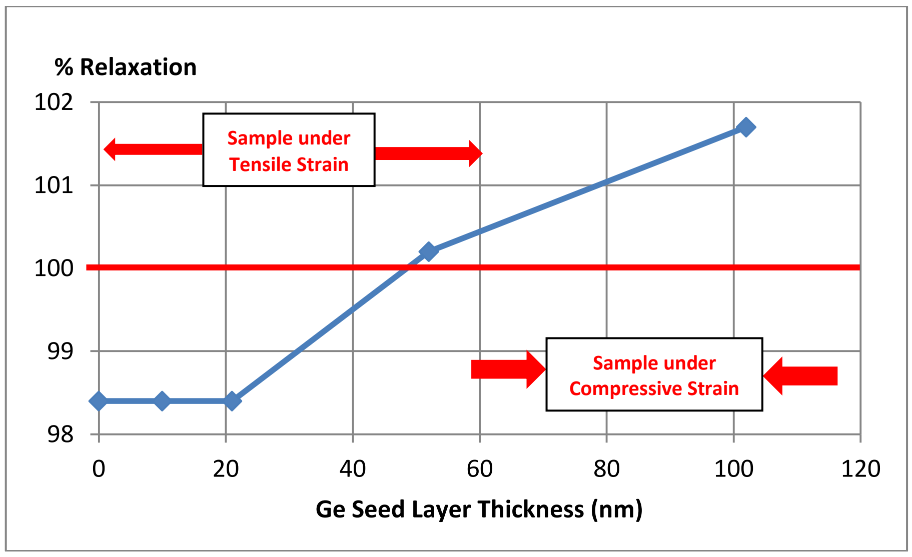


Figure 37: Increasing the Ge seed layer thickness causes an increase in relaxation for Si0.3Ge0.7. Error margins considered negligible

Figure 37 shows a similar trend for $Si_{0.3}Ge_{0.7}$ % relaxation values as the $Si_{0.05}Ge_{0.95}$ samples. The samples are initially under compressive strain between a Ge seed layer thickness between 0-20 nm but after an increase in Ge seed layer thickness beyond 20 nm, the samples relax further and finally enters the tensile strain region. However a difference was observed between the rates at which the samples relax for both batches. Although 95% SiGe samples had a final Ge thickness of 87 nm, while 70% SiGe samples had a final Ge seed layer thickness of 102 nm, the 95% samples had a greater value for tensile strain at 103.7%, while the 70% sample had a final tensile strain value of 101.7%. This means that a 95% SiGe sample is quicker to relax than a 70% SiGe sample, both with a Ge under-layer.

Once again, the samples were placed in an AFM to assess surface morphology. Figure 38 shows AFM images of the 70% SiGe samples.

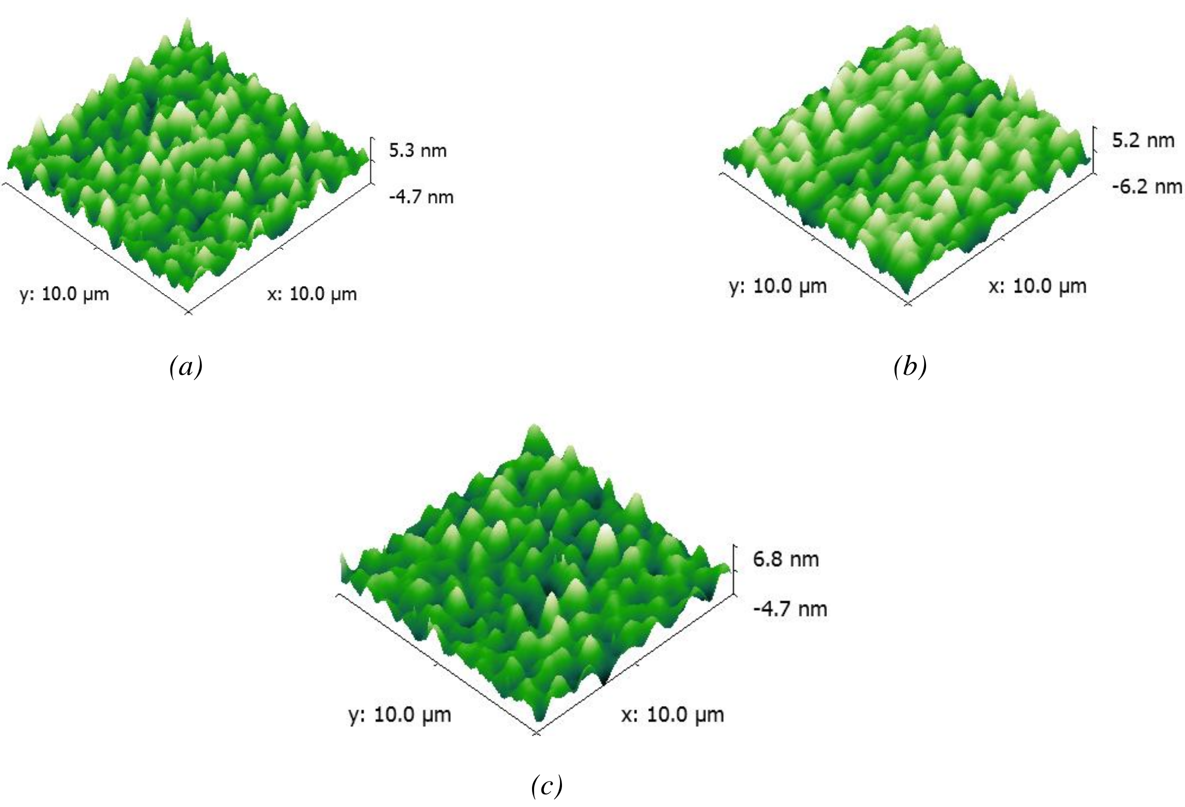


Figure 38: 10µm × 10µm AFM images for $Si_{0.3}Ge_{0.7}$: (a) without Ge under-layer (b) with 52nm Ge under-layer (c) with 102 nm Ge under-layer

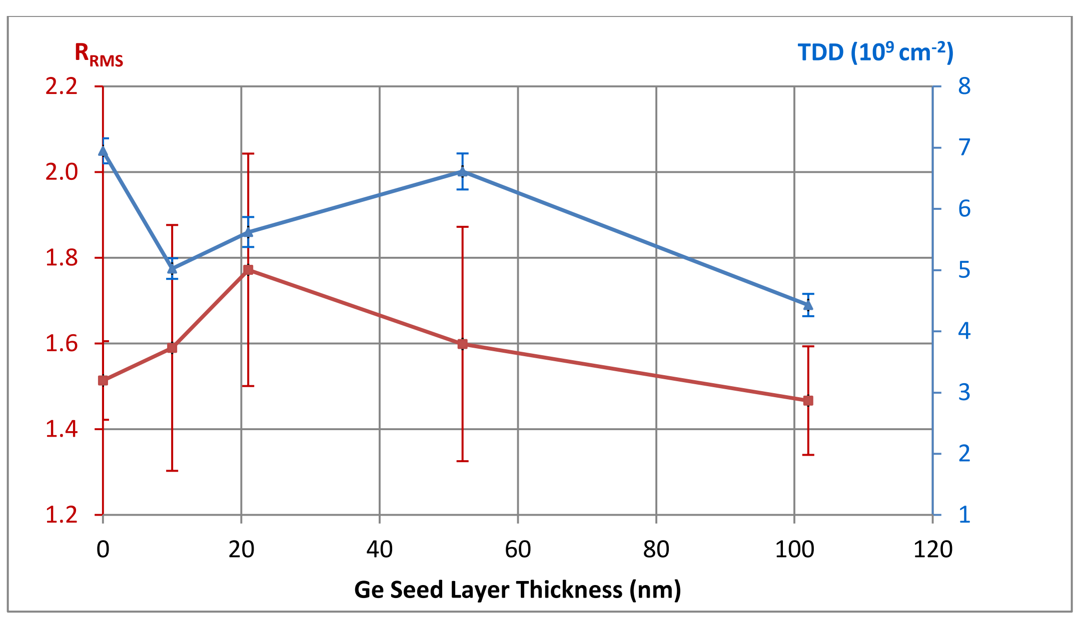


Figure 39: the R_{RMS} and TDD show a relatively similar trend similar trend for $Si_{0.3}Ge_{0.7}$

A plot of R_{RMS} and *TDD* versus varying Ge under-layer thickness was plotted and the results are shown. The samples show a considerable decrease in R_{RMS} values than for $Si_{0.05}Ge_{0.95}$. This result is somewhat unexpected since the expectation was that a lower lattice mismatch between the Ge under-layer and a 95% SiGe sample than a 70% SiGe sample would yield a smoother surface. However, the possible explanation for this result is due to the *TDD* values. The 95% SiGe batch showed *TDD* values ranging from (1.93- 4.23) × 10^9 cm^{-2}, while the 70% SiGe batch had a *TDD* value ranging from (4.43-6.61) × 10^9 cm^{-2}. The concept is that a greater number of TDs reaching the sample's surface will cause an increase in R_{RMS}.

4.3 Discussion of Samples being tested

Both batches of samples showed consistency in relaxing from a value just below 100%, and being under compressive strain, to a value just above 100%, and then being under tensile strain. The samples showed that the R_{RMS} is roughly one order of magnitude lower for 70% Ge content SiGe

layers than 95%. The resulting R_{RMS} values are in general agreement with the work done by Xie et al which states that materials that go through a state of compressive strain to a state of tensile strain will have a reduced R_{RMS} value [50]. This phenomenon can easily be visualised by considering a sinusoidal wave. Assume that the amplitude represents the roughness of a surface. If the wave is stretched in the x-direction, the amplitude will decrease and therefore so will the surface roughness. However, if the wave is compressed in the x-direction, the amplitude will increase and therefore the surface roughness increases. Also, figure 36 ($Si_{0.05}Ge_{0.95}$) gives a roughly 4% lattice relaxation range while figure 40 ($Si_{0.3}Ge_{0.7}$) roughly only 2% which is in agreement with their expected lattice mismatches for the SiGe over-layer.

Turning to *TDD* values, figure 40 shows two sample structures with varying lattice constants grown on a similarly sized substrate (red blocks). The $Si_{0.3}Ge_{0.7}$ structure (blue blocks) has a smaller lattice constant than the $Si_{0.05}Ge_{0.95}$ structure (green blocks).

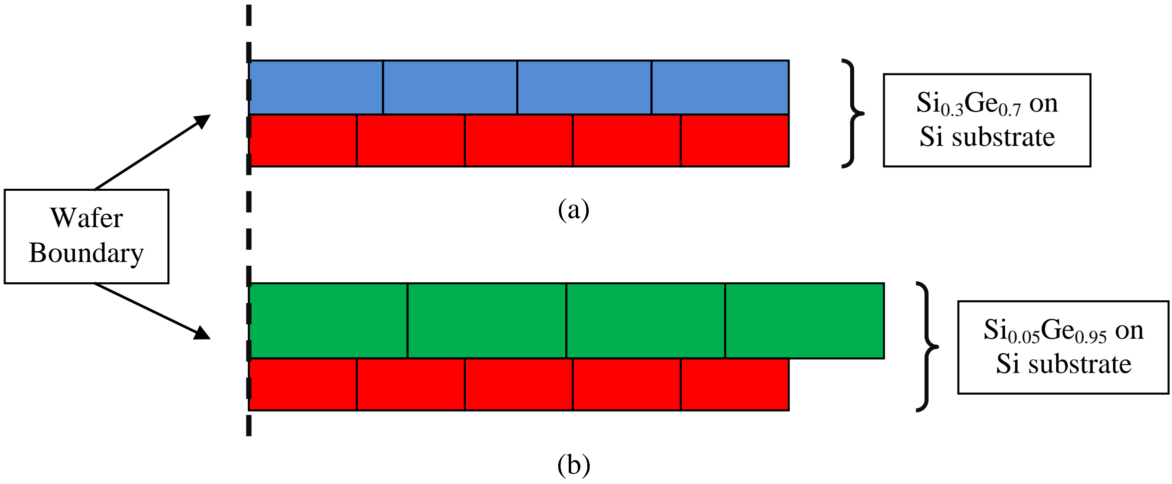


Figure 40: (a) The Si0.3Ge0.7 structure is in registry with a substrate. While (b) a larger lattice constant layer grown on a similarly sized substrate would yield a higher TDD value due to a larger number of misfit dislocations

Both sample structures from figure 40 represent the samples grown in this investigation without a Ge under-layer. The theory behind the *TDD* values is understood by considering the fact that when *n* Si

atomic planes line up with an *n-m* SiGe planes, then the number of misfit dislocations would be the difference between the lattice constants of the two planes, which in this case is simply *m.* The conclusion of which would suggest that $Si_{0.05}Ge_{0.95}$ would yield a higher TDD value because of a larger lattice constant than $Si_{0.3}Ge_{0.7}$. The data obtained however shows that the values for $Si_{0.05}Ge_{0.95}$ and $Si_{0.3}Ge_{0.7}$ are 2.90×10^9 cm^{-2} and 6.95×10^9 cm^{-2}, respectively. The discrepancy of this result could be due to the fact that Ge segregation from the seed layer to the alloy layer (as is evident in figure 37) significantly distorted the % Ge content composition, thereby rendering the lattice constants used for calculation erroneous.

However, considering the *TDD* values for the samples grown with a Ge under-layer, both sets of samples exhibited a similar trend. From roughly 10-50 nm, all *TDD* values are within the computed error margins. However, a thickness greater than 50 nm shows a sharp decline in *TDD*. The reason for this is because with an increased thickness, *TDs* have more space to combine as is seen in figure 32. It is worth noting however that this dramatic drop in *TDD* is easily noticeable because the *TDD* value is relatively high, in comparison to published works, which gives a greater probability for TDs to combine.

5 Conclusion and Future Work

R_{RMS} values obtained from this study for $Si_{0.05}Ge_{0.95}$ and $Si_{0.3}Ge_{0.7}$ were (3.7-8.1) nm and (1.47- 1.77) nm, respectively. *TDD* values were all of the order of $10^9 cm^{-2}$. However the 70% Ge content samples exhibited higher *TDD* values with an average *TDD* of 5.73×10^9 cm^{-2}, while 95 % Ge content samples had an average *TDD* value of 3.36×10^9 cm^{-2}.

The values obtained for $Si_{0.3}Ge_{0.7}$ were in general agreement with the values obtained by Capellini et al. [37] except for the *TDD* values which were 2 orders of magnitude lower than those presented in this study (10^9 cm^{-2}). The reason for this is because of the varying growth parameters. This study involved annealing the SiGe layer for 5 minutes at 800 °C. However, Capellini used a 2-step deposition of Ge at low and high temperatures. This limited the propagation of TDs to the top SiGe surface as was seen in figure 22. The research did also mention that the *TDD* value was 10^9 cm^{-2} before the growth of high temperature Ge deposition, the same *TDD* value as was obtained from this research.

Although the samples do yield a high *TDD* value, a list of some of the advantages with the samples grown is:

- Low R_{RMS} values of a few nanometers will results in device fabrication without the use of CMP, thereby saving time and money to industry.
- Relatively thin structure provides high thermal conductivity for use in power generation applications [41].
- Wafer bending is suppressed due to the growth of thin layers.

From the results obtained in this research, further work still needs to be done to reduce *TDD* by varying growth and structural parameters such as varying:

- Annealing temperature and annealing time.
- Structural growth temperature.
- Varying structural parameters:
    1. Thin linear grading structures.
    2. Thin terrace grading structures- involves the growth of both linear and constant composition layers.

The samples grown do show great potential in enhancing the quality of buffer layers as the samples where less than 400 nm in total thickness and relaxation of 100% was achieved. Further work still needs to be done to enhance thin SiGe buffer layers on Si (100) substrates to reduce *TDD*.

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