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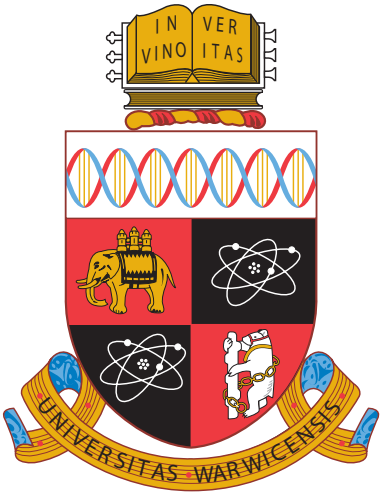

Low Temperature Semiconductor-Superconductor Junctions & Their Optimisation

by

James Sedgwick Richardson-Bullock

Thesis

Submitted to the University of Warwick

for the degree of

Doctor of Philosophy

Department of Physics

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THE UNIVERSITY OF
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Contents

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Lastly, I should like to thank my wife Rachael Richardson-Bullock. Fully expressing the depth of her care, consideration and patience and the resulting love and gratitude I feel towards her would likely put this document over the page limit.

'The scientist does not study nature because it is useful to do so. He studies it because he takes pleasure in it, and he takes pleasure in it because it is beautiful. If nature were not beautiful it would not be worth knowing, and life would not be worth living. I am not speaking, of course, of the beauty which strikes the senses, of the beauty of qualities and appearances. I am far from despising this, but it has nothing to do with science. What I mean is that more intimate beauty which comes from the harmonious order of its parts, and which a pure intelligence can grasp.'

— *Jules Henri Poincaré*

Declarations

This thesis is submitted to the University of Warwick in support of the author's application for the degree of Doctor of Philosophy. Except where specifically stated, all investigations and experiments presented herein were carried out by the author or by specialists under his direction.

Abstract

The research presented in this thesis focuses on the relatively young field of direct electron cooling via semiconductor-superconductor tunnel junctions. These devices utilise the superconducting energy gap to form a high pass electron filter, capable of lowering the effective electron temperature in the semiconductor electrode. The presented research focuses on optimizing the performance of such junctions i.e. the minimum achieved electron temperature, primarily by modifying the electrical properties of the semiconductor/superconductor and influencing the quality of the semiconductor-superconductor interface.

In the semiconducting electrode, the effect of carrier type on the thermal coupling of the system is studied, as is the effect of mechanical strain, induced via lattice mismatch. A study is made of alternative superconductors, modifying their properties through the use of thin films for the superconducting contact.

Finally, a comprehensive investigation is presented into the importance of fabrication procedures on device characteristics, leading to the development of the first semiconductor-insulator-superconductor junction.

List of Publications

Refereed Articles

2014 Advances in Semiconductor Electron Cooling using Improved Superconductor Tunnel Junctions

D. Gunnarsson, **J. S. Richardson-Bullock**, M. J. Prest, N. Hung, A. Timofeev, M. Prunnila, T. E. Whall, E. H. C. Parker and D. R. Leadley, *in preparation for submission to Nature Communications.*

2014 Comparison of electron-phonon and hole-phonon energy loss rates in silicon

J. S. Richardson-Bullock, M. J. Prest, M. Prunnila, D. Gunnarsson, V. A. Shah, A. Dobbie, M. Myronov, R. J. H. Morris, T. E. Whall, E. H. C. Parker and D. R. Leadley, *accepted for publication in Solid State Electronics.*

2014 Superconducting platinum silicide for electron cooling in silicon

M. J. Prest, **J.S. Richardson-Bullock**, Q. T. Zhao, J. T. Muhonen, D. Gunnarsson, M. Prunnila, V. A. Shah, T. E. Whall, E. H. C. Parker and D. R. Leadley, *accepted for publication in Solid State Electronics.*

2012 Electrical isolation of dislocations in Ge layers on Si(001) substrates through CMOS-compatible suspended structures

V. A. Shah, M. Myronov, C. Wongwanitwatana, L. Bawden, M. J. Prest, **J. S. Richardson-Bullock**, S. Rhead, E. H. C. Parker, T. E. Whall and D. R. Leadley, *Science and Technology of Advanced Materials*, volume 13, pp. 055002, 2012.

2011 Strain enhanced electron cooling in a degenerately doped semiconductor

M. J. Prest, J. T. Muhonen, M. Prunnila, D. Gunnarsson, V. A. Shah, **J. S. Richardson-Bullock**, A. Dobbie, M. Myronov, R. J. H. Morris, T. E. Whall, E. H. C. Parker and D. R. Leadley, *Applied Physics Letters*, volume 99, pp. 251908, 2011.

Conference Papers

2014 High Quality Semiconductor-Superconductor Junctions for Thermal Detectors and Electron Coolers

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2014 Strain and Interface Engineered Semiconductor-Superconductor Coolers and Detectors

D. Gunnarsson, **J. S. Richardson-Bullock**, M. J. Prest, A. Timofeev, T. Brien, M. Kiviranta T. E. Whall, E. H. C. Parker, D. R. Leadley, P. Mauskopf and M. Prunnila, *International Workshop On Low Temperatures Electronics (WOLTE).*

2014 New Concepts in Infra-red Bolometry

E. H. C. Parker, M. J. Prest, **J. S. Richardson-Bullock**, M. Myronov, T. E. Whall, D. R. Leadley, T. Brien, P. Mauskopf, D. Gunnarsson, M. Prunnila, M. Kiviranta and L. Piccirillo, *International Workshop On Low Temperatures Electronics (WOLTE).*

2014 High Quality Superconductor-Semiconductor Tunnel Junctions

D. Gunnarsson, **J. S. Richardson-Bullock**, M. J. Prest, H. Q. Nguyen, T. E. Whall, E. H. C. Parker, D. R. Leadley and M. Prunnila, *European Conference on Applied Superconductivity (EUCAS).*

2013 Electron-Phonon Coupling Engineering for Thermal Devices

M. Prunnila, D. Gunnarsson, **J. S. Richardson-Bullock**, M. J. Prest, T. E. Whall, E. H. C. Parker, L. Donetti and F. Gamiz, *European Materials Research Society (EMRS)*.

2013 Cooltronics: A new low-temperature tunneling-technology based on Silicon

T. E. Whall, M. J. Prest, **J. S. Richardson-Bullock**, V. A. Shah, M. Myronov, E. H. C. Parker, D. R. Leadley, M. Prunnila, D. Gunnarsson, T. Brien, D. Morozov and P. Mauskopf, *Ultimate Integration on Silicon (ULIS).*

2013 Hole-phonon energy loss rate in boron doped silicon

J. S. Richardson-Bullock, M. J. Prest, M. Prunnila, D. Gunnarsson, V. A. Shah, A. Dobbie, M. Myronov, R. J. H. Morris, T. E. Whall, E. H. C. Parker and D. R. Leadley, *Ultimate Integration on Silicon (ULIS).*

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2012 Ultra-High Hall Mobility ($1\times10^6 cm^2V^{-1}S^{-1}$) in a Two-Dimensional Hole Gas in a Strained Germanium Quantum Well Grown by Reduced Pressure CVD

A. Dobbie, M. Myronov, R. J. H. Morris, M. J. Prest, **J. S. Richardson-Bullock**, A. H. A. H Hassan, V. A. Shah, E. H. C. Parker, T. E. Whall and D. R. Leadley, *Silicon-Germanium Technology and Device Meeting (ISTDM).*

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2011 Improved Cooling Performance in Strained Silicon Tunnel Junctions

J.S. Richardson-Bullock, M. J. Prest, J. T. Muhonen, M. Prunnila, D. Gunnarsson, V. A. Shah, R. J. H. Morris, A. Dobbie, M. Myronov, T. E. Whall, E. H. C. Parker and D. R. Leadley, *Silicon Epitaxy and Heterostructures (ICSI).*

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Abbreviations and Symbols

BCS	Bardeen Cooper Schrieffer theory of superconductivity and the origin of the superconducting band gap
β	A parameter describing the fraction of power deposited in the superconducting electrode and that is returned to the semiconductor
Δ	Superconductor half band gap
E_F	Fermi level/energy
Γ	Quality factor given by the ratio of the normal state resistance and the sub-gap resistance
IV	Current-Voltage
NEP	Noise Equivalent Power
N-I-S	Normal metal - insulator - superconductor
Ω	Actively cooled volume of a given device
P_C	Voltage dependent cooling power
P_{e-ph}	Heating power manifested as a result of energy loss between electrons and phonons
P_J	Heating power caused by Joule heating
P_{opt}	Cooling power at an optimum bias voltage
P_{QP}	Heating power associated with quasiparticle effects
PtSi	Platinum Silicide
R_S	Sheet resistance
R_{Sm}	Resistance of semiconductor electrode
R_T	Normal state tunnelling resistance
Sm-I-S	Semiconductor - insulator - superconductor
Σ	Carrier - phonon conductance
TLM	Transfer Length Method
TJC	Tunnel Junction Cooler
T_b	Bath temperature
T_C	Superconductor critical temperature
T_e	Electron temperature
T_{min}	Minimum electron temperature
V_C	Voltage across a cooler junction
V_T	Voltage across a thermometer junction
VT	Voltage-Temperature

1

Introduction

1.1 The need for cryogenics

The most accurate and sensitive scientific equipment ever built operates in the low temperature regime. Terahertz security cameras that generate and capture imaging radiation at 10 K are now a common site in airports [1]. Cutting edge hospital magnetoencephalography machines study the human brain with electronics operating at 4 K [2], and the D-Wave system, hailed as the world's first quantum computer, is built around a chip set kept at a cool 20 mK [3].

For these systems it is not technology that limits their ability to function, but the background noise that can obscure or destroy whatever it is they are studying. Quantum computers for example, require the sub-kelvin environment necessary to both read and manipulate information free from the coherence shattering chaotic and classical effects associated with higher temperatures [4].

Low temperature environments are subsequently used in applications that include the most powerful computers on the surface of the planet and the most advanced satellites orbiting above it. Furthermore, a vast proportion of modern day astronomical instruments rely on the low thermal noise of the sub-Kelvin environment. The Background Imaging of Cosmic Extragalactic Polarization (BICEP) experiment [5] and the Atacama B-Mode Search [6] are two recent examples, utilis-

ing a temperature of $\sim 300\,\mathrm{mK}$ to garner increasingly detailed images of the cosmic microwave background (CMB). Similarly, on board the Planck space observatory [7], ultra-sensitive radiation detectors cooled to 100 mK continuously scan the CMB for anisotropies and structures in the after effects of the big bang, hoping to shed light on the begins of the universe.

Unfortunately, operating at these temperatures can prove to be very difficult and perhaps more importantly, prohibitively expensive.

Currently, such temperatures are reached through conventional cryogenic systems that consume ^{3}He, utilising its low boiling point [8]. This element is in increasingly short supply, is difficult to store and transport, and its use limits the operational lifetime of remote cryostat systems which will eventually run dry. Furthermore, for non-terrestrial experiments and applications that require a sub-Kelvin sensing environment, the difficulty and monetary cost of carrying a liquid helium supply into orbit presents a serious impediment.

Tunnel junction coolers (TJCs) [9, 10] form part of a relatively young area of cryogenics that has generated a great deal of interest in its short life. Through the use of an energy selective tunnel junction the effective temperature of an electron population in a conducting material can be lowered. This cooling can in turn be used to reduce the temperature of thermally contacted bulk material [11], allowing for cryogen free refrigeration. The cooling power associated with TJCs is typically of the order of picowatts ($10^{-12}\,\mathrm{W}$) [12], implying that their operational range is limited to sub-Kelvin temperatures where the heat load is sufficiently low so as to be overcome. Established closed cycle cooling methods, such as pulse tube refrigerators (section 3.1.1) and adsorption pumps (section 3.1.2) are capable of handling cooling from 300 K to 3 K and 3 K to 0.3 K respectively, therefore combing these technologies would allow TJCs to form the final stage of a compact, all electrical/dry cooling route from room temperature down to 0.01 K. Additionally, with reports of TJCs cooling from temperatures as high as 1 K [13], there is the possibility of bypassing

the adsorption stage altogether, leading to simpler cryostat operation and a further conservation of cryogenic material.

Such cryogen-free systems could see the application of low noise environments to entirely new projects, domestic, laboratory and otherwise, that would previously have been impossible due to the high cost and large volumes imposed by conventional cryogenics.

Furthermore, TJCs have more direct applications to the fields of bolometry and remote sensing in which the cooled electrons themselves form part of a detector circuit with the high signal to noise ratio afforded by low temperature operation. The absence of moving parts and subsequent vibrations is also a major benefit to this field of applications.

To summarise, with TJCs forming part of a self-contained, low running cost cooling system, existing cryogenics can become cheaper and more accessible, having a significant impact on the worlds of astronomy, computing and medicine in which low temperature sensing is key.

1.2 Thermoelectric cooling and the alternatives

Thermoelectric cooling has been an active field of research since the discovery of the thermoelectricity by T. J. Seebeck in 1821 [14]. The Seebeck effect describes the generation of an electric current through a junction formed of two different conductors in the presence of a thermal gradient. When this process is reversed, a current flowing through the junction will establish a temperature difference between the two sides in a process known as the Peltier effect [15].

The Peltier effect can be explained as follows. When a junction is formed from two materials with differing electrical conductivity there will exist a voltage between them, known as the contact potential. Depending on the sign of this potential, charge carriers accelerated across the junction will either absorb or radiate energy,

resulting in local cooling or heating at the material interface.

Utilising this method, Peltier coolers are capable of maintaining a temperature difference across a device of around 70 K at room temperature [16], though they are limited by the size and thermal conductivity of their component materials, with performance dropping to only a few degrees at 77 K [17], making them rather unsuitable for modern cryogenic applications.

Adiabatic demagnetization refrigerators (ADRs) were the next step in cryogenic technology and were first successfully demonstrated in 1933 [18]. They operate through the application of large magnetic fields (of the order of several tesla [19]) to an electromagnetic spin system. The spins orientate themselves with the magnetic field and when this field is removed, the spins relax into a random distribution, absorbing thermal energy in order to perform their reorientation. ADRs can typically access temperatures of the order of 100 mK, with systems utilising the spins of paramagnetic salts reaching 38 mK [20]. Furthermore, special types of ADRs known as an NDRs or a nuclear demagnetization refrigerators work with the magnetic dipoles of atomic nuclei rather than electrons, and have been demonstrated to cool a solid to temperatures as low as 2 μK [21].

Unfortunately, ADRs and NDRs suffer from a number of drawbacks. The high magnetic fields require superconducting magnets, which require a large amount of power to operate and must be constantly cooled below their transition temperature. Additionally, Adiabatic demagnetization is a 'one shot' method, in that the cooling power of the system is delivered in one temporary burst when the magnetic field is disengaged and the spins disorient. Once the minimum temperature is achieved, the system will begin to warm, and the magnetization cycle must be repeated. This naturally limits its use to short time-scale applications.

Dilution refrigerators were developed in order to solve this issue. They operate using a mixture of ^{3}He and ^{4}He and are capable of continuous operation at temperatures below 100 mK, with base temperatures approaching 1 mK [22]. The

operational principles of dilution refrigerators are explained in detail in section 3.1.3.

Whilst it is possible to cool further via this method, practical limitation come into play. Chiefly, dilution refrigerators require a large amount of power and their base temperature exponentially proportional to the volume of the helium mixing chamber, leading to impractically large designs [23, 24].

1.3 Tunnel junction coolers

Tunnel junction coolers stand apart from the preceding cryogenic technology, offering sub-Kelvin temperatures without any of the moving parts, cryogens, magnetic fields or high power requirements of the competition. They instead operate on the principle of direct electron cooling. Similar in concept to the 'Maxwell's demon' thought experiment [25], the technique utilises an energy dependent filter to selectively remove electrons with an energy greater than the population average, denoted by the Fermi level E_{FN}. This leads to a sharpening of the Fermi distribution and the remaining electrons can be said to have been cooled. This method was pioneered in the normal metal - insulator - superconductor (N-I-S) junction [26, 27] which utilises the band gap of a superconductor as the energy filter.

1.3.1 The superconducting band gap

Superconductivity was first formally explained Bardeen, Cooper and Schrieffer in the well known theory that bears their names (BCS) [28]. It details the formation of a band gap in superconducting materials, a range of energy within which the electron density of states is zero. In other words, superconductors are capable of discriminating between electrons of certain energies, conducting some and blocking others.

This energy gap Δ is related to the superconducting transition temperature

T_C according to the expression

$$\Delta_0 = 1.764 k_b T_C, \tag{1.1}$$

common to all superconducting materials, where Δ_0 is the energy gap at a temperature of 0 K.

BCS theory also predicts how the band gap will change with the temperature of the superconductor, with $\Delta = 0$ at T_C, the point at which superconductivity is extinguished. This relationship is derived in references [29] and [28] and is shown in figure 1.1.

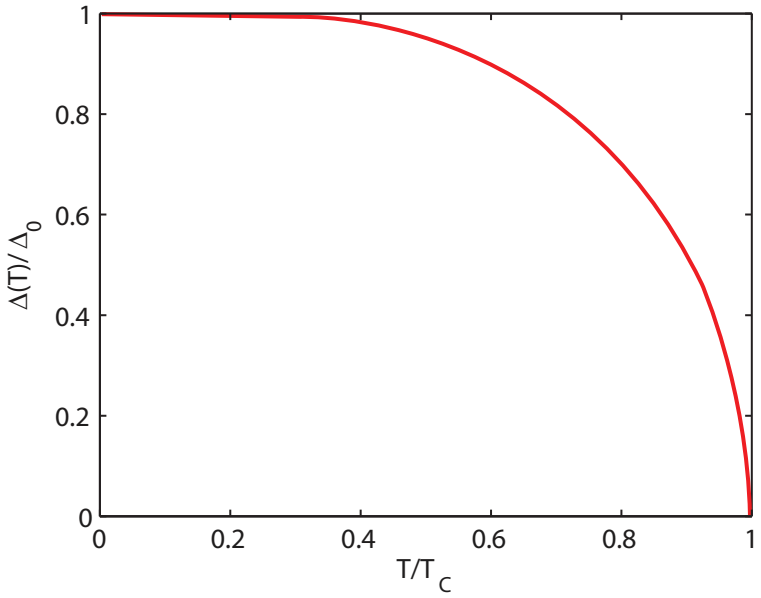


Figure 1.1: Variation of band gap with temperature.

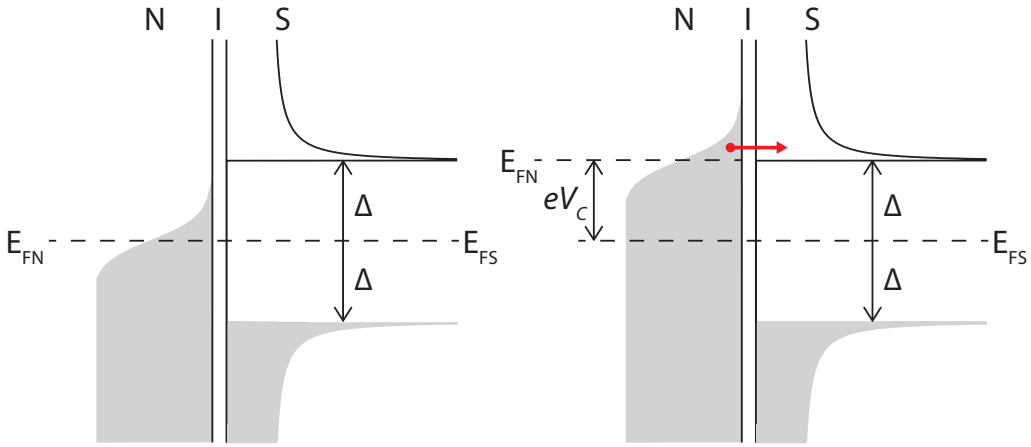
It is immediately apparent that providing $T < 0.4T_C$, the band gap is approximately equal to its zero temperature magnitude. Given that the results presented within this thesis are drawn from experiments carried out well below this limit, it should be noted that within this investigation the temperature dependance of Δ is largely ignored, with $\Delta = \Delta_0$ assumed throughout.

With the band gap energies of many superconductors being well known [30],

it is possible to design and operate devices that take advantage of their selectivity.

1.3.2 Normal metal - insulator - superconductor junctions

An energy diagram of a normal metal - insulator - superconductor junction is presented in figure 1.2 and shows the energy distribution of the electrons in the normal metal relative to the band energies of the superconductor (with a half-band gap of Δ). The metal and superconductor are separated by a thin insulating tunnel barrier which breaks thermal equilibrium and enables a bias voltage to be applied across the two electron subsystems.



(a) Unbiased.

(b) Biased at an optimum voltage of $V_C = \Delta/e$, with each tunnelling electron removing an energy $E - eV$ from the metal side, where e is the charge of a single electron.

Figure 1.2: An energy level diagram of an N-I-S junction with and without an applied bias.

For temperatures $k_B T \ll \Delta$, all states below the band gap in the superconductor will be occupied, whilst all states above will be empty. If the junction is unbiased, as is the case in figure 1.2a, there is no electron transfer across due to the energy inequality between the electrons in the metal and the available (unoccupied) states in the superconductor. If, however, a voltage bias is applied so as to lift the Fermi-level of the metal towards the upper edge of the superconductor band gap,

electrons with energy $E > E_{FN}$ will be preferentially removed from the metal, as shown in figure 1.2b. This ability to filter 'hot' electrons is lost if the junction is biased beyond the energy gap, at voltages greater than $V_C = \Delta/e$, illustrated in figure 1.3. The junction is therefore said to be optimally biased at $V_C = \Delta/e$, at which point the electron temperature will minimize.

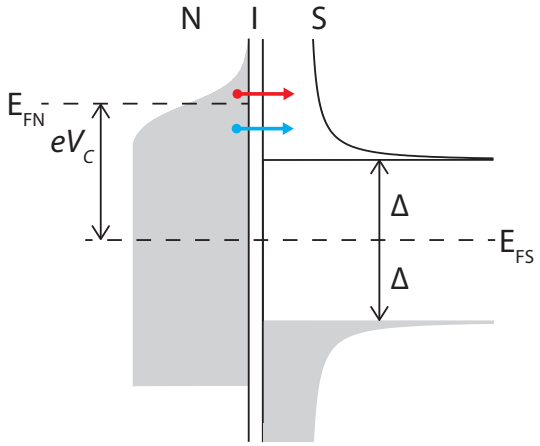


Figure 1.3: When the Fermi level in the metal is biased above the superconducting band edge both 'hot' and 'cold' electrons (with energy $E < E_{FN}$) are able to tunnel out. This removes the cooling effect and leads to heating in the device due to the uncompensated ohmic heating (see section 1.4.6).

1.3.3 Semiconductor - superconductor junctions

Semiconductor - superconductor (Sm-S) junctions were developed as an alternative to N-I-S devises, replacing the normal metal with a highly doped semiconductor [31]. A moderately doped semiconductor (with a dopant concentration below 10^{18}cm^{-3} in the case of silicon [32]) contains individual impurities that act as localized states, donating carriers by thermionic emission or phonon-assisted tunnelling. At higher doping concentrations these localized states can be treated as a continuous impurity band and the semiconductor will act as a conductor with a temperature independent resistance, though possessing far fewer charge carriers than a true metal. Such a semiconductor is classified as degenerate [32].

In principle, the reduced electron density in semiconductors makes it easier to reach lower electron temperatures given that less entropy has to be extracted from the system, however, this limits their ability to cool a thermally connected load and makes them less suitable to cooling bulk material [11].

The Schottky tunnel barrier that forms between a degenerate semiconductor and a superconductor ([32], [33], [34]) is employed in the same role as the insulating layer in an N-I-S device, forming an energy-selective tunnel junction with the superconductor. The automatic formation of the barrier simplifies device fabrication and allows for the tunnelling probability (and hence the resistance of the junction) to be tuned by controlling the doping density. These advantages over the N-I-S designs are coupled with a greater robustness and reliability [35] as well as industry compatible, high yield micromachining techniques.

Sm-S devices do however suffer from some drawbacks, most notably the fact that even highly doped semiconductors have a higher resistivity than metals (due, at least in part, to the smaller density of states at the Fermi level) and it is of the order of $(10-100)\,\mathrm{k\Omega\,\mu m^2}$ as compared to $(1-2)\,\mathrm{k\Omega\,\mu m^2}$ [11] or $0.3\,\mathrm{k\Omega\,\mu m^2}$ [36] for metal coolers. The tunnel resistance across the Schottky barrier of an Sm-S junction is therefore, in general, higher than the tunnel resistance across the insulator used in a N-I-S junction. This is currently a major factor in limiting device performance.

1.3.4 Double junctions

In practice, two junctions are often used in series in a symmetric configuration, as shown in figure 1.4. The second junction assists in the cooling of the system by enabling electrons with energy below the Fermi level to replace the more energetic electrons that are removed by the first junction. Furthermore, this serves to prevent charge build up within the device. Within this investigation, all devices utilize such a double junction geometry, with an optimum operational voltage of $V_C = 2\Delta/e$, or Δ/e per junction, as in the single junction case.

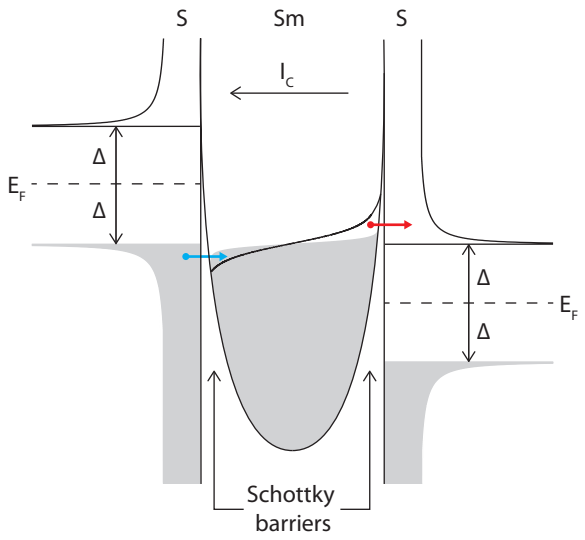


Figure 1.4: An energy level diagram of an S-Sm-S junction depicting the energy distribution of electrons in the conduction band of the semiconductor and the conduction and valence bands of the superconductor. Although the Schottky barrier is not susceptible to the same defects as an oxide layer, impurities and surface imperfections will still affect the barrier height and tunnelling resistance.

1.4 Tunnel junction theory

1.4.1 Metal-semiconductor contacts

To understand the operating principle of a semiconductor-superconductor tunnel junction cooler it is necessary to first understand the nature of the interface between a metal and a semiconductor (as summarised in Rhoderick [34], Schroder [33] and Sze [32]).

The work function of a solid Φ is defined as the difference in energy between the vacuum level (the energy of a free electron in vacuum) and the Fermi level, or in other words, the energy required to free an electron with energy E_F from a material. The electron affinity χ of a semiconductor is defined as the energy difference between the vacuum level and the conduction band edge. The requirement for both the vacuum level and the Fermi level to be continuous across the metal-semiconductor interface results in the formation of a potential barrier; the magnitude of which Φ_B

can be expressed as the difference between the metal work function Φ_M and the electron affinity, as shown in figure 1.5.

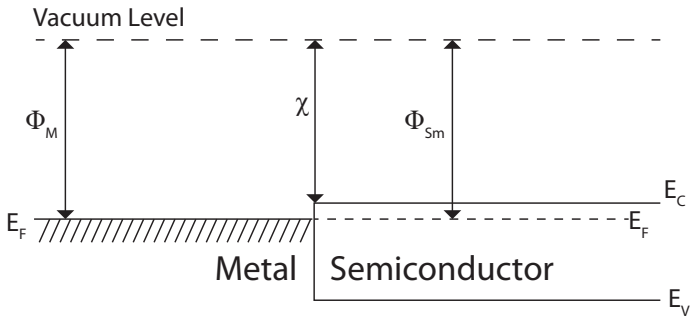
$$\Phi_B = \Phi_M - \chi. \tag{1.2}$$

This is known as a Schottky barrier and according to equation 1.2, its height is independent of the doping density in the semiconductor and any of the three types of barrier shown in figure 1.5 can be implemented simply by choosing a metal with the appropriate work function.

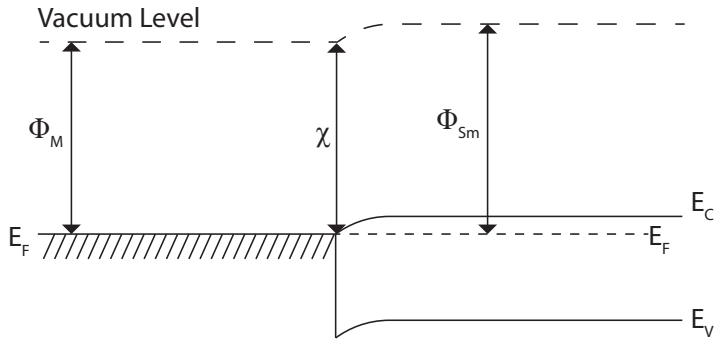
In reality, barrier heights and types determined by experiments [37] exhibit only a weak dependence on the work function of the metal, with a depletion type contact forming in almost all cases. Figure 1.6 shows a depletion contact to n-type silicon, which proves to be the most relevant case to this investigation.

As indicated by figure 1.6a, at the moment of contact electrons will pass from the semiconductor into the metal and the Fermi levels will align. The excess negative charge on the metal side of the interface is balance by the now uncompensated donor ions in the electron depleted region of the semiconductor. These donor atoms, which occupy a width w, proportional to the difference in the semiconductor and metal work functions, give rise to a uniform space charge and an electrostatic potential that increases quadratically towards the interface ($\propto w^2$), resulting in the barrier depicted in figure 1.6b.

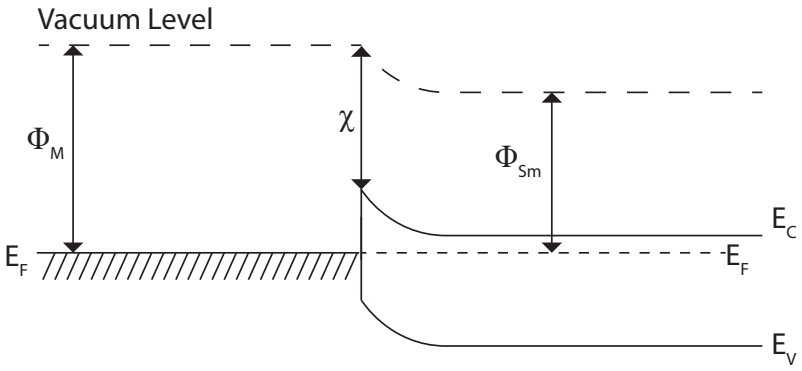
The apparent insensitivity of barrier height to work function is often attributed to a phenomenon known as Fermi level pinning. In broad terms, this involves the Fermi level in the semiconductor being pinned at some energy in the band gap as a result of states present at the interface between the semiconductor and the metal. It has been suggested that these states may be dangling bonds [38] and that their density can be affected by preparation of the semiconductor surface [39]. Regardless of their nature, their effect on contact formation can be explained



(a) Neutral, $\Phi_M = \Phi_{Sm}$

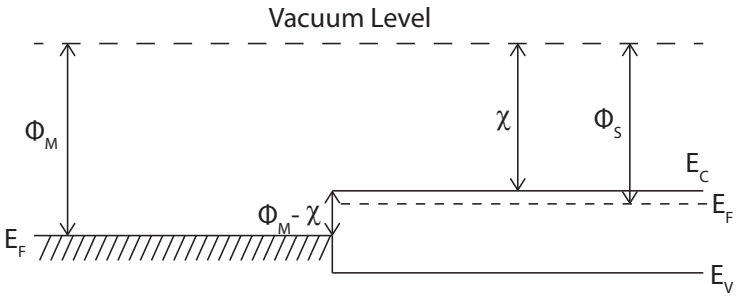


(b) Accumulation, $\Phi_M < \Phi_{Sm}$

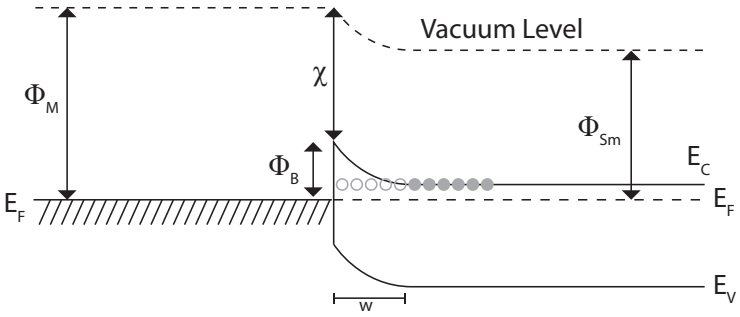


(c) Depletion, $\Phi_M > \Phi_{Sm}$

Figure 1.5: The three possible band structures of a metal-semiconductor interface, depending on the relative values of the metal and semiconductor work functions, Φ_M and Φ_{Sm}. Thermal equilibrium forces the Fermi levels in the two materials to be continuous across the interface.



(a) Prior to contact.



(b) In contact, with open (shaded) circles representing uncompensated (compensated) donors.

Figure 1.6: A more detailed diagram of a depletion contact showing the band structure immediately prior to and after contact.

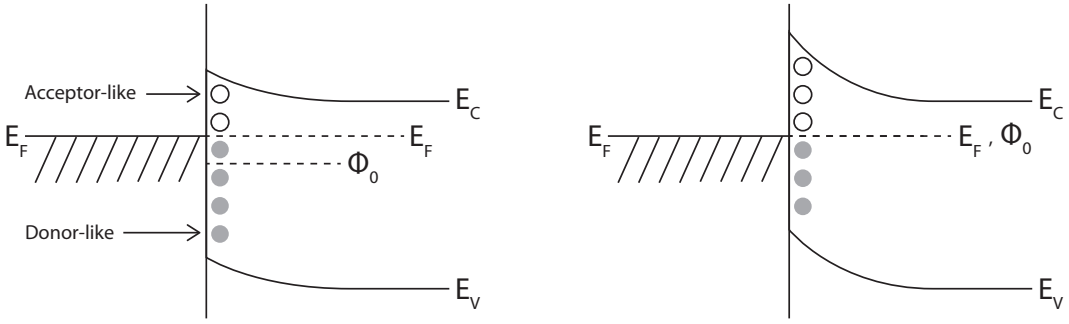
by imagining a constant distribution of states at the metal-semiconductor interface, centered around a neutral level ϕ_0 as shown in figure 1.7.

Conservation of charge across the junction requires that

$$Q_M + Q_D + Q_{SS} = 0 \tag{1.3}$$

with Q_M being the negative charge on the metal surface, Q_D representing the positive charge due to the uncompensated donors in the semiconductor and Q_{SS} being the charge due to surface/interface states.

The occupancy of these states is determined by the Fermi level and if we fo-



(a) Initial barrier height expected when ignoring interface states.

(b) Pinning and its affect on the Schottky barrier height.

Figure 1.7: Energy level diagrams showing the effect of the neutral level and the Fermi level being pinned together. Ocupied states (circles) are shaded.

cus on the case where ϕ_0 is below E_F, the surface states will contain a net negative charge. According to equation 1.3, Q_D must then be larger than it would be should the surface states be absent, implying a greater number of uncompensated donors. This results in an increase in the depletion width w along with a corresponding increase in the band bending and subsequently the barrier height, which (as mentioned earlier) is $\propto w^2$. Figure 1.7illustrates how the rise in Φ_B shifts the neutral level upwards, narrowing the gap between the neutral level and E_F and reducing the effective negative charge of the interface. It can therefore be seen that the surface states behave as a negative feedback loop, driving the Fermi level towards ϕ_0 and pinning it to the middle of the metal-semiconductor interface, effectively precluding the barrier types shown in figure 1.5a and 1.5b.

Clearly, this presents a problem when attempting to fabricate low resistance metal-semiconductor contacts for device purposes. Whilst electrons can be thermally excited across the Schottky barrier, these excitations become negligible at the low operational temperature relevant to this investigation. It is therefore desirable to modify the Schottky barrier in order to boost the probability of an electron being able to tunnel through quantum mechanically.

With the barrier height pinned and therefore relatively immune to engineer-

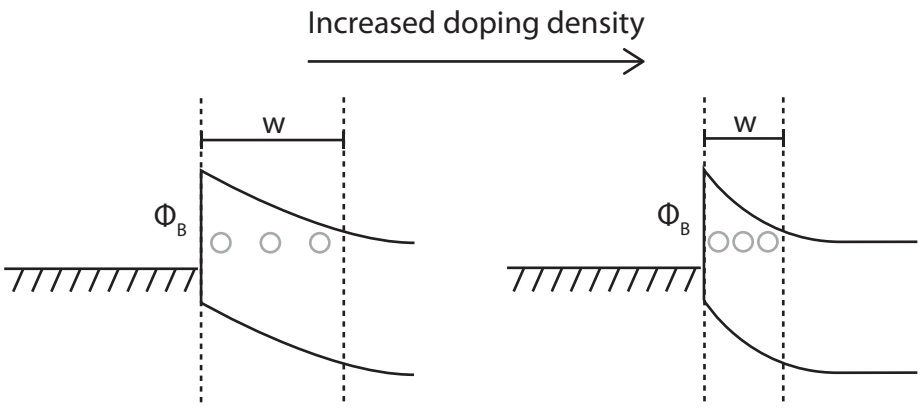
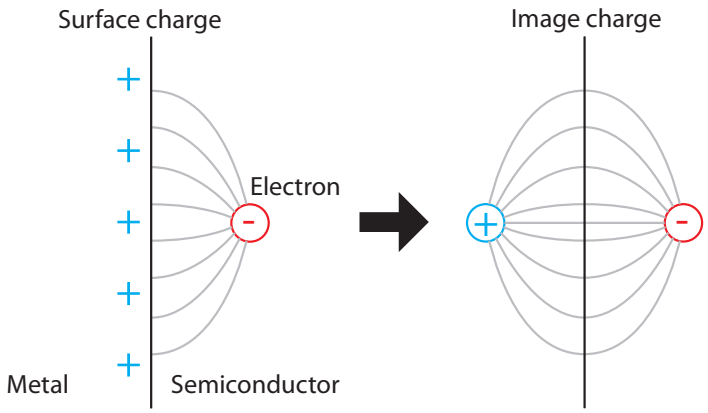


Figure 1.8: The affect of doping density on the width of the Schottky barrier.

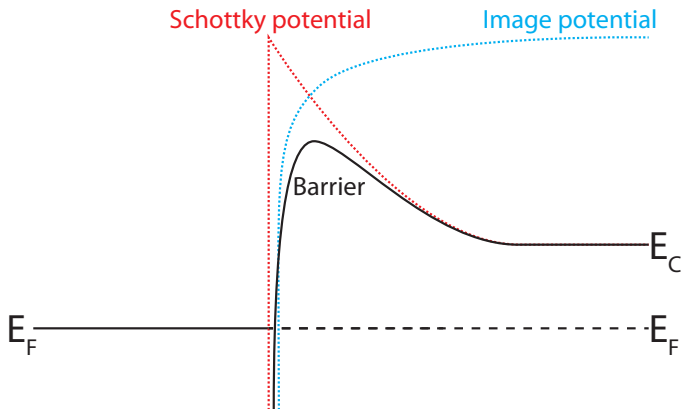
ing, it is necessary instead to reduce the barrier width which can be achieved by raising the doping concentration N_D of the semiconductor, thus increasing the uniform space charge on the semiconductor side of the contact [34]. This enables the accumulation of negative charge on the metal side to be balanced out by a shorter depletion region, producing a narrower barrier as illustrated by figure 1.8.

Furthermore, increased doping concentration will in fact lower the height of the Schottky barrier as a result of what is known as the image force [33]. Due to the fact that the electric field must be perpendicular to the metal surface, one can treat the situation of an electron approaching the barrier as that of approaching a positive charge in the position of its own reflection. This adds an 'image potential' of the familiar $1/r^2$ form to that of the Schottky barrier which results in a slight decrease in its magnitude ($\propto N_D^{1/4}$ [34]), depicted in figure 1.9

For high doping concentrations the Schottky barrier can become narrow enough at the base of the conduction band to allow for the direct tunnelling of electrons between the metal and the semiconductor (i.e. field emission rather than thermionic emission) and the contact can be thought of as ohmic, with a characteristic tunnel resistance R_T determined by the field emission probability [40].



(a) Surface charge and image charge equivalence.



(b) The addition of the two potentials and the resulting barrier.

Figure 1.9: Image force lowering of the barrier height.

1.4.2 Tunnel current

At temperatures below 1 K the thermal coupling between an electron gas and its associated crystal lattice can weaken [41], with the electron-phonon interaction rate dropping below the electron-electron iteration rate [42]. In other words, the internal relaxation rate of the electron system is faster than any external couplings. This allows the electrons to maintain a quasi-equilibrium, their energy described by the Fermi-Dirac thermal distribution with a well defined effective electron temperature. Furthermore, as a result of the decoupling, the electron system may be cooled to a

temperature below that of the lattice with only a moderate cooling power.

This cooling power arises from the current of electrons with energy greater than E_F leaving the semiconductor, each removing an energy $E - eV$ [26, 43, 44]. This current is given by [26, 45, 46, 36]

$$I = \frac{1}{eR_T} \int_{-\infty}^{\infty} F(E, V, T_e, T_b).g(E)dE \tag{1.4}$$

with

$$F = f(E - eV, T_e) - f(E, T_b), \tag{1.5}$$

where f is the Fermi-Dirac distribution function of electrons

$$f(E, T) = \frac{1}{exp^{E/k_bT} + 1}. \tag{1.6}$$

This current is illustrated in figure 1.10a.

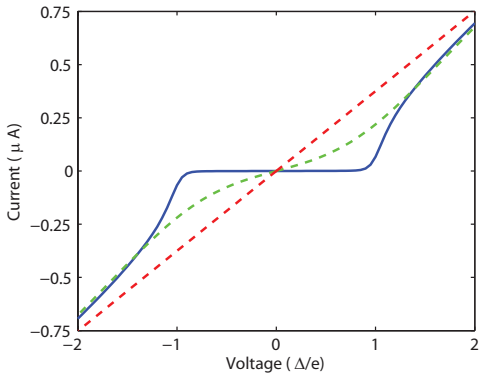
Here R_T is the tunnelling resistance across the Schottky barrier at the semiconductor-superconductor interface, T_e is the electron temperature in the semiconductor and T_b is the temperature of the superconductor, assumed to be equal to the temperature of the thermal bath. $g(E)$ is the density of states within the superconductor (see figure 1.10b) into which the electrons tunnel and can be written as [47, 46]

$$g(E) = \begin{cases} 0 & \forall |E| < \Delta \\ \frac{|E|}{\sqrt{E^2 - \Delta^2}} & \text{otherwise} \end{cases}$$

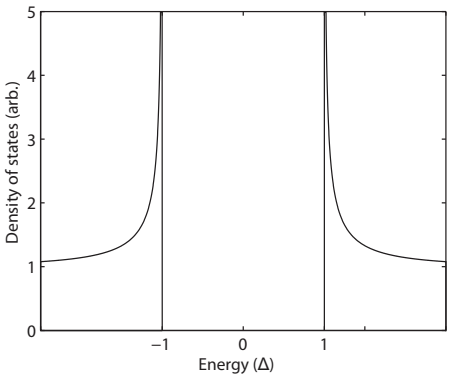
1.4.3 Cooling power

The current removes energy from the semiconductor at a rate [36]

$$P_C = \frac{1}{e^2 R_T} \int_{-\infty}^{\infty} (E - eV).F(E, V, T_e, T_b).g(E)dE \tag{1.7}$$



(a) Characteristic junction IV at 5 K (red), 1 K (green) and 0.1 K (blue)



(b) Superconductor density of states

Figure 1.10: The ideal IV characteristics and superconducting density of states of a single Sm-S tunnel junction [12]. The low temperature current is zero for $V < \Delta/e$ ($V < 2\Delta/e$ for a double junction), then asymptotically approaches the room temperature value given by $I = V/R_T$. R_T is often found in this way. At higher temperatures ambient electrons are more likely to gain enough energy through thermal excitation to tunnel across the junction, described by the broadening of the Fermi-Dirac distribution. The IV curve was calculated using equation 1.10 with the parameters: $\Delta = 0.2\,\text{meV}$ (aluminium) and $R_T = 500\,\Omega$.

In the low temperature limit ($T \leq \Delta k_B$), this cooling power can be approximated by an analytical function [48] that maximizes at

$$P_{opt} \approx \frac{\Delta^2}{e^2 R_T}\left[0.59\left(\frac{k_B T_e}{\Delta}^{3/2}\right) - \sqrt{\frac{2\pi k_B T_b}{\Delta}} \times exp\left(-\frac{\Delta}{k_B T_b}\right)\right]. \tag{1.8}$$

There exist alternative analytical expressions for this optimum power [36, 49, 44], however these are only valid in the situations where $(\Delta - eV)/k_B T_e >> 1$ or $\Delta = eV$, neither of which apply in the more relevant case described above.

The associated optimum tunnel current can also be written as

$$I_{opt} \approx 0.48\,(\Delta/eR_T)\sqrt{k_B T_e/\Delta}. \tag{1.9}$$

For a full derivation of equations 1.8 and 1.9, I refer the reader to the work of D. V. Anghel [50].

As mentioned in section 1.3.4, two junctions are often employed in series, doubling the cooling power and dividing the applied voltage between the two junctions equally. This results in equations 1.4 and 1.7 becoming [44, 9]

$$I = \frac{1}{eR_T}\int_{-\infty}^{\infty} F(E, V/2, T_e, T_b).g(E)dE \tag{1.10}$$

and

$$P_C = \frac{2}{e^2R_T}\int_{-\infty}^{\infty} (E - eV/2).F(E, V/2, T_e, T_b).g(E)dE \tag{1.11}$$

respectfully. It is clear from equation 1.11 that the cooling power has a strong dependence on the tunnelling resistance of the junction.

The current flow across the junction also gives rise to a number of heating mechanisms that limit electron cooling. Experimental investigations into Sm-S junctions have attributed these performance degrading powers to states in the superconductor band gap [51, 9], nonequilibrium effects [51], and quasiparticle back-tunnelling from the superconductor[52, 53]. What follows is a brief description of each of these mechanisms.

1.4.4 Sub-gap leakage and the Dynes parameter

Early experiments with Sm-S junctions [53] noted that at bias voltages below the superconductor band gap the current flow was in excess of that described by equation 1.10. This behaviour was termed sub-gap leakage. It can be accounted for by introducing the Dynes parameter [54] to the superconductor density of states, so that it becomes

$$g(E) = Real\left|\frac{E - i\Gamma}{\sqrt{(E - i\Gamma)^2 - \Delta^2}}\right|. \tag{1.12}$$

Γ modifies the superconducting density of states to allow for non-zero values within the band gap (as shown in figure 1.11a) and effectively parameterises the availability of sub-gap states. Such states are believed to be the result of non-idealities of

the superconductor material and include mechanical defects, impurities and the proximity of the normal state material (the inverse proximity effect) [47, 9].

At low energies $|E| \ll \Delta$ equation 1.12 equals Γ/Δ, as shown in figure 1.11a. Combining this with the result of Pekola et al. [55], who demonstrate that in the low temperature limit the current through an Sm-S junction is given by

$$I = \frac{1}{eR_T} \int_0^{eV} g(E) dE \tag{1.13}$$

and that the differential conductance is

$$\frac{dI}{dV} = \frac{g(E)}{R_T}, \tag{1.14}$$

one is left with the equation

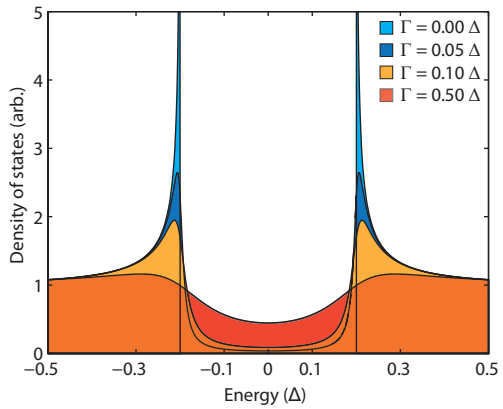
$$\frac{dI}{dV} = \frac{\Gamma}{R_T \Delta}. \tag{1.15}$$

The value of Γ/Δ can therefore be determined experimentally by the ratio of the normal state resistance R_T and the sub-gap resistance, where the sub-gap resistance is defined as $\frac{dV}{dI}(V = 0)$, satisfying the low energy condition mentioned above.

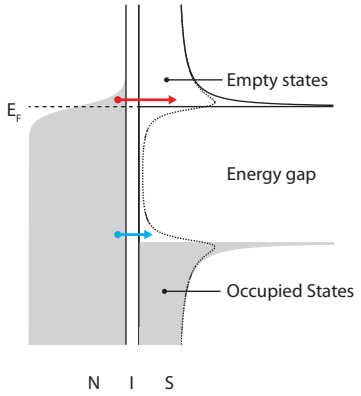
Typical values of Γ are of the order $\sim 1 \times 10^{-5}\Delta$ [55] and $\sim 1 \times 10^{-2}\Delta$ [56] for N-I-S and Sm-S junctions respectively.

A non-zero value of Γ enables electrons below the threshold energy of $(E - eV)$ to tunnel out of the semiconductor (figure 1.11b), reducing the average energy removed from the system per electron which represents a loss of filtration and manifests as a net heating power. This effect becomes more prominent at low bath temperatures, when the sharpened Fermi-distribution favours sub-gap tunneling.

It has recently been demonstrated that a Dynes-like density of states can in fact originate from the electromagnetic environment of a tunnel junction [55]. In this process, insufficient shielding results in a sample being exposed to radiation



(a) Density of states as given by the Dynes formula for $\Delta = 0.2\,\mathrm{meV}$



(b) Energy level diagram of an N-I-S device with available states in the bandgap

Figure 1.11: Γ parameterises the population of sub-gap states and allows for low energy electrons ($E < E_F$) to escape the normal state material

from the surrounding high temperature environment, leading to the photon-assisted tunnelling of sub-gap electrons. Once again this results in a loss of effective cooling power, however it may be solved by simply improving the shielding on the sample stage.

It is worth noting that in this investigation a number of samples were used for benchmark measurements in separate cryostats with varying experimental setups, each providing a different noise environment. In each case, the value of Γ measured was of the same order of magnitude indicating that it is intrinsic to our devices and therefore the result of some material property and not of the measurement environment.

1.4.5 Carrier-phonon coupling

Electron-phonon coupling results in a power flow from the lattice to the electron gas as the former is cooled. It can be interpreted as either a drain on the cooling power of a junction, or an opposing heating power.

Due to the many-body nature of electron wavefunctions in solid state sys-

tems, the coupling, although conceptually simple, is generally not possible to calculate directly and approximations are needed. The most used one, is the so-called deformation potential theorem [57], the application of which is described thoroughly in previous work [42]. Other works have focused on the role of valley degeneracy in carrier-phonon coupling, though a detailed theoretical analysis for the carrier-phonon or coupling in strongly disordered, many-valley semiconductors has only recently started to develop [58, 59, 60, 61, 62]. This theory will be touched upon in more detail in chapter 5.

At low temperatures this energy transfer is mediated by the electron-acoustic phonon interaction given by [41, 21]

$$P_{e-ph} = \Sigma\Omega(T_e^n - T_p^n) \tag{1.16}$$

with Σ being the material specific electron-phonon coupling constant and Ω the cooled volume. The power n varies with material [58] with $n = 6$ being typical for degenerately doped 3D bulk semiconductors [53, 58, 60]. One advantage of Sm-S junctions is that Σ is generally lower in semiconductors compared with normal metals [31]. Furthermore, Σ can be tuned by doping concentration [59], carrier type (see chapter 5) and tensile strain [63]. The latter two factors form an important part of my investigations in this thesis, with further discussion of the power law and its exponent value given in chapter 5.

In the simplest case, the temperature to which the electrons are cooled may be determined by balancing the cooling power (equation 1.11) and the power drain due to electron phonon coupling (equation 1.16) and solving the following equation for T_e.

$$P_C + P_{e-ph} = 0 \tag{1.17}$$

Figure 1.12 depicts this equation graphically for a range of bath temperatures (equal to the initial electron temperature), with the equilibrium electron temperature in-

dicated by the intersection of the P_C and P_{e-ph} lines.

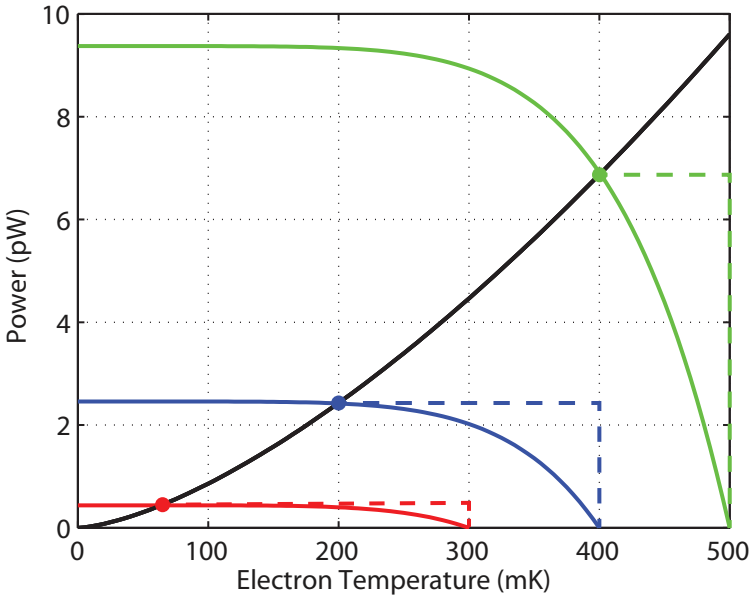


Figure 1.12: P_C (black) and P_{e-ph} for bath temperatures of 300 mK (red), 400 mK (blue) and 500 mK (green), depicting cooling to 65 mK, 200 mK and 400 mK respectively. Calculated using equations 1.11 and 1.16 with the parameters: $\Delta = 0.2\,\text{meV}$ (aluminium), $R_T = 500\,\Omega$, $\Sigma = 1 \times 10^8\,\text{W}\,\text{K}^{-6}\,\text{m}^{-3}$ and $\Omega = 30\,\text{nm} \times 20\,\mu\text{m} \times 10\,\mu\text{m}$.

However, it is found in practice that this simple equation overestimates the cooling performance for a given set of parameters and therefore other factors must be considered that limit the electron cooling (see section 1.4.6 onwards).

1.4.5.1 Modification through strain

Mechanical strain can be induced by growing silicon atop a substrate with a different lattice parameter, with the silicon conforming to the atomic spacing of the material beneath. In this and other work [63], a silicon germanium virtual substrate is used to induce biaxial tensile strain in the overlaid silicon as depicted in figure 1.13.

The lattice parameter a of the silicon germanium alloy can be calculated

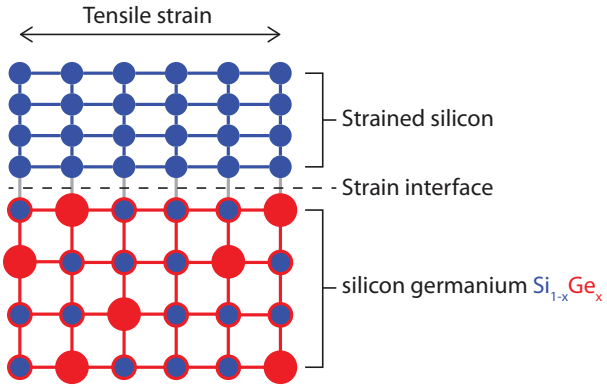


Figure 1.13: Lattice mismatch induced strain

using the Kasper-corrected Vergard's law [64]:

$$a_{Si_{1-x}Ge_x} = a_{Si}(1-x) + a_{Ge}x + 0.02733x^2 - 0.02733x \tag{1.18}$$

where x is the proportional germanium content.

The strain experienced by the silicon grown on this material can then be expressed as a percentage calculated from the ratio of its modified and original lattice parameters, with silicon grown on $Si_{0.8}Ge_{0.2}$ (20% germanium content) having a strain of approximately 0.8%.

As the thickness of the strained layer is increased, there is a proportional change in the energy density at the strain interface [65, 66]. Above a certain point, known as the critical thickness, this will result in the spontaneous formation of dislocations that allow the strained layer to relax, as shown in figure 1.14. For silicon on $Si_{0.8}Ge_{0.2}$, this critical thickness is approximately 10 nm, however it has been shown that at low temperatures (where the thermal budget is not exceeded), no significant strain relaxation ($< 1\%$) occurs until the layer thickness exceeds ~ 40 nm [67], comfortably above those reported on in this work.

To understand the strain induced modification of the electron-phonon coupling it is necessary to understand the mechanisms through which the electron and phonon subsystems interact. Firstly, in a degenerate material such as a highly doped

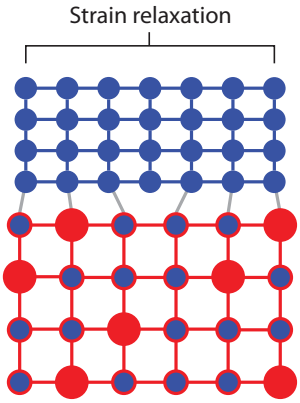
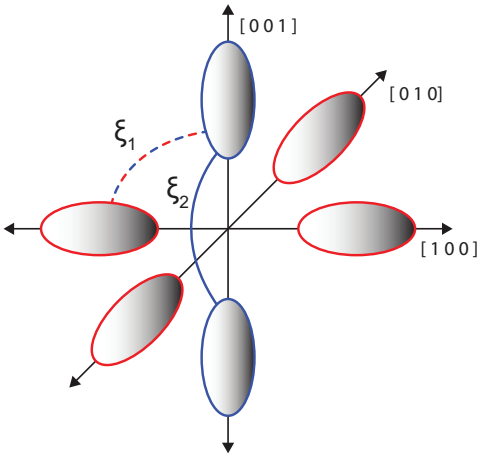


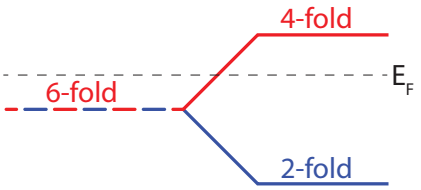
Figure 1.14: Strain relaxation through disclocation

semiconductor, the excitation of an acoustic phonon creates a charge density fluctuation due to the vibrations of the charged ions that make up the lattice [15, 33]. This results in perturbations to the electron gas which will then renormalise via electron-electron scattering, thus transferring energy between the electrons and phonons. In the case of many valley semiconductors, such as silicon, there exists a separate population of electrons for each of the six equivalent points where the conduction band minima occur [15] resulting in two conduction channels [60, 61]: scattering between valleys on different axes (ξ_1) and inside one valley (or between the valleys on the same axis) (ξ_2), with intervalley scattering dominating at the degenerate, low temperature limit of interest [61].

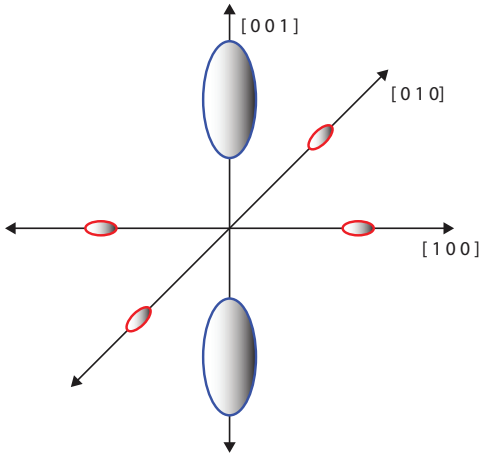
Figure 1.15a illustrates the conduction band energy valleys in bulk silicon. Valleys that lie on the same axes have a symmetrical response to a phonon, which is to say that the phonon is unable to lift their degeneracy. The fields set up by the perturbation of the electrons in such valleys interfere constructively to screen the initial ionic charge and the resulting scattering, proportional to the electron-phonon coupling of the system. It can therefore be said that the ξ_2 scattering process contributes little to the electron-phonon constant Σ. Conversely, valleys on different axis have an asymmetric response, with their degeneracy being lifted. The ionic charge distribution is therefore unscreened and energy will be conducted



(a) Illustration of the constant energy ellipsoids of Si conduction band valleys.



(b) Strain raises the energy of the four in plane valleys above the Fermi energy.



(c) The four in plane valleys are therefore depopulated by the applied strain.

Figure 1.15: The affect of strain on the population of the conduction band valleys in silicon.

between the phonon and the electrons as the latter relax towards a local equilibrium by scattering between the two, now degenerate valleys.

Biaxial tensile strain is capable of depopulating the valleys along the axes of applied strain, raising their energy above the Fermi level [68, 63] by changing the in-plane and out-of-plane lattice constants of the silicon. This is depicted in figure 1.15b, leaving only the in-axes valleys as shown by figure 1.15c. The unscreened asymmetric heat conduction channel (ξ_1) is therefore removed, leaving the strongly

screened channel (ξ_2) as the only mechanism by which the electrons within the silicon can renormalise. This slows the rate of energy transfer between the electrons and the phonon, which manifests as a lower electron-phonon coupling and a smaller heating power P_{e-ph}.

1.4.5.2 Hole systems

In silicon, the valence band comprises sub-bands of light holes, heavy holes and spin-orbit split-off bands [15], with their origin explained by the tight-binding model [69]. Such a plurality of bands naturally results in a number of different inter-band scattering mechanisms, with each one contributing to the hole-phonon coupling term. These mechanisms have so far received little theoretical attention [70], though an experimental study of the hole-phonon coupling is made in chapter 5 of this work.

1.4.6 Heating powers

The cooling power through the junction is opposed by a number of heating powers set up in turn by the flow of current from the semiconductor to the superconductor. These are outlined below.

1.4.6.1 Joule heating

A Joule heating results from the cooling current experiencing the series resistance between the coolers of a double junction device. This results in a heating power given by

$$P_J = I^2 R_{Sm} \tag{1.19}$$

where I is the current through the device and R_{Sm} is the resistance of the semiconductor. At low temperatures and for $V < 2\Delta/e$ the tunnel current through the device is low and the effective resistance dV/dI is very high, meaning that most of the voltage drops across the junctions and this term is negligible. For higher

biases, as the tunnel current begins to rise, the Joule heating becomes significant and will impact the minimum temperature achievable by a cooler device. At the same time, dV/dI decreases so that the voltage drop across the junctions becomes a smaller proportion of the total bias across the device, with the applied voltage being split more evenly between the semiconductor-superconductor junctions and the series resistance between them. The net effect of this is to spread out the temperature versus bias characteristic of the cooler junctions toward higher biases, as to provide the optimum voltage $V_C = 2\Delta/e$ to the cooler junctions (at which point the electron temperature would reach a minimum (section 1.3.2)), a voltage greater than $2\Delta/e$ must be applied in order to account for the drop across the series resistance of the semiconductor.

1.4.6.2 Quasiparticle heating

Quasiparticles are low energy excitations of a complex system that themselves have a well-defined energy and can therefore be treated semi-classically. An electron in a semiconductor for example, is subjected to complex interactions with other charge carriers and the bulk material yet can be approximated as an unperturbed electron possessing an alternate effective mass. In the context of this work, the term quasiparticle is primarily used to describe a carrier and the associated quanta of energy that it carries across the junction. That being so, quasiparticles entering the superconductor from the semiconductor can cause significant heating of the superconducting electrode if they linger near the junction area [71]. Two quasiparticles can recombine to form a superconducting Cooper pair and a phonon, which is absorbed by the junction. Secondly, quasiparticles may tunnel back through the barrier into the semiconductor, effectively decreasing the net cooling current across the junction. These two mechanisms can be modeled jointly by the term [52, 11]

$$\beta P_{QP} \tag{1.20}$$

A simplifying assumption where $\beta < 1$ denotes the fraction of the power deposited in the superconducting electrode P_S that is returned to the semiconductor. β is a parameter assumed to be dependent only on the temperature of the surrounding bath [52], and

$$P_{QP} = IV + P_C \tag{1.21}$$

Quasiparticle heating can seriously limit the cooling power of the device, and it is important to allow the quasiparticles to leave the tunneling region of the junction before they can tunnel back or recombine. The simplest solution is to use a thick superconductor ($\sim 100\,\text{nm}$), with minimum overlap between superconductor and semiconductor to encourage diffusion away from the junction area [72, 11]. It also helps to use arrays of many small area junctions [73] in order to spread the quasiparticles out and avoid highly localized concentrations. An alternate option is to incorporate a quasiparticle trap consisting of a normal metal in direct contact with the superconductor, or via an oxide tunnel junction [74, 75, 11], into which the quasiparticles can fall and minimise their energy, as illustrated in figure 1.16. With the electron-phonon coupling (section 1.4.5) and thermal conductivity being stronger in the metal, the traps act as a heat sink for the superconducting electrode and prevent local overheating. The trap should be positioned some distance away from the junction (of the order of the coherence length of the superconductor, ξ_0 [76]), in order to not suppress superconductivity at the junction by means of the proximity effect [47].

In metal based N-I-S junctions, traps have been shown to improve cooling performance by almost a factor of five at 300 mK. Furthermore, it has been shown that in such devices cooling from bath temperatures below 200 mK is simply not viable without some from of quasiparticle management [74].

Regarding the Sm-S junctions, it is widely accepted [77] that the smaller quasiparticle current (a direct result of the characteristically higher junction resis-

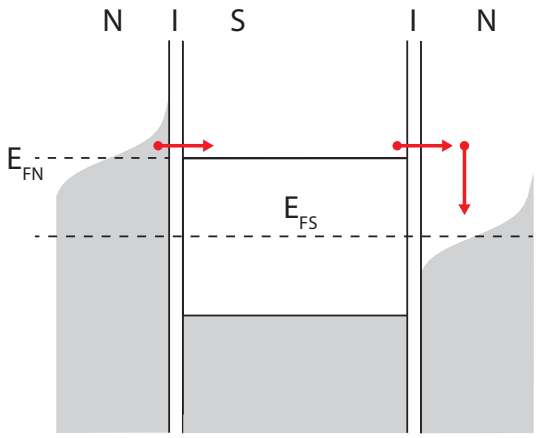


Figure 1.16: An energy level diagram showing a quasiparticle trap applied to the superconducting electrode of a single junction N-I-S.

tance R_T) and the resulting low power deposition in the superconductor render the inclusion of metal traps an unnecessary complication in the fabrication procedure.

1.4.6.3 Andreev heating

For voltages $eV \ll \Delta$, charge transfer occurs through Andreev reflection if the barrier transparency is high [78]. Any electron (hole) in the semiconductor impinging on the superconducting interface is reflected as a hole (electron) and creates a Cooper pair [79] in the superconductor. The energies of the hole and electron are located symmetrically around E_F and hence there is no energy transfer out of the semiconductor. Thus the Andreev current will result in Joule heating with no associated cooling, identifying i, t as an additional heating power, dissipating energy within the semiconductor. Disorder in the normal state material leads to carrier confinement near the interface and greatly enhances the Andreev process by forcing carriers to experience multiple reflections before escaping the junction area.

It has also been suggested that with higher order processes being neglected when deriving equation 1.4, the multi-electron Andreev process may be responsible for the equation's failure to adequately describe currents in the sub-gap, rendering the Dynes model obsolete [80]. However it is noted in this and other works [10] that

the effects of an Andreev current are only significant in junctions with low sub-gap conductance (more common to N-I-S junctions) and diminish towards the optimum operation voltage with no affect on the minimum electron temperature achieved by a cooler. For these reasons, the Andreev term is largely neglected in this investigation.

1.4.7 Power balance equation

Incorporating the effects so far discussed, the power flows within a junction can be described by the equation

$$P_C = P_{e-ph} + P_J + \beta P_{QP} \tag{1.22}$$

which shows the performance of a refrigerator depending on the balance between P_C and the power loads and self-heating processes within the device. For a given applied voltage bias these processes will eventually reach an equilibrium with the electrons in the semiconductor at a stable temperature that can be calculated by solving equation 1.22 for T_e.

1.5 Tunnel current thermometry

In order to measure electron temperature experimentally, a suitable probe is required. Given that TJCs operate to reduce the electron temperature below that of the surrounding thermal bath, conventional thermometry is not an option, as the electrons are not in thermal equilibrium with anything but themselves.

Fortunately, the semiconductor-superconductor junctions used in TJCs have an intrinsic relationship with electron temperature, as shown in figure 1.10a of section 1.4.2. The equation for the current through a double tunnel junction was given by equation 1.4 and in the limit $\Delta \ll k_B T_e$, which is satisfied below 1 K, the current through a tunnel junction depends only on the temperature of the electrons in the normal state material [47]. This is due to the fact that the Fermi level in

the superconductor lies in the middle of the band gap (as depicted in figure 1.4) and therefore any deviation in the Fermi distribution due to the temperature of the superconductor can be neglected as the product with the density of states will be zero.

This allows equation 1.4 to be rewritten as

$$I = \frac{1}{eR_T}\int_{-\infty}^{\infty} \frac{|E|}{\sqrt{E^2-\Delta^2}}\left[f(E-eV)-f(E)\right]dE, \tag{1.23}$$

where

$$f(E) = \frac{1}{exp^{E/k_b T_e}+1}. \tag{1.24}$$

From this equation it is possible to deduce the voltage response to a change in electron temperature of a Sm-S junction operating under a constant current bias, allowing one to probe the electron temperature within the semiconducting electrode. The derivation is given in full below and was first formalised by D. V. Anghel in an unpublished work [50]. It is reproduced here for clarity.

Integrating over possible energies,

$$\begin{aligned} I = \frac{1}{eR_T}\Bigg(&\int_{\Delta}^{\infty} \frac{|E|}{\sqrt{E^2-\Delta^2}}\left[f(E-eV)-f(E)\right]dE \\ &- \int_{-\infty}^{-\Delta} \frac{|E|}{\sqrt{E^2-\Delta^2}}\left[f(E-eV)-f(E)\right]dE\Bigg) \end{aligned} \tag{1.25}$$

and using the substitutions $x+\Delta = E$ and $x+\Delta = -E$ in the first and second integrals respectively, the equation becomes

$$\begin{aligned} I = \frac{1}{eR_T}\Bigg(&\int_{0}^{\infty} \frac{x+\Delta}{\sqrt{x(x+2\Delta)}}\left[f(x+\Delta-eV)-f(x+\Delta)\right]dE \\ &- \int_{0}^{\infty} \frac{x+\Delta}{\sqrt{x(x+2\Delta)}}\left[f(-x-\Delta-eV)-f(-z-\Delta)\right]dx\Bigg). \end{aligned} \tag{1.26}$$

With the general relationship $f(-\xi) = 1 - f(\xi)$, it can be seen that

$$I = \frac{1}{eR_T}\int_{0}^{\infty} \frac{x+\Delta}{\sqrt{x(x+2\Delta)}}\left[f(x+\Delta-eV)-f(x+\Delta+eV)\right]dE. \tag{1.27}$$

Expanding the Fermi function,

$$f(\xi) = [1 + \exp(\xi/k_bT_e)]^{-1} = \exp(-\xi/k_bT_e)[1 + \exp(-\xi/k_bT_e)]^{-1} \tag{1.28}$$

$$= \exp(-\xi/k_bT_e) \sum_{m=0}^{\infty} (-1)^m \frac{\exp(-m\xi/k_bT_e)}{m!} \tag{1.29}$$

which is valid for $\xi > 0$ and substituting $\xi = x + \Delta - eV$ and $x + \Delta + eV$, yields

$$I = \frac{2}{eR_T} \sum_{m=0}^{\infty} (-1)^{m+1} \exp\left(-\frac{m\Delta}{k_BT_e}\right) \sinh\left(\frac{meV}{k_BT_e}\right) \times \int_0^{\infty} \frac{x + \Delta}{\sqrt{x(x + 2\Delta)}} \exp\left(\frac{-mx}{k_BT_e}\right) dx. \tag{1.30}$$

Using the Laplace transformation

$$\int_0^{\infty} \frac{t + a}{\sqrt{t(t + 2a)}} \exp(-pt)dt = a \exp(ap)K_1(ap) \tag{1.31}$$

where K_1 is the first order modified Bessel function of the second kind, gives

$$I = \frac{2\Delta}{eR_T} \sum_{m=0}^{\infty} (-1)^{m+1} K_1\left(-\frac{m\Delta}{k_BT_e}\right) \sinh\left(\frac{meV}{k_BT_e}\right). \tag{1.32}$$

Neglecting terms of order $m > 1$, using the asymptotic form of $K_1(z) \cong \sqrt{\frac{\pi}{2z}} \exp(-z)$ valid for $\Delta \ll k_BT_e$ and noting that for $0 \leq eV \leq \Delta$, $\sinh(z) = \frac{1}{2}\exp(z)$, allows the equation to be rewritten as

$$I = \frac{1}{2} \frac{2\Delta}{eR_T} \sqrt{\frac{\pi k_BT_e}{2\Delta}} \exp\left(\frac{-\Delta}{k_BT_e}\right) \exp\left(\frac{eV}{k_BT_e}\right) \tag{1.33}$$

$$= \frac{\Delta}{eR_T} \sqrt{\frac{\pi k_BT_e}{2\Delta}} \exp\left(\frac{eV - \Delta}{k_BT_e}\right). \tag{1.34}$$

Hence it can be seen that if the junction is biased with a constant current, the

temperature response becomes

$$\frac{dV}{dT_e} \approx \frac{k_B}{e} \ln\left(\frac{I}{I_0}\right) \tag{1.35}$$

where $I_0 = (\Delta/eR_T)(\pi k_B T_e/2\Delta)^{\frac{1}{2}}$ which is approximately linearly dependent on the electron temperature of the normal state material.

For this reason, Sm-S junctions make for a rather elegant method of electron thermometry, owing to their simplicity and the fact that they can be fabricated in conjunction with cooler junctions and other tunnel devices, without the need for any separate processing steps.

They do suffer from some disadvantages however. The Sm-S junction thermometers will become less sensitive at lower temperatures with the temperature independent sub-gap leakage becoming the dominant mechanism of current flow. Furthermore, the current bias employed in the operation of a thermometer junction will inevitably lead to power being dissipated in the device under study. Though this can be minimised by reducing the applied current, it can result in a saturation point at lower temperatures, below which the thermometer is useless. Whilst any low temperature calibration can be extrapolated from the region in which the temperature/voltage response is linear, such extrapolations are made at a cost of uncertainty in the end result.

At temperatures approaching the critical temperature of the superconductor T_C, the junction resistance will tend asymptotically towards its normal state resistance R_T. R_T is temperature independent and so once again the thermometer response will saturate. However, given the thermometers application to tunnel junction coolers, which require temperatures well below T_C to operate, this is of no real concern.

1.5.1 Thermometer bias current

The selection of the thermometer bias current plays a significant role in the sensitivity and effectiveness of a tunnel junction thermometer. As shown in figure 1.17a, as the temperature decreases, the voltage across it traces a path between the isotherms, along the line of constant current. It is important to select a bias current that provides for a sufficient voltage response in order for the thermometer to be able to resolve temperatures across an experimentally useful range.

Figure 1.17b depicts the change in thermometer voltage with temperature for a range of bias currents. It is clear that the middle blue line would be the most suitable in this case, offering the largest response to temperature and remaining linear over the majority of the temperature range.

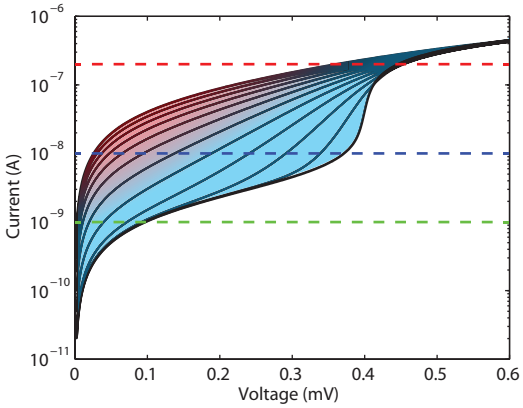
The selection of the optimum bias current is made more straightforward by figure 1.17c which plots the difference in thermometer voltage at the extreme ends of the temperature range for a number of currents, with the coordinates of the peak identifying the optimum bias.

1.5.2 Thermometer saturation

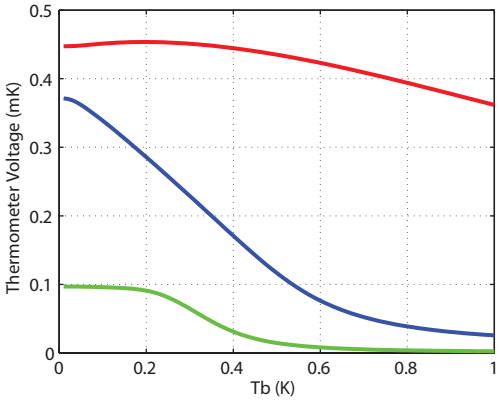
A number of non-idealities and other such factors can influence the saturation temperature of a tunnel junction thermometer. Those encountered in this work are introduced below.

1.5.2.1 Γ induced saturation

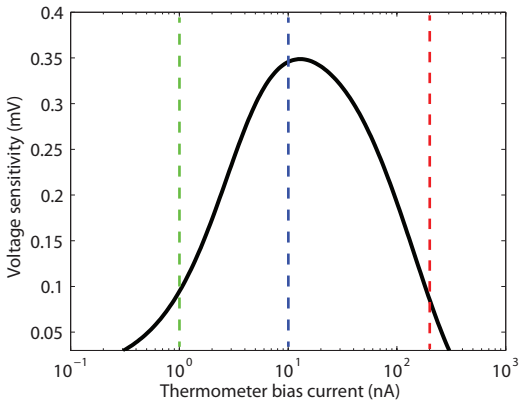
Any finite value of Γ (see section 1.4.4) will result in a premature thermometer saturation. Operating under a constant current bias (typically $(0.1 - 10)\,\mathrm{nA}$), the voltage across the thermometer junction will increase as the temperature decreases. For junctions with a finite Γ a temperature will eventually be reached below which sub-gap tunnelling will become the dominant factor affecting current flow. Given



(a) A range of isothermal current voltage plots for temperatures between $(0.01 - 1)\,\mathrm{K}$. The coloured lines represent particular bias currents of 1 nA (green), 10 nA (blue) and 200 nA (red).



(b) Thermometer voltage as a function of temperature, calculated from the intercepts of the bias currents and the isothermal IV plotted in figure 1.17a.



(c) Voltage sensitivity across a temperature range of $(0.01 - 1)\,\mathrm{K}$ as a function of thermometer bias current.

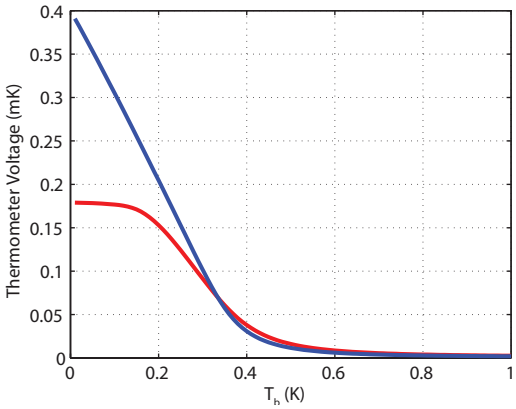
Figure 1.17: Simulations of an S-Sm-S thermometer junction with $\Delta = 0.2\,\mathrm{meV}$, $\Gamma = 0.01\,\Delta$ and $R_T = 500\,\Omega$.

that it has only a weak dependance on electron temperature, the thermometer voltage will plateau. This saturation of thermometer response will occur at higher temperatures for larger values of Γ, as illustrated in figure 1.18a.

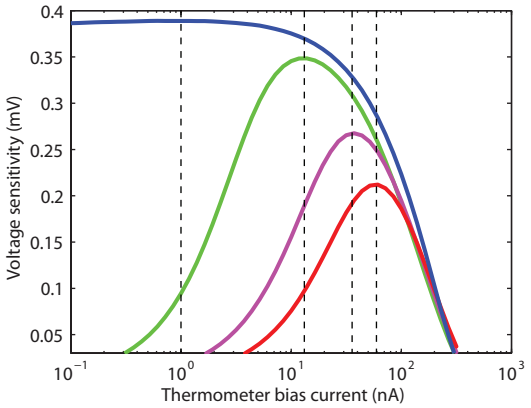
Moving to larger current biases will go someway towards negating this problem, as shown in figure 1.18b where the optimum current changes with Γ. Selecting a current above the artificial shoulder imposed upon the thermometer IV by a finite

Γ will limit its effect on the behaviour of the thermometer, though at a cost of a greater heat load on the device.

As will become clear later in this work, for experiments involving electron cooling the necessity to minimise any internal heating power from the thermometer overrides any other considerations and the thermometer bias current is set as low as possible. For measurements of carrier-phonon coupling however, any Joule heating in the thermometer is negligible compared to the power injected to heat the carriers. This allows the optimum current to be utilised, maximizing temperature sensitivity.



(a) Thermometer voltage as a function of temperature with a typical bias current of 1 nA, for $\Gamma = 0\,\Delta$ (blue) and $\Gamma = 0.005\,\Delta$.



(b) Voltage sensitivity across a temperature range of $(0.01 - 1)\,\mathrm{K}$ as a function of thermometer bias current for $\Gamma = 0$ (blue), $\Gamma = 0.01\,\Delta$ (green), $\Gamma = 0.05\,\Delta$ (pink) and $\Gamma = 0.1\,\Delta$ (red).

Figure 1.18: Further simulations of an S-Sm-S thermometer junction with $\Delta = 0.2\,\mathrm{meV}$ and $R_T = 500\,\Omega$. In figure 1.18b, the optimum current bias in each case is identified by a dashed line.

1.5.2.2 Thermometer current induced saturation

As a result of Joule heating, any current flow through a thermometer junction will lead to a finite heating power. In extreme cases this can lead to a significant additional heat load on any cooling junctions under test. Even if this current is minimised, the heat dissipated in the thermometer will manifest as a fixed minimum temperature, with the thermometer being blind to any further cooling.

Figure 1.19 shows the resulting insensitivity of a thermometer junction biased with a range of currents typically used in tunnel junction experiments. The electron temperature of the thermometer is calculated from the heat balance equation that includes both the lattice coupling and Joule heating terms. The deviation of this 'measured' electron temperature from the true temperature defined in the simulation demonstrates the necessity to minimise the bias currents when low temperature sensitivity is a priority.

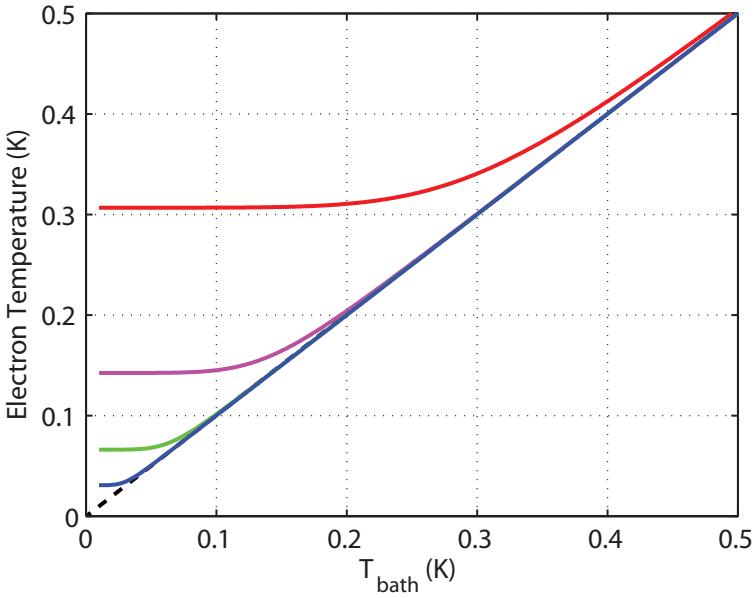


Figure 1.19: A simulation of the electron temperature measured by a junction thermometer biased at a current of 0.1 nA (blue), 1 nA (green), 10 nA (magenta) and 100 nA (red), with $\Delta = 0.2\,\mathrm{meV}$, $R_T = 500\,\Omega$ and $\Omega = 30\,\mathrm{nm} \times 20\,\mu\mathrm{m} \times 10\,\mu\mathrm{m}$. The black dashed line represents the true electron temperature, as measured by an ideal thermometer.

This effect is stronger in devices that utilise materials with a weaker electron-phonon conductivity, such as strained silicon. A lower coupling constant Σ impedes the thermalisation of the electrons to the environment and increases the influence of cooling and heating powers alike. Whilst this is generally desirable when seeking to minimise the electron temperature achieved in cooling experiments, it can have significant effects on the reliability of tunnel junction thermometry as illustrated in

figure 1.20.

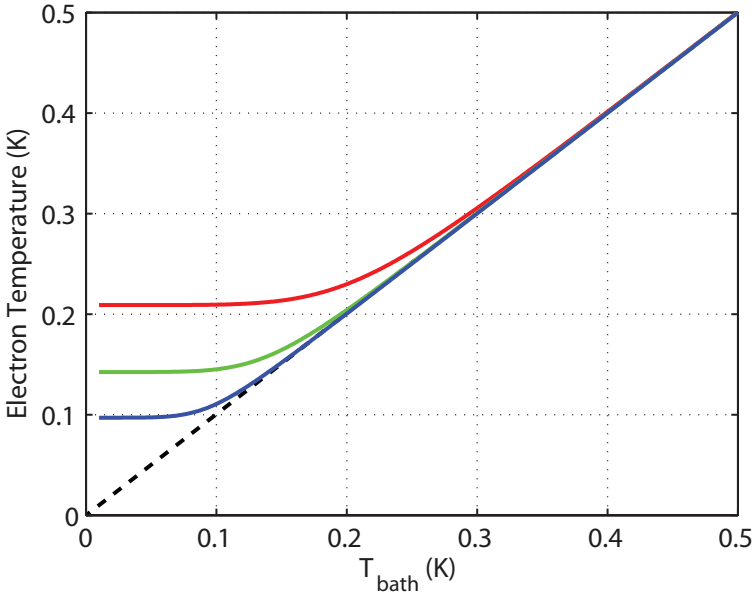


Figure 1.20: A simulation of the electron temperature measured by a junction thermometer biased at a current of 10 nA with an electron-phonon coupling constant of $\Sigma = 1 \times 10^9\,\mathrm{W\,K^{-6}\,m^{-3}}$ (blue), $1 \times 10^8\,\mathrm{W\,K^{-6}\,m^{-3}}$ (green) and $1 \times 10^7\,\mathrm{W\,K^{-6}\,m^{-3}}$ (red), with $\Delta = 0.2\,\mathrm{meV}$, $R_T = 500\,\Omega$ and $\Omega = 30\,\mathrm{nm} \times 20\,\mu\mathrm{m} \times 10\,\mu\mathrm{m}$.

1.5.3 Non-empirical tunnel current thermometry

It is possible to work around the saturation of the thermometer response by employing an alternative, non-empirical calibration method which avoids low temperature extrapolation. The measured current-voltage data from a junction is superimposed on a series of theoretical isotherm curves generated from equation 1.10, using the parameters of the device under test. Each point of intersection between the experimental data and an isotherm yields the electronic temperature in the semiconductor island at that particular bias.

This process, illustrated in figure 1.21, is useful in situations where the optimum performance of a device is at temperatures below the saturation point of conventional junction thermometers. It is therefore more common in experiments dealing with high power NIS devices [81] which in general can obtain the lowest

electron temperatures.

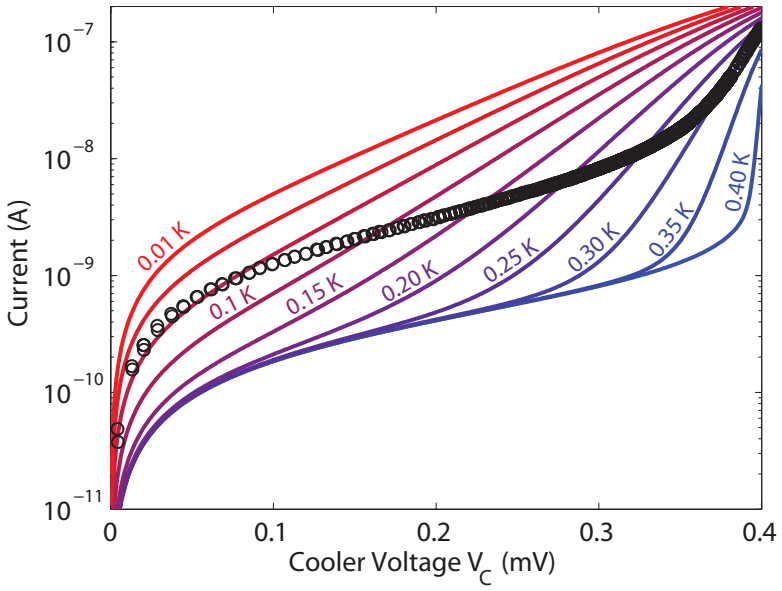


Figure 1.21: Calibration of experimental data (black circles) against theoretical isothermal junction behaviour from $T = 0.01\,\mathrm{mK}$ to $T = 0.40\,\mathrm{mK}$ as given by BCS theory [28].

Whilst this method is used to good effect in this and other works, the fact that the temperature data is extracted from a simulation of the junction and not the junction itself brings its accuracy into question [82]. A slight change in inputted parameters can result in significant changes in extracted temperatures and furthermore, equation 1.10 does not take into account any internal heating of the thermometer. For these reasons non-empirical thermometry is perceived as somewhat unreliable in isolation and it is therefore primarily used in conjunction with conventional junction thermometry to corroborate low temperature data.

2

Fabrication techniques

The overall fabrication processes for the different families of devices are summarised in the sections below. Many different samples were produced throughout this investigation requiring a number of often minute variations in processing methods. The precise details particular to the fabrication of each sample are given in the relevant results chapters. All processes were carried out on wafers that already contained a degenerately doped, electrically active layer formed by either standard CVD techniques or through ion implantation. Such fundamental techniques will not be described in detail in this work and I refer the reader to the standard textbooks of those fields [83, 84, 85].

All devices presented in this work were fabricated using contact optical lithography and a lift-off procedure, standard techniques within the micro-fabrication industry with a resolution limit of $\sim 1\,\mu m$. The operating principle involves patterning a photosensitive resist via exposure to ultra-violet light through a photomask. The resulting pattern is then used to selectively expose the material beneath either to an etch or a some form of material deposition.

2.1 Sm-S junction fabrication

The standard lithographic process for a Sm-S junction is outlined below and is the principle fabrication method employed at the University of Warwick.

1. S1813 photoresist is spun onto the substrate and the mesa is patterned using a MJB3 mask aligner.

2. This is followed by a 300 second treatment in an inductively coupled plasma etcher, leaving a raised pillar containing the active layer, effectively isolating the degenerate doped silicon and leaving the mesa geometry well defined.

3. An acetone rinse is then applied in order to remove any residual photoresist.

4. Native oxide is then removed by immersion in 1% Hydrogen Fluoride (HF) solution for one 1 minute, followed by a cleaning rinse in deionized (DI) water and dry nitrogen gas.

5. The sample is placed in the loadlock of a PP400 sputterer and pumped down to 10^{-8} mbar before any oxide can reform.

6. Aluminium is then deposited to a depth of approximately 200 nm, taking 240 seconds at a power of 150 W.

7. Step 1 is then repeated using the contact mask to define the superconducting electrodes and contacts.

8. The excess aluminium is then removed in a phosphoric-nitric acid wet etch at 40 °C lasting 120 seconds.

9. A final acetone rinse is employed to clean the finished device.

2.2 Sm-I-S junction fabrication

The fabrication process for a Sm-I-S junction is similar to that described above, with an addition step of blanket $Si0_2$ growth before the aluminium deposition (in the case of a standard Sm-I-S junction device). This occurs between steps 5 and 6 in the previous method. After the removal of the native oxide (step 4) and relocation

to the sputter, the sample undergoes an in-situ oxidation by flowing pure oxygen gas at 200 Torr at a temperature of 550 °C for 600 seconds.

The process for the so-called oxide-window Sm-I-S devices is more complex and requires a second round of lithography in order to define the junction areas (windows) in which an $Si0_2$ oxide is grown at a range temperatures for a given time, laid out in table 6.1 in chapter 6. These oxide-window devices were fabricated on whole 6 inch wafers at VTT labs in Helsinki, Finland.

Each of the above processes is presented graphically in figure 2.1.

2.3 Vanadium junction fabrication

A bi-layer method was utilised for the fabrication of the Si-V junctions. The process is depicted in figure 2.2 and was combined with a thin (< 10 nm) aluminium layer to ensure good adhesion of the vanadium.

Steps 1 to 5 of the method described in section 2.1 were carried out as normal before aluminium was deposited to a depth of approximately 10 nm, taking 20 seconds at a power of 100 W. The sample was then shipped to the Scuola Normale Superiore di Pisa, Italy, where it underwent a second native oxide removal (step 4) followed by vanadium deposition. This was achieved using a DV Discovery 635 sputterer, depositing 200 nm of vanadium in 300 seconds at a power of 150 W.

2.4 PtSi junction fabrication

In the special case of the platinum silicide-semiconductor junction, fabrication begins with a purchased silicon-on-insulator (SOI) wafer. The wafer incorporates a buried oxide layer that serves to isolate the device layers from the bulk silicon substrate. SOI technology is chiefly utilised within the transistor industry as well as in high-performance radio-frequency (RF) applications and silion photonics [86]. Within this investigation it is simply utilised as a convenient starting material and

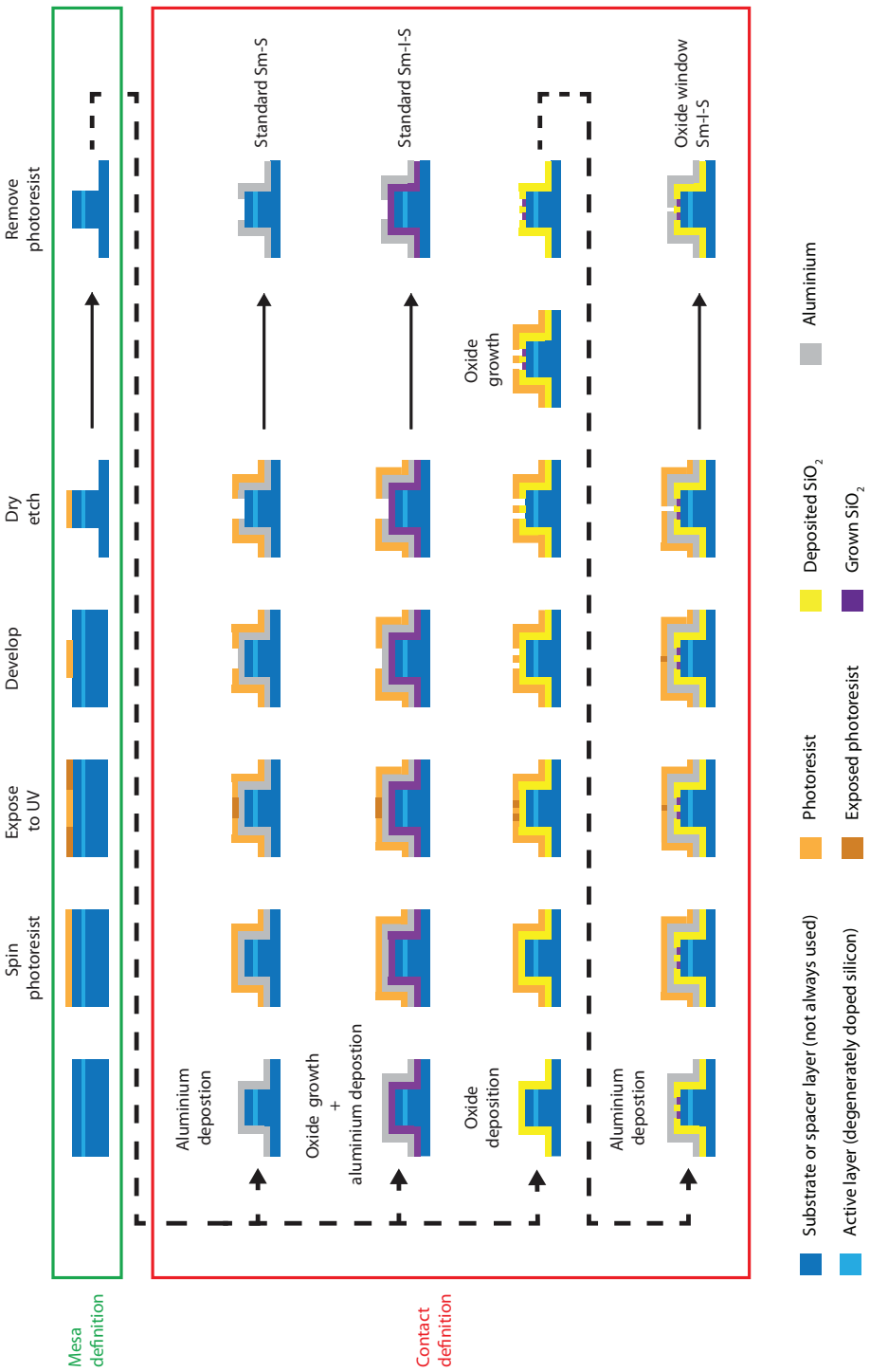


Figure 2.1: The fabrication process for Sm-S and Sm-I-S junctions (Advise rotating head 90° anticlockwise).

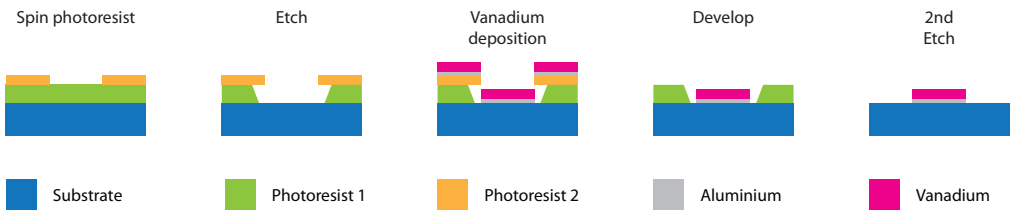


Figure 2.2: The bi-layer process for silicon-vanadium junctions.

in fact SOI technology does not provide any significant benefit to tunnel junction coolers. This is understandable, given the electrical isolation already provided by the freezing out of the substrate at the characteristically low temperatures at which TJCs operate.

The samples were prepared using the following process, carried out at Aalto University, Finland:

1. The whole wafer is loaded into a pressure enhanced chemical vapour deposition (PECVD) chamber to undergo growth of a blanket surface oxide. This served to define the region for ion implantation and as such its growth specifics are not important.

2. The sample is transferred to an OPTIMA HDx ion implanter at which point the surface is bombarded with arsenic ions at energy 200 keV with a dosage of 1×10^{14} ions/cm^2. These ions incorporate into the exposed silicon, and acting as donors, create a degenerately doped layer. This step is similar in principle to the mesa definition process described in section 2.1.

3. The PECVD oxide is re-patterned using standard photolithography and etched to aid in the definition of PtSi contacts.

4. Platinum is deposited to form the superconducting electrode. This is achieved using a magnetron sputtering system, taking 200 seconds at a power of 150 W to deposit a layer of 200 nm.

5. Silicidation is performed in-situ at 500 °C for 1 min, causing the platinum and

underlying silicon to form an alloy.

6. The sample then undergoes a final round of photolithography (steps 7 and 8 of section 2.1) to create aluminium contacts to the PtSi electrodes.

3

Experimental techniques and equipment

A wide and varied array of equipment and measurement techniques have been utilised over the course of this project. Those that formed the principle methods of investigation and that contributed most notably to the results presented in this thesis are outlined below.

3.1 Cryostats

3.1.1 Closed Cycle

The bulk of electrical characterisation was carried out in a pulse tube refrigerator (PTR) closed cycle cryomagnetic system, with a base temperature and high field value of 10 K and 1.2 T respectively. The operation of a PTR is reasonably simple [87]. First a piston compresses ^{4}He. The heated gas, being at a higher pressure than the average, flows through an orifice into a reservoir and transfers its energy via a heat exchanger at the warm end of the pulse tube. The piston then moves back to expand the ^{4}He adiabatically, lowering its temperature. This cold, low-pressure gas is then forced toward the cold end of the pulse tube as the warmer helium is returned through the orifice. As the cold gas flows through a second heat exchanger

at the cold end of the pulse tube it picks up heat from the payload being cooled. In this work, the cooled payload is a sample stage.

The temperature of the sample is indicated by a calibrated Cernox thin film resistance thermometer in thermal contact with the sample stage. Cernox thermometers have an operational range of $\sim$ 400 K to $\sim$ 100 mK with a maximum response time of $\sim$ 50 ms and an reproducibility error of $\pm$15 mK [88]. Unlike conventional resistance thermometers they do not suffer from any significant magnetic field-induced errors, deviating by less than 5% at fields as high as 20 T [89].

3.1.2 Heliox AC-V

The majority of low temperature measurements made at the University of Warwick were carried out in an Oxford Instruments Heliox AC-V (Actively Cooled Vacuum) cryogen free cryostat, with an operational range of 5 K to 300 mK. The working principle of the Heliox AC-V system is shown in figure 3.1.

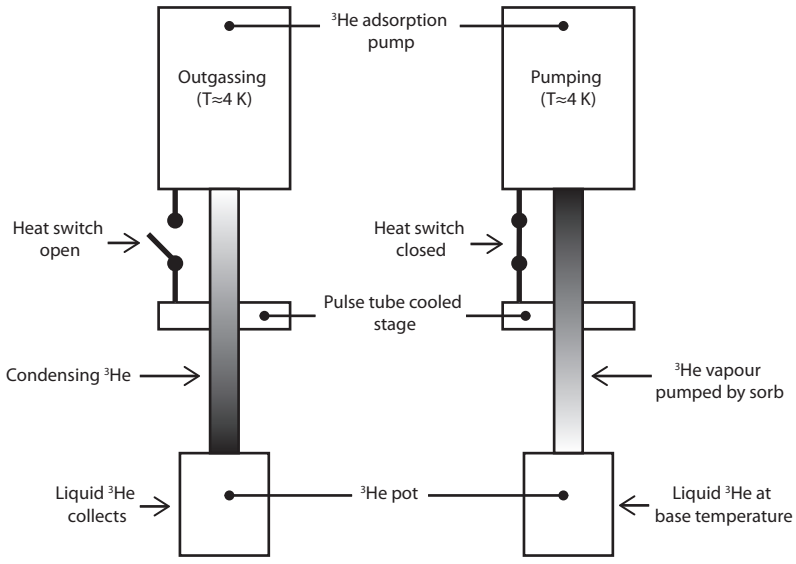


Figure 3.1: A simplified depiction of the two cooling phases of the Heliox AC-V cryostat (reproduced from the Heliox Operator's Handbook).

The ^{3}He is cryo-pumped from its dump vessel by the cryogenic adsorption pump (sorb). The dump is isolated from the rest of the insert and the sorb is heated

so that it releases the adsorbed ^{3}He gas, which is then pre-cooled to 3 K by a PTR. Next, the ^{3}He is allowed to expand into the empty dump vessel, resulting in further cooling to the point where liquid condenses and collects in the ^{3}He pot. The sorb heater is then turned off and once the temperature of the sorb is reduced below 15 K, it begins to pump vapour from the ^{3}He pot and the temperature of the pot (and sample) is reduced to a base value of 300 mK through evaporative cooling. For high temperature measurements (above 3 K) there is a heater on the ^{3}He pot, monitored by a thermometer. The temperature is controlled using an intelligent temperature controller (ITC), which automatically balances the heater power against the cooling from the PTR.

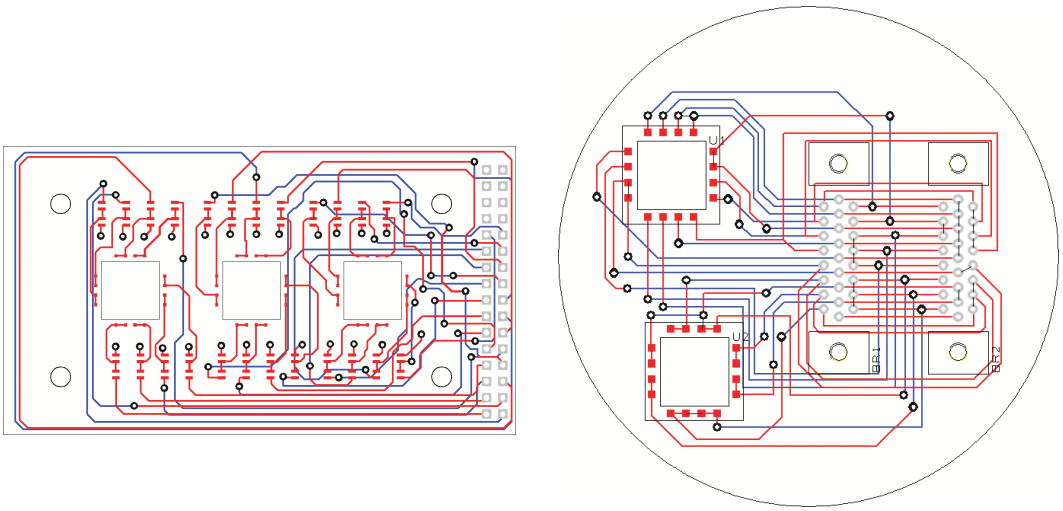
The thermometers located on each stage of the cryostat, including the sample mount, are ruthenium oxide thick film resistors. These operate well from room temperature down to 50 mK with a typical accuracy of $\pm$15 mK and a response time of 2 s. Large magnetic field can cause the calibration of ruthenium oxide sensors to drift (up to 20% at 20 T) however over the course of this investigation the magnet on the Heliox AC-V system was deactivated. Equally, the longer response time of the thermometers did not affect data acquisition due to the long time scale of the cooling and coupling measurements carried out on this equipment.

The electrical connections to the sample are made by constantan wires in a twisted pair configuration. This serves to reduce any external noise from electromagnetic fields [90]. Furthermore, a Resistor Capacitor (RC) filter stage is employed immediately prior to the wires entering the cryostat in order to suppress any external electrical noise from entering the measurement environment. Due to the superconducting electromagnet, this system included an external magnetic shield.

3.1.2.1 Multi-sample stage

The original configuration of the Heliox cryostat allowed for only a single sample to be loaded at a time, with eight connecting wires for external measurements.

One of my first projects was to design and install a new sample stage to boost measurement capacity. Figure 3.2a shows the final design. This new stage allowed for three independent samples to be loaded simultaneously, with eight connections per sample. The platform on which the samples are placed is made of high purity copper, known for its high thermal conductivity even at low temperatures. The samples are connected to a printed circuit board (PCB) by aluminium bonding wire. Each connection is made through a 680 Ω resistor and 220 nF capacitor forming a low pass filter with a cut-off frequency of $\sim 1\,\mathrm{k}\Omega$. These RC filters are positioned as close to the sample as possible in order to short out the maximum amount of electrical noise picked up inside the cryostat.



(a) Muti-sample stage (b) Shielded sample stage

Figure 3.2: The PCB layouts of the Heliox AC-V's two sample stages.

3.1.2.2 Shielded sample stage

As our fabrication and experimental procedures advanced, it became apparent that radiation from warmer parts of the cryostat were limiting some aspects our electrical measurements. A second sample stage was therefore designed, shown in figures 3.2b and 3.3, utilising a fully shielded sample mount and PCB. Due to space limitations,

the sample side RC filters were not placed directly on the PCB and instead attach directly to the rear connector of the sample stage.

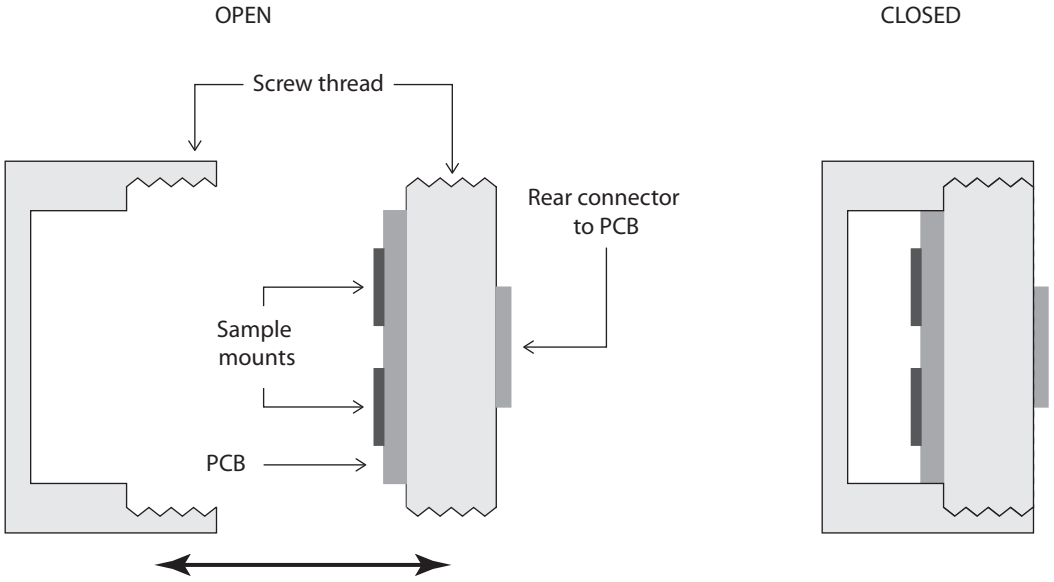


Figure 3.3: The Configuration of the shielded sample stage. When sealed, the samples are entirely enclosed in copper save for a small outlet for the PCB connector on the rear facing side. The two parts of the shield are screwed together, the thread creating a meandering path for any incident radiation.

3.1.3 Dilution refrigerator

For measurements requiring temperatures in the range of 300 mK down to 50 mK it was necessary to switch to a dilution refrigerator. Dilution refrigerators operate using a mixture of ^{3}He and ^{4}He isotopes. When cooled to just below 1 K the mixture separates into two liquid phases in equilibrium (a ^{3}He-rich phase and a ^{4}He-rich phase), with the lower density ^{3}He-rich liquid floating on the top. Pumping on the ^{4}He-rich phase will preferentially remove the ^{3}He [22], destroying the equilibrium between the two phases. This draws ^{3}He across from the ^{3}He-rich phase, requiring it to cross the phase boundary in an endothermic transition. The energy for this transition is provided in the form of heat from the chamber walls which are in turn in thermal contact to the sample stage.

The wires that run down to the sample are manganin twisted pairs, with thermocoax cabling at the sample end, forming an efficient low-pass filter [91]. The cryostat did not incorporate any dedicated magnetic shielding, though the laboratory in which it operated was kept free from any significant magnetic fields (with the ever present geomagnetic field being far too small to affect the measurements carried out [33]). The sample stage is similar to the shielded holder depicted in figure 3.3.

Thermometry in this system was achieved by ruthenium oxide sensors, as in the Heliox AC-V.

3.2 Electrical characterisation techniques

As discussed in section 1.4.6, a tunnel junction device experiences a Joule heating power dependent on the resistance of the semiconductor electrode R_{Sm}. This power has a significant effect on the power balance equation (equation 1.22) and the equilibrium electron temperature achieved. Similarly, according to section 1.4.1, the doping density (as indicated by the product of sheet density and sample thickness) is directly related to the tunnel resistance R_T which itself governs the current and cooling power of a tunnel junction device (sections 1.4.2 and 1.4.3). For these reasons it is important to fully characterise each sample, to be able to both parameterise the device and model its performance. The following techniques are used to that purpose.

3.2.1 Hall effect

The Hall effect measurement technique [33, 32] is widely used in the characterisation of semiconductor materials, yielding the resistivity, carrier density and the mobility of a sample. The two principle methodologies are described below.

3.2.1.1 Van der Pauw method

The van der Pauw method is used to measure arbitrary, two dimensional samples (in practice, samples with a thickness much less than their width and length). It does not require that the physical dimensions of the sample be known and is therefore a useful technique for wafer characterisation. Four ohmic contacts are placed in a symmetrical configuration, as close to the sample boundary as possible, in order to minimise their influence on the measurement of the intrinsic properties of the material under test. The equations below are based on the assumption of negligibly small contacts located on the periphery of the sample.

The sheet resistance R_S of the sample is measured in the absence of any magnetic field using the setup shown in figure 3.4a, according to the equation

$$R_S = \frac{\pi}{ln2}\frac{V}{I}. \tag{3.1}$$

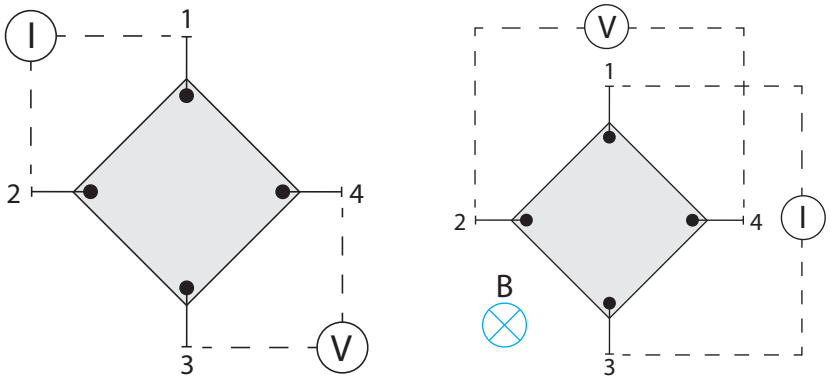
Switching to the setup illustrated in figure 3.4b and applying a magnetic field B normal to the sample plane, the sheet density is given by

$$n_S = \frac{IB}{qV}. \tag{3.2}$$

Equation 3.1 and equation3.2 are then combined to give the Hall mobility

$$\mu_H = \frac{V}{R_S IB} = \frac{1}{qn_S R_S}. \tag{3.3}$$

In each of these equations, the values of I and V are given by the average of the current and voltage measured in every possible unique configuration of the setups illustrated in figure 3.4, i.e. those which are rotationally symmetric. This helps take account of any inhomogeneity of the sample under test. In the case of a direct current DC measurement, the current is also reversed and the extracted I and V magnitudes included in the average.

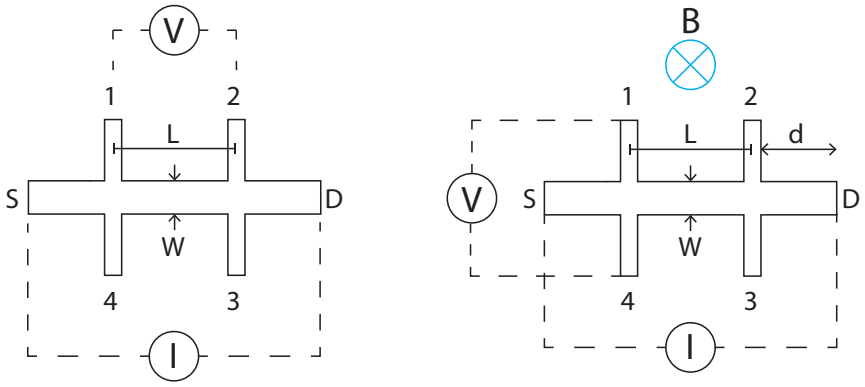


(a) Resistivity setup (b) Hall effect setup

Figure 3.4: A van der Pauw type sample set up for a measurement of (a) resistivity and (b) Hall effect.

3.2.1.2 Hall bar method

For greater accuracy, a Hall bar structure is defined on the sample using photolithography. The contact spacing is well defined and can be used in the calculation of the sample parameters, and therefore assumptions used in the van der Pauw method are no longer necessary.



(a) Resistivity setup (b) Hall effect setup

Figure 3.5: A Hall bar type sample set up for a measurement of (a) resistivity and (b) Hall effect. In base cases the current flows from the source (S) to the drain (D).

Setting up a measurement as shown in figure 3.5a, the sheet resistance is

given by

$$R_S = \frac{V}{I}\frac{W}{L} \tag{3.4}$$

where W and L are defined in diagram.

The sheet density n_S and mobility μ_H can then be calculated using equations 3.2 and 3.3.

Care must be taken when designing a Hall bar structure that the Hall effect induced electric field is not shorted by the metallic contacts at either end of the bar and at the end of each protruding arm. In practice this is achieved by ensuring the ratio $L/W \geq 10$ and that d measures tens of nanometers.

3.2.1.3 Common voltage errors

A number of voltage effects are common to this type of electrical measurement and if ignored can lead to significant errors in the calculated parameters of a sample. These include:

1. Misalignmnet / Offset voltage
2. Ettinghausen voltgae
3. Nernst voltage
4. Righi-Leduc effect
5. Thermoelectric error voltage

The misalignment voltage occurs due to any asymmetry in the contacts on the sample and results in a finite Hall voltage being measurement in zero magnetic field. This error is therefore independent of the magnetic field and can be removed by reversing the field direction and averaging the two measurements.

The Ettinghausen and Nernst effects are the converse of each other. In a conducting sample, when a current and a magnetic field are applied perpendicularly,

a thermal gradient will form orthogonal to the direction of the current and magnetic field. Equally, applying a thermal gradient to a conductive material that is subjected to a perpendicular magnetic field will induce a current normal to both. Furthermore, the Righi-Leduc effect results in a secondary temperature gradient arising from an initial thermal gradient in the presence of a perpendicular magnetic field. These three effects combined form a significant source of error in any measurement of the Hall voltage. Fortunately they can be effectively removed by using an alternating current AC source, which reverses direction on a sufficiently short time-scale to prevent any anisotropic build-up of heat or electric charge.

A thermoelectric voltage arises from electrical contact between two different materials. It does not depend on any thermal gradients present and is independent of the direction of both current flow and magnetic field. Reversing either of these will therefore allow for the effects of the thermoelectric voltage to be negated.

There are additional sources of error, such as voltage dependencies that are proportional to the time derivative of the magnetic field. However, provided a sufficiently stable magnet, these can be ignored.

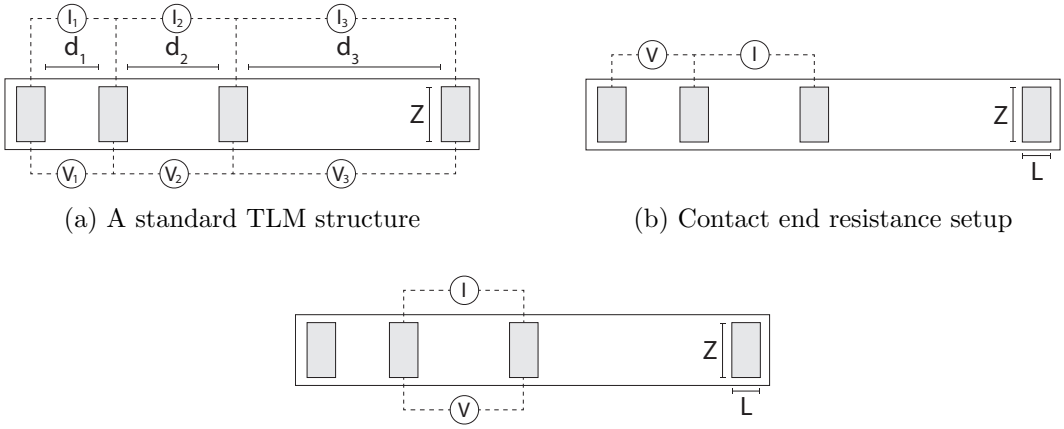
3.2.2 Transfer length method

The transfer length method (TLM) is used to determine the contact resistance between a semiconductor and a metal. A number of total resistance R_{Tot} measurements are made for a range of contact spacings d along a bar like structure, illustrated in figure 3.6a.

R_{Tot} is then plotted against d with the slope of the plot yielding the sheet resistance according to

$$\frac{\Delta R_{Tot}}{\Delta d} = \frac{R_S}{Z}. \tag{3.5}$$

The value of $R_{Tot}(d = 0)$ is equal to $2R_C$ or twice the contact resistance and the



(a) A standard TLM structure

(b) Contact end resistance setup

(c) Contact front resistance setup

Figure 3.6: Test structures and setups with contacts of width Z and length L.

specific contact resistivity ρ_C is found from the relationships

$$d(R_{Tot} = 0) = -2L_T \tag{3.6}$$

where L_T is the transfer length (the distance over which the majority of current transfers through the contact) and

$$\rho_C = L_T^2 R_S. \tag{3.7}$$

3.2.2.1 Contact End Resistance

When the contact length L greatly exceeds the transfer length, local variations in current density can lead to current crowding in the contact region which can affect the measured contact resistance. Furthermore, when $L \ll L_T$, measurements of the specific contact resistivity will be dependent on the contact area [92], when in fact ρ_C is a property solely of the metal semiconductor interface and should be independent of contact geometry.

In each of these cases, a measurement of the contact end resistance R_{CE}

(3.6b) will provide a more accurate value of ρ_C, where

$$R_{CE} = \frac{V}{I} = \frac{\rho_C}{L_T} \frac{1}{\sinh(L/L_T)}. \tag{3.8}$$

Additionally, the contact front resistance R_{CF} (figure 3.6c) is related to the R_{CE} by the useful equation

$$\frac{R_{CE}}{R_{CF}} = \frac{1}{\cosh(L/L_T)}. \tag{3.9}$$

3.3 Electron cooling measurements

The majority of cooler devices presented in this work utilise two main double junction coolers and a single, smaller double junction positioned symmetrically between the two coolers for thermometry purposes. Whilst geometry and design vary between devices, a generic layout is presented in figure 3.7 to illustrate the experimental setup.

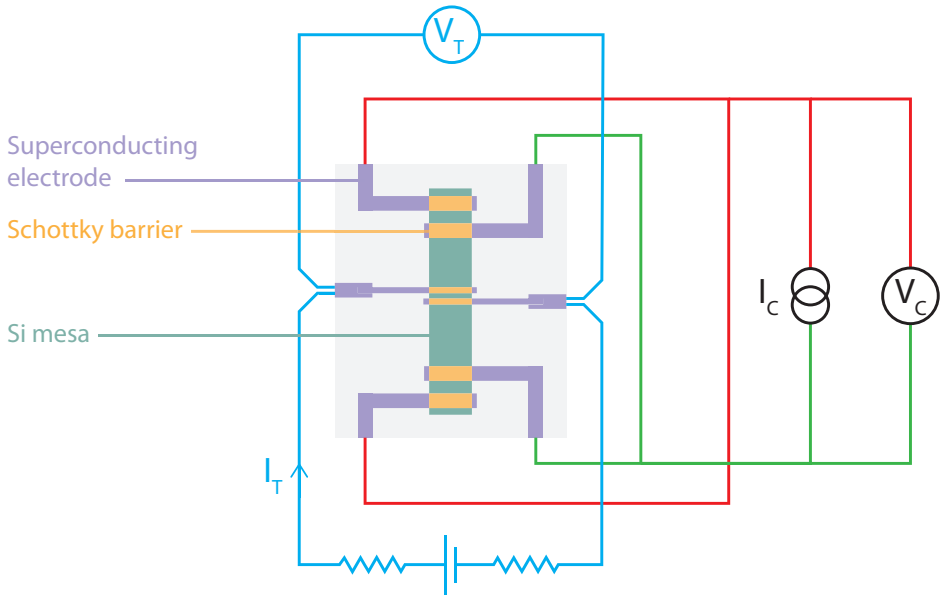


Figure 3.7: A standard measurement setup of a typical cooler device.

The cooler junction pairs are connected in parallel and a range of voltages V_C

is applied using a variable current bias. Simultaneously, the thermometer junction is biased using a high impedance battery powered current source and the voltage drop V_T is amplified using a floating differential voltage amplifier. Cooler voltage sweeps are repeated for a set of bath temperatures T_b and the thermometer junction voltage can be calibrated against a conventional ruthenium oxide thermometer at points where $V_C = 0$. This assumes that with the cooler junctions off, the electron temperature is equal to that of the surrounding bath T_b (as discussed in the tunnel junction thermometry subsection of the theory chapter, 1.5). It is therefore possible to measure electron temperature as a function of the voltage applied to the cooler junctions.

3.3.1 Treatment of errors

As discussed above, the electron temperature is taken from a calibration of the measured thermometer voltage and the readout of the ruthenium oxide thermometers. In this and all such cases wherein equipment accuracy introduces a known error into the independent variables, a 'measurement error model' regression analysis [93] is carried out to find the error in the dependent variable (T_e in this example).

Not only does this incorporate the individual measurement errors arising from equipment accuracy, it also provides a measure of the otherwise unquantifiable errors resulting from electrical and thermoelectric noise. These are unavoidable when dealing with low temperature, low current environments and can be especially devastating to experiments requiring floating measurements, such as those used in this investigation.

Overall and as in previous works on TJCs [42], any noise visible in the cooling data is a direct result of noise in the voltage measurement of the thermometer junctions, which is the dominant error source in each of the experiments. The error that arises from the voltage to temperature conversion is small at the temperature ranges employed and possible error in the absolute temperature scale (estimated at

around 1%) plays no role in this measurement.

3.4 Carrier-phonon coupling measurements

3.4.1 DC method

The standard methodology of a carrier-phonon coupling measurement is almost identical to the setup detailed in the previous section and in figure 3.7. A large resistive bar is used in place of the small cooled volume and the pair of junctions at each end are utilised simply as contacts to supply a variable heating current. As such their geometry is not optimised for cooling. The voltage across the bar is measured using a high input impedance nanovoltmeter and the thermometer junctions are operated as before. The power through the bar is calculated using the applied current or voltage and the bar resistance measured at each bath temperature, with $P = I^2 R_{Bar} = V^2/R_{Bar}$. Thus the electron temperature is measured as a function of applied heating power. This relationship can then be differentiated to provide the carrier-phonon conductance.

Any heating from the AlSi junctions at the ends of the bar is neglected under the assumption that due to the relatively high resistivity of the doped silicon and the distance of the thermometer from the junctions, the total e-ph coupling is much stronger than the heat conductivity through the wire. This implies that the measured electron temperature is dominated by the electron-phonon coupling (see also section 1.5.2.1).

3.4.2 AC method

For devices that exhibit large current leakage, electrical noise in the junction subgap region limits the accuracy of the measurement of the thermometer voltage. To counter this, a pair of lock-in amplifiers is used in the configuration shown in figure 3.8.

The signal from lock-in 1 is capacitively coupled to the thermometer so as not to disturb its DC bias. To enable this, the ac signal is applied to one contact and its inverse (180° out of phase) to the other. The resulting differential bias, balanced across the thermometer is in phase with this signal and double its amplitude. Lock-in 1 is used to measure the voltage across the thermometer whilst the magnitude of the bias current is monitored by lock-in 2, synchronised to the signal generated by lock-in 1.

This setup better isolates the thermometer current bias from the varying heating current supplied to the bar. The paired lock-in amplifiers completely remove any DC noise and filter out any component noise at frequencies other than that of the thermometer signal. Furthermore, any remaining noise at that frequency is reduced by integrating over a set time window.

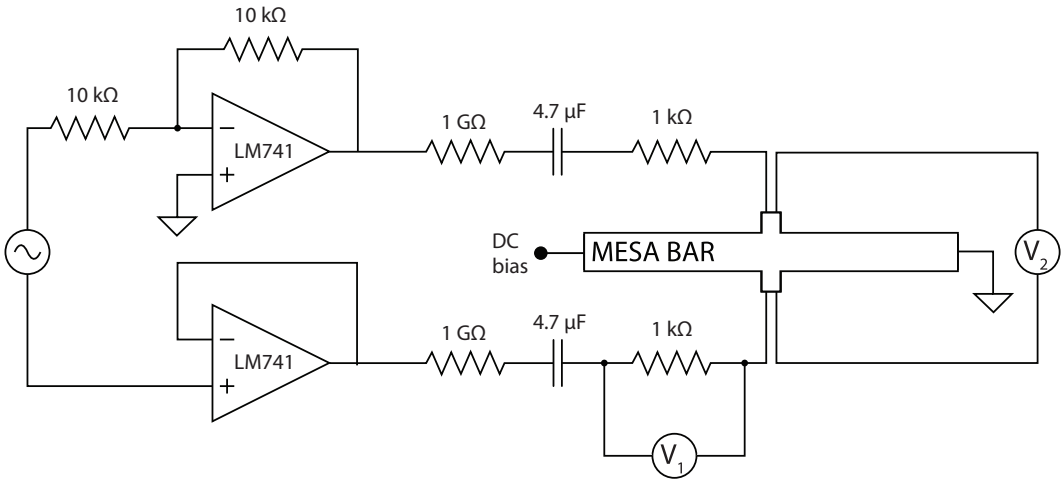


Figure 3.8: The AC measurement circuit complete with 1 GΩ current setting resistors.

3.4.3 Treatment of errors

As in section 3.3.1, the error in the determined electron temperature is given by a regression analysis. The error in injected power is calculated from the errors in the measured current and voltage, with the accuracies of the source-meters used

in the experiments being known. The errors in temperature and power are then propagated through a numerical differentiation (which introduces its own round-off and truncation errors [94]), yielding the error in the coupling term via the standard error propagation formulae [95] (see chapter 5). In each case, the dominant error is found to be the noise in the voltage measurement of the thermometer junctions.

3.5 Structural characterisation methods

This section provides a brief overview of the equipment and techniques used in the preparation and imaging of various samples from unprocessed wafers to fully fabricated devices. The details given are only those necessary to understand which particular structural characterisation methods should be employed depending on what information is required. For a more thorough explanation of each technique I refer the reader to the relevant leading textbooks referenced in each subsection.

3.5.1 Transmission electron microscopy

Transmission electron microscopy (TEM) is used to probe the microstructure of a material, giving information on its morphology, crystal structure, defect density and composition [96]. Within this investigation, TEM is principally used to image wafer cross-sections in order to check the quality, thickness and uniformity of the composite layers.

Before being imaged, a sample is first thinned such that it becomes electron transparent ($\sim 100\,\mathrm{nm}$). This is accomplished by mechanically grinding the sample to a few tens of microns, followed by ion polishing and milling using a precision ion polishing system. A high voltage electron beam is then focused onto the sample using electromagnetic lenses. The electrons are generated via thermionic emission from a heated tungsten filament. They are then accelerated towards a grounded anode at a typical voltage of $200\,\mathrm{kV}$, directing the beam towards the sample, with the source-

lens-sample column is kept under a high vacuum (¡ 10-7 mbar) to reduce electron interaction with matter. The beam is then passed through a condenser lens which sets the spot size (the fraction of the sample illuminated). A condenser aperture is then employed to control the beam intensity and collimate the electron stream before it strikes the sample under observation. Due to the high energies involved, the majority of the electrons are transmitted through the material. Once the beam has passed through, a second lens is used to expand the beam, magnifying the image produced. Further sets of lenses are then used to correct for any aberrations before the final image is projected onto a digital camera.

Contrast in the image is a result of the varying absorption of electrons across the sample as well as interactions and interference patterns formed between the transmitted and diffracted electrons. The short electron wavelength ($\sim 0.0025\,\text{nm}$ at $200\,\text{keV}$) allows TEM to exceed the resolution of conventional optical microscopes ($\sim 200\,\text{nm}$), being limited not by the wavelength of the probe but by imperfections in the focusing lenses, with a resolution close to $0.1\,\text{nm}$.

3.5.2 Focused ion beam scanning electron microscopy

For the development of the semiconductor-insulator-superconductor junctions presented in chapter 6, it was necessary to view the cross-sections of completed devices in order to confirm the thickness of the oxide-insulator layer and study its incorporation into the junction. Conventional TEM preparation methods would obliterate any structures on the surface of the sample and are thus unsuitable. Instead, one can utilise focused ion beam scanning electron microscopy (FIBSEM) [97, 98], using the process outlined below [99].

A gallium ion beam is focused onto the sample under investigation, resulting in the sputtering of secondary ions and electrons from the sample surface. At low beam energies, these secondary ions along with any reflected gallium ions may be detected in order to form an image. Similarly, a built-in scanning electron micro-

scope (SEM) may be used, detecting either the electrons generated via the focused ion beam (FIB), or a separate incident electron beam.

At higher ion beam energies, a large amount of material can be removed via sputtering. This allows for precision etching of the sample and is often used to expose a buried cross-section of interest. However, the gallium ion beam used to cut through the sample results in a degree of ion implantation. To stop this from damaging the top layers of the cross-section of interest, a protective layer of carbon is first deposited. A carbon precursor gas adsorbs on to the sample surface and is decomposed into volatile and non-volatile components (carbon) by the ion beam. The non-volatile carbon remains as a film, as shown in figure 3.9.

The gallium ion beam operating at high energy is then used to etch a trench either side of the desired cross-section (figure 3.10). A lower energy beam is then used to clean each face and thin the section before lift-out. The beam is again used to etch into the material, this time to cut around the cross-section, leaving it supported only at its top edge (figure 3.11). A micromanipulator is maneuvered into position and adhered to the section using the carbon film process described earlier (figure 3.12). This allows for the final cuts to be made before the cross-section is lifted out and positioned on a sample holder, where it is again thinned to $\sim 100\,\mathrm{nm}$ using the gallium beam (figures 3.13 and 3.16). The sample is then ready to be imaged in a transmission electron microscope.

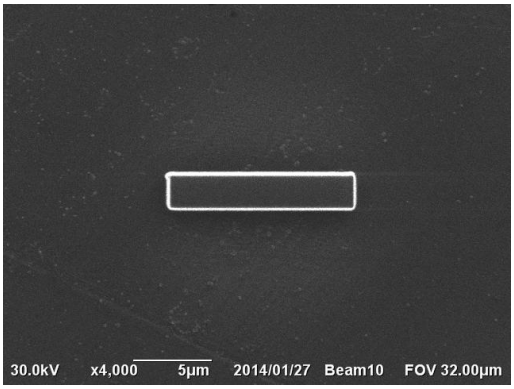


Figure 3.9: A protective carbon strip is deposited over the top of the cross-section to be excised.

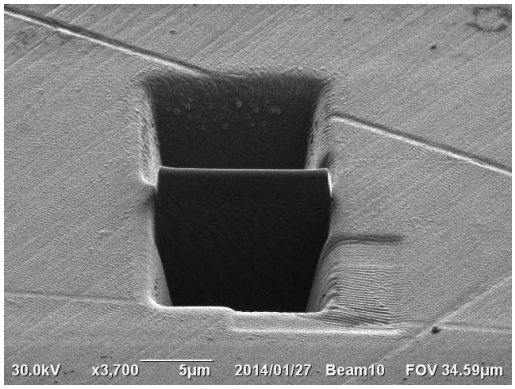


Figure 3.10: The cross-section is exposed.

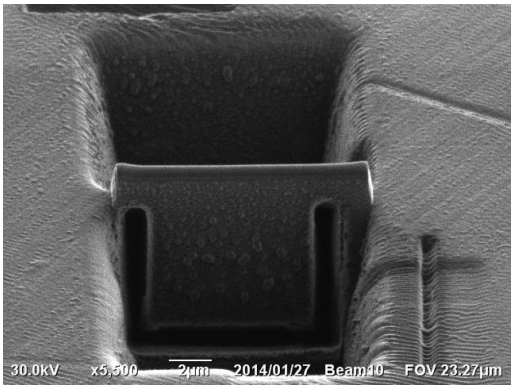


Figure 3.11: A U-cut is made to prepare the cross-section of extraction.

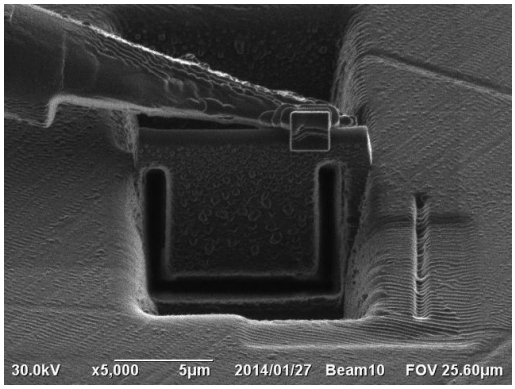


Figure 3.12: A micromanipulator is attached to the top of the cross-section, to support it once free of the bulk material.

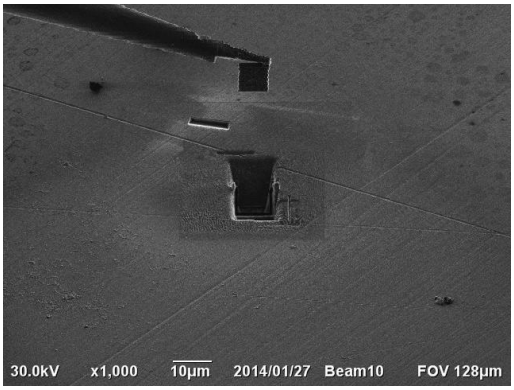


Figure 3.13: The release cuts are made and the cross-section is lifted out in-situ.

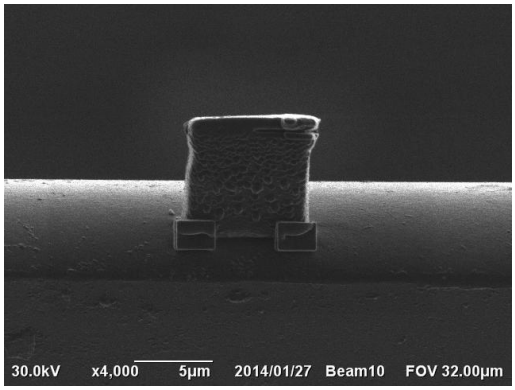


Figure 3.14: The cross-section is then placed on and adhered to a TEM support grid before being cut free from the micromanipulator.

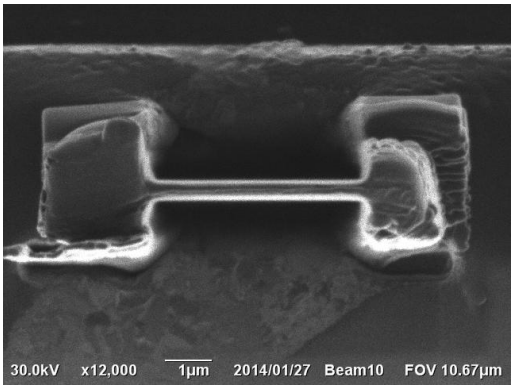


Figure 3.15: The cross-section then undergoes a final stage of thinning.

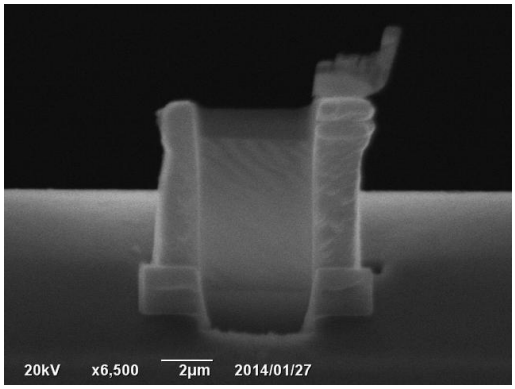


Figure 3.16: The cross-section is now electron-transparent and can thus be imaged using conventional TEM.

4

Alternatives to aluminium superconducting contacts

In this chapter I investigate the use of both platinum-silicide and vanadium as replacements for conventional aluminium superconducting electrodes in Sm-S junctions. Despite the fabricated devices not performing as well as was hoped, I believe there is much to be learnt from this work. It is therefore well worth discussing before the later chapters in which the more successful investigations are presented.

I showed in section 1.4.3 that the optimum cooling power of junction is given by

$$P_{opt} \approx \frac{\Delta^2}{e^2 R_T}\left[0.59\left(\frac{k_B T_e}{\Delta}^{3/2}\right) - \sqrt{\frac{2\pi k_B T_b}{\Delta}} \times exp\left(-\frac{\Delta}{k_B T_b}\right)\right] \tag{4.1}$$

with the tunnel current through the junction being

$$I_{opt} \approx 0.48\,(\Delta/eR_T)\,\sqrt{k_B T_e/\Delta}. \tag{4.2}$$

Cooler devices are often compared using their coefficient of performance, otherwise known as their efficiency. This is defined as the ratio between the useful cooling

power P_{opt} and the total input power, where

$$\eta = \frac{P_{opt}}{I_{opt}V}. \tag{4.3}$$

In the low temperature limit $T_e << T_C$ and for $V = \Delta/e$ and $\Delta = 1.764 k_b T_C$ [28, 9], equation 4.3 simplifies to

$$\eta = 0.7\frac{T_e}{T_C} \tag{4.4}$$

where T_C is the critical temperature of the superconductor material. Figure 4.1 highlights the difference between this and the full expression for η.

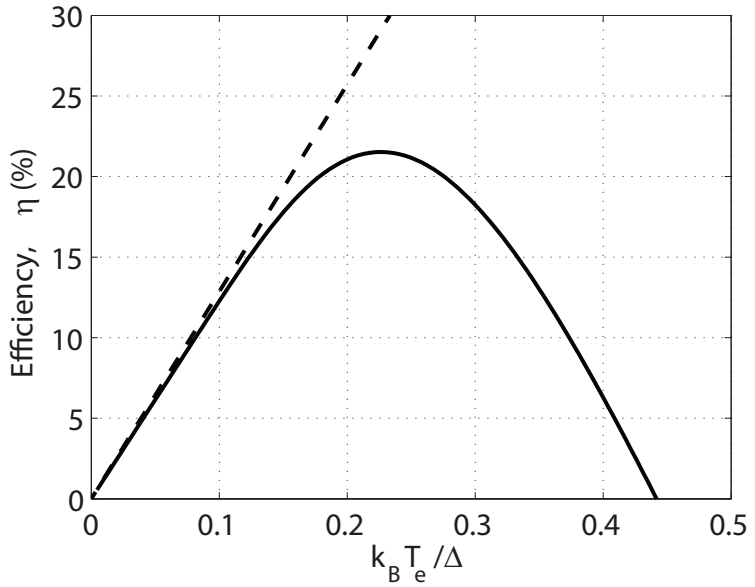


Figure 4.1: The efficiency of an aluminium based Sm-S cooler junction calculated using equation 4.3 (solid line) and 4.4 (dashed line).

According to equation 4.4, one would expect a cooler with a lower T_C superconductor to have a greater efficiency. In reality however, considering equation 4.3 and figure 4.1, this improved efficiency in the low temperature limit will be counterbalanced by an earlier reduction in efficiency as temperature increases. Still, this

implies that one can tune the optimum cooling performance of a junction to a temperature range determined by its application by sacrificing performance at certain other bath temperatures.

This is perhaps better demonstrated by calculating P_{opt} as a function of temperature T_e for multiple values of T_C. Whilst at first inspection the optimum power does not appear to depend on the superconductor critical temperature, one notes that it does depend on Δ where $\Delta = 1.764 k_B T_C$ [9]. To this end, figure 4.2 shows the cooling power at the optimum voltage for both a conventional aluminium based device and those utilising platinum silicide or vanadium as the superconducting electrode. Platinum silicide has a typical critical temperature of around 1 K but this can be suppressed to approximately 0.6 K in thin films such as those utilised in cooler devices [100]. Using this value of 0.6 K, I calculate that a silicon-platinum silicide cooler junction would have a peak performance at ~ 0.2 K as opposed to an aluminium device which would peak at ~ 0.6 K. Whereas a silicon-vanadium cooler junction, with a T_C of 5.4 K and a half band gap of $\Delta = 0.7$ meV, would perform best at ~ 0.95 K.

4.1 Vanadium

The motivation behind the transition to a vanadium based TJC is therefore quite apparent. Expressed in another way, the cooling power at the optimum bias voltage increases as a function of the superconducting half band gap Δ, as shown by figure 4.3. It was hoped that this greater cooling power would be capable of compensating a larger heat load from the environment, thus enabling cooling from higher bath temperatures. Quaranta et al. [13] had demonstrated cooling from 1 K to 0.4 K using a vanadium aluminium superconductor-insulator-superconductor (SIS) junction [9] and with this promising result, work began on the first silicon-vanadium Sm-S device, with half band gap of $\Delta = 0.7$ meV compared to $\Delta = 0.2$ meV for

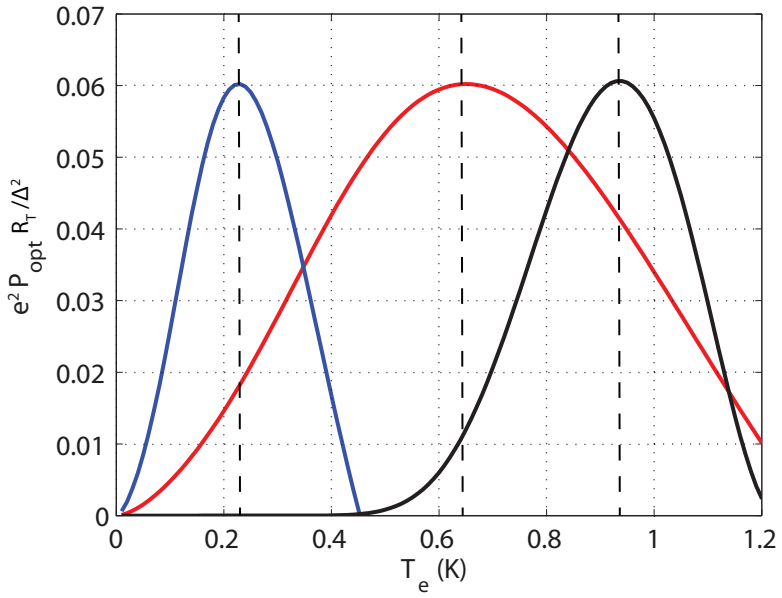


Figure 4.2: Plotting cooling power normalised to R_T and Δ allows for a direct comparison of the relationship between optimum power and temperature for devices incorporating either aluminium (red), platinum silicide (blue) or vanadium (black).

aluminium.

Figure 4.4 illustrates a problem encountered early in the fabrication process when it proved difficult to form well defined superconducting electrodes due to the poor adhesion of the vanadium and the subsequently poor lift-off. This issue was eventually solved by utilising the bi-layer process and an aluminium adhesion layer, detailed in section 2.3

Also depicted in figure 4.4 is the cooler geometry, consisting of four S-Sm-S junctions in parallel, with a single Sm-S junction area of $4\,\mu\text{m} \times 4\,\mu\text{m} = 16\,\mu\text{m}^2$. The layout was designed to allow for a degree of misalignment of the photolithography masks during fabrication, ensuring the junction area remained the same across device batches despite any relative offset between the semiconductor and superconductor electrodes. It should be noted as an aside that the limbs of the semiconducting electrode, connected in series, present in this design had the additional effect of increasing the semiconductor resistance R_{Sm}, and that this geometry was subsequently abandoned in favour of alternate cooler junction designs discussed in later

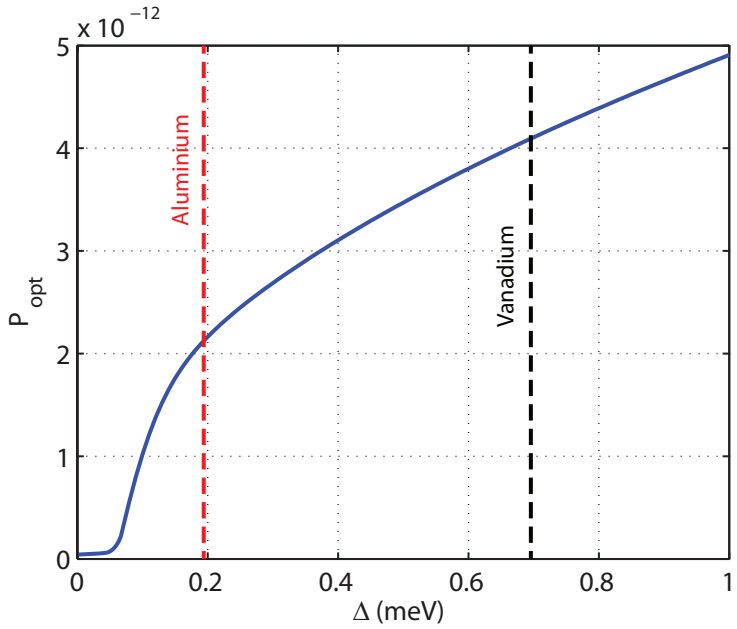
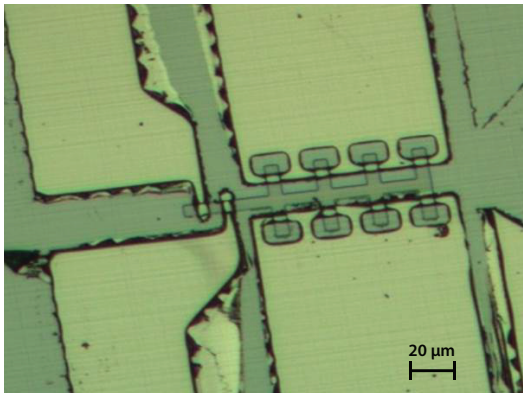
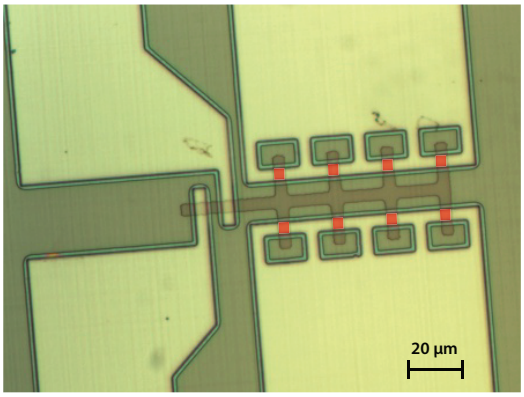


Figure 4.3: A large band gap allows for a greater voltage to be applied across a junction before it becomes over-biased. Calculated with the parameters: $R_T = 500\,\Omega$, $\Sigma = 1 \times 10^8\,\mathrm{W\,K^{-5}\,m^{-5}}$ and $\Omega = 30\,\mathrm{nm} \times 20\,\mu\mathrm{m} \times 10\,\mu\mathrm{m}$. The band gaps of aluminium (red) and vanadium (black) are highlighted.



(a) Initial problems with adhesion and poor lift-off.



(b) Solved by using an aluminium adhesion layer and bi-layer resist with a well defined undercut. Junction areas are highligted in red

Figure 4.4: Optical micrographs showing fabrication issues with vanadium devices.

chapters.

A preliminary electron cooling measurement was carried out and the results are summarised in figure 4.5. The electron temperature is inferred from a calibration

of thermometer voltage against bath temperature, as described in section 3.3 of chapter chap:Experimental.

The actively cooled volume, that of the semiconductor electrode, is 23 µm^3 (typical for TJCs [56, 101]). It is clear that any applied bias across the cooler junction results in a substantial temperature increase in the semiconductor and that this attempt to capitalise on the larger band gap of vanadium has failed.

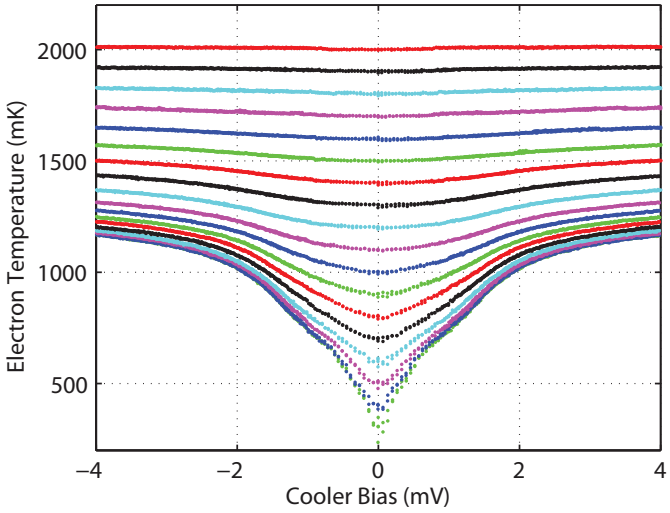
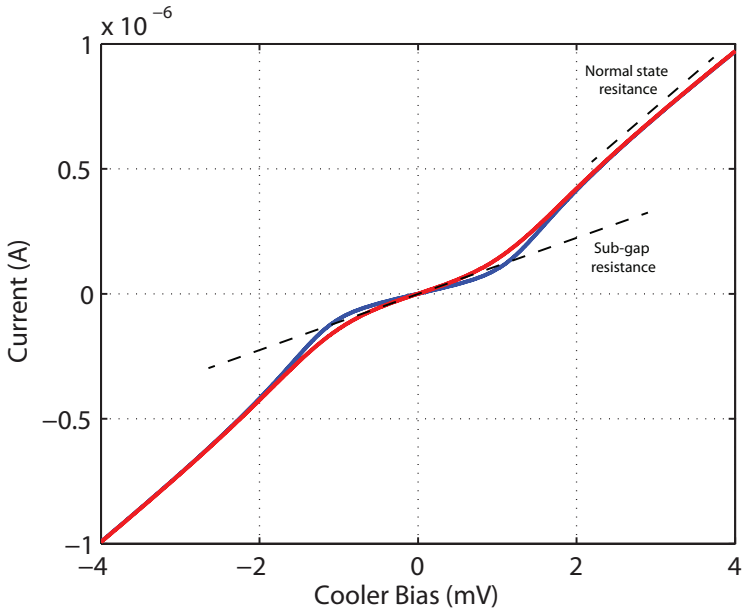


Figure 4.5: Extracted voltage-temperature data of the cooled semiconductor volume. Each coloured data group represents a voltage sweep at a single bath temperature, ranging from 300 mK to 2 K.

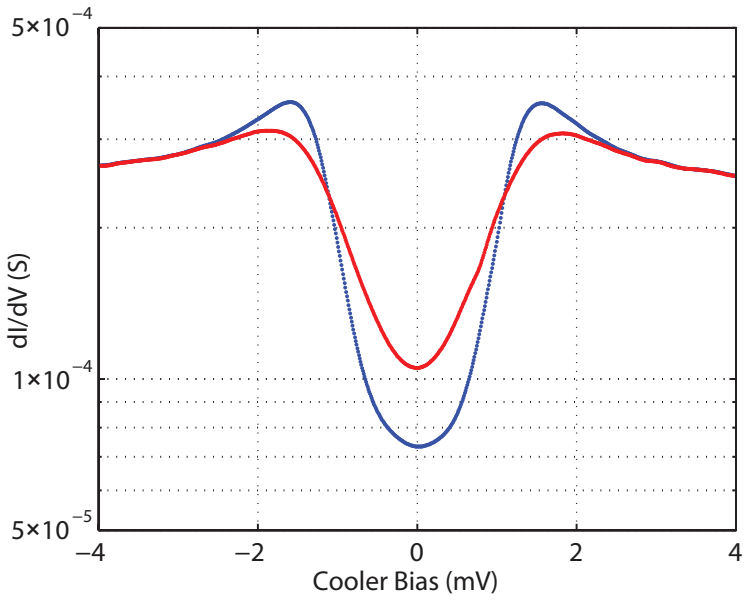
From Figure 4.3 one would expect the cooling power from a silicon-vanadium junction to be double that of a silicon-aluminium device. One may therefore deduce that either the cooling power is not what was expected, or that the silicon-vanadium junction is subjected to a greater total heating power than its aluminium predecessors.

Figure 4.6 shows the current voltage behavior of the finished silicon-vanadium cooler junction. It is immediately apparent from the dI/dV (figure 4.6b) data that the sub-gap resistance is very low even at a base temperature of 300 mK, being approximately 14 kΩ compared to the 4 kΩ normal state resistance. This low resistance highlights the apparent high concentration of sub-gap states, parameterised

by a Γ value of $0.29\,\Delta \pm 0\,02\Delta$. Γ/Δ is given by the ratio of the normal state resistance and the low temperature limit of the sub-gap resistance and its error is found by propagating the uncertainties introduced by the experimental instruments through the numerical differentiation algorithm and finally through the ratio of the two resistances [95]. This value of Γ is over an order of magnitude greater than that observed in aluminium based devices [56].



(a) Cooler IV of the cooler junction array.



(b) Differential conductance data.

Figure 4.6: Current voltage characteristics of the silicon-vanadium cooler device at 2 K (red) and 300 mK (blue).

Taking the data on optimum cooling power versus Δ and inserting it into a simple heat balance model, one can simulate the cooling performance of a test junction and observe the effect of a wider band gap on the minimum temperature achieved. As shown by figure 4.7, whilst the greater cooling power benefits the ideal device, introducing a finite sub-gap density of states leads to a significant loss of performance as Δ increases. This makes sense, given that a constant sub-gap state density will lead to a larger absolute number of sub-gap states in superconductors with larger half band gaps, with each state constituting a drain on the effective cooling power of the junction (as shown in section 1.4.4). This explanation is further borne out by the unusually rapid change in electron temperature with applied voltages V_C in the $-\Delta/e > V_C < \Delta/e$ range at low temperature, in which one would typically expect little activity due to the diode-like nature of TJCs.

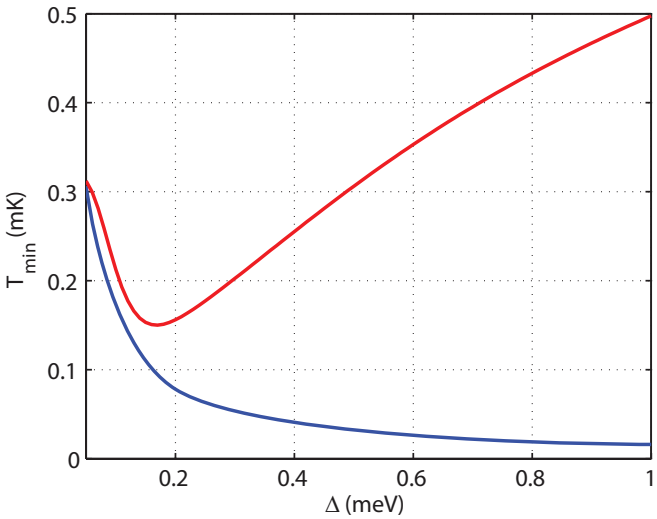


Figure 4.7: The minimum electron temperature versus half band gap achieved by a cooler junction at the optimum operational voltage in the ideal ($\Gamma = 0$) case (blue) and non-ideal ($\Gamma = 0.01\,\Delta$) case (red). Calculated with the parameters: $R_T = 500\,\Omega$, $\Sigma = 1 \times 10^8\,\mathrm{W\,K^{-5}\,m^{-5}}$ and $\Omega = 30\,\mathrm{nm} \times 20\,\mu\mathrm{m} \times 10\,\mu\mathrm{m}$.

A second explanation for this result can be found when inspecting equation 4.3 that governs tunnel junction cooling efficiency. Whilst the optimum cooling power of a vanadium based junction was predicted to be twice that of a conventional

aluminium junction, figure 4.8 implies a dramatic fall off in efficiency with increasing bang gap: That is, for larger Δ superconductors, the proportion of injected power that contributes to the cooling of the electrons is significantly curtailed. Therefore, by transitioning from aluminium to vanadium, the efficiency will drop by almost a factor of three, severely counteracting any expected increase in cooling power.

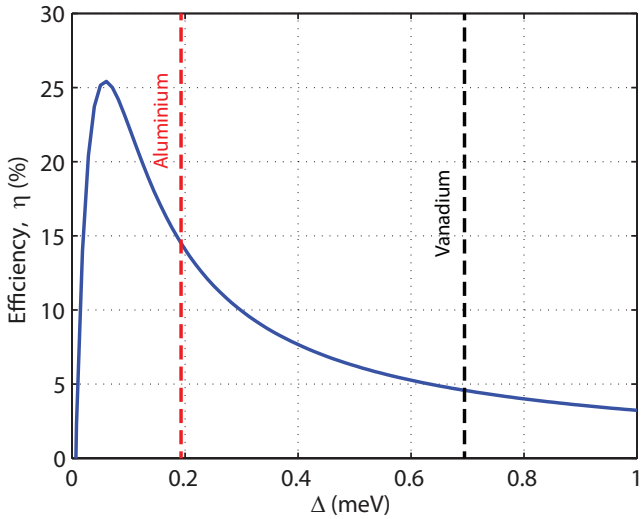


Figure 4.8: The efficiency is shown to decrease for higher values of Δ. Calculated with the parameters: $R_T = 500\,\Omega$, $\Sigma = 1 \times 10^8\,\mathrm{W\,K^{-5}\,m^{-5}}$ and $\Omega = 30\,\mathrm{nm} \times 20\,\mu\mathrm{m} \times 10\,\mu\mathrm{m}$.

It was therefore decided that the development of a silicon-vanadium cooler junction be halted in favor of more promising alternatives, and that work be undertaken to attempt to solve the apparent problem of performance hindering sub-gap states indicated by the low sub-gap resistance, as demonstrated in figure 4.7, and the resulting high value of Γ.

4.2 Platinum Silicide

As mentioned in section 1.4.4 and evidenced above in section 4.1, sub-gap leakage as a result of states in the superconducting band gap represent a major drain on the performance of tunnel junctions and their cooling properties. Regardless of the

origin of these gap states, it was reasoned that utilising a superconducting material with a narrower gap, such as PtSi, would limit their effect. This concept is illustrated by figure 4.9, in which a constant density of sub-gap states coupled with a smaller gap results in fewer states available within the bad gap.

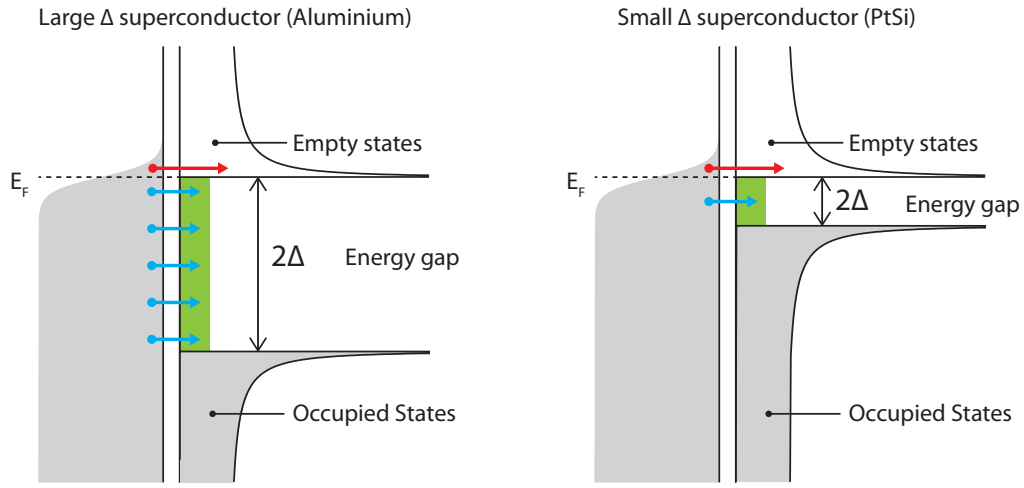


Figure 4.9: The effect of a band gap width on unwanted cold electron tunnelling. By shrinking the total number of available gap states (green) one can reduce the fraction of junction current made up of electrons with energy below the Fermi level E_F.

Secondly, as touched upon in section 1.5.2.1, saturation of the temperature response of an Sm-S junction is a significant impediment to junction based thermometry. By adopting a superconductor with a lower half band gap Δ one can shift the temperature range over which the thermometer junction will have a satisfactorily linear response, as shown in figure 4.10.

This effect results from the presence of a finite sub-gap tunnelling Γ, which both reduces and broadens the peak in the superconductor density of states function $g(E)$ (see figure 1.11a). For smaller values of Δ, whilst the peak is still lowered, it is broadened to a lesser extent, as demonstrated in figure 4.11. It is clear that the peak in the lower Δ case has a much higher rate of change with energy. Looking back to section 1.4.2 and equation 1.4, the tunnel current through a junction is calculated using the product of the Fermi function describing the electron distribution in the

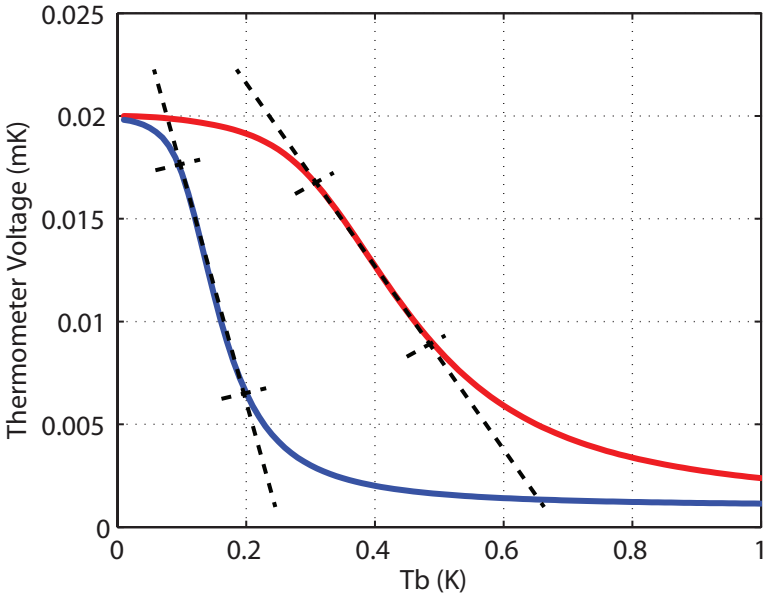


Figure 4.10: Simulated response of a S-Sm-S thermometer with $\Delta = 0.2\,\text{meV}$ (aluminium - red) and $\Delta = 0.07\,\text{meV}$ (platinum silicide - blue), with $R_T = 500\,\Omega$.

semiconductor and the superconductor density of states. Thus any current response due to a change in temperature is proportional to the change in the energy spread of the Fermi function multiplied by the density of states over that energy range. Therefore, as the spread in the Fermi function of the semiconductor decreases with temperature, the resulting change in current will be more pronounced in the low Δ case, as a result of the greater change in the density of states function over the same range of energy.

Motivated by these points, a platinum silicide-silicon tunnel junction was fabricated to the specifications given in figure 4.12. A silicon-on-insulator (SOI) substrate was utilised, and underwent arsenic ion implantation to define an electrically active mesa with approximate dimensions of $30\,\mu\text{m} \times 5\,\mu\text{m} \times 88\,\text{nm}$ with a doping concentration of $8 \times 10^{19}\,\text{cm}^{-3}$. Further details on the sample fabrication can be found in section 2.4.

Low temperature ($< 15\,\text{K}$) Hall measurements on the arsenic implanted SOI gave a sheet resistance of $\sim 100\,\Omega/\square$, confirming the value expected for that doping

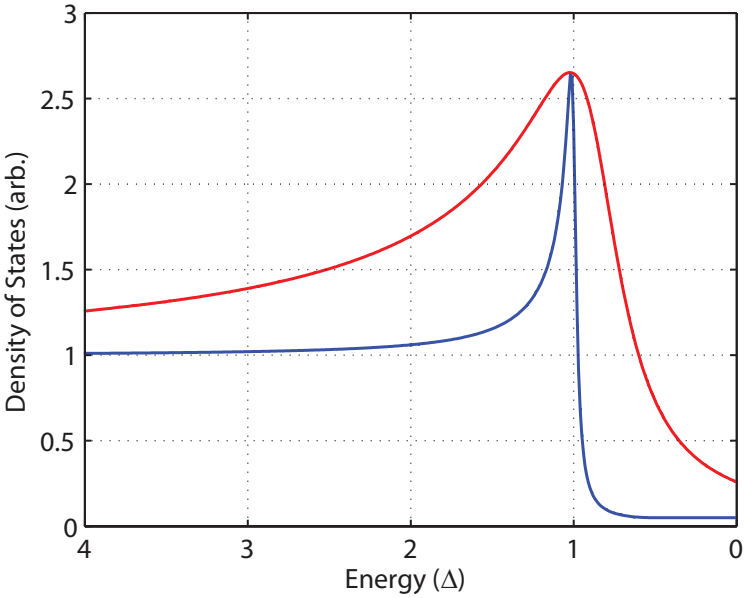


Figure 4.11: Broadened density of states ($\Gamma = 0.05\,\Delta$) calculated using the Dynes model (equation 1.12) for $\Delta = 0.2\,\text{meV}$ (aluminium, red) and $\Delta = 0.07\,\text{meV}$ (platinum silicide, blue).

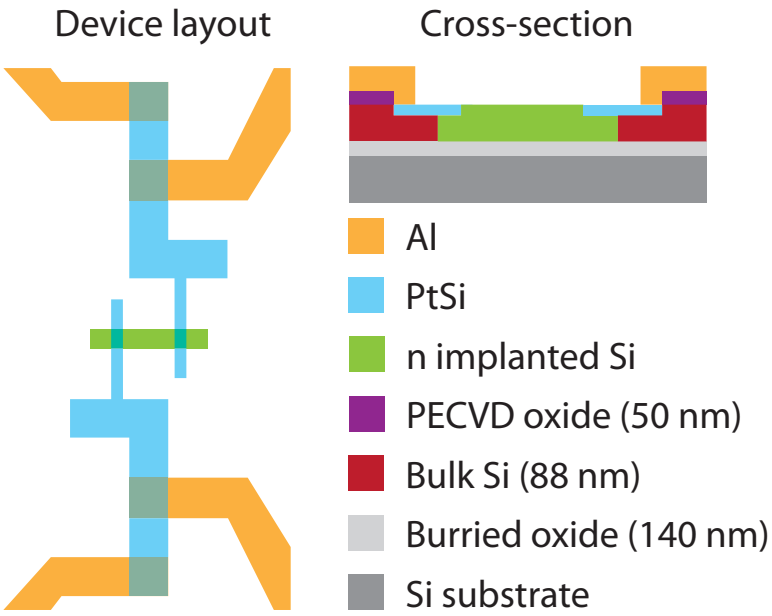
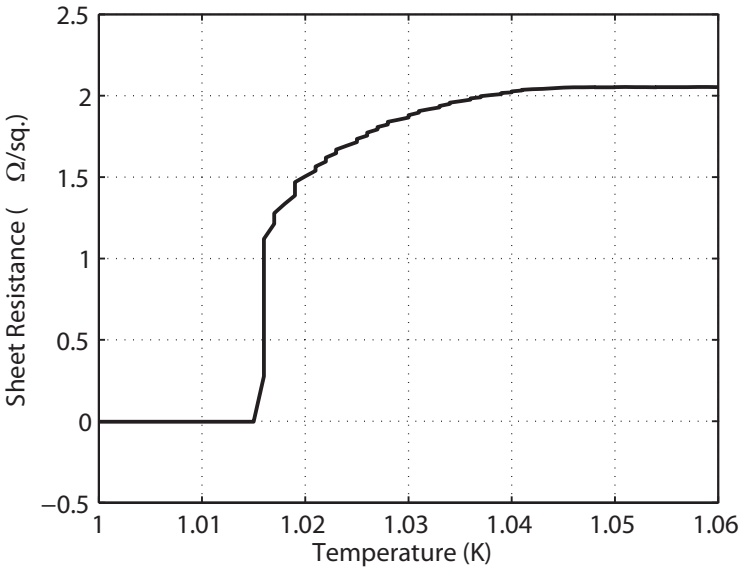


Figure 4.12: Device layout and cross-section of the PtSi cooler. The junction areas are 2.5 µm by 5 µm and the implanted region has a length to width ratio of 3, giving a series resistance R_{Sm} of 320 Ω.

density [32]. Figure 4.13 compares T_C measurement for PtSi films of different thickness on low doped silicon. The T_C is reduced from 1.015 K±0 005K for the 100 nm film, to 0.786 K±0 05K in the 10 nm film, where the increased sheet resistance of the thinned sample works to suppress superconductivity [102]. This reduction is ever so slightly less than expected given that a T_C of $\sim$ 0.63 K was obtained for a similar film in previous work [100].



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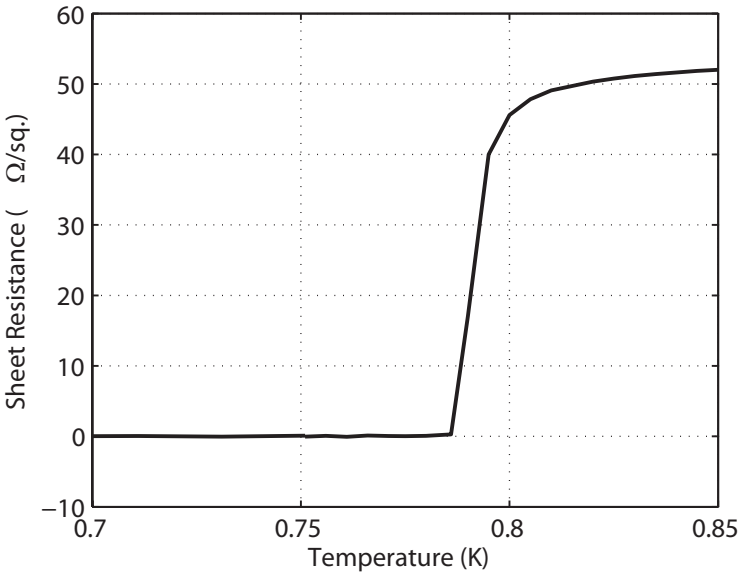


(b)

Figure 4.13: Sheet resistance versus temperature, showing superconducting transition temperature T_C of PtSi for layer thicknesses of (a) 100 nm (b) 10 nm.

Current-voltage measurements were performed on the 10 nm thick PtSi device at 100 mK in a dilution refrigerator and are shown in figure 4.14. The same data is then used to calculate the differential conductance dI/dV (figure 4.14b). The data has been fitted with a constant electron temperature T_e, using equations

from section 1.4.2, which are reproduced here for clarity.

$$I = \frac{1}{eR_T}\int_{-\infty}^{\infty} F(E, V/2, T_e, T_b).g(E)dE \tag{4.5}$$

with

$$F = f(E - eV, T_e) - f(E, T_b). \tag{4.6}$$

and

$$g(E) = Real\left|\frac{E - i\Gamma}{\sqrt{(E - i\Gamma)^2 - \Delta^2}}\right|. \tag{4.7}$$

This constitutes the isothermal model.

If one allows the electron temperature T_e to vary (known as the cooling model, see section 1.4.3) the expression for the cooling power of the S-Sm-S junctions

$$P_C = \frac{2}{e^2R_T}\int_{-\infty}^{\infty} (E - eV/2).F(E, V/2, T_e, T_b).g(E)dE \tag{4.8}$$

is used along with a heat balance equation to solve for T_e.

$$P_C = P_{e-ph} + P_J \tag{4.9}$$

with the electron-phonon coupling heat power given by

$$P_{e-ph} = \Sigma\Omega(T_e^n - T_p^n) \tag{4.10}$$

and the Joule heating power

$$P_J = I^2R_{Sm}. \tag{4.11}$$

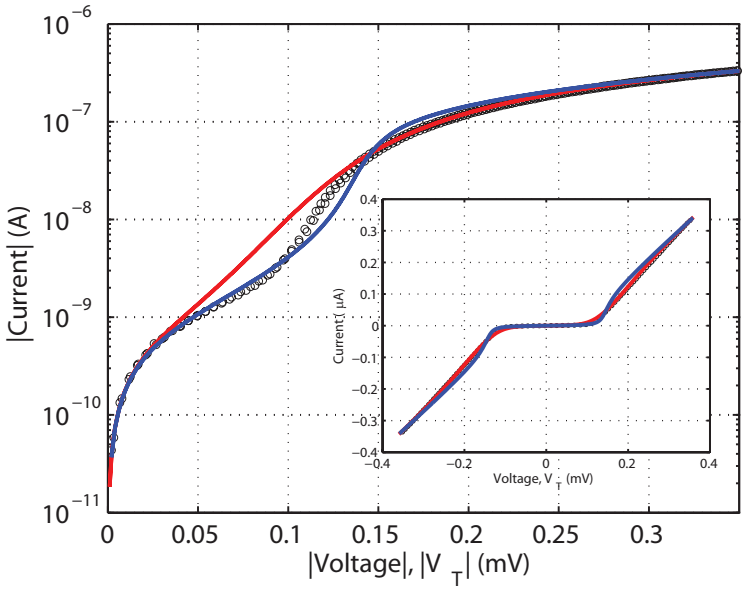
The isothermal model (equations 4.5 to 4.7 with $T_e = 100\,\mathrm{mK}$) provides a reasonable fit to the data as shown by the dashed curves in figure 4.14, giving a tunnel resistance $R_T = 300\,\Omega$ ($3.75\,\mathrm{k\Omega\,\mu m^2}$), superconductor half band gap $\Delta = 70\,\mu\mathrm{eV}$ and sub-gap leakage parameter $\Gamma = 0.8 \times 10^{-2}\,\Delta$, a typical value of semiconductor-

superconductor devices [56]. In figure 4.14b, the isotherm curve (dashed) falls to the minimum with straight sides on the log-linear plot. This exponential behavior is typical of an isotherm plot and provides a clear distinction from a device with cooling [81]. Figure 4.14a shows that the isotherm does not capture the low current around $V_C = 0.1\,\mathrm{mV}$, although the isotherm model fits well for higher biases ($V_C > 0.14\,\mathrm{mV}$). Reduced current relative to the iostherm is characteristic of cooling in the device [81].

When using the cooling model (equations 4.5 to 4.11 with T_e set by the solution of equation 4.9), one is better able to reproduce the experimental data in the sub-gap region (for bias $|V_C| < 2\Delta/e$). A value of $\Sigma = 3.1 \times 10^8\,\mathrm{W\,K^{-6}\,m^{-3}}$ was used from similar sample studied by Kivinen et al. [59], along with the volume $\Omega = 32\,\mu\mathrm{m} \times 5\,\mu\mathrm{m} \times 88\,\mathrm{nm} = 1.41 \times 10^{-17}\,\mathrm{m}^3$. The model predicts cooling from 100 mK to about 50 mK, as shown in figure 4.15. The cooling power at 100 mK was 0.72 pW (or 29 fW $\mu\mathrm{m}^{=}2$). Additionally, figure 4.15 shows the predicted cooling if all the parameters were the same except for $\Delta = 190\,\mu\mathrm{eV}$; as might be expected for a thicker layer of PtSi or aluminium. The larger Δ allows more leakage current and hence prevents cooling below the bath temperature.

Discrepancies in the experimental and predicted data are most noticeable at biases beyond the sub-gap ($|V_C| > 2\Delta/e$) and are shown more clearly in the dI/dV curve. As shown in figure 4.14b, the cooling model predicts peaks in dI/dV at the $\pm 2\Delta/e$ bias points. In both the experimental data and the isotherm, these peaks are very weak; also, in the IV curves they both display an abrupt transition from sub-gap to normal state resistance (as shown in the inset of figure 4.14a).

By inspection of equation 4.5, it can be seen that dI/dV should have maxima which correspond to peaks in the superconductor density of states (equation 4.7), though these will be located at voltages of $\pm 2\Delta/e$ rather than $\pm\Delta/e$ given that the device is formed from two junctions in series. The peak height is reduced in the presence of high sub-gap leakage ($\Gamma = 0.8 \times 10^{-2}\,\Delta$ is quite high compared



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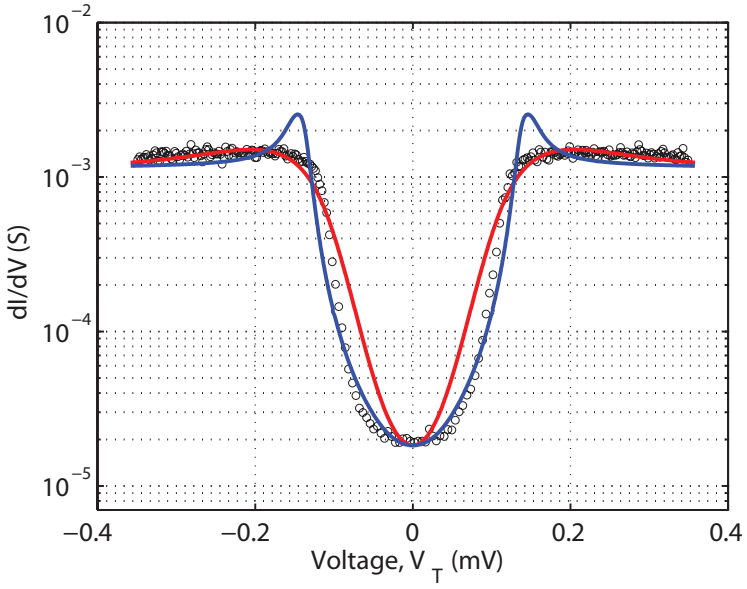


(b)

Figure 4.14: (a) Log current axis IV results for the 10 nm thick PtSi cooler (the inset shows the same data with a linear current axis) (b) Differential conductance. All figures use the same experimental data measured at 100 mK (black circles). The red line shows the 100 mK isotherm fit to the experimental data. The isotherm model uses the parameters $\Delta = 70\,\mu\text{eV}$, $\Gamma = 0.8 \times 10^{-2}\,\Delta$, $R_T = 300\,\Omega$, $R_{Sm} = 320\,\Omega$. The solid lines (blue) use a cooling model, with additional parameters: $\Sigma = 3.1 \times 10^8\,\text{W}\,\text{K}^{-6}\,\text{m}^{-3}$ and $\Omega = 1.41 \times 10^{17}\,\text{m}^3$.

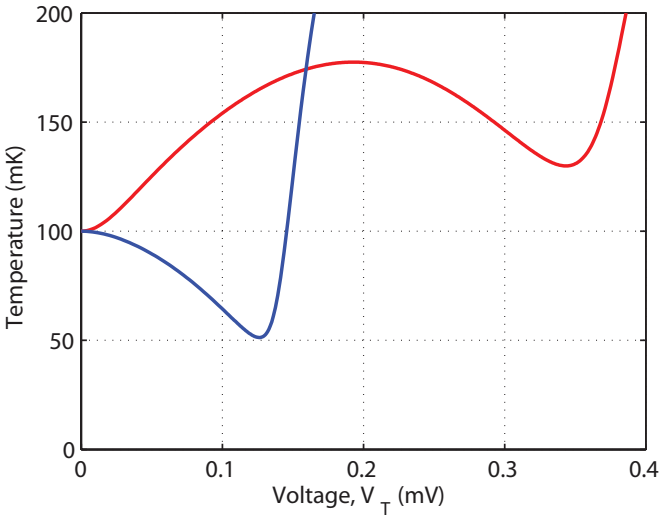


Figure 4.15: Temperature-Voltage calculations for a bath temperature of 100 mK. The blue line uses the cooling model and parameters of figure 4.14. The red line uses the same parameters except for a larger delta ($\Delta = 190$ meV).

to conventional N-I-S junctions [55]). Also, high series resistance spreads the voltage dependence and Joule heating enhances the Fermi smearing which reduces the sharpness. These factors (high sub-gap leakage and series resistance in the PtSi device) explain why the peaks are diminished in both the experimental data and the isotherm model.

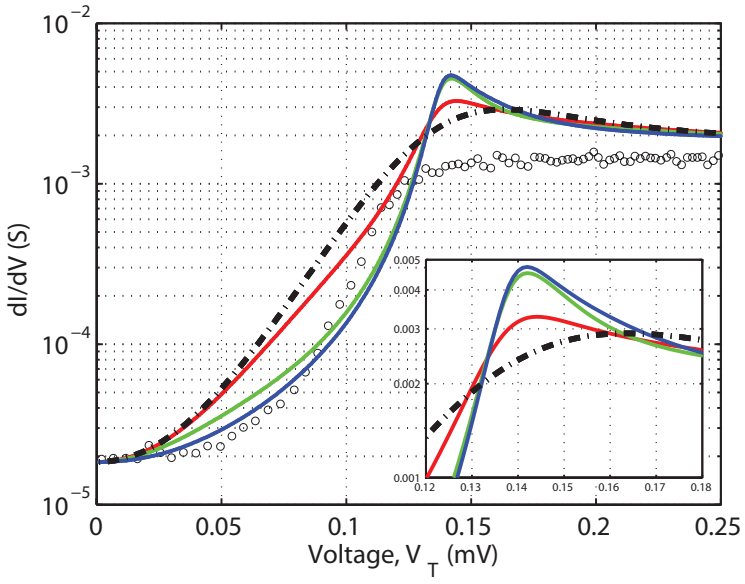
For the cooling model, it is suggested that the dI/dV peaks are enhanced by junction heating for biases beyond $2\Delta/e$, where a rise in temperature results in a greater current flow (according to equation 4.5, which in turn results in more heating, forming a feedback mechanism that strengthens the peaks in the differential conductance). In an attempt to better understand this, the differential can be expanded to

$$\frac{dI}{dV} = \frac{dT_e}{V} \times \frac{dI}{dT_e} \tag{4.12}$$

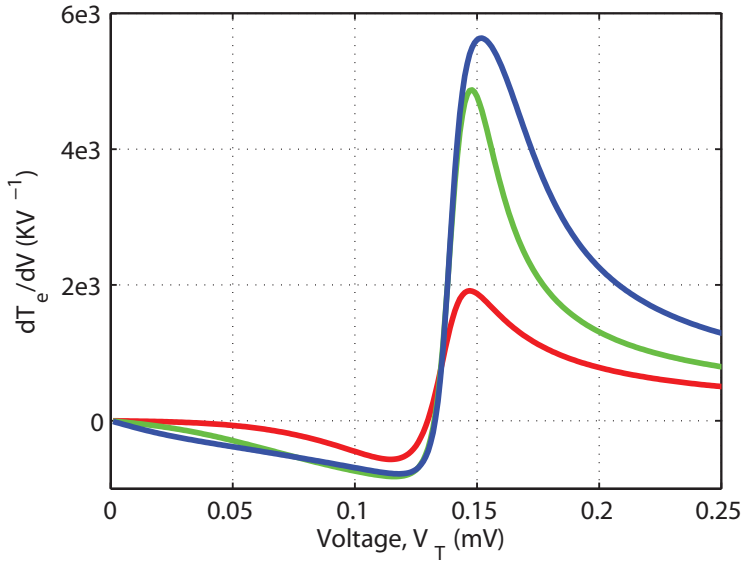
where the dT_e/dV term dominates in the region about the peaks in the density of states. The enhancement of the peak as the electron temperature is allowed to vary

is shown in figure 4.16a with figure 4.16b showing the calculated dT_e/dV. It can be seen that the differential conductance peaks correspond with the sharp temperature rise for biases beyond the cooling maximum. As the experimental data do not contain peaks in dI/dV, this implies that our model overestimates the temperature rise in this region.

Perhaps, in the measured device, the junction heating is not as strong as predicted by the cooling model, either because of damping due to heat dissipation in the device, or perhaps the density of states in PtSi is not as strongly peaked as predicted by the Dynes expression (equation 4.7), although the mid-gap density of states is consistent with the experimental results.



(a)



(b)

Figure 4.16: Simulations as the electron temperature is allowed to vary and the cooling power is increased from zero in the isothermal case (black dot-dashed) through 1% (red), 10% (green), to that calculated in the full cooling model (blue), showing (a) the enhancement of the peak in the differential conductance (The inset is a close-up of the peak region) and (b) the temperature change per volt.

4.3 Summary

In summary, PtSi is known to act as a superconductor, and because silicides have been widely used as contact materials in the semiconductor industry (due to their reliability and good electrical characteristics) it seemed natural to try PtSi for electron cooling in silicon. The first PtSi-Si-PtSi electron cooling device has been fabricated and and it has been shown that when PtSi is used as a thin layer (10 nm), its T_C is suppressed (and superconducting gap 2Δ is also reduced) which is beneficial for cooling at low bath temperatures. As there is a significant sub-gap leakage current in the device, the tunneling of low energy electrons could reduce the cooling power. By suppressing the gap, it is possible to reduce the sub-gap leakage current, and this aids in providing an effective cooling power. A calculation of cooling using the parameters from the fit to the experimental data, except for a larger Δ demonstrates that sub-gap leakage prevents cooling in that case; this highlights the advantage of the thin layer with low Δ in this sample.

Experimental data are compared to a cooling model (with varying electron temperature as predicted by an energy balance equation) and an isotherm (with constant electron temperature). The experimental data are best described by the cooling model, particularly for biases $V_C < 0.1$ mV, where most of the cooling occurs. The fit provides good evidence for electron cooling from 100 mK to 50 mK. Slight discrepancies between the model and the data are more marked at higher biases. The abrupt transition from sub-gap to normal state resistance deviates from the cooling model, so may be a characteristic of the material or device geometry.

5

Hole-Phonon coupling

In the low temperature (sub 1 K) regime, charge carriers are heated only weakly by the crystal lattice due to the strong temperature dependence of the carrier-phonon coupling (see section 1.4.5). However, phonon heating of charger carriers is still a major factor in the heat balance for electron cooling applications [9, 103] and is also responsible for the phonon noise equivalent power (NEP) [104]. NEP ($\mathrm{W\,Hz^{-\frac{1}{2}}}$) is defined as the incident signal power required to obtain a signal to noise ratio of one in a one Hz bandwidth (i.e. half a second of integration time) and is an important parameter for the measurement of electromagnetic ration in astronomical detectors [9]. A lower noise equivalent power implies a greater sensitivity and therefore NEP is often cited as a figure of merit. Previous studies in this field have illustrated the dependence of the electron-phonon coupling on mechanical strain (see [63] and section 1.4.5.1). In this chapter I have sought to illustrate the effect of carrier type on the carrier-phonon coupling and investigate both hole and electron devices. To the best of my knowledge this work presented the first direct analysis of the hole-phonon coupling constant in bulk silicon via tunnel junction thermometry.

The hole sample consisted of a 30 nm silicon layer with a boron doping concentration of $4 \times 10^{19}\,\mathrm{cm^{-3}}$ grown by reduced pressure chemical vapour deposition (RP-CVD). Replacing the dopant with phosphorus, an otherwise identical sample was grown to serve as our electron control. Aside from the change in dopant type

the two samples underwent the same fabrication process in order to allow for a direct comparison between the two. The samples were fabricated using the standard Sm-S lithography process depicted in figure (2.1). The exact device geometry is shown in figure (5.1). The mesa consists of a raised rectangular pillar 100 nm tall with dimensions of 205 µm by 5 µm. Aluminium contacts were then placed to form contacts at both the ends and the middle of the semiconductor bar.

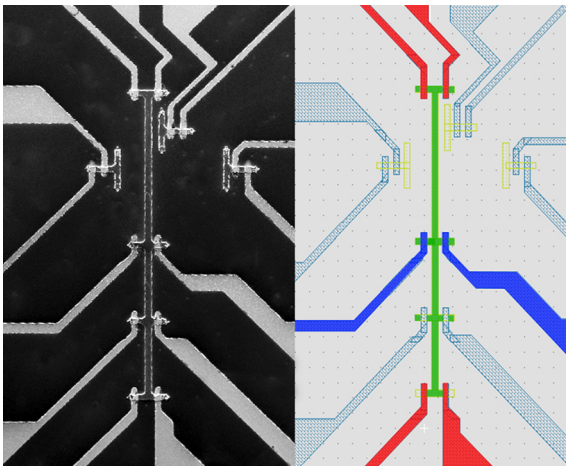


Figure 5.1: (left) An SEM micrograph of a carrier-phonon test structure. (right) The original device schematic. Aluminium leads for the heating of the bar are shown in red whilst the thermometer leads are coloured blue. Each individual junction has an area of 16 μm^2. The central green area is the highlighted mesa bar structure.

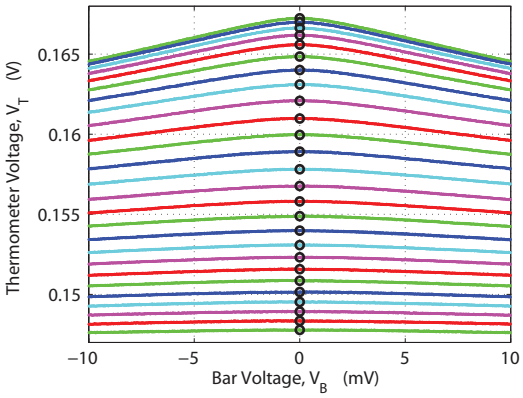
The parameters of the two samples investigated in this experiment are presented in table (5.1).

Table 5.1: Sample parameters from Hall measurements made at 10 K

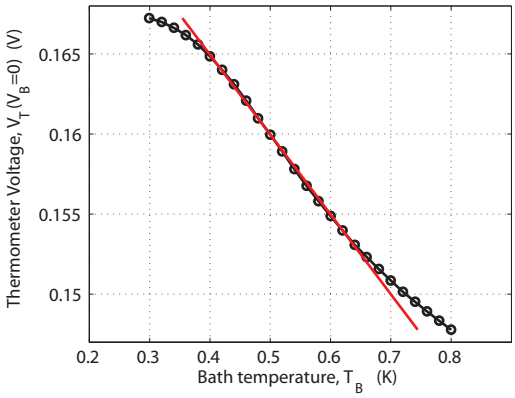
Sample	Mobility $(\mathrm{cm^2\,V^{-1}\,s^{-1}})$	Carrier Density $(10^{19}\,\mathrm{cm^{-3}})$	Sheet resistance $(\Omega/\square)$
Hole	68	4.3	354
Electron (control)	192	3.1	350

The measurement of carrier-phonon coupling was carried out using the method described in section 3.4.2. The carrier temperature was recorded as a function of the applied heating power, calculated from the voltage through the semiconductor bar and the measured bar resistance R_{bar} according to $P = V^2/R_{bar}$. This method

was repeated over a range of bath temperatures T_b from 300 mK to 700 mK. As mentioned in section 3.3, the principle error in this measurement stems from the calibration of the electron thermometers, which for this experiment is found to be approximately 2%.



(a) Voltage sweeps across the p-doped silicon bar versus measured thermometer voltage. Each coloured set of data represents a complete voltage sweep at a particular bath temperature. The bath temperature was varied between 300 mK and 700 mK in 700 mK steps.



(b) Hole sample thermometer voltage against bath bath temperature with the bar voltage at zero (thus no heating). The red marks the extrapolation of the temperature/voltage calibration over the regions of thermometer saturation (see section 1.5.2).

Figure 5.2: The $V_B = 0$ points in the data (black circles) are used to calibrate thermometer voltage against temperature.

5.1 Extracted coupling and the observed power law

We know from section 1.4.5 that the heat flow between the carrier gas and the lattice can generally be modelled by the equation

$$P \propto (T_e^\alpha - T_b^\alpha) \tag{5.1}$$

where α depends on the characteristic scattering mechanisms in the material under test. The carrier-phonon thermal conductance is thus given by

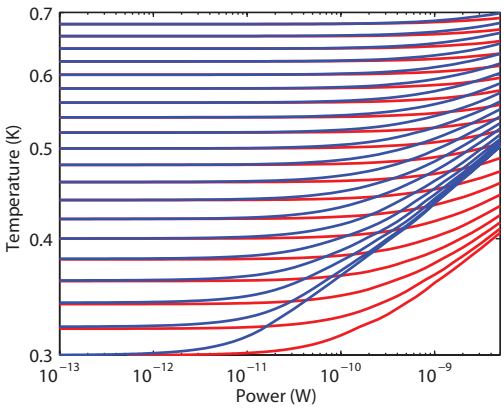
$$G = \frac{\partial P}{\partial T_e} \propto T_e^{\alpha-1} \tag{5.2}$$

Zieve et al. [105] describe situations in which carrier diffusion at the ends of a sample can lower the average carrier temperature, artificially suppressing the temperature exponent extracted from coupling measurements. In such cases, it is necessary to add a second term to equation (5.1) in order to extract the corrected value of α,

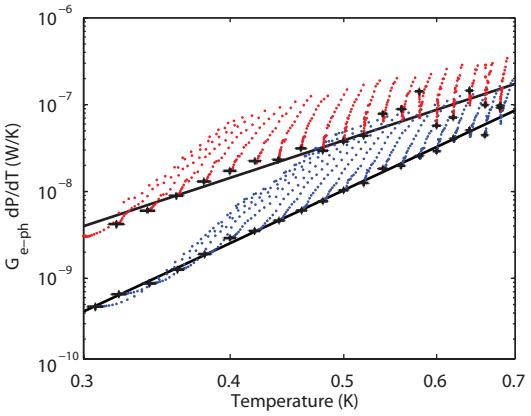
$$P = A\left(T_e^{\alpha} - T_b^{\alpha}\right) + B\left(T_e^2 - T_b^2\right) \tag{5.3}$$

where the T^2 term describes the power flow as a result of diffusive effects. B is given by $B = 4\mathcal{L}/R_S L^2 n$, with $\mathcal{L}$ being the Lorenz constant $\frac{1}{3}\left(\pi k_B/e\right)^2 = 2 \times 10^{-8}\,\mathrm{W\,\Omega\,K^{-2}}$, R_S the sheet resistance, L the length of the sample and n the electron density. A calculation of the diffusion heat-loss for our sample at the lowest bath temperature (300 mK), with an electron temperature of $T_e = 320\,\mathrm{mK}$, yields a value of $\sim 5 \times 10^{-17}\,\mathrm{W}$, more than six orders of magnitude smaller than the power we observe ($\sim 1 \times 10^{-10}\,\mathrm{W}$). It is therefore unlikely to have a significant effect and, for this reason, we are confident that any measurements of conductance we make are as a result of carrier-phonon coupling only. We therefore calculate G using only equation(5.1).

The main findings of this experiment are presented in figure 5.3. Figure 5.3a illustrates how the carrier temperature changes with the injected heating power. As the applied heating power increases, the hole temperature rises much less rapidly than the electron temperature which indicates that holes are more strongly coupled to the lattice phonons. From this data one can extract the carrier-phonon thermal conductance and the exponent of its temperature dependence, which is plotted in figure 5.3b, as well as the parameter Σ mentioned in equation (1.16).



(a) Measured hole (red) and electron (blue) temperatures as a function of heating power for a range of bath temperatures between 300 mK and 680 mK in 20 mK steps. The power through the bar is calculated from the the bar voltage data presented in figure 5.2b



(b) The hole-phonon (red) and electron-phonon (blue) conductance derived from the power temperature curves shown in figure 5.3a. Data markers trace out the lowest power points and include calculated error bars. The black lines are fits to the low power data and indicate the exponent of the power law. They give a power law of $P \propto T^{5.3\pm0.3}$ and $P \propto T^{7.3\pm0.3}$ for holes and electrons respectively.

Figure 5.3: Hole and electron coupling data.

The thermal conductance is then extracted according to equation 5.2. From figure 5.3b we can see that at the lower limit of the temperature range the carrier-phonon conductances differ by a full order of magnitude. This difference reduces to a factor of two at 0.6 K. Furthermore, it can be seen that the electron-phonon conductance varies as T^7, with the exponent being indicated by the gradient of the $\log(G)\log(T)$ data, whilst the hole conductance varies to a lesser degree, demonstrating a T^5 relationship. Propagating the experimental errors in the measurements of injected power and electron temperature and including these in the algorithm used to fit the data, we are left with an uncertainty of ±0.03 on each exponent.

It is assumed that the electronic temperature can increase independently of the phonon temperature and that in effect the phonon and bath temperature are assumed constant and equal in the range of powers applied, in line with previous

experiments of this nature [63]. This assumption is expected to become less valid for higher injected powers, indeed more so in the case of p-type material where the apparent stronger coupling between carriers and phonons will facilitate heat transfer between the two. It is for this reason that we draw our conclusions principally from the lowest power data, highlighted by black circles on the plot, for which the assumption is most valid.

5.2 Theoretical considerations

The theory behind carrier-phonon coupling has been a topic of intense study. Sergeev et al. [62] presented one of the first descriptions of the mechanisms underpinning carrier-phonon relaxation rates in semiconductors, which was later generalized [61]. From these two papers it is possible to predict the exponent of the carrier-phonon coupling temperature dependence in certain limiting cases and compare it with that extracted from the hole and electron data.

The first step is therefore to identify which of these limits the hole sample occupies. The carrier-phonon interaction is governed by both carrier-phonon scattering and inelastic electron scattering as a result of impurities and material defects. If the thermal phonon wavevector q_T is shorter than the electron mean free path l_e, one would expect the dominant scattering to be from phonons. This is known as the pure limit, in which ($q_T l_e >> 1$) [15]. In the opposite case, known as the impure limit ($q_T l_e << 1$) the phonon wavevector will exceed the electron mean free path and electrons will scatter mostly from impurities and defects.

In SI units the thermal phonon wavevector is given by [106]

$$q_T = \frac{k_B T}{\hbar v_s} \approx 1 \times 10^7 \,\mathrm{m}^{-1} \tag{5.4}$$

with $v_s = 5000\,\mathrm{m\,s}^{-1}$ being the velocity of sound in silicon [58].

The electron mean free path can be calculated from the product of the Fermi

velocity $v_f = \sqrt{\frac{2E_F}{m_0}}$ and the relaxation time (or the average time between scattering events) $\tau = \frac{\mu m_0}{e}$ [15] with

$$l_e = v_f \tau. \tag{5.5}$$

The mobility μ of our sample is known, and the Fermi energy $E_F \approx 60\,\text{meV}$ can be calculated by plugging the measured carrier density n into the free electron model [15, 107]. The effective electron mass is given by $m_0 = 0.25 \cdot m_e$ [108] where m_e is the well known electron rest mass. Therefore $l_e \approx 3\,\text{nm}$ and $q_T l_e \approx 0.03$ putting the hole sample firmly within the impure limit as ($q_T l_e >> 1$).

As discussed in section 1.4.5, interactions between electron and phonons can be weakly or strongly screened. The transition from weak to strong screening occurs at the limit $\kappa << q_T$ [15] with κ being the inverse screening length [109], where 'screening length' is defined as the distance beyond which local changes in electric field (caused by phonons) are damped by a shell of mobile charge carriers.

κ is given by the equation [109]

$$\kappa = \sqrt{4\pi e^2 \left(\frac{2}{3}\frac{n}{E_F}\right)} \approx 3 \times 10^9\,\text{m}^{-1}, \tag{5.6}$$

which confirms strong screening of the hole-phonon interaction [62]. According to Sergeev's theory, we should therefore expect the hole-phonon coupling to exhibit a T^8 dependence, rather than the T^5 relationship demonstrated by our data.

It has been suggested [110, 61] that the disagreement between the theoretical and observed power laws may originate from Sergeev's use of the single-valley model, which would neglect any inter-valley scattering between light and heavy holes etc., which is not subject to screening effects [61], further complicating the temperature dependence of carrier-phonon interactions. With these interaction mechanisms pro-

viding an additional conduction channel between the holes and phonons, one could expect a stronger coupling and a consequently lower variation in hole temperature with injected power [61]. Furthermore, whilst I have done my best to mitigate any effects of carrier diffusion at the ends of a sample (via an elongated sample geometry and by measuring carrier temperature at the centre of the mesa bar), it is still possible that the observed T dependence is affected by electron diffusion cooling. It should be noted, however, that any such influence would be expected to apply to both the hole and electron sample, allowing any comparative conclusion to remain valid.

5.3 Summary

In summary, I have shown that holes in Si are more strongly coupled to the phonons than the electrons, with holes requiring a greater power input before their temperature lifts above that of the bath. This result may be useful for phonon thermometry and in the application of Sm-S junctions to cooling of thermally isolated platforms. These results should stimulate theoretical work to include scattering between the heavy, light and spin-orbit split valleys.

This measurement can be collated with previous investigations made into the carrier-phonon coupling in heavy doped silicon [63], with the data collectively presented in figure 5.4.

The evident variation of the carrier-phonon behaviour with temperature, strain and dopant type demonstrates the necessity for further study of the underlying theory in order to understand and thus manipulate the carrier-phonon coupling in future generations of silicon devices. To this end, work is on-going to fit the experimental results presented in figure 5.4 using a theoretical framework that quantifies the effects of disorder in the samples on the carrier-phonon energy loss rate.

Further experimental work is planned to expand this study to the effect of

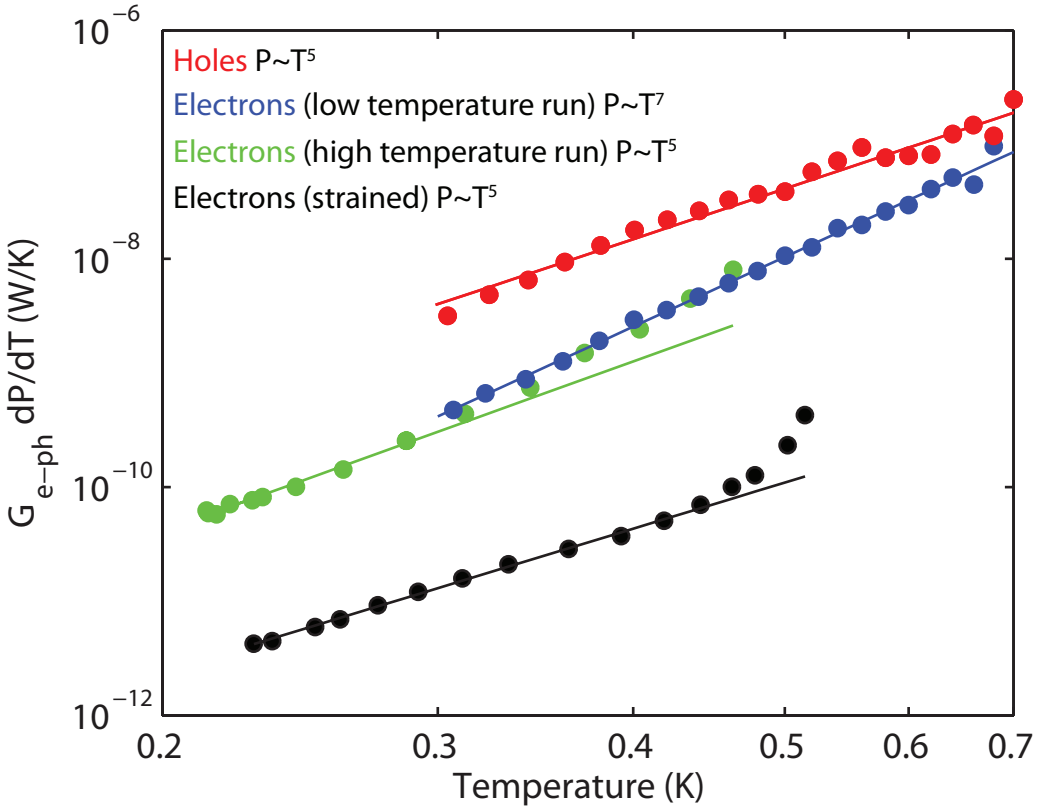


Figure 5.4: Carrier phonon conductance for a hole (red) and electron control (green) device. The two lower data sets are taken from measurements carried out in Helsinki of the same electron control device (blue) and the strained electron device (black). The open circles are the lowest power points of the measurement. The slope of the fitted line, indicating the exponent of the power law, is noted for each data set.

both strain and doping density on the hole-phonon coupling. Furthermore, it has been proposed that impurity (dopant) mass can be varied to alter the dominant scattering mechanism in the silicon structures, providing more data towards a comprehensive, quantitative analysis of the mechanisms behind carrier-phonon coupling [111].

6

Semiconductor-insulator-superconductor junctions

In preceding chapters it has been made clear that the tunnel resistance R_T and the sub-gap conductance (parameterised by Γ) are the two major factors limiting cooler performance.

In 2004, Connelly et al. [112, 113] demonstrated that the introduction of an oxide layer between a metal and a semiconductor could substantially reduce the Schottky barrier height of the tunnel junction, thus increasing its transitivity. It is suggested that this is accomplished by decreasing the Fermi-level pinning (section 1.4.1), a result of intrinsic, metal-induced gap states (MIGS), and removing defects associated with physical non-idealities of the interface such as dangling bonds [114]. These dangling bonds are simply trivalent silicon atoms with one unpaired valence electron and constitute a build up of negative charge that serves to deplete the interface and effectively increase the Schottky barrier.

It would therefore seem that the oxide layer is capable of pacifying these interfacial defects and prevents metal states from penetrating into the silicon band gap. If this same effect could be reproduced in a semiconductor-superconductor

junction, one may expect that the apparent interface state pacification would work to minimise Γ whilst the accompanying de-pinning would simultaneously reduce the tunnel resistance. The applications to Sm-S TJCs are therefore self-evident.

Simply adding an oxide betwixt the semiconducting and superconducting electrodes of a cooler junction is not particularly straight forward, however. As discussed in section 1.4.1, the resistance of a metal-semiconductor contact depends not just upon the height of the barrier, but also upon its width. It is therefore necessary to utilise an oxide layer that is both thick enough to block the formation of gap states and thin enough to allow free carries to tunnel through. To this end, the oxide layer should be of the order of a few monolayers $\sim 1\,\mathrm{nm}$ [113].

Silicon dioxide SiO_2 was chosen as the material for the insulating oxide layer. Readily available as a natural oxide of silicon, it could be incorporated into the established fabrication methodology with relatively little effort.

6.1 Oxidation studies and Sm-I-S junction characterisation

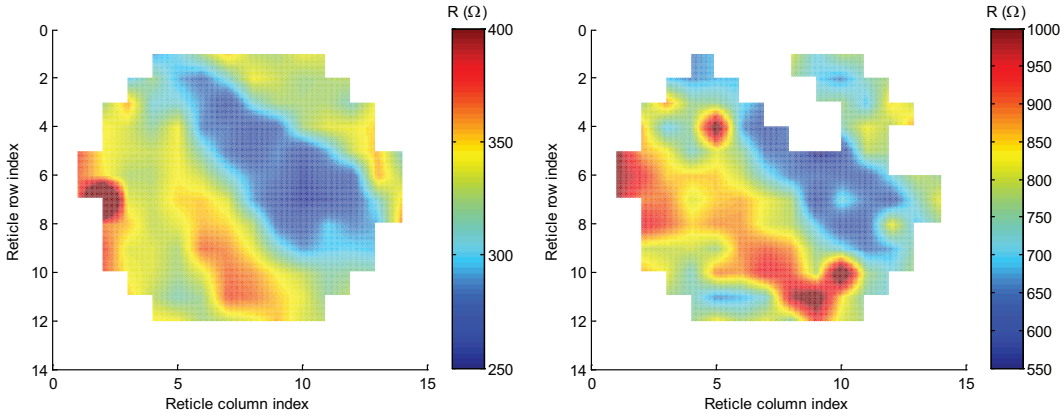
Whole wafers were processed with differing oxidation times in order to produce batches of characterisation and cooler structures with a range of oxide thicknesses. Aluminium is used for the superconducting electrode, it being readily available and easy to work with. The wafer preparation details are given in table 6.1 with the device fabrication process described in section 2.2 and figure 2.1. The samples were doped using ion implantation [85], with calibration samples implying the formation of an electrically active layer of thickness 150 nm.

The wafers were then electrically characterised by using the transfer length method (TLM, section 3.2.2) with supplementary measurements of contact resistance made on single junctions Sm-S junctions with an area of $1\,\mu\mathrm{m}^2$ or $4\,\mu\mathrm{m}^2$. Identical devices were tested across the wafer, with the results presented by device

Table 6.1: Wafer preparation details.

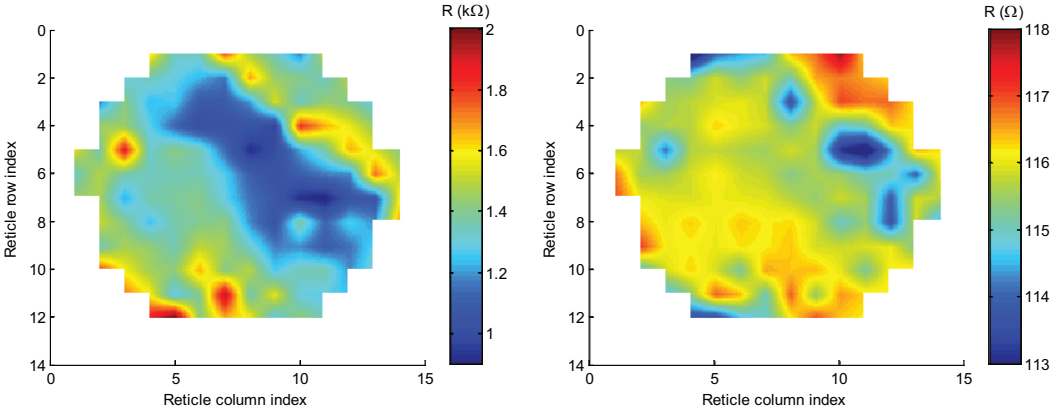
Wafer ID	HF-Dip (s)	Heat Treatment ($°C - s$)	Oxidation ($Torr - s - °C$)
W6 (control)	40	550 - 720	-
W7	40	550 - 720	1.4 - 600 - 550
W8	40	550 - 720	300 - 600 - 550
W9	40	550 - 720	760 - 300 - 700

grid reference in figures 6.1 to 6.8. Gaps in the wafer maps are a manifestation of absent data due to damaged devices. The anomalous discontinuous regions of colour are a result of an error in the fitting algorithm used to extract the contact and sheet resistances from the TLM data (section 3.2.2).



(a) 4 µm^2 single junction resistance. (b) 1 µm^2 single junction resistance.

Figure 6.1: W6 single junction resistance wafer map.

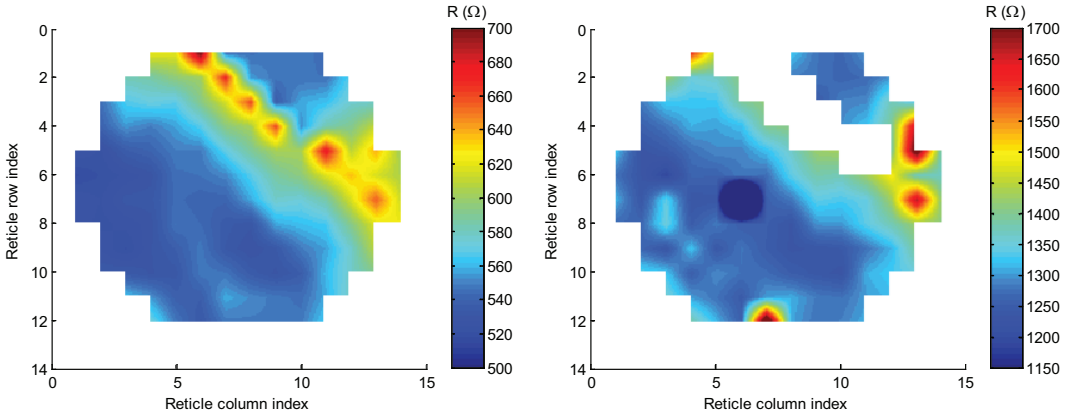


(a) TLM contact resistance. (b) TLM sheet resistance.

Figure 6.2: W6 TLM device wafer map.

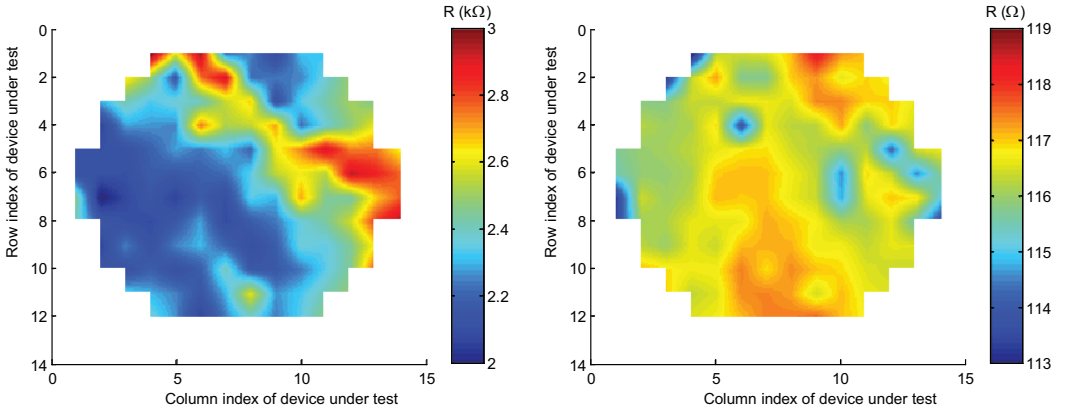
These wafer maps demonstrate that the oxide growth is uniform and that the whole-wafer Sm-I-S fabrication process is viable, with the characterisation parameters exhibiting a wafer-wide spread well below one order of magnitude, the acceptable standard for 4-inch wafer processing [115].

The measurements of contact resistance are summarised in figure 6.9. It is immediately apparent that sample W9 with the longest oxidation time (and therefore the thickest oxide layer) is too resistive for any practical applications, whilst samples W6, W7 and W8 show no significant differences. From this it is possible to conclude



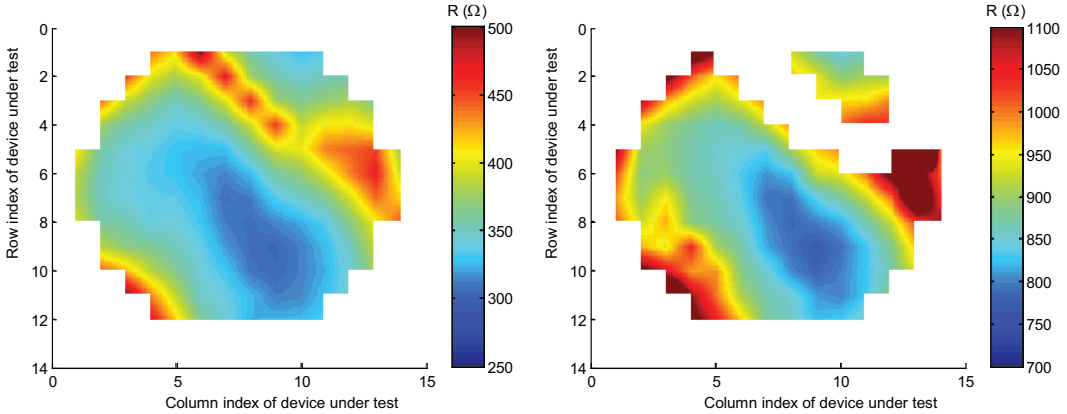
(a) 4 µm^2 single junction resistance. (b) 1 µm^2 single junction resistance.

Figure 6.3: W7 single junction resistance wafer map.



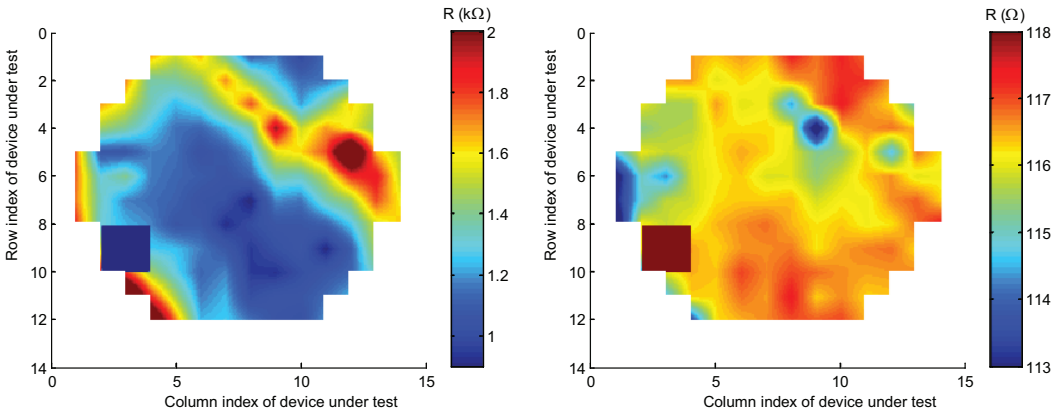
(a) TLM contact resistance. (b) TLM sheet resistance.

Figure 6.4: W7 TLM device wafer map.



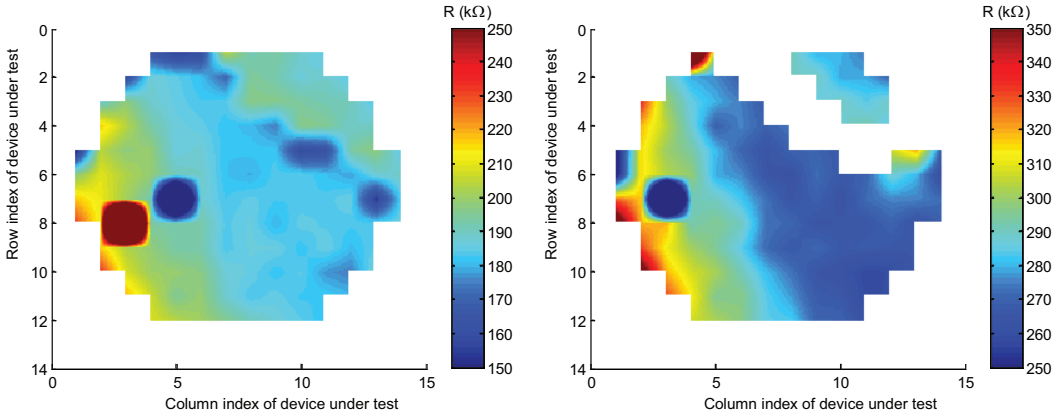
(a) 4 µm^2 single junction resistance. (b) 1 µm^2 single junction resistance.

Figure 6.5: W8 single junction resistance wafer map.



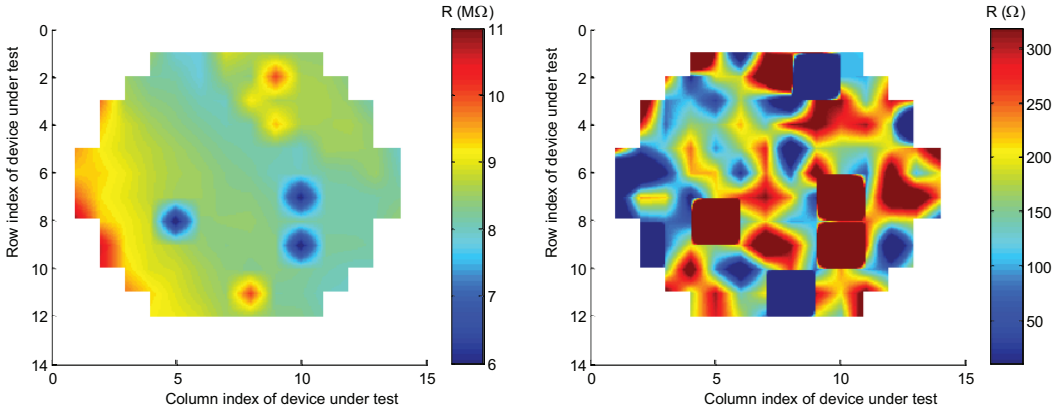
(a) TLM contact resistance. (b) TLM sheet resistance.

Figure 6.6: W8 TLM device wafer map.



(a) 4 µm^2 single junction resistance. (b) 1 µm^2 single junction resistance.

Figure 6.7: W9 single junction resistance wafer map.



(a) TLM contact resistance. (b) TLM sheet resistance.

Figure 6.8: W9 TLM device wafer map.

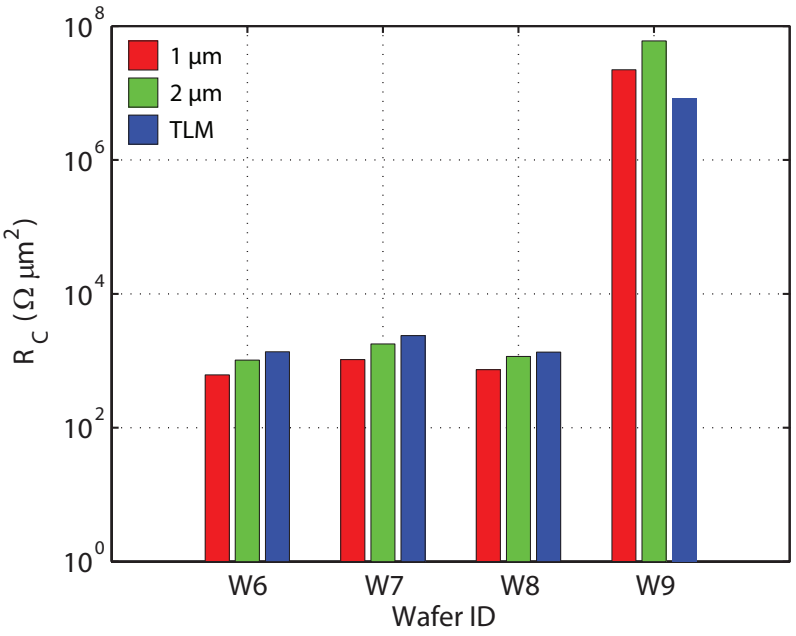


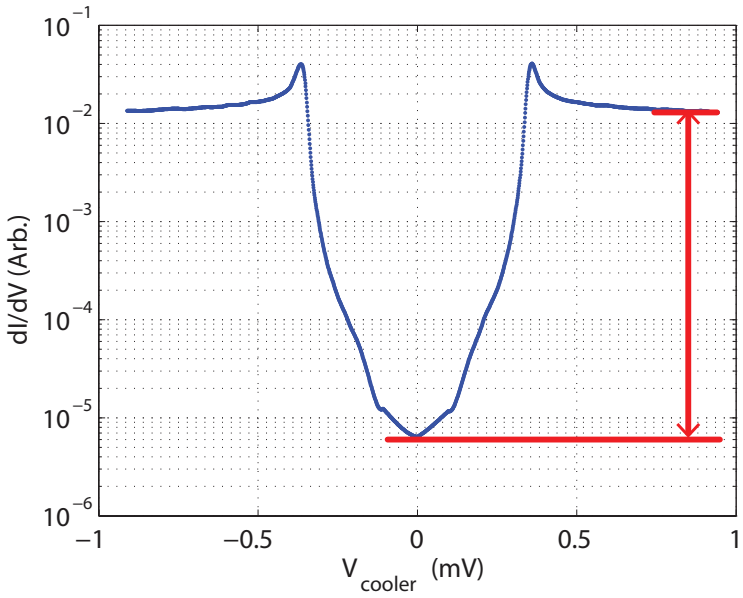
Figure 6.9: The wafer average contact resistance as measured for the three different characterisation structures.

that the oxide layer present in the latter two samples has 'paid for itself'. That is, the insulating layer has lowered the resistance enough to make up for any increase in resistance caused by the wider tunnel barrier, maintaining the contact resistance of the control sample.

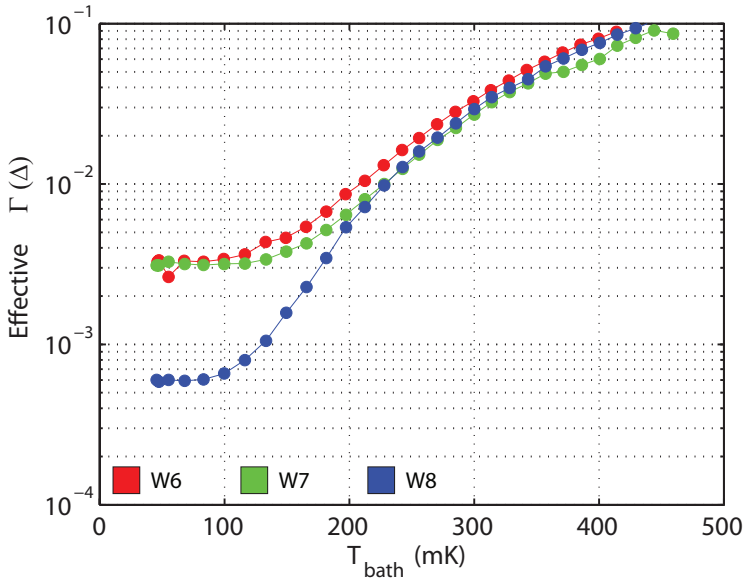
This reduction in resistance could well be a result solely of the Fermi level de-pinning and the subsequent lowering of the Schottky barrier, however there is a secondary mechanism to consider. The growth of the silicon dioxide layer consumes silicon from the phosphorus doped mesa layer. Due to the low solubility of phosphorous in oxide, the positively charged donor ions are pushed into the adjacent silicon, a process known as dopant segregation [116]. This so called 'snowplough' effect results in an increased positive surface charge density, which will counter the negative depletion charge originating from the interfacial defects and reduce the Schottky barrier further.

6.1.1 Junction quality

Figure 6.10b displays measured Γ/Δ for typical junction devices on each wafer across a range of temperatures. Whilst W7 is clearly no better than the control, wafer W8 shows a marked improvement with an intrinsic (temperature independent, base value) Γ almost an order of magnitude smaller at $\Gamma = (6 \pm 0.5) \times 10^{-4}\Delta$. We can therefore conclude that the oxide layer in W7 is thin enough to remain suitably transparent to free carriers but not quite thick enough to block states from seeding in the superconducting band gap. The W9 oxide, on the other hand, would arguably have resulted in clean interface, albeit a highly resistive one. It seems therefore that the thickness of the oxide layer in W8, measured at 1.8 nm$\pm$0 1nm, is just right. W8 may therefore be considered to be a Goldilocks type sample.



(a) Differential conductance of an Sm-I-S junction at 100 mK with the ratio of plateau (normal state) and valley (sub-gap) height from which the value of $\Gamma = (6 \pm 0.5) \times 10^{-4} \Delta$ is extracted.



(b) The measured Γ/Δ (given by ratio of the normal state and sub-gap resistances) for 4 µm by 5 µm test Sm-I-S junction on W6, W7 and W8 for range of bath temperatures.

Figure 6.10: The fit generated by the thermal model shows excellent agreement with the experimental data.

6.1.2 Sm-I-S Tunnel junction cooling

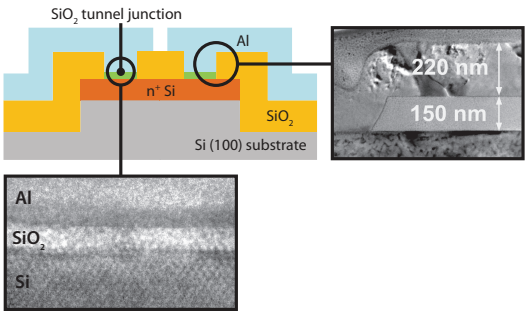
With a Γ value of $(6 \pm 0.5) \times 10^{-4}\Delta$, the lowest value so far demonstrated in any semiconductor-superconductor TJC (a single order of magnitude larger than that of a typical metal-superconductor junction [55]), a run was carried out on the cooler structures on sample W8 to see by how much, if at all, the cooler performance had improved with the quality of the junction. A schematic of the cooler device cross-section, the experimental set up are shown in figure 6.11

The cooler devices tested incorporated two S-I-Sm-I-S junctions operating in parallel, cooling a silicon mesa with a volume of approximately $10\,\mu\text{m} \times 25\,\mu\text{m} \times 150\,\text{nm} = 37.5\,\mu\text{m}^3$. The results of a full electrical characterisation of the W8 cooler are listed in table 6.2.

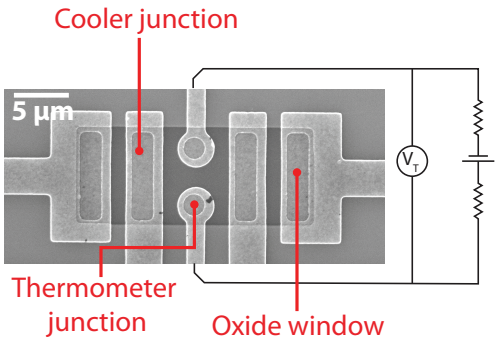
Table 6.2: Sample parameters. Resistances measured at 40 mK. Carrier density and mobility from Hall measurements at 10 mK.

Junction resistance $R_T\,(\text{k}\Omega\,\mu\text{m}^2)$	1.1
Si sheet resistance $(\Omega/\square)$	11
Carrier density $(10^{19}\,\text{cm}^{-3})$	3.4
Mobility $(\text{cm}^2\,\text{V}^{-2}\,\text{s}^{-1})$	200

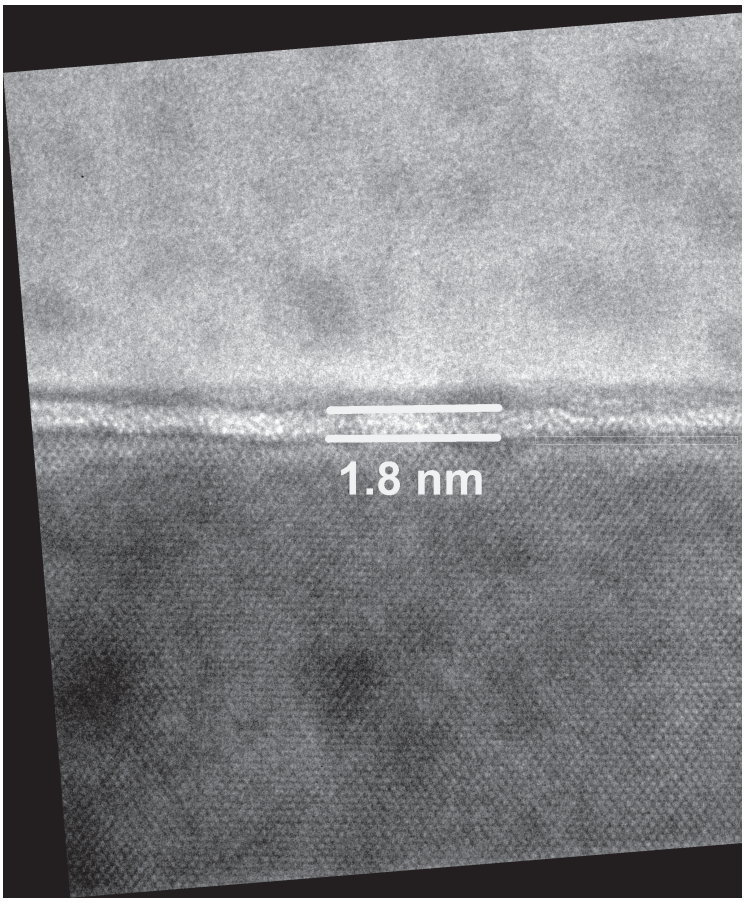
The procedure for the cooling experiment is outlined in section 3.3. And the measured current-voltage and voltage-temperature behaviors are shown in figures 6.12a and 6.12b. The measurements were performed in a ^{3}He/^{4}He dilution refrigerator within a liquid ^{4}He bath and the main results of the cooling experiment are presented in figure 6.14.



(a) A schematic cross section of the device depicting the utilisation of oxide windows for targeted oxide growth. Also included are high resolution FIBSEM enabled TEM images showing the interfacial oxide layer.



(b) An SEM micrograph of the cooler junctions.



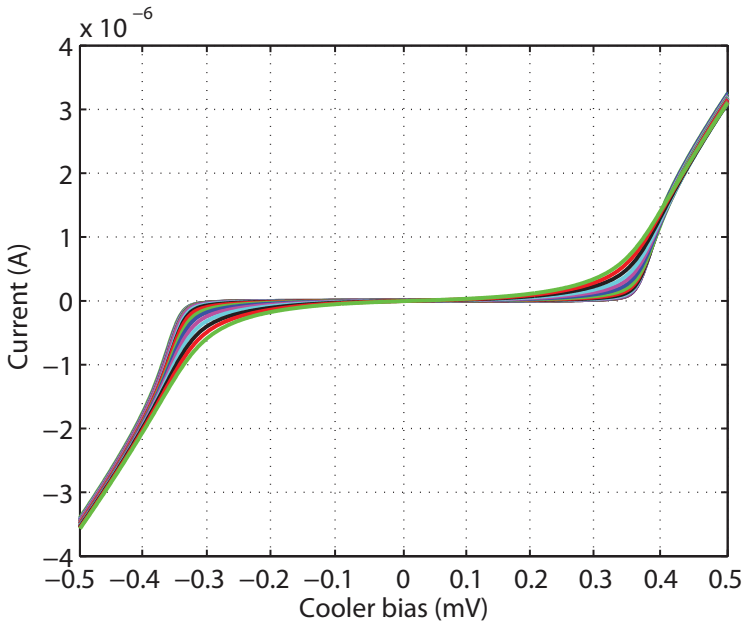
(c) A larger print of a high resolution TEM image of the Sm-I-S interface, from which the oxide thickness was determined.

Figure 6.11: The device layout. The single cooler junction area was $2 \times 9\mu m^2$ and the thermometer junctions have a diameter of 1 µm. The cooled volume is given by the dimensions of the electrically active layer of the mesa, being 10 µm × 25 µm × 150 nm = 37.5 µm^3.

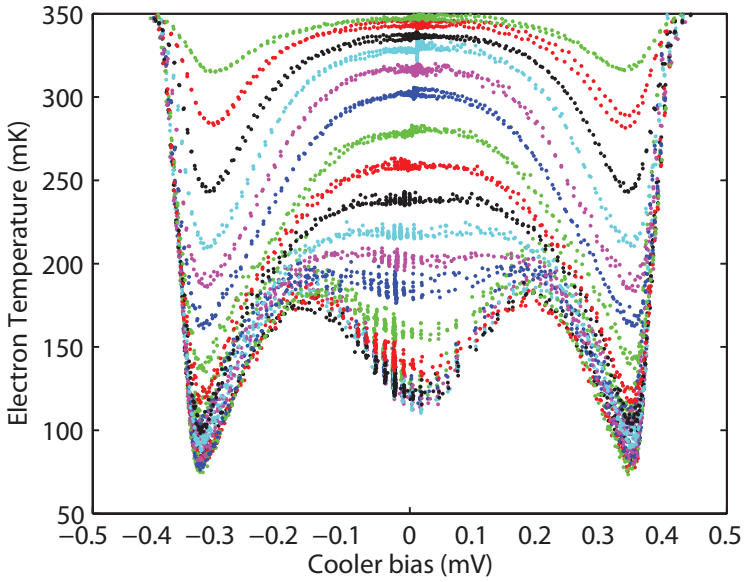
Figure 6.13 shows the electron thermometer present on the sample saturates comfortably below the minimum electron temperature measured during the cooling run from 300 mK. This principle result is therefore considered to be both reliable and accurate, with the electron being cooled to a temperature of 160 mK. To reiterate a point made in the introduction, 300 mK is considered a technologically significant bath temperature to start from, given that it is relatively easy to reach using a conventional ^{3}He adsorption fridge.

The major results of the cooling experiment are presented in figure 6.14. The sample demonstrates cooling from a bath temperature of 300 mK to 160 mK which represents a significant improvement in performance over the previous best result from an unstrained Sm-S device which cooled to only 258 mK from the same bath temperature [56]. Furthermore, from a starting temperature of 200 mK, the oxide cooler is able to reach a stable minimum electron temperature of ~ 100 mK, which at the time of this result was the closest a semiconductor-based cooler device had come to breaching the sub 100 mK regime dominated by the well established N-I-S junctions.

Taking the minimum electron temperature T_{min} from each cooler sweep and plotting the ratio T_{min}/T_b against T_b allows one to view cooling performance over the entire range of starting temperatures.



(a) Cooler IV exhibiting the characteristic diode-line temperature dependence of an N-I-S/Sm-S junction.



(b) Extracted voltage temperature data of the cooled semiconductor volume.

Figure 6.12: Characteristic IV and VT plots for the semiconductor-insulator-superconductor junction cooler junction on wafer W8. Each coloured set of data represents a complete voltage sweep at a particular bath temperature. The bath temperature was varied between 120 mK and 400 mK in 20 mK steps.

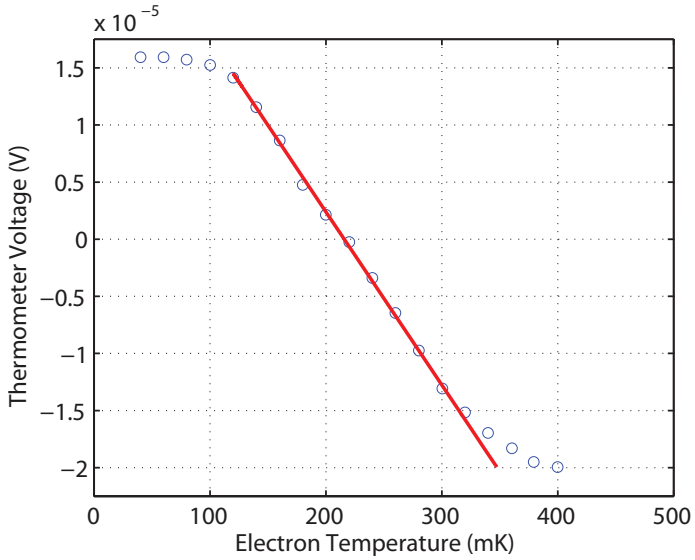


Figure 6.13: Empirical calibration of thermometer junction voltage against electron temperature at zero cooler bias. The red line shows the calibration extrapolated from the linear region of the thermometer data.

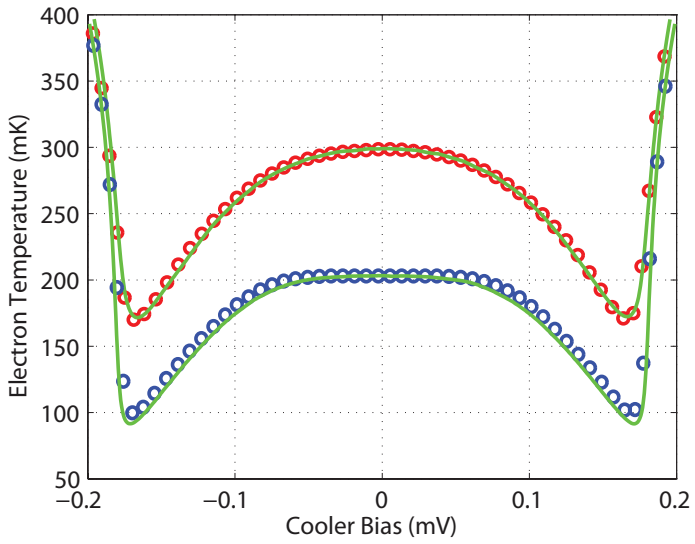


Figure 6.14: Electron temperature T_e against cooler bias V_C. The red and blue markers are experimental data showing cooling from 300 mK and 200 mK respectively. The green curves are fits generated by the cooling model. Both fit lines are generated from the same set of parameters, given in table 6.3.

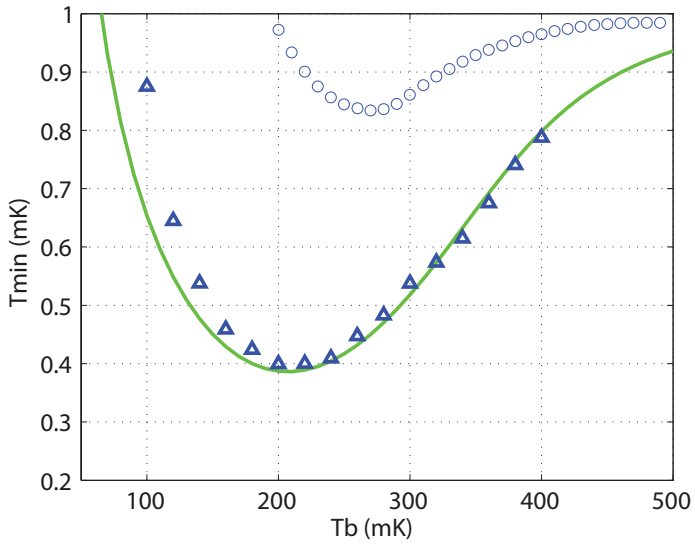


Figure 6.15: T_{min}/T_b versus T_b showing cooler performance of the strained silicon Sm-I-S cooler (triangles) over a range of temperatures. The results from a previous generation of Sm-S cooler (circles) from [56] are included for comparison. The solid green lines represent the minimum temperature predicted by the cooling model for each of the two samples.

A series of cooling and heating power equations were used to model the experimental data [52, 46], each fully described in section 1.4.7. The resulting power balance equation can be written as

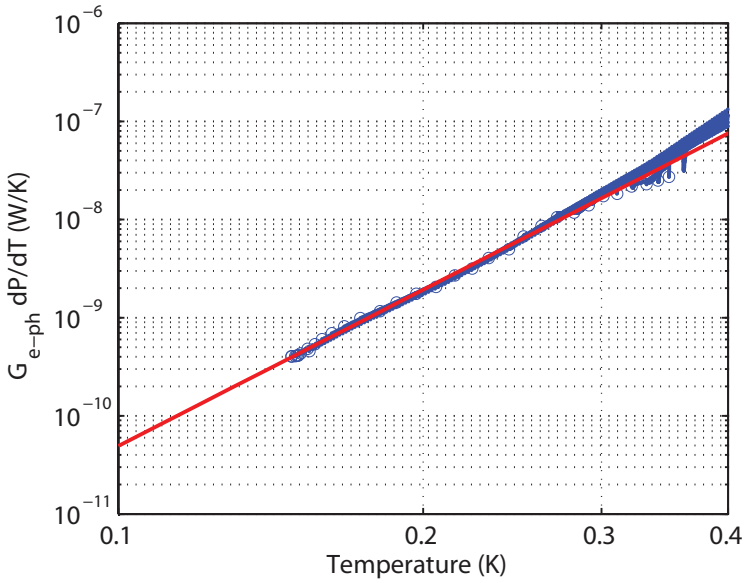
$$P_C\left(V_C, T_e\right) + P_{e-ph}\left(T_e\right) + P_J\left(V_C, T_e\right) + P_{QP}\left(V_C, T_e\right) = 0, \tag{6.1}$$

which is solved for the electron temperature at a given voltage.

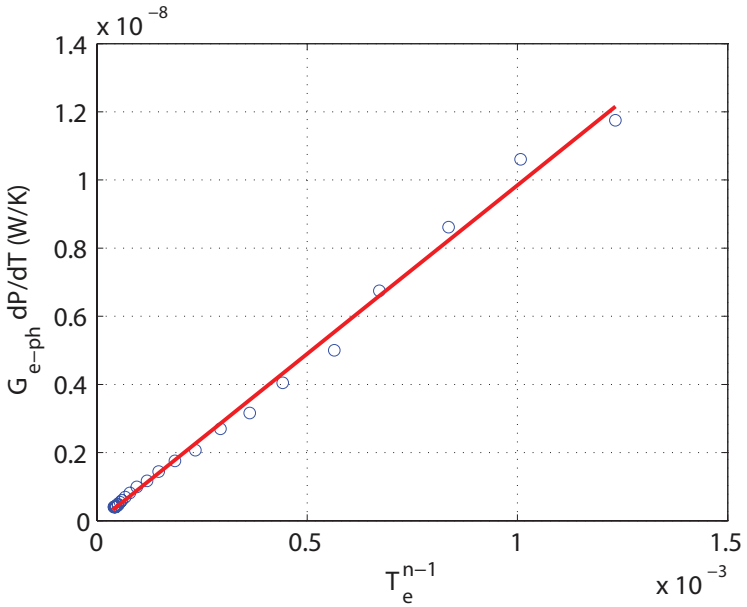
In previous work [56], the electron-phonon coupling term P_{e-ph} would be calculated from the known volume Ω and the coupling constant of the material being cooled Σ, as in section 1.4.5. However, in this work an attempt was made to measure this term experimentally, with the hope of improving the agreement between the cooling data and the thermal model.

To this end, an electron-phonon coupling measurement was carried out on the W8 sample using the method detailed in sections 3.4 and 5 and described in reference [63]. A resistive bar structure with a volume of $3420\,\mu m^2$ was heated,

generating a data set of conductance G versus electron temperature T_e. A number of methods may then be employed to extract the electron-phonon coupling power.



(a) A linear fit to the experimental electron-phonon conductance data. The $log(G)$ $log(T_e)$ data has a y-intercept of $log(n\Sigma\Omega)$



(b) Plotting G against T_e^{n-1}, the data follows a straight line with gradient $n\Sigma\Omega$.

Figure 6.16: Electron-phonon conductance of the W8 wafer.

Remembering that

$$G = \frac{dP}{dT} = n\Sigma\Omega T_e^{n-1}, \tag{6.2}$$

and

$$\log(G) = (n-1)\log(T_e) + \log(n\Sigma\Omega), \tag{6.3}$$

plotting $\log(G)$ against $\log(T_e)$ yields a straight line with a gradient of $n-1$ (see figure 6.16). Using this value of $n-1$ and plotting G versus T_e^{n-1} produces a straight line with a gradient of $n\Sigma\Omega$. One can then simply divide by n and correct for the disparity between the volumes of the coupling and cooling devices to be left with a value of $\Sigma\Omega$ that can in turn be fed into equation 1.16.

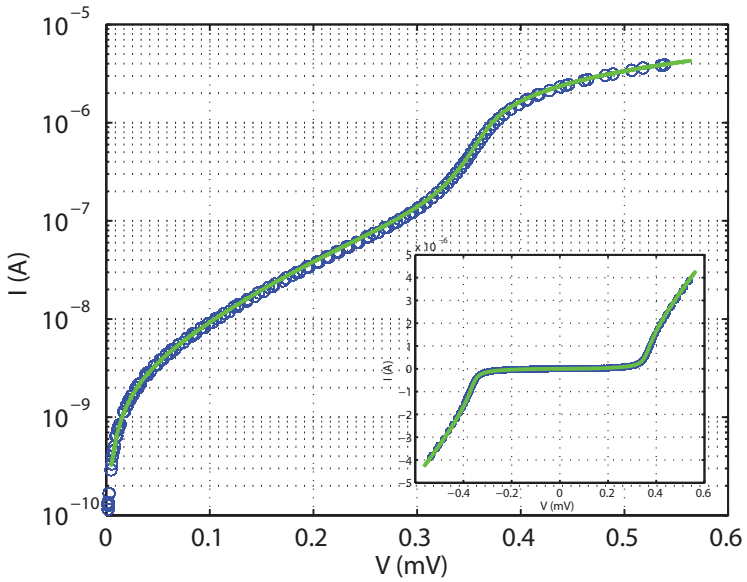
An alternative, but similar method would be to calculate Σ from the intercept of the same logarithmic plot, though this method is subject to the extrapolated point of intercept and is thus susceptible to a potentially large error.

One final method, that which I have employed, is to calculate P_{e-ph} directly from the coupling data, bypassing entirely the need for an exact value of Σ. Integrating the measured conductance G between the limits of T_b and T_e

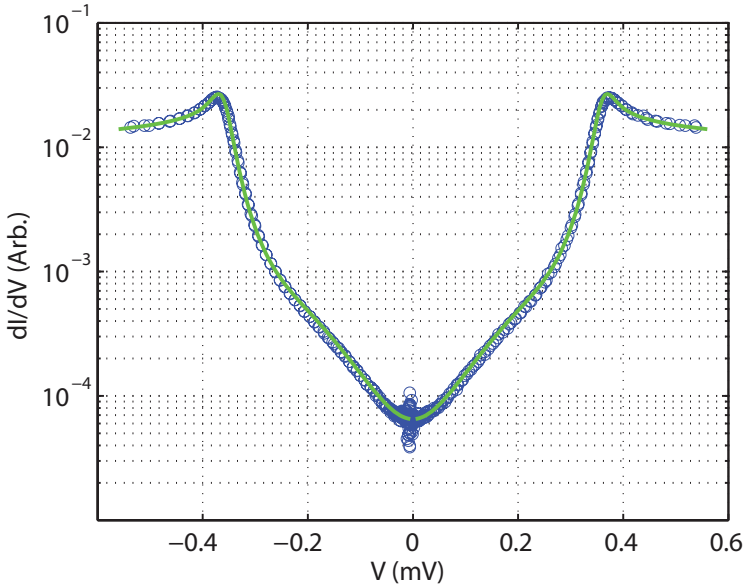
$$P_{e-ph} = n\Sigma\Omega \int_{T_b}^{T_e} T^{n-1} = \int_{T_b}^{T_e} G = n\Sigma\Omega \left[\frac{T_e^n}{n} - \frac{T_b^n}{n}\right] = \Sigma\Omega\left(T_e^n - T_b^n\right) \tag{6.4}$$

provides an exact value of P_{e-ph} for each electron temperature, which can then be used in the power balance equation (equation 6.1). This is quite beneficial, as given the nature of dopant implantation, it is difficult to define the exact volume of the W8 cooling and coupling devices. Secondly, by removing Σ from the thermal model I have removed a variable parameter which in the past has been used as an additional fitting factor [56].

As evidence to the efficacy of this method, figure 6.17 demonstrates the excellent fits to the IV and differential conductance behaviour of the W8 cooler.



(a) A fit to the experimental IV of the W8 cooler device.



(b) A fit to the differential conductance of a single W8 cooler junction.

Figure 6.17: The fit generated by the thermal model shows excellent agreement with the experimental data at 300 mK.

The thermal model was fitted to the experimental cooling data using the parameters listed in Table 6.3. In figure 6.14, the simulation shows good agreement with both the 300 mK and 200 mK data. Furthermore, figure 6.15 demonstrates that the fit is satisfactory across the range of bath temperatures used in this experiment.

Table 6.3: Model parameters. R_{Sm} is calculated from the measured sheet resistance through five squares in parallel between the cooler contacts. Γ is calculated from the measured zero bias conductance of the junction at base temperature, divided by the asymptotic conductance.

R_T (Ω)	R_{Sm} (Ω)	Δ (meV)	Γ $\left(\Delta^{-1}\right)$	β
76	29	0.19	0.0008	0.08

6.2 Summary

In summary, it has been demonstrated that Sm-S junctions can benefit from an oxide layer in the tunnel junction, and that such a layer pacifies the high sub-gap leakage typical of highly doped devices first noticed by Savin et al. [40]. The semiconductor-insulator-superconductor junction demonstrates the lowest sub-gap conductance, to date, of a semiconductor/superconductor cooling tunnel junction, and this has been linked this to a dramatic increase in cooler performance.

7

Strained semiconductor-insulator-superconductor junctions

In chapter 6 I discussed the newly developed methods for the fabrication of semiconductor-insulator-superconductor (Sm-I-S) devices and the subsequent production of extremely high quality tunnel junctions, exhibiting very low leakage currents. This was accompanied by an increase in the performance of Sm-I-S cooling tunnel junctions with a demonstration of direct electron cooling from a bath temperature of 300 mK to 160 mK.

It has previously been shown that tensile strain significantly reduces the electron-phonon coupling in silicon [63] and furthermore, that this allows lower minimum electron temperatures to be attained by a given cooling junction [56]. Following on from this work, I present the first strained Sm-I-S cooling tunnel junction with the intention of combining the reduced electron-phonon coupling with low Γ in order to access lower electron temperatures.

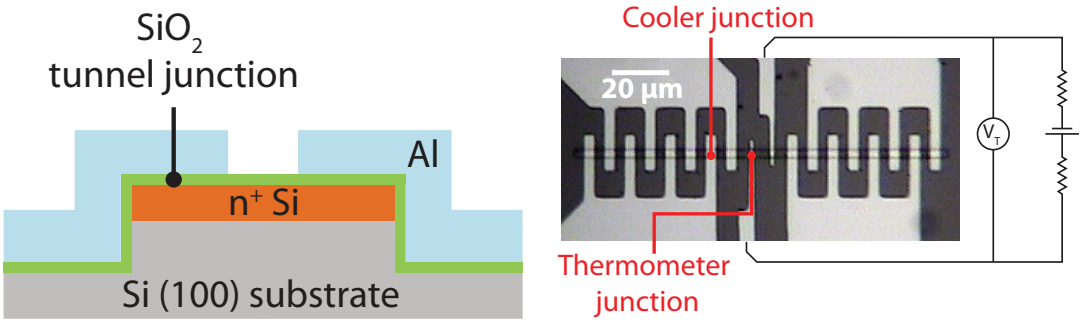
Biaxial tensile strain was induced via lattice mismatch between silicon and its germanium alloy, the lattice parameter of which varies linearly with germanium content. Firstly, a linearly graded $Si_{1-x}Ge_x$ layer was grown with the germanium

content x increasing to 0.22 over 2 µm. This was followed by a constant composition layer of 500 nm $Si_{0.78}Ge_{0.22}$. Finally, a 30 nm silicon layer was grown, conforming to the lattice spacing of the alloy below. Given that the lattice spacings of $Si_{0.78}Ge_{0.22}$ and silicon are 5.48 Å and 5.43 Å respectively, the silicon is under approximately 0.95 % of tensile strain. This figure is confirmed by X-ray diffraction.

The mesa was patterned by photolithography followed by a plasma etch, leaving a raised rectangular pillar approximately 100 nm tall with lateral dimensions 148 nm by 4 nm. The active layer is confined within the top 30 nm, thus the degenerately doped silicon is effectively isolated and the mesa geometry well defined. The native oxide was removed using 1 % HF before a thin oxide tunnel barrier was grown via an in-situ oxidation at 200 Torr and 550 °C for 600 seconds. This constituted an oxide blanket, moving away from the oxide window design utilised in chapter 6. This was largely due to both time and equipment constraints. Aluminium was then deposited, patterned and etched to form the superconducting electrode and contact metal. Sample parameters are presented in Table 7.1; the layer structure and a SEM of the tunnel junction geometry are shown in figure 7.1. Once again, a smaller set of thermometer junctions positioned in the middle of the mesa have a negligible cooling power and when biased with a constant current show a voltage that is linearly dependent on electron temperature T_e (see section 1.5).

Table 7.1: Sample parameters. Resistances measured at 40 mK. Carrier density and mobility from Hall measurements at 10 mK.

Junction resistance R_T $\left(\mathrm{k\Omega\,\mu m^2}\right)$	40
Si sheet resistance $(\Omega/\square)$	569
Carrier density $\left(10^{19}\,\mathrm{cm^{-3}}\right)$	2.7
Mobility $\left(\mathrm{cm^2\,V^{-2}\,s^{-1}}\right)$	155



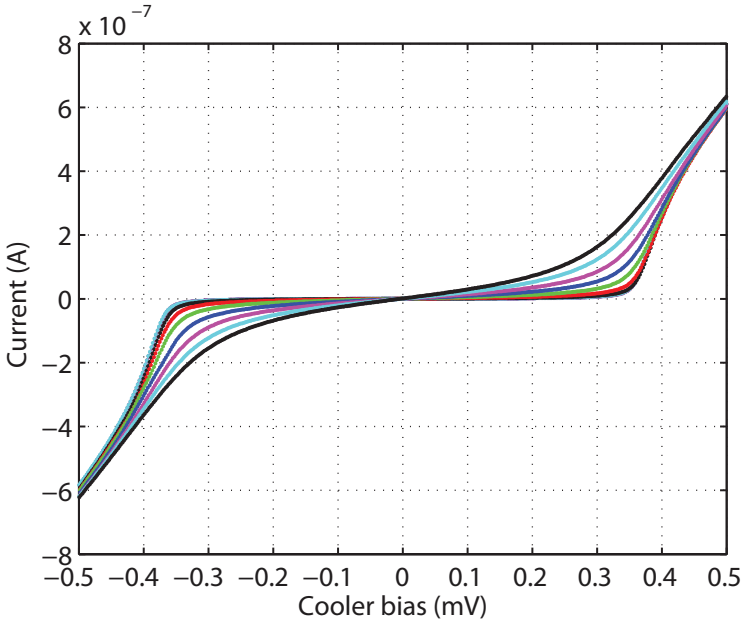
(a) A schematic cross section of the device showing the blanket oxide deposition.

(b) An optical micrograph of the cooler junctions

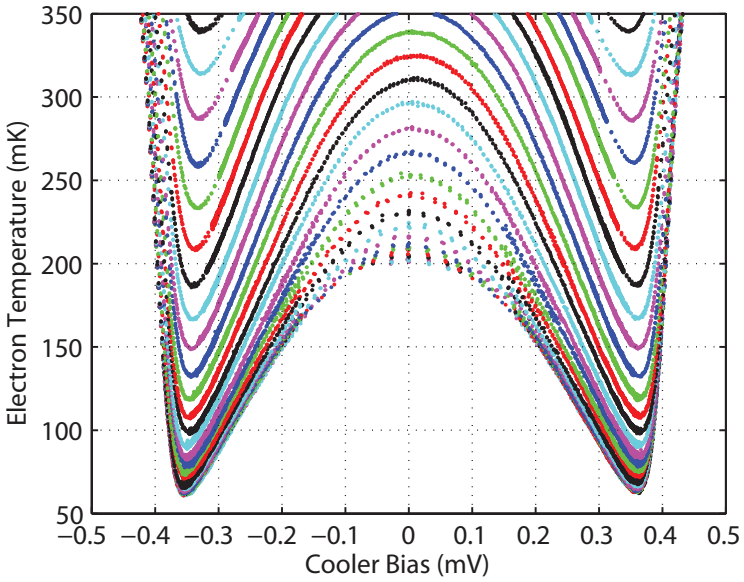
Figure 7.1: The device cross section and an optical micrograph of the cooler junctions. The device has an array of interdigitated parallel junctions that are used to cool the electron gas in the long thin central mesa, with an individual cooler junction area of $4 \times 6\mu m^2$. The geometry both improves the quasiparticle thermalisation [117] and reduces the total resistance of the silicon. The cooled volume is given by the dimensions of the electrically active layer of the mesa, being $148\,\mu m \times 4\,\mu m \times 30\,nm = 17\,\mu m^3$

The procedure for the cooling experiment is outlined in section 3.3. And the measured current-voltage and voltage-temperature behaviors are shown in figures 7.2a and 7.2b. The measurements were performed in a $^3He/^4He$ dilution refrigerator within a liquid ^4He bath and the main results of the cooling experiment are presented in figure 7.4.

Figure 7.3a shows that at a temperature of approximately 125 mK, the junction thermometers will saturate due to the relatively low sub-gap resistances [118] and therefore below this point, it is necessary to extrapolate the thermometer calibration.

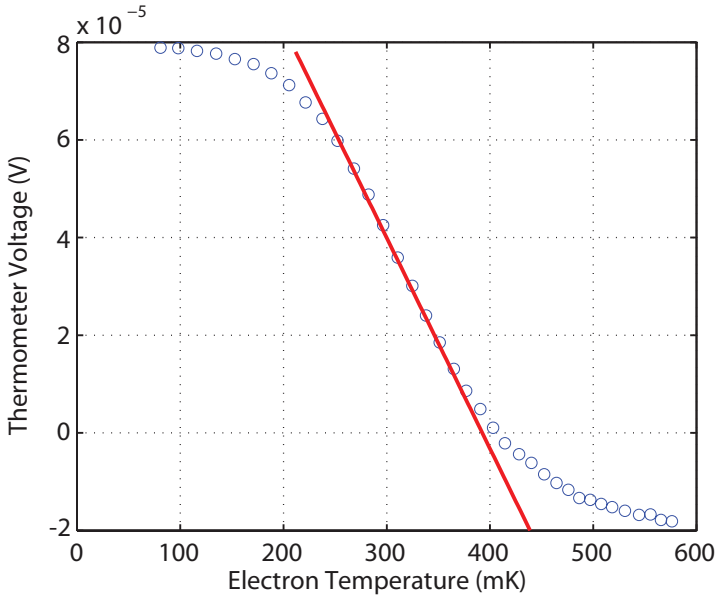


(a) Cooler IV exhibiting the characteristic diode-line temperature dependence of an N-I-S/Sm-S junction.

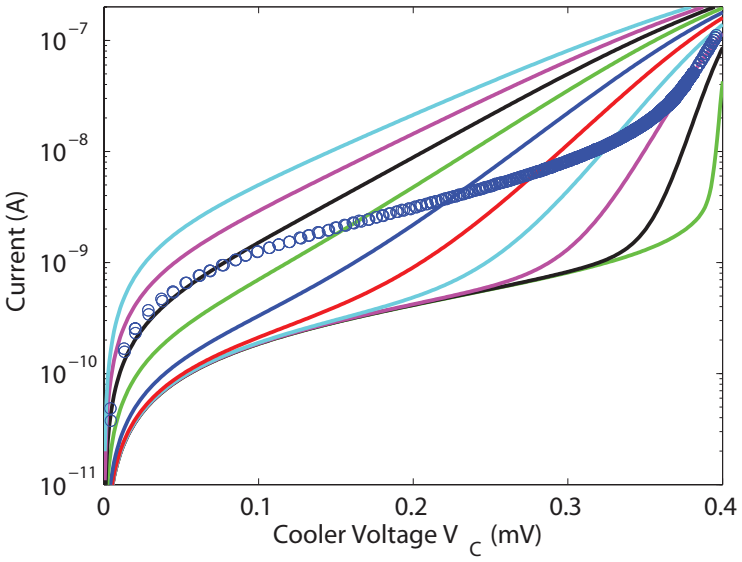


(b) Extracted voltage temperature data of the cooled semiconductor volume.

Figure 7.2: Characteristic IV and VT plots for the strained semiconductor-insulation-superconductor junction. Each coloured set of data represents a complete voltage sweep at a particular bath temperature. The bath temperature was varied between 200 mK and 570 mK in 10 mK steps.



(a) Empirical calibration of thermometer junction voltage against electron temperature at zero cooler bias. The red line shows the calibration extrapolated from the linear region of the thermometer data.



(b) Calibration of experimental data (blue circles) against theoretical isothermal junction behaviour as given by BCS theory [28].

Figure 7.3: Thermometer calibration.

As the major cooling results of this experiment were concluded from the extrapolated region of the electron temperature calibration, there was some initial doubt regarding their veracity. I therefore applied an alternative, non-empirical calibration method that is common in experiments dealing with low temperature N-I-S devices [81]. As discussed in section 1.5.3, the experimental current-voltage data from the cooling junction is superimposed on a series of theoretical isotherm curves generated from equation 1.10 using the parameters of the device under test. Each point of intersection between the experimental data and an isotherm thus yields the electronic temperature in the semiconductor island at that particular bias. Figure 7.3 illustrates the differences between the empirical and theoretical methods of temperature. Using these two methods I was able to confirm the initial conclusions, with the calibrations agreeing to within 5 mK.

From figure 7.4 one can see that the sample clearly demonstrates cooling from 300 mK down to 90 mK and from 200 mK down to as low as 60 mK.

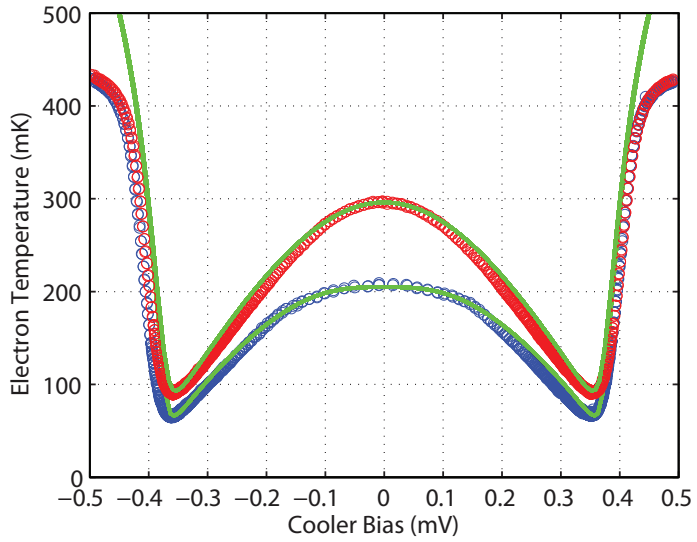


Figure 7.4: Electron temperature T_e against cooler bias V_C. The red and blue markers are experimental data showing cooling from 300 mK and 200 mK respectively. The green curves are fits generated by the cooling model. Both fit lines are generated from the same set of parameters, given in table 7.2.

Taking the minimum electron temperature T_{min} from each cooler sweep and

plotting the ratio T_{min}/T_b against T_b allows one to view cooling performance over the entire range of starting temperatures. We can see from figure 7.5 that the largest fractional change in temperature is at $T_b = 250\,\mathrm{mK}$, at which point the electrons are cooled to below 75 mK. The greatest absolute drop in temperature is 220 mK, which occurs at a bath temperature of 340 mK.

A series of cooling and heating power equations were used to model the experimental data [52, 46], each fully described in section 1.4.7. The resulting power balance equation can be written as

$$P_C\left(V_C, T_e\right) + P_{e-ph}\left(T_e\right) + P_J\left(V_C, T_e\right) + P_{QP}\left(V_C, T_e\right) = 0, \tag{7.1}$$

which is solved for the electron temperature at a given voltage.

This model is fitted to the experimental data using the parameters listed in Table 7.2. In figure 7.4, the simulation shows good agreement with both the 300 mK and 200 mK data. It should be noted that at temperatures approaching 500 mK the junction thermometers will saturate, as shown in figure 7.3a. This results in the extracted electron temperature leveling off whilst the model predicts continued heating. Figure 7.5 demonstrates that the fit is satisfactory across the range of bath temperatures used in this experiment. This model was first applied to the original strained Sm-S device [56] and its ability to model the cooling performance of different devices across a range of temperatures is evidence of its validity.

Table 7.2: Model parameters. R_{Sm} is calculated from the measured sheet resistance through twenty eight squares in parallel between the cooler contacts. Γ is calculated from the measured zero bias conductance of the junction at base temperature, divided by the asymptotic conductance.

R_T (Ω)	R_{Sm} (Ω)	Δ (meV)	Σ $\left(\mathrm{W\,K^{-6}\,m^{-3}}\right)$	Γ $\left(\Delta^{-1}\right)$	β
220	20	0.19	3×10^7	0.001	0.03

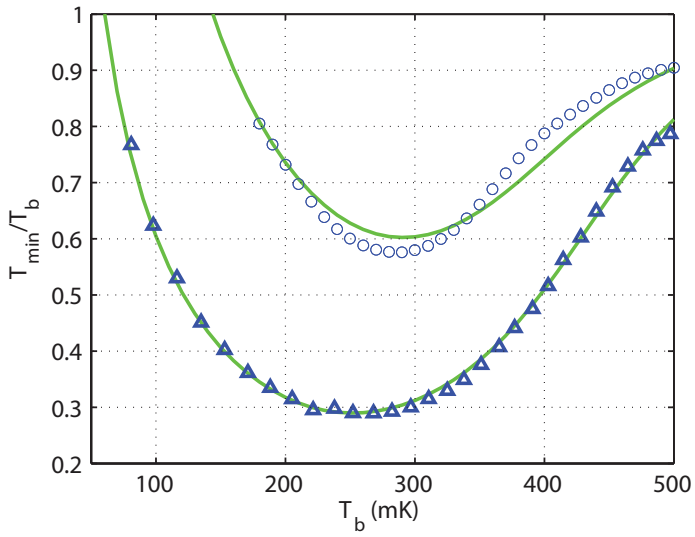


Figure 7.5: T_{min}/T_b versus T_b showing cooler performance of the strained silicon Sm-I-S cooler (triangles) over a range of temperatures. The results from a previous generation of strained silicon Sm-S cooler (circles) from [56] are included for comparison. The solid green lines represent the minimum temperature predicted by the cooling model for each of the two samples.

7.1 Summary

These results represents a major improvement in performance over the previous best result from any semiconductor based cooler device [56, 40, 31]. However, when making a comparison to the earlier strained Sm-S device [56], I am careful to note that the geometries are not identical. The cooled volume of the most recent device is lower at $17\,\mu m^3$ and the junction area is $384\,\mu m^2$ compared to $37.5\,\mu m^3$ and $576\,\mu m^2$ in the previous generation of strained device. On the other hand, adjusting for these factors in the simulations, I find that the Sm-S cooler would still only reach $\sim 170\,mK$ from a bath temperature of $300\,mK$, being significantly outperformed by the Sm-I-S device.

Furthermore, I demonstrate that semiconductor based coolers are able to access the sub $100\,mK$ temperature regime previously dominated by metal N-I-S devices with figure 7.6 clearly showing that starting from a bath temperature of

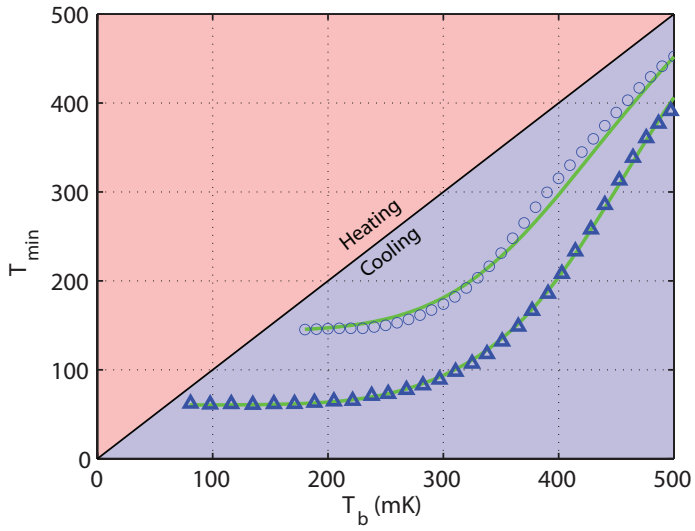


Figure 7.6: T_{min} versus T_b of the strained silicon SmIS cooler (triangles) and the strained silicon Sm-S cooler (circles). Plotting the data on these axes makes it clear that the coolers work to reduce the net temperature of the electrons across a wide range of temperature, operating below the $T_b = T_{min}$ line, and are only in danger of self-heating in the region below 100 mK.

200 mK it was possible to reach a minimum electron temperature of 60 mK.

It should be noted that the cooling power, normalised to junction area, is still much lower in the Sm-I-S junction $\left(\sim 26\,\mathrm{mW\,m^{-2}}\right)$ compared to its N-I-S counterpart $\left(\sim 90\,\mathrm{mW\,m^{-2}}\right)$ [52]. This is due in part to the higher R_T of semiconductors over metals. However, for applications based solely on electron temperature (such as bolometry) the Sm-I-S device is a competitive option, with the established advantages of a significantly higher cooled volume [9], robustness and reliability [35], as well as industry compatible, high yield fabrication methods.

Finally, it has been shown that higher doping in the semiconductor can reduce R_T to as low as $\sim 1\,\mathrm{k\Omega\,\mu m^2}$ [101], approaching that of metal based junctions. These low resistances would result in an increased cooling power in line with equation 1.7, and if applied to our current Sm-I-S device, suggest even lower electron temperatures could be achieved.

8

Further work

A natural extension to the work in carrier-phonon coupling would be a study into the effect of p-type doping density on the hole-phonon energy relation. Similar work has already been carried out with n-type donors, with hole systems being relatively unexplored. By varying dopant concentration enough to include the transition point between pure and impure doping regimes, one could get a further indication of the applicability of the Sergeev [62] model to p-type semiconductors. Furthermore, as suggested at the end of chapter 5, expanding the investigation to include a variation in dopant/impurity mass for both n-type and p-type material would be extremely valuable, potentially shedding light on why attempts to influence carrier-phonon coupling through mechanical strain have been significantly less effective than theory suggests [63].

With regards to continuing work on the electron coolers, there is nothing to suggest that the results reported to date represent the limit in electron temperature achievable by such means. Strained Sm-I-S devices could benefit from an iterative optimisation process, with doping density being increased to further lower their characteristic resistances. The findings of the further investigation into carrier-phonon coupling suggested above could likely be applied to cooler junctions, with a lower coupling constant leading to additional reductions in minimum reachable electron temperature. Furthermore, minimizing the cooled volume of the semicon-

ductor will obviously allow for a greater electron cooling performance with the same cooling power. The natural progression of this would see the development of both two-dimensional and one-dimensional semiconductor electrodes.

Two-dimensional electron gas (2DEGs) devices would benefit from a number of advantages over conventional bulk coolers. Whilst not particularly applicable to platform cooling, they would present a significant step in the quest for the lowest absolute electron temperature. 2DEGs are characterised by a low resistance and a high electron mobility, resulting in less Ohmic dissipation and a longer mean free path. One could therefore expect carriers, once removed from the semiconductor, to leave the tunnelling region more quickly. This would likely result in less back-tunnelling as well as a reduced heating effect from quasiparticle recombination in close proximity to junction.

Given that a 2DEG forms in the quantum well of a heterostructure, they occupy a thin layer below the surface and are subsequently removed from the immediate vicinity of the junction interface. Whilst this increase in the required tunnel length will no doubt affect the tunnelling probability, the remote doping should aid junction quality, much in the same way as the interfacial oxide in the Sm-I-S devices. Existing designs of cooler geometries could be easily re-purposed for 2DEG devices, with the only difference being the thickness of the active layer within the mesa, controlled during wafer growth.

One-dimensional, suspended nano-wire coolers have also been suggested [119], taking advantage of the transition in the behaviour of phonons in reduced dimensionality. Currently, only metal based N-I-S nano-wire coolers have been fabricated and the advantages to be gained from switching to silicon Sm-S junctions have yet to be explored. A number of such devices were designed over the course of my research with figure 8.1 showing one particular design.

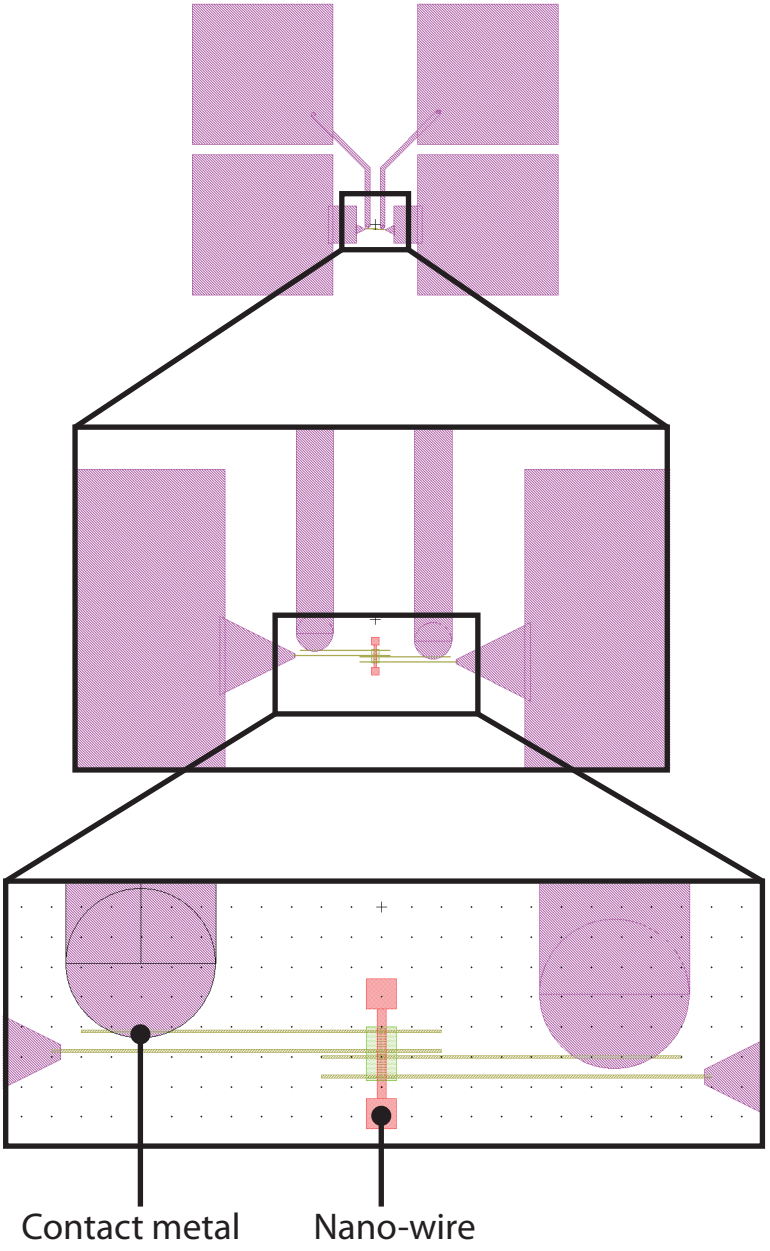


Figure 8.1: Lithography photomask designs showing the proposed layout of a 1D Sm-S nano-wire cooler. The nano-wire measures 3 µm in length, with a width of 300 nm. The green highlighted section of the substrate would be etched away leaving the wire (red) suspended.

9

Conclusions

To conclude, I have carried out an investigation into tunnel junction assisted electronic cooling that I believe has demonstrated a significant advance in both our understanding of semiconductor-superconductor TJCs and the minimum temperature obtained by such devices.

A preliminary investigation was made into alternative superconducting materials for use in Sm-S cooler junctions (chapter 4). Whilst not outperforming conventional aluminium based devices, the vanadium junction, with its large band gap, highlighted the detrimental effect of a high sub-gap density of states and made a clear case for the importance of being able to reduce the effective Γ value if cooling from high bath temperatures is ever to be achieved using semiconductor-superconductor coolers.

The fabrication of the first ever silicon-platinum silicide junction demonstrated the potential to offer enhanced cooling performance at lower temperatures, with a critical temperature successfully lowered by use of an ultra thin film. The experimental results were modeled and well-fitted by a cooling simulation that would later be applied to a range of devices with varying geometries, structure and material properties (see chapters 6 and 7), pointing to its usefulness and validity. By comparing the performance of the PtSi cooler to that of a theoretical twin device, identical in all particulars save an aluminium-like band gap, it is shown that in the

presence of a finite Γ, a thin layer with a low Δ is advantageous to cooling both in general and at lower temperatures (sub 300 mK) especially.

A study has been made into the variation of carrier-phonon coupling with carrier type (chapter 5), providing useful data towards a comprehensive, quantitative analysis of the mechanisms governing the energy loss rate between carriers and the lattice. The stronger coupling experienced by holes, which sees them better trace the phonon temperature power curve, has potential applications in phonon thermometry. Furthermore, it would find a use in the application of Sm-S junction to the cooling of thermally isolated platforms, where a reduction in lattice temperature is the main desirable rather than lowering the energy of the charge carriers alone. It is hoped that this result will stimulate theoretical work to include scattering between the heavy, light and spin-orbit split valleys, in attempt to explain the deviation from theory demonstrated by the extracted temperature exponent of the hole-phonon coupling data.

In chapter 6 I show that the energy selectivity of the tunnelling process in TJCs is highly dependent on the quality of the interface and these dependencies are discussed with evidence from changes in the formation of the junction interface. The first ever semiconductor-insulator-superconductor tunnel junction cooler was developed and the incorporation of an oxide barrier was demonstrated to improve the tunnel junction quality in respect of both sub-gap leakage and tunnel junction resistance. This led to quantifiably dramatic enhancements in junction performance, likely due to reductions in interface states and consequent Fermi level de-pinning producing a reduction in the tunnelling barrier height. I admit that the addition of an oxide barrier to the Sm-S junction is seemingly counter intuitive at first. After all, one of the benefits of Sm-S junctions is that the automatic formation of a Schottky barrier does away with the need for an insulating interfacial layer. However, I conclude that the oxidation process likely caused dopant segregation, sharpening the dopant profile in the silicon and reducing tunnelling distance, a previously ob-

served means of Schottky barrier thinning. The oxide also shifts the silicon surface away from the superconductor interface, reducing metal-induced band gap states, and certainly reducing the impact of proximity effects in the superconducting aluminium. With the Sm-I-S cooler devices it has been shown that these improvements produced a model electron cooling performance, taking electron temperatures from the comfortable 300 mK cryogenic platform temperature to 160 mK, and finally to below 100 mK with the application of tensile strain to the silicon electrode. This demonstrates that large scale, industry compatible CMOS processing techniques are capable of producing high quality silicon-superconductor tunnel junctions capable of accessing the sub 100 mK regime, a development that overturns the previous conception that silicon junctions could not compete with their metal counterparts.

Given that the quality of the Sm-S junction interface is clearly determined by the fabrication process (in contrast to metal based TJCs, the properties of which seem to be governed by the choice of material), it is likely that wider band gap superconductors (such as niobium) may be employed to initiate cooling in silicon from higher bath temperatures, giving them a distinct advantage over their metal counterparts. In conclusion, I anticipate that this result will be the starting point of further advances in electronic cooling and wider adoption of low-temperature technologies. As there are no indications that limits have been reached, I expect the lowest temperatures to extend downwards, and starting temperatures to reach upwards. Integrations with developments in other refrigeration technologies may soon enable compact, turn-key cooling from room temperature, in low-cost, low-power devices. This would allow for many applications to be explored, such as bolometric detectors for both space-borne missions and terrestrial uses, as well as wide application in fast single photon detector modes in photonics and quantum information processing.

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