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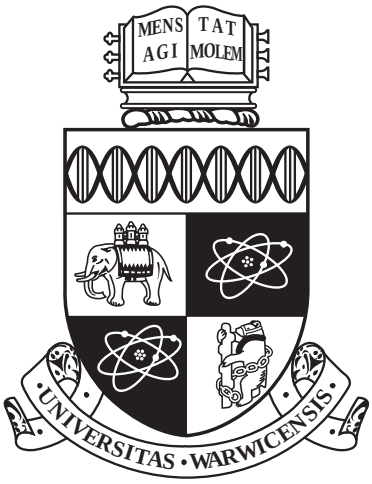

Electrical and Physical Characterization of Ge Devices

by

Catarina Beatriz Antunes Casteleiro

Thesis

Submitted to The University of Warwick

for the degree of

Doctor of Philosophy

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Declarations

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has not been submitted for a degree at any other University.

All of the work described in this thesis was carried out by the author, or under her direction, in the Department of Physics at the University of Warwick except in the following cases:

- The AFM and TEM images were taken by John E. Halpin.

- The XPS spectra were taken by Dr. Marc Walker and James Mudd.

Abstract

With continued scaling down of devices it is necessary to look into new materials in order to improve device performance. Ge and SiGe are good candidates for channel materials since they present high carrier mobility. Also, in order to reduce the gate leakage as the dielectric thickness is reduced it is necessary to look at high-κ materials to substitute the Si-SiO_2 as it reaches its limits. This thesis investigates different properties of Ge devices.

The first part of this work investigates Ge channel MOSFETs and the effects of different growth parameters such as Ge surface passivation scheme, channel thickness and doping concentration on device performance. It is shown that, for these devices, strain can provide a 50% increase in mobility, but channel thickness and doping concentration do not show significant enhancement in mobility.

The second part looks at the transport properties of very high mobility, strained Ge channel, modulation doped devices. A mobility of around 7×10^5 $cm^2V^{-1}s^{-1}$ was measured at 300 mK for a Ge heterostructure grown by CVD. Values for the hole effective mass of 0.083 ± 0.002 m_0 were obtained from the temperature and field dependence of Shubnikov-de Hass oscillations in the magnetoresistance.

In the last chapter, developments on thermal growth of GeO_2 are investigated using a simple oxidation process. It is shown that this process demonstrates good device characteristics and a smooth Ge-GeO_2 interface. For devices under study an interface trap density around $10^{11}eV^{-1}cm^{-2}$ is estimated using the low-high frequency method.

Publications

0.1 Publications

M. Myronov, C. Morrison, *C. Casteleiro*, J. Foronda, S. Rhead, D.R. Leadley

"'Ground breaking room-temperature mobility of 2D holes in a strained Ge quantum well heterostructures grown by Reduced Pressure Chemical Vapor Deposition"'

Int. Conf. on Solid State Devices and Materials (SSDM) Sept 24-27, Fukuoka, Japan. 2013

C. Casteleiro, J. E. Halpin, V. A. Shah, M. Myronov, D. R. Leadley,

"'Thermally grown GeO2 on epitaxial Ge on Si(001) substrate."'

Intl Conf on Ultimate Integration on Silicon (ULIS-14) Warwick, March 2013

J. Jasiński, L. Łukasiak, A. Jakubowski, *C. Casteleiro*, T. E. Whall, E. H. Parker, M. Myronov, D. R. Leadley,

"'Influence of series resistance determination on the extracted mobility in MOS transistors with Ge channel."'

Submitted in SPIE proceedings

0.2 Participations/attendance in Conference

2013 8^{th} International Conference on Silicon Epitaxy and Heterostructures - **Poster** presentation

Electrical and Structural Characterization of Thermally Grown GeO2 on Epitaxial Ge on a Si(001) Substrate

2013 14^{th} International Conference on Ultimate Integration on Silicon - **Poster** presentation

Thermally grown GeO2 on epitaxial Ge on Si(001) substrate.

2012 Condensed Matter and Materials Physics Conference **Poster** presentation

Electrical and structural properties of thermally grown GeO2 on epitaxial Ge on Si(001) substrate

2012 13^{th} International Conference on Ultimate Integration on Silicon

2011 Condensed Matter and Materials Physics Conference - **Poster** presentation

Study of the effect of channel thickness and Si cap passivation on hole mobility of strain Ge pMOSFETs

2010 Condensed Matter and Materials Physics Conference - **Poster** presentation

Effective hole mobility in relaxed and strained Ge Channel transistor

2009 Condensed Matter and Materials Physics Conference

Chapter 1

Introduction

1.1 Motivation

Gordon Moore (Intel's co-founder) predicted, in 1965, that the number of transistors on a chip would double every year [1] which became known as Moore's Law. This law has been the driving force behind the scaling down of devices, in particular the metal-oxide-semiconductor-field-effect transistors (MOSFET) that underpin the whole electronics industry through complimentary MOS (CMOS) circuitry. Between each 'technology node' devices have been scaled by a factor κ, which according to Moore's law is 2. The parameters to be scaled are device dimensions (oxide thickness, width and channel length and junction depth), by a factor of $1/\sqrt{\kappa}$, substrate doping concentration by κ, and supply voltage by $1/\sqrt{\kappa}$ [2].

Initially, this scaling was simply performed by taking advantage of developments in the fabrication process, in the main through advances in lithography techniques. However, in order to maintain the enhancements in performance it has become necessary to look at new materials, and to develop novel interface systems and alternative gate concepts, whilst still maintaining compatibility with silicon based-technologies [3].

Although the first transistor was made of germanium (Ge), silicon (Si) is the main component in device fabrication mainly due to the good quality of the interface of Si with is natural oxide, silicon dioxide, SiO_2 and it is abundant therefore cheaper. Ge, on the other hand, is not abundant and does not possess a good interface with its natural dielectric, GeO_2. Also, since the melting point of Ge, 937° C, is lower than for Si, a smaller thermal budget can be used for CMOS processing. Nevertheless, Ge is again being considered to be a good candidate for future MOSFETs, as it has a higher bulk mobility being more than 4 times that of Si for holes and 2 times for electrons. The principal aim of this thesis is to explore the possibilities offered by Ge channel devices and how these can be realised in practice.

Ge channel MOSFETs are already a reality, presenting good results for both n-channel and p-channel [4–7]. Because of the narrower band gap, devices made with a Ge and/or SiGe channel present higher junction leakage current, which is a concern for low power applications. Also, Ge presents a channel orientation dependency due to the anisotropy of the hole effective mass. In scaling down the SiO_2 layer used within the MOSFET gate stack to a few monolayers, the gate leakage current increases which consequently leads to devices degradation. Replacing the SiO_2 with a high-κ dielectric can allow the physical oxide thickness to be increased while maintaining a low equivalent oxide thickness (EOT). In order to integrate high-κ dielectrics it is necessary to take account a range of factors, such as the dielectric permittivity, oxide to semiconductor barrier height, gate metal work function, charge trapping in the oxide, as well as the effect on transport within the semiconductor channel of the oxide-semiconductor interface. A high dielectric permittivity element is associated with a low band gap and consequently lower barrier heights, which

are responsible for the tunnelling process. There will be a trade-off between all these parameters, but for a practical MOSFET, the high-κ dielectric constant should be between 10 to 30, the band offset should be above 1eV also, in order to attain a good electrical interface it is necessary for the high-k dielectric to be thermally stable for thermal budget temperatures, that is, 1000K for 90s [8, 9].

Another promising route for higher performing devices has been to develop III-V compounds for the n-type devices in CMOS, because of their high electron mobilities, for example 77,000 cm^2/Vs, 40,000 cm^2/Vs, 9,200 cm^2/Vs and 5,400 cm^2/Vs for indium antimonide (InSb), indium arsenide (InAs), gallium arsenide (GaAs) and indium phosphorus (InP), respectively. The enhancement factor in electron mobility compared to Si can reach 50 in the bulk [10]. However, the integration of III-V devices with silicon infrastructure, while maintaining the same quality, is not easy. Problems start with the high cost of III-V substrates and the fact that these are simply not available at the sizes used for silicon mass production (now 450 mm diameter). In addition, there are difficulties with both the epitaxial growth of III-Vs directly on Si and with a layer transfer/wafer bonding approach. Epitaxial growth is difficult because of the high lattice mismatch between Si and the III-Vs, which means a high dislocation density. Consequently, an additional strain-tuning buffer layer is required, for which Ge-on-Si is a possible candidate because of the closer lattice match to GaAs. On the other hand, integration via bonding has problems concerning damage to the conducting channel, caused during the H^+ implants, and a mismatch of the thermal coefficients of expansion, which leads to wafers bowing and/or cracking during the bonding process. A combination of the two developments just mentioned, that is, co-integration of III-V n-type and

Ge p-type devices on the same Ge-on-Si platform may provide the ultimate solution for high performance CMOS [11, 12].

1.2 Basic properties of Si and Ge

Both Si and Ge are group-IV elements that crystallize in the diamond lattice and have an indirect band gap, with silicon having the largest ($E_{g_{Si}}$ = 1.12 eV and $E_{g_{Ge}}$ = 0.66 eV). In Si, the conduction band minima lie in the [100] direction (Δ minima) and are sixfold degenerated, whereas in Ge they are in the [111] direction (L minima) and are eightfold degenerated [2, 13–16], see Figure 1.1. The valence band minima, Γ-point, consists of three bands: i) heavy-hole (HH) band, ii) light-hole (LH) band and iii) a split off band due to spin-orbit interaction. The effective mass, m^* depends on the crystal direction. When compared with Si, Ge possess a lower hole effective mass and has longer relaxation times, which can explain the higher mobilities encountered for Ge. Table 1.1 shows the basic properties of selected semiconductors.

Si and Ge are the only group IV elements that are miscible across the alloy composition range. Si can be combined with Ge to form an alloy of $Si_{1-x}Ge_x$, where x represents the Ge composition and takes values between $0 < x < 1$, still with the diamond lattice structure. On changing x the alloy characteristics are changed, such as the lattice parameter and band gap value. Figure 1.2 shows how the band gap of the alloy varies with Ge content. Although the lowest lying conduction band changes from the Δ-valley to the L-valley once x exceeds 0.85, the band gap of SiGe alloys remains indirect for all compositions.

	Si	Ge	GaAs	InP	InAs	InSb
Lattice constant at 300 K(Å)	5.43095	5.64613	5.6533	5.8686	6.0584	6.4794
Crystal Structure	Diamond	Diamond	Zincblende	Zincblende	Zincblende	Zincblende
Band Gap (eV)	1.12	0.66	1.42	1.34	0.36	0.17
Permittivity	11.8	16	12	12.6	14.8	17
Electron mobility (cm^2/Vs)	1600	3900	9200	5400	40000	77000
Electron effective mass (/mo)	m_t:0.19 m_l:0.916	m_t:0.0082 m_l:1.467	0.067	0.082	0.023	0.014
Hole mobility (cm^2/Vs)	430	1900	400	200	500	850
Hole effective mass (/mo)	m_{HH}:0.49 m_{LH}:0.16	m_{HH}:0.28 m_{LH}:0.044	m_{HH}:0.045 m_{LH}:0.082	m_{HH}:0.45 m_{LH}:0.12	m_{HH}:0.57 m_{LH}:0.35	m_{HH}:0.44 m_{LH}:0.016

Table 1.1: Basic parameter of Semiconductors [10, 17, 18]

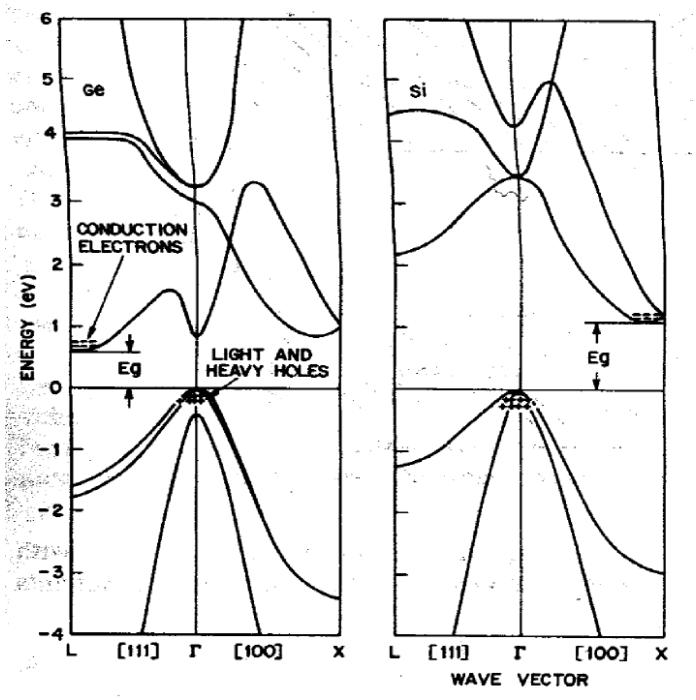


Figure 1.1: Energy band structure for Ge (left) and Si (right). Reproduced from [2].

The lattice parameter of the alloy follows Kasper-corrected-Vegard's law, which states that the increase of lattice parameter with x follows equation 1.1 [15, 19].

$$a_{Si_{1-x}Ge_x} = a_{Si} \cdot (1 - x) + a_{Ge} \cdot x - 0.00273x(1 - x) \tag{1.1}$$

where the lattice parameters for Si and Ge, $a_{Si} = 0.5431$ nm and $a_{Ge} = 0.5658$ nm, differ by 4.2%. This is a linear interpolation between both lattice parameters [20]. As can be seen in Figure 1.2, the band gap of the alloy decreases with increasing Ge content, although it does not change linearly and there is an additional bowing parameter which makes a significant difference for the bulk alloy.

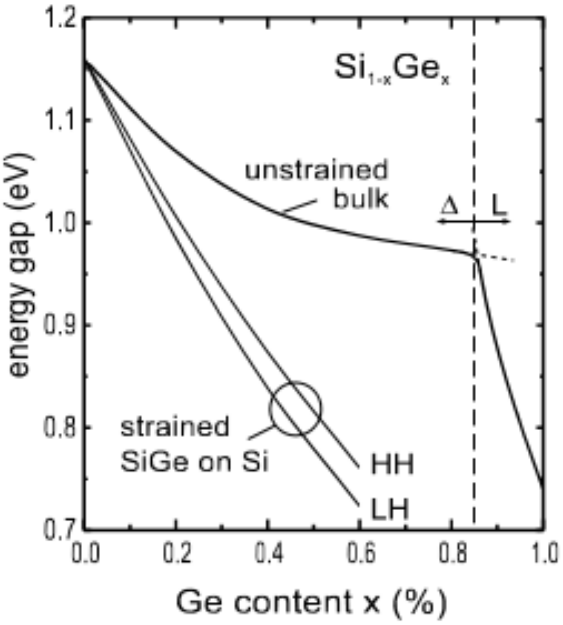


Figure 1.2: Variation of band gap of $Si_{1-x}Ge_x$, with Ge content x. At x=0.85 it is possible to observe the alloy crossover from the Si-like to Ge-like band structure for unstrained layers (top curve). For strain layers (bottom curves) is depicted the valence band splitting. Taken from [15]

1.3 Strained layers

Figure 1.2 also shows the resulting band gap for $Si_{1-x}Ge_x$ on Si for a range of x. It can be seen that there are now two lines for the band gap, since the degeneracy between heavy holes (HH) and light holes (LH) at the zone centre is lifted by the strain, with the heavy hole band being displaced upwards. This is very important for charge transport in Ge because the scattering rate for holes in the strained system is much less by having a reduced density of states to scatter into. Furthermore, the strain also distorts the shape of the hole bands which leads to a lighter effective mass for HHs under compressive strain, again improving their transport properties and leading to an increase in the hole mobility [13, 14, 21].

In addition to the changes in material characteristics caused by alloying, further desirable changes can be achieved by straining the material. The 4.2% difference in lattice parameter between Si and Ge means that a thin epitaxial alloy layer grown pseudomorphically on a silicon substrate, i.e. retaining the same in-plane lattice spacing in the epitaxial overlayer as the underlying material, will be under biaxial compressive strain.

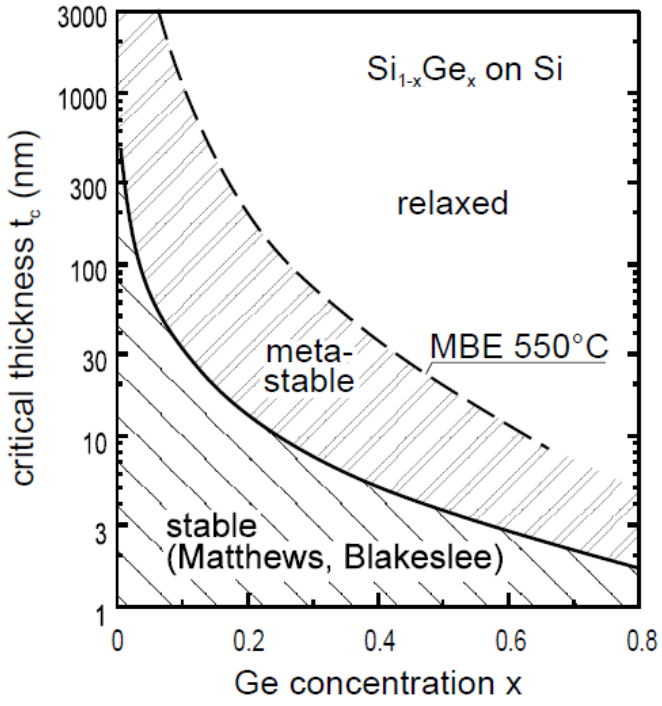


Figure 1.3: Critical thickness as a function of Germanium composition on a SiGe alloy grown on Si. Both the theoretical limit and the experimental curve for a metastable layer grown by MBE are shown. Reproduced from [15].

There is a limit to the amount of strain energy that can be built up in an epilayer before relaxation occurs through the nucleation of dislocations in the crystal [22–24]. Dislocations have a misfit segment that runs parallel to the heterointerface, which serves to accommodate the lattice difference, and also threading dislocations that can run up through the epilayer to terminate

on the free surface. Threading dislocations are potentially very bad for device properties as they can provide a leakage path and so their density must be minimised, or avoided entirely by keeping the layer below the critical thickness. For Ge grown directly on Si the critical thickness would be only a couple of nanometres (see Figure 1.3), which would make device processing impossible as this layer would be entirely removed in the first cleaning step. Instead, fully strained Ge layers that are thick enough to process devices on can be grown on a relaxed $Si_{1-x}Ge_x$ 'virtual substrate' [25–31].

It is also possible to produce Ge layers that are thicker than the critical thickness, by growing in perfectly clean conditions and at sufficiently low temperature so that there are no nucleation sites and insufficient thermal energy for dislocations to appear. Such layers are in a metastable state, which means they may start to relax if subject to further thermal processing so care for the overall thermal budget is needed [22].

1.4 Ge surface passivation

A major concern when implementing high-κ materials is the Ge-high-κ interface quality. To optimise this it is necessary to correctly passivate the Ge surface. Several methods have been used to passivate the surface [8] such as Si-based methods, sulphur, nitridation, and GeO_2. Common high-κ dielectrics used are HfO_2, ZrO_2, Al_2O_3 and GeO_2 the native oxide. The majority of the dielectrics used have oxygen in their composition, which forms an interlayer (IL) of GeO_2, and it has been shown that this IL is responsible for improving device characteristics [32–34].

Sulphur passivation presented the worst results, not showing any en-

hancement in the interface trap density, the lowest value obtained was 4.8×10^{11} $cm^{-2}eV^{-1}$, which is at least an order of magnitude too large for practical devices.

	κ
SiO_2	3.9
Si_3N_4	7
Al_2O_3	9
Ta_2O_5	22
TiO_2	80
$SrTiO_3$	2000
ZrO_2	25
HfO_2	25
$HfSiO_4$	11
La_2O_3	30
Y_2O_3	15
a-$LaAlO_3$	30
GeO_2	5-6

Table 1.2: Dielectric constant of candidate gate dielectrics. Taken from[35].

According to Chui *et al.* [36, 37] nitridation of Ge oxides lowers the interface trap density which can be reduced even further by annealling in forming gas. However, this presents an abnormal behaviour of the gate leakage due to charge trapping. Similarly, nMOSFETs treated in this way showed poor electrical characteristics, although the electrical characteristics could be improved by controlling the nitrogen concentration and the GeON thickness [38, 39]. It was found that a GeON IL, with a low N/Ge ratio, could reduce the deterioration caused by atomic laser deposition (ALD), a D_{it} of 4×10^{11} $cm^{-2}eV^{-1}$ was obtained.

Si passivation consists of growing a thin Si cap on top of the Ge and SiGe surfaces. The Si cap reduces the gate leakage current, reduces the subthreshold slope (SS) and can enhance drive current, which leads to an improvement

in the mobility of Ge devices [33, 40–43]. The Si cap can be grown using two precursors, SiH_4 and Si_3H_8, which will be examined in some detail in Chapter four.

More recently, the interest in GeO_2 as a passivation layer has increased. In order to passivate the surface several methods have been used, such as high pressure oxidation (HPO) [44], with and without low temperature oxidation annealing (LOA). The GeO_2 layer can also be grown by ozone oxidation [45], thermal oxidation [46], electron-cyclotron-resonance (ECR) plasma irradiation [47] and by direct growth on Ge substrates [48, 49]. A more detail description on different passivation methods will be given in Chapter six. Table 1.2 shows dielectric constants of candidate gate dielectrics.

1.5 Thesis outline

This thesis will look into the effects of different growth conditions and device fabrication processes on Ge devices. In chapter two a brief description of concepts needed to understand this investigation is provided. Chapter three introduces the experimental techniques and data analyses techniques used to characterise the devices. The effects of Si cap growth, doping and channel thickness in relaxed and strained Ge MOSFETs are investigated in chapter four. In chapter five, results of magneto-transport measurements performed on a 2DHG in a strained Ge quantum well will be shown. Chapter six will describe thermally grown GeO_2 on epitaxial Ge-on-Si(100) substrates. Finally, in chapter seven, a summary of the main conclusions will be given as well as an outlook on further work.

Chapter 2

Theoretical Background

In this chapter an overview is presented of the theory necessary to perform and interpret the experiments and their results. In the first two sections a description will be given of the operation modes of MOS capacitors and MOSFETs.

2.1 Metal-Oxide-Semiconductor capacitors

A metal oxide semiconductor (MOS) capacitor consist of a metal layer (gate) on top of a dielectric grown or deposited on a semiconductor body or substrate, see Figure 2.1.

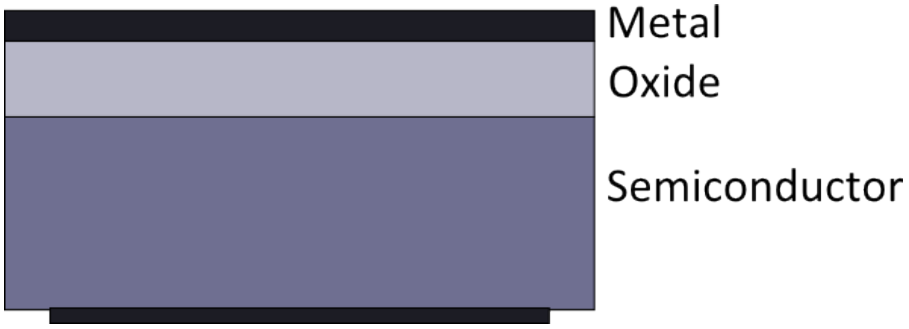


Figure 2.1: Schematic of a Metal-Oxide-Semiconductor capacitor with the back contact present. The semiconductor can be n- or p-type. The metal gate act as a gate for the device.

The substrate is usually grounded and the gate can be biased with a voltage, V_G. The substrate can be doped n-type (pMOS capacitor) or p-type (nMOS capacitor). MOS capacitors are relatively simple devices to fabricate and to measure which provide useful information about the properties of a gate stack and channel that would be obtained after a full transistor fabrication process, but with some hundred fewer processing steps.

Below are shown the band diagrams of an nMOS capacitor in the flatband condition (Figure 2.2) and under different bias conditions: accumulation (Figure 2.3), depletion (Figure 2.4), inversion and strong inversion (Figure 2.5).

In an ideal MOS capacitor no band bending is observed when the bulk semiconductor and the dielectric are put in contact (see Figure 2.2), that is, there is no charge either in the oxide or at the oxide-semiconductor interface.

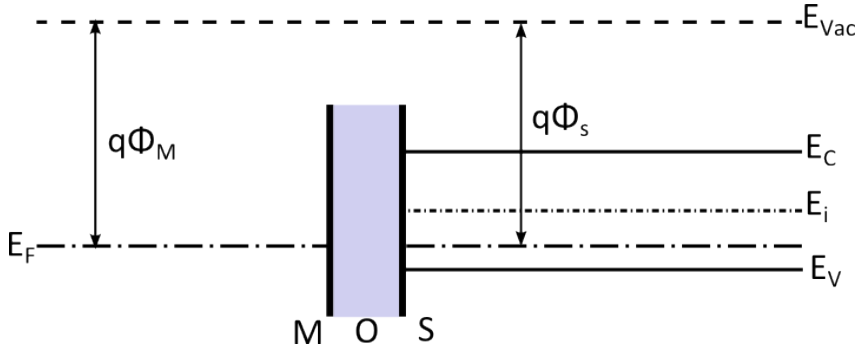


Figure 2.2: Energy band diagram for a nMOS capacitor in flatband. In real devices this condition is achieved by applying a voltage to the gate. Φ_M and Φ_S are the metal and semiconductor work function respectively.

However, when the two interfaces are put together in real MOS capacitors band bending does occur, due to the difference in the work functions of the materials. The band bending changes by applying a voltage to the gate, so, in order to align the Fermi levels it is possible to apply a voltage that

counterbalances the difference in work functions, called the flatband voltage, V_{FB}:

$$V_{FB} = \Phi_g - \Phi_s \tag{2.1}$$

where ψ_g and ψ_s are the gate work function and the semiconductor work function, respectively. These work functions are defined as the difference between the vacuum level and the Fermi level. For simplicity, the contributions of interface charge traps and any charge within the oxide are ignored in calculating the band bending.

For an n-type (p-type) semiconductor applying a positive (negative) voltage to the gate causes the conduction (valence) band to bend towards the Fermi level causing electrons (holes) to move and accumulate at the surface: the capacitor is said to be in 'accumulation' (Figure 2.3).

If a negative (positive) voltage is now applied to the gate, the valence (conduction) band bends towards the Fermi level causing the electrons (holes) to be repelled from the surface: the device is said to be in 'depletion' (see Figure 2.4). By continuing to decrease (increase) the voltage to the gate, the bands will bend even further causing the Fermi level to be closer to the

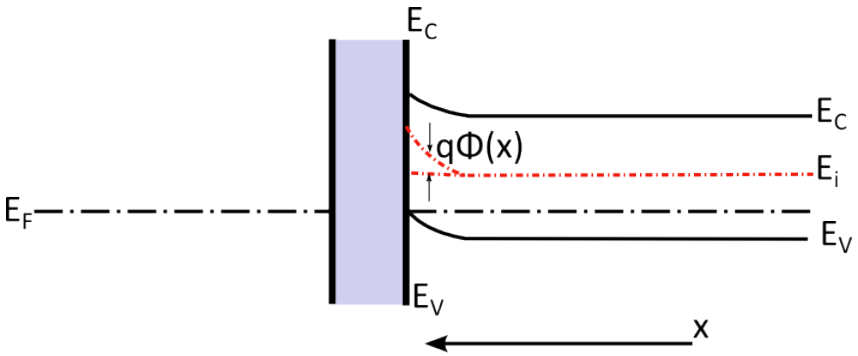


Figure 2.3: Sketch of energy band diagram for a nMOS capacitor in accumulation condition.

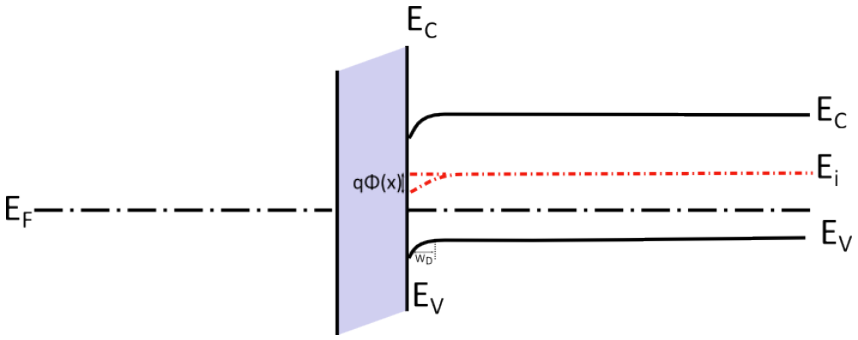


Figure 2.4: Sketch of energy band diagram for a nMOS capacitor in depletion conduction.

conduction (valence) band and eventually reach the onset of inversion, when the majority carrier concentration will be equal to the donor concentration. Continuing to apply voltage to the gate causes the device to change from n-type (p-type) to p-type (n-type) (see Figure 2.5) i.e. to become 'inverted'.

In inversion is possible to relate the voltage applied to the gate with the flatband voltage, the oxide voltage (V_{ox}) and the potential at the surface of the semiconductor (ψ_s):

$$V_G = V_{FB} + V_{ox} + \psi_s = V_{FB} + \frac{Q_s}{C_{ox}} + \psi_s \tag{2.2}$$

where C_{ox} is the oxide capacitance, and Q_s is the total charge at the semiconductor-oxide. The total charge is composed of the inversion and depletion charge, Q_{inv} and Q_{dep}, respectively. The surface potential ψ_s is defined as the difference between the Fermi level at the surface and the Fermi level in the bulk. The band perturbation potential ψ is a function of the distance perpendicular to the interface, that is, $\psi_s \equiv \psi_s(z)$, and is parabolic. The minimum of this potential is at $z = W_d$ and at this point $\psi(= W_d) = 0$, where W_d is the depletion layer width. At the surface, $z = 0$, the band perturbation potential is equal

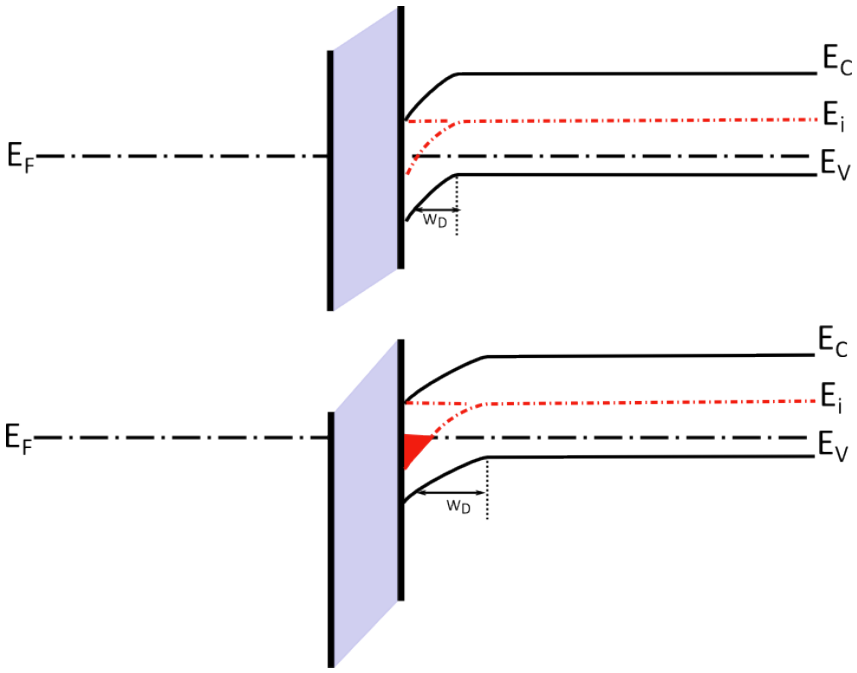


Figure 2.5: Energy band diagram for a nMOS capacitor in inversion and strong inversion.

to the surface potential, that is, $\psi(z = 0) = \psi_s$. Solving the Poisson equation and taking the depletion regime gives a depletion layer width:

$$W_{dep} = \sqrt{\frac{2\epsilon_{sc}\epsilon_0\psi_s}{qN_a}} \tag{2.3}$$

where ϵ_{sc} is the semiconductor relative permittivity, ϵ_0 the permittivity of free space, q the electron charge, ψ_s the surface potential and N_a the density of ionised acceptors. The depletion charge sheet density is given by

$$Q_{dep} = qNW_{dep} = \sqrt{2\epsilon_0\epsilon_{sc}qN\psi_s} \tag{2.4}$$

for which the surface potential at the onset of strong inversion is two times

the bulk potential

$$\psi_s = 2\psi_b = 2\frac{k_B T}{q} ln\left(\frac{N}{n_i}\right) \tag{2.5}$$

with the bulk potential also given by

$$\psi_b = \frac{E_F - E_i}{q} \tag{2.6}$$

where n_i is the intrinsic carrier concentration, k_B is the Boltzmann constant and T the temperature.

In strong inversion the bands are no longer affected by the voltage applied at the gate; the depletion layer width is at its maximum and is given by

$$W_{dep} = \sqrt{\frac{4\epsilon_{sc}\epsilon_0 k_B T ln(N/n_i)}{q^2 N}} \tag{2.7}$$

2.1.1 MOS CV characteristics.

Figure 2.6 shows a schematic current-voltage (CV) characteristic for a MOS capacitor, with measurements made at both low and high frequency. The curve can be divided in the 3 regions: in accumulation the capacitor behaves as a regular parallel plate capacitor, so the capacitance measured is the oxide capacitance; as the capacitor enters the depletion region the carriers are repelled away from interface, so the oxide capacitance is in series with the depletion region capacitance; when the capacitor enters inversion the carriers from the bulk cannot respond to a high frequency AC signal, so the curve remains constant at the bottom of the depletion region. However, at sufficiently low frequencies the carriers can respond to the AC signal and the capacitance becomes equal to the oxide capacitance again.

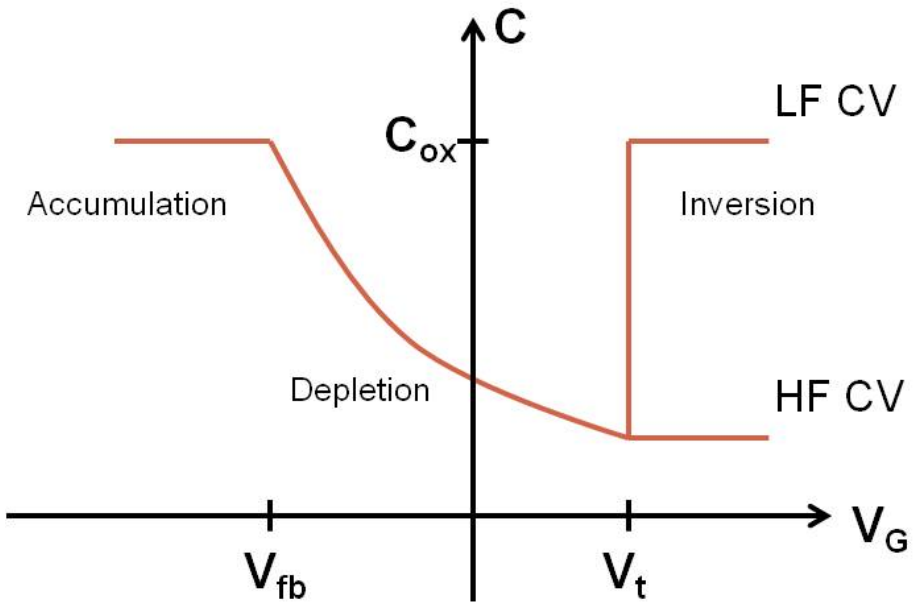


Figure 2.6: CV characteristics for a MOS capacitor for both high frequency and low frequency.

2.2 Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET).

The metal-oxide-semiconductor-field-effect transistor consist of a MOS capacitor with highly doped contacts, source and drain on either side of the channel, each with a metal contact. A p-channel MOSFET consist of an n-doped body with highly p-doped source and drain, see Figure 2.7. In an n-MOSFET, the doping is of the opposite polarity. The gate oxide is a thin dielectric insulating layer that enables a vertical electric field to be established between the gate metal electrode and the body, but not a leakage current between them. This electric field attracts charge carriers into the channel region and in varying it the conductivity of the channel can be controlled. The basic parameters of the MOSFET are channel length L (the distance between

the drain and the source), channel width W, gate-oxide thickness d, junction depth r_j and substrate doping N [2, 50].

When no voltage is applied to the gate, the drain and source are

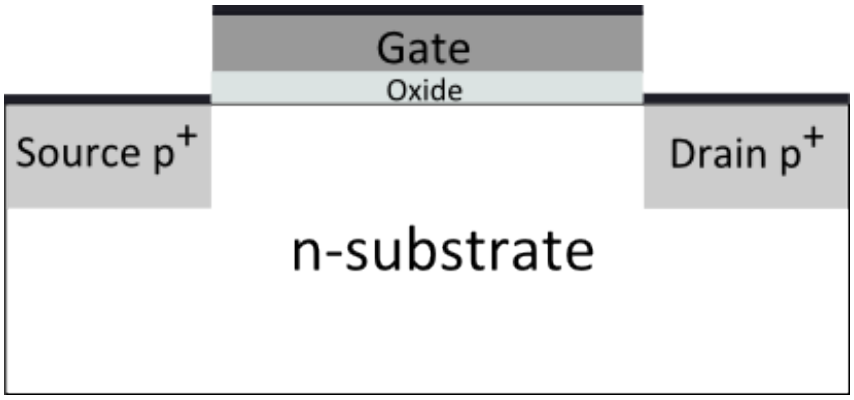


Figure 2.7: Schematic of a pMOSFET. A MOSFET is a four-terminal device: source, drain, gate and substrate. For a pMOSFET the source and drain are p^+ doped and the substrate is n doped.

isolated so no current flows across the channel, the device is in the off-state. The MOSFET behaves as two back-to-back diodes in series between drain and source, that is, a pn junctions. When a negative voltage is applied to the gate, the majority carriers will be repelled from the region under the gate downwards into the substrate, reducing the electron density leading to the formation of a positive charge, the depletion charge. The applied voltage attracts the minority carriers, holes, from the metal contacts to the area under the gate, the channel region, forming an inversion layer that connects the drain and the source and current can now flow between the two (the MOSFET is in the on-state). If a negative voltage continues to be applied there will be a point where the substrate is depleted of electrons near the surface and the conductivity of the semiconductor is inverted [2, 13, 14, 51].

MOSFET operation can be described using the charge sheet approxi-

mation [13, 14, 51, 52], which assumes that the inversion charge is located in a sheet at the semiconductor surface, with no potential drop or band bending occurring across the inversion layer.

The inversion charge, Q_{inv}, as function of the position along the channel is written as

$$Q_{inv}(x) = -C_{ox}\left(V_G - V_t - V_c(x)\right) \tag{2.8}$$

where C_{ox} is the oxide capacitance, V_c(x) is the potential at the surface in the channel region, V_t is the threshold voltage, which is defined as the voltage need to start inversion:

$$V_t = V_{FB} + 2\Phi_B + \frac{\sqrt{2\epsilon_s q N_D(2\Phi_B)}}{C_{ox}} \tag{2.9}$$

The first term refers to the flatband voltage, which ideally should be zero, the second term is the condition for the onset of the inversion layer, and the last term is the necessary voltage at the oxide to form the depletion layer.

The inversion layer is populated by holes that are moving at a velocity, $v(x)$, along the channel. The velocity, denominated carrier velocity, is related to the longitudinal electric field, E_l, by the carrier mobility, μ, which is considered constant and independent of the electric field through the channel:

$$v(x) = -\mu\frac{dV_c(x)}{dx} \tag{2.10}$$

The drain current, I_D, is defined via equations 2.8 and 2.10 by

$$I_D = WQ_{inv}(x)\cdot v(x) = C_{ox}\mu W\left(V_G - V_t - V_c(x)\right)\frac{dV_c(x)}{dx} \tag{2.11}$$

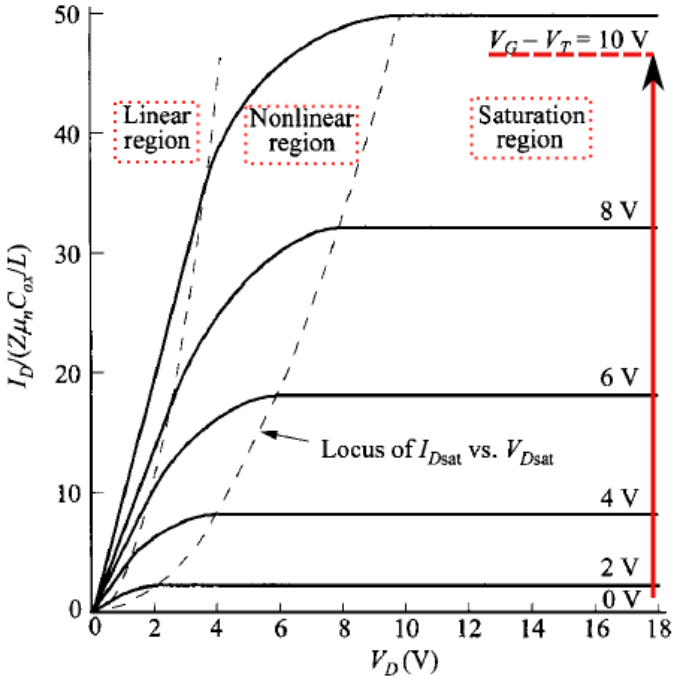


Figure 2.8: Ideal output characteristics of a MOSFET. Both operation regions are represented: saturation region ($V_D << V_G - V_t$) and linear region ($V_D \geq V_G - V_t$). Reproduced from [53]

.

Performing the integration from $V_c(0) = 0$ to $V_c(L_c) = V_D$, the expression for the drain current will be:

$$I_D = \frac{\mu C_{ox} W}{L_c} \left[(V_G - V_t) V_D - \frac{V_D^2}{2} \right] \tag{2.12}$$

which describes the output characteristics of a MOSFET.

Figure 2.8 shows the drain current plotted as a function of the source-drain voltage at different gate voltages. The curves can be divided into two regions, the linear region and the saturation region. The linear region is characterized by a linear increase of drain current with gate voltage and in this

region equation 2.12 can be written as

$$I_{D_{linear}} \approx \mu \frac{W}{L} C_{ox} \left(\left(V_G - V_t \right) V_D \right) \tag{2.13}$$

Increasing the drain voltage leads to a decrease in the inversion charge, reaching a stage with no inversion charge which is the 'pinch-off' point. An increase in the drain current moves the physical position of the pinch-off point in the channel towards the source. In this situation, the drain current depends on the channel length, not on the source-drain voltage, and the device reaches the saturation region. The drain current is then given by

$$I_{D_{sat}} = \mu \frac{W}{L} C_{ox} \left(V_G - V_t^2 \right) \tag{2.14}$$

2.3 Carrier Mobility and Scattering

The carrier mobility is an important parameter in device performance [14, 15], since a higher mobility translates into a higher drive current. The mobility is determined by a range of processes that scatter the charge carriers in the channel and is limited by the scattering mechanism with the highest relaxation rate.

The mobility is related to the transport scattering time τ by

$$\mu = \frac{e\tau}{m^*} \tag{2.15}$$

In the presence of multiple scattering mechanisms the mobility can be calculated by summing the inverse relaxation times for each mechanism to find an average relaxation time. For each process, the relaxation rate (inverse relax-

ation time) is given by solving the Boltzmann equation.

2.3.1 Scattering mechanisms

As the carrier moves along the channel it might encounter impurities, such as defects, which are responsible for the delay in their motion. If the carrier goes from the source and the drain without any impediment it is said to be in the ballistic regime, but this is very rare. Usually the carriers will interact with impurities in the lattice. The main mechanism responsible for scattering are ionized impurities or Coulomb scattering; phonon scattering; surface roughness scattering and alloy scattering.

2.3.1.1 Ionized impurities or Coulomb scattering

There will be a certain level of background impurities in any material, dopants are introduced into the body of a MOSFET to set the electrostatics, and in addition dopants can diffuse into the channel as a result of the heavy doping of the source and drain regions. The amount of dopants in the channel can also increase as a result of diffusion during high temperature stages of device fabrication. What is important for carrier scattering is how many of these impurities are ionised and thereby create an electrostatic potential.
Coulomb scattering can also arise from defects at the gate/semiconductor interface that attract charge. The impurities will change the lattice periodicity locally and consequently will change the potential. Since the Coulomb potential is a static potential it is possible for high energy carries to screen this effect. At low temperatures, when carriers have low energy, and for short channel devices this scattering mechanism is more accentuated and will often

be the limiting factor on the carrier mobility [14].

The matrix element M_q for Coulomb scattering is given by

$$|M_q| = \left[\frac{2\pi e^2}{\kappa_0 q}\right]^2 \int N_l(z) \left[F_l(q,z)\right]^2 dz \tag{2.16}$$

where $N_l(z)$ is the impurity concentration.

2.3.1.2 Phonon scattering

Lattice vibrations (phonons) cause atoms to displace from their equilibrium positions, causing changes in the band structure and hence in the band energies. Thus lattice vibrations act as a perturbation on the potential. There are two branches of phonons: acoustic and optical phonons, see Figure 2.9.

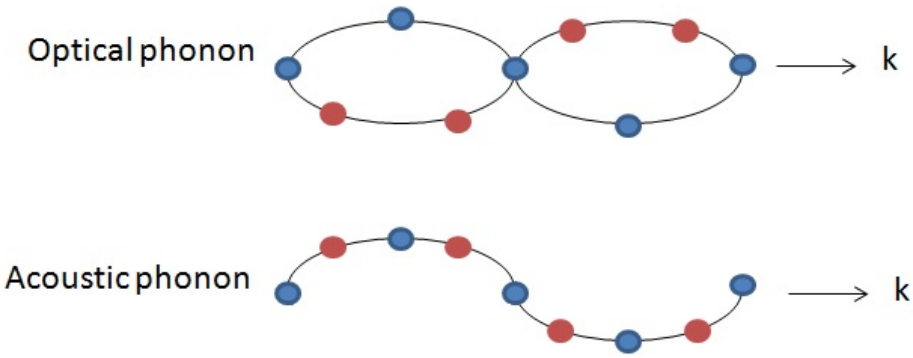


Figure 2.9: Schematic showing the difference between the acoustic and optical phonons with the same wavelength. Taken from [54].

Both Si and Ge have three acoustic phonon modes (one longitudinal and two transverse) and three optical phonon modes (one longitudinal and two transverse). In the longitudinal mode all atoms move in the direction of the wave vector, while in the transverse mode atoms move in the perpendicular direction [2, 55]. Acoustic phonons behave like sound waves with atoms moving together in the same direction. The motion of adjacent atoms in optical mode

is in opposite directions.

Scattering by acoustic phonons can be considered to be quasi-elastic, as the phonon energy is small compared to the energy of the carrier. By contrast, optical phonons have a minimum energy that is not small, making optical phonon scattering an inelastic process that modifies the carrier energy.

Lattice vibrations behave as the vibrations of the harmonic oscillator, with phonons having an associated energy $E(\mathbf{k})$ and a momentum $\mathbf{k}$.Figure 2.10 shows a schematic version of the phonon dispersion relation for the optical mode $\omega(\mathbf{k}) = \omega_0$ and acoustic mode $\omega = v_s\mathbf{k}$.

Phonon scattering is the dominant scattering mechanism at room

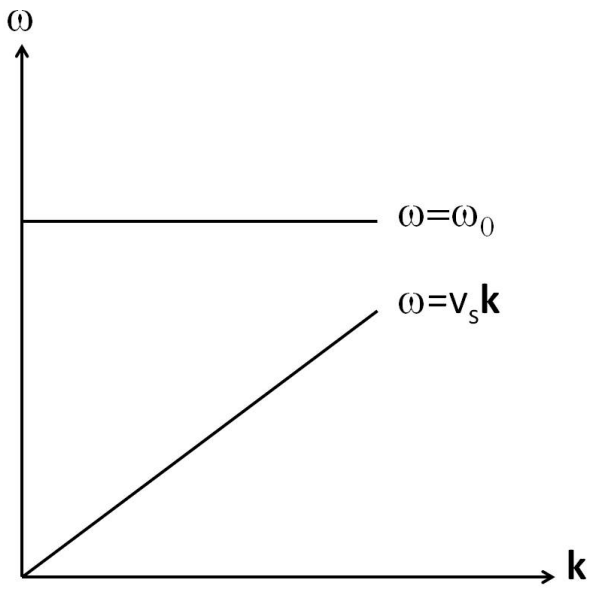


Figure 2.10: Schematic representation of phonon acoustic and optical modes.

temperature, since the scattering rate will increase with temperature as the number of phonons increases.

2.3.1.3 Surface roughness scattering

Since the interface between semiconductor and dielectric is never perfectly smooth, surface roughness causes carriers to scatter. The interface roughness scattering process is parameterised by an average height Δ and a correlation length Λ [13, 14, 56]. It assumes a Gaussian distribution which is valid when $\Delta << L$ and $\Lambda >> L$.

2.3.1.4 Alloy scattering

An alloy implies the introduction of a different atom, for example Si and Ge, which causes atomic disorder due to the change in the local band structure. When the concentration of Ge is of 50% the alloy scattering has its maximum [14, 56, 57]. However, in most cases for devices made of SiGe, alloy scattering is not a dominant scattering mechanism because interface roughness and impurity scattering are far more important processes in real materials [58].

2.4 Magneto Transport theory

2.4.1 The Hall effect

An electric field E_x is applied in the x direction and a current density I_x flows through a cross section of a metal bar, A. A magnetic field B_z perpendicular to the surface is also applied. As a result, the Lorentz force will deviate the electrons in the negative direction of y. Electrons will accumulate at one end of the bar creating an electric field in the y direction, E_y (the Hall field). This implies that the two forces are in balance and current will flow in the x direction.

The sheet resistivity of the bar is given by

$$\rho_{xx} = \frac{V_x}{I_x}\frac{w}{l} \tag{2.17}$$

and has units of Ω/sq. The velocity of the carries is related to the current I by $I = n_s qvw$, where n_s $(= nt)$ is the sheet carrier density. The Hall voltage, that is, the voltage across the bar produced by the electric field, is given by [59]

$$V_H = \frac{IB}{n_s qw} \tag{2.18}$$

where n_s is the sheet carrier density, q the electron charge and w the width of the bar. The Hall resistivity is given by

$$\rho_{xy} = \frac{V_H}{I} = \frac{B}{n_s q} = R_H B \tag{2.19}$$

From Equations 2.17 and 2.19 we deduce

$$n_s = \frac{IB}{qV_H} \tag{2.20}$$

The conductivity σ is defined by $nq\mu$ and at low magnetic fields, that is, $\mu B << 1$ [53, 59]:

$$\rho_{xx} = \frac{1}{n_s q\mu} \tag{2.21}$$

$$\mu_H = \frac{1}{n_s q\rho_{xx}} = \frac{\rho_{xy}}{B\rho_{xx}} = \frac{1}{B}\frac{V_H}{V_x}\frac{i}{w} \tag{2.22}$$

for high fields, that is $\mu B >> 1$, the conductivity is defined by

$$\rho(B) = \rho_{xx} = \frac{\sigma_{xx}}{\sigma_{xx}^2 + \sigma_{xy}^2} \tag{2.23}$$

$$R_H(B) = -\frac{\rho_{xy}}{B} = -\frac{1}{B}\frac{\sigma_{xy}}{\sigma_{xx}^2 + \sigma_{xy}^2} \tag{2.24}$$

where σ is the conductivity.

In the previous calculations we have assume a single carrier is present. For multiple carriers we have

$$R_H = \frac{\pm n_1\mu_1^2 \pm n_2\mu_2^2}{q\left(n_1\mu_1 + n_2\mu_2\right)^2} \tag{2.25}$$

for low fields approximation. Which becomes

$$R_H = \frac{1}{q\left(\pm n_1 + \pm n_2\right)} \tag{2.26}$$

in high fields. In this approximation, carriers will complete many orbits around the magnetic flux lines before being scattered. This orbits have an angular frequency $\omega_c = qB/m^*$. This angular frequency is called the cyclotron frequency. This frequency leads to the formation of Landau levels which are given by

$$E_n = \hbar\omega_c\left(n + \frac{1}{2}\right) \tag{2.27}$$

with $n = 0, 1, 2, ...$

With increasing magnetic field, the separation between two adjacent Landau levels will increase. The density of states associated with each level is given by [60],

$$n_{2D} = \frac{eB}{h} \tag{2.28}$$

The number of levels occupied is given by the filling factor, ν:

$$\nu = \frac{hp_s}{eB_0} \tag{2.29}$$

where p_s is the sheet carrier density and B_0 is the fundamental field. For ν integer the Fermi level is located in between two Landau levels so no scattering occurs.

2.4.2 Shubnikov-de-Haas effect

The Shubnikov-de-Haas (SdH) effect occurs at low temperatures, where while measuring the longitudinal resistance, R_{xx}, with varying magnetic field oscillations appear. When the transversal resistance, R_{xy}, is measured with varying magnetic field, plateau appears which is called of Quantum Hall effect.

In order to observe the SdH oscillations the 2 dimensional carrier gas, 2DCG, the carrier distribution needs to be degenerated, high field approximation, and the measurement needs to be performed at low temperatures.

It is assumed that the Landau levels have the shape of a Lorentzian, the SdH oscillations can be described in function of $\rho_{xx}(B)$ and $\rho_{xy}(B)$ as [57, 61, 62]:

$$\rho_{xx} = \frac{1}{\sigma_0}\left(1 + 2\frac{\Delta g(T)}{g_0}\right) \tag{2.30a}$$

$$\rho_{xy} = \frac{\omega_c\tau}{\sigma_0}\left(1 - 2\frac{1}{(\omega_c\tau)^2}\frac{\Delta g(T)}{g_0}\right) \tag{2.30b}$$

$$\frac{\Delta g(T)}{g_0} = 2\sum\nolimits_{s=1}^{\infty}\left(-\frac{\pi s}{\omega_c\tau}\right)\frac{A}{\hbar\omega_c}.\frac{1}{sinh\left(\frac{A}{\hbar\omega_c}\right)}.cos\left(\frac{2\pi s E_F}{\hbar\omega_c} - \pi s\right) \tag{2.30c}$$

with $A = 2\pi^2 s k_B T$, σ_0 is the conductivity at zero field, g is the density of states (DOS), Δg is the oscillatory part of DOS, s is the Fourier harmonic index, s takes values above 1 only for very high mobilities. In the following

calculations, s=1 will be used:

$$\sigma_{xx} = \sigma_0 \frac{1}{1+(\omega_c\tau)^2}. \left[1 - \frac{2.(\omega_c\tau)^2}{1+(\omega_c\tau)^2} \frac{A}{\hbar\omega_c} cosh\left(\frac{2A}{\hbar\omega_c}\right).cos\left(\frac{2\pi E_F}{\bar{\omega}_c}\right).exp\left(-\frac{\pi}{\omega_c\tau}\right)\right] \tag{2.31}$$

The longitudinal resistance can be separated in 3:

$$\Delta\rho_{xx} \approx A_1(E_F, \omega_c).A_2(\omega_c, \tau).A_3(\omega_c, T) \tag{2.32}$$

with

$$A_1(E_F, \omega_c) = cos\left(\frac{2\pi E_F}{\hbar\omega_c}\right) \tag{2.33a}$$

$$A_2(\omega_c, \tau) = exp\left(-\frac{\pi.s}{\omega_c\tau}\right) \tag{2.33b}$$

$$A_3(\omega_c, T) = \frac{A}{\hbar\omega_c} \frac{1}{sinh\left(\frac{A}{\hbar\omega_c}\right)} \tag{2.33c}$$

The period of oscillations is taken from A_1 and is proportional to the inverse of magnetic field, $\Delta(1/B)$, knowing the period the sheet density n_s is known

$$n_s = \frac{q}{\pi\hbar\Delta(1/B)} \tag{2.34}$$

The amplitude of oscillations in function of the applied magnetic field is controlled by the second term, A_2. The amplitude of oscillations depends on the effective mass and relaxation time. A_3 is used to determine the effective mass, it changes with temperature and magnetic field. By varying the temperature, the amplitude of oscillations vary but not its positions.

Chapter 3

Experimental Techniques

In this chapter we will look at the experiments used to obtain the results for this thesis. It is divided in three parts:

- Sample growth and preparation.
- Electrical and structural characterization.
- Data analyses techniques.

The majority of the experiments were performed at the University of Warwick.

3.1 Sample growth and preparation.

Ge epilayers were grown in an ASM Epsilon 2000 Reduced Pressure Chemical Vapour Deposition (RP-CVD) reactor, on 100 mm diameter Si(100) substrates. On top of these layers three types of devices were grown. The simplest devices fabricated were capacitors using evaporated Al as a top contact. Hall bars were fabricated by lithography and MOSFETs by atomic layer deposition (ALD) at IMEC. In the next sections a brief overview of RP-CVD and the device fabrication processes will be given.

3.1.1 Chemical Vapour Deposition.

As mentioned earlier, the Ge epilayers were grown by RP-CVD. CVD is a chemical process used to deposit materials onto a substrate. In the CVD process the substrate is loaded into the reaction chamber where it is heated by infra-red radiation; the substrate temperature is controlled by thermocouples below the wafer. Precursors, gaseous chemicals, are then flowed over the substrate surface and deposition occurs. The precursor flux is controlled by valves that depending on the growth recipes open and close. Depending on the desired end product different precursors will be used. The common precursors used for Ge and Si are, respectively, germane (GeH_4) and silane (SiH_4). In the epitaxial growth of our layers GeH_4 and di-silane Si_2H_6. The most probable reaction pathway of GeH_4 on the surface is $GeH_4 \rightarrow GeH_2 + H_2$ [26, 63]. The reaction scheme for this process is

$$GeH_4(g) + 2(s) \longrightarrow H_2(g) + 2H(s) + Ge(b) + e(b) \tag{3.1}$$

$$2H(s)(s) + 2(b) \longleftrightarrow H_2(g) + 2(s) \tag{3.2}$$

where s is a free surface site and b is the solid bulk lattice atom. The decomposition of disilane is done following the reaction $Si_2H_6(g) \rightarrow 2Si(g) + 3H_2(g)$ [64]. The reaction pathway on the surface is described as [64, 65]:

$$Si_2H_6(g) + 2Si(s) \rightarrow 2SiH_3(s) + 2Si(b) \tag{3.3}$$

$$SiH_3(s) + Si(s) \rightarrow SiH_2(s) + SiH(s) \tag{3.4}$$

$$SiH_2(s) + Si(s) \rightarrow 2SiH(s) \tag{3.5}$$

$$2SiH(s) \rightarrow 2Si(s) + H_2(g) \tag{3.6}$$

The gas flow rate is usually given in standard cubic centimetres per minute (sccm) and standard litres per minute (slm). The by-products are then removed form the chamber [66]. In Figure 3.1 is shown a simplified illustration of the CVD process. The temperature of the substrate is very important because it will determine the reactions that will take place. In CVD both temperature and gas flow determine the growth rate and consequently layer thickness. There are two processes that limit the rate of CVD growth: either the surface reaction rate or the mass transport rate. The first occurs when there are an over abundance of reactants, so the growth rate is limited by the reaction speed. The second occurs when the reactants are consumed at a faster rate than they are supplied.

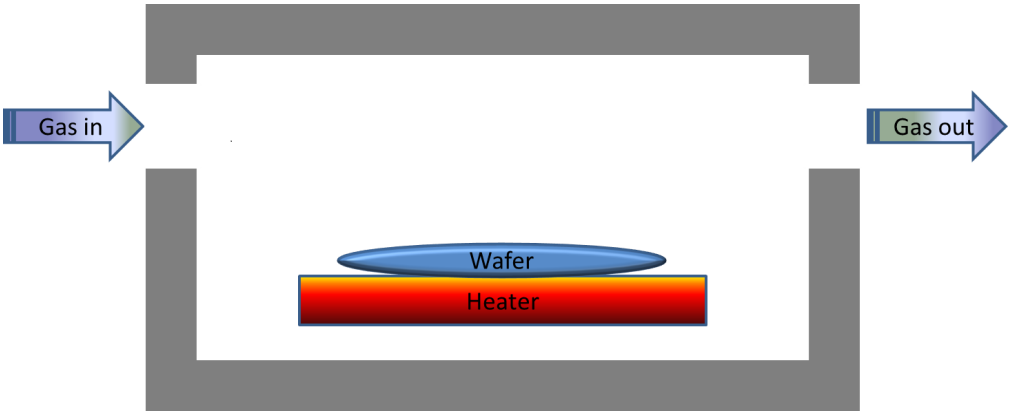


Figure 3.1: A simple illustration of the CVD process (taken from [26]).The precursor is sent to the chamber where it reacts with the wafer, the precursors used in this thesis were Si_2H_6 and GeH_4 for Si and Ge, respectively.

3.1.2 Evaporation

Evaporation is a method of physical vapour deposition using resistive heating, requiring high or ultra-high vacuum. In evaporation the metal, in the solid state, is put in a crucible which acts as a resistor. A current is

then applied to the crucible, heating it and the metal it contains. When the metal reaches its melting point atoms will be ejected, covering the substrate surface. Initially, the sample is protected by a shutter, since any impurities on the metals sources surface will be evaporated when it is first melted by the crucible. This shutter also determines the duration of the evaporation. The coverage uniformity depends on the sample distance to the crucible.

3.1.3 Lithography

Lithography is the process by which a pattern is printed on a sample, from that pattern structures are fabricated, devices. There are different types of lithography, from the relatively simple optical contact or proximity lithography to more complicated ones like projection printing and electron beam lithography. All lithography techniques use a mask to transfer a pattern.

In optical lithography the process starts (see Figure 3.2) by applying primer to the surface, the primer will remove any particulates on the surface, which can cause poor surface adhesion. The surface is then coated with photoresist which is then baked. The photoresist is a polymer and can be of two types: positive or negative. The bake, known as a soft-bake, helps adhesion and reduces contamination. The sample is then aligned with the mask and put in contact with the mask. The photoresist is then exposed to UV light and developed. If the photoresist is positive what has not been covered by the mask will be removed during development, if it is negative we get the inverse process. Afterwards it is necessary to etch the material uncovered by the photoresist and remove the photoresist.

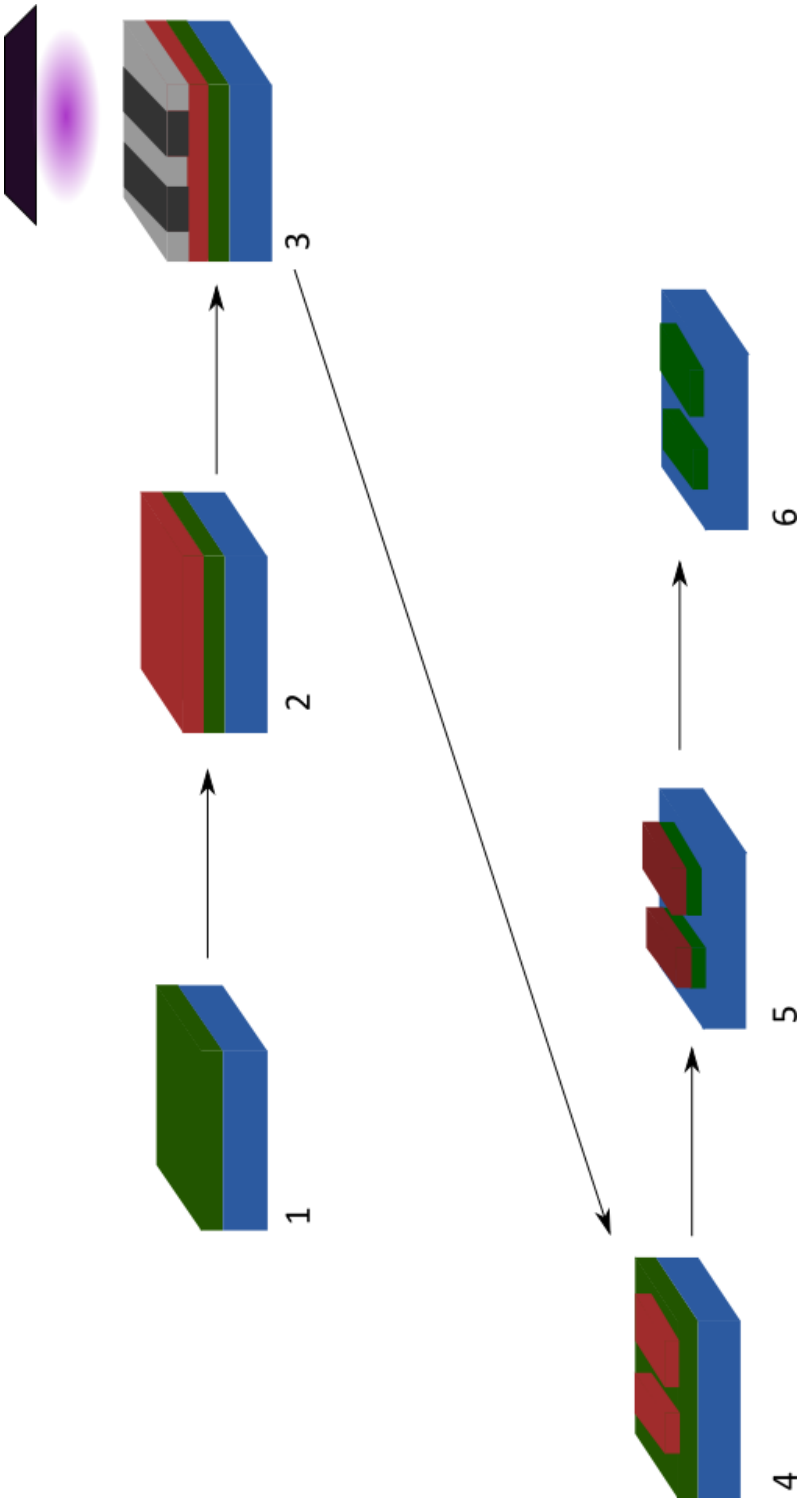


Figure 3.2: Lithography process: 1) sample to process, 2) photoresit coating, 3) exposing to UV light, 4) development, 5) etching and 6) photoresit removal.

3.1.4 Atomic Layer Deposition.

Like CVD, in ALD gas precursors are used, however, in ALD the precursors are separated by inert gas purges. By purging the system, between precursors, it is possible to avoid gas-phase reactions and it also removes volatile by-products. In Figure 3.3 is present a sketch of the deposition process by ALD.

The surface is covered with molecules from the first precursor, then when the surface is saturated the excess gas is purged and a second precursor is introduced to the growth chamber. The second precursor will react with the layer formed previously, as the surface of the second layer saturates extra precursor gas will be purge. This process is repeated until the desired thickness is achieved [9, 66]. A good ALD precursor should react rapidly with substrate in a self limiting way, volatile, stable since thermal decomposition is not allowed and its by products should not compete for surface states. Standard precursors for HfO_2 deposition are $(C_2H_5)_2N_4Hf$(TDEAH)/H_2O [67–69] and $HfCl_4/H_2O$ [36, 67, 70–72]. As an example, the overall reaction for $HfCl_4/H_2O$ is shown:

$$HfCl_4(ad) + 2H_2O(ad) \rightarrow HfO_2(s) + 4HCl(g) \tag{3.7}$$

where ad means the reactions take place between adsorbed molecules on the surface.

The main advantage of ALD is the great control of the film thickness, of the order Å as it is a layer by layer growth.

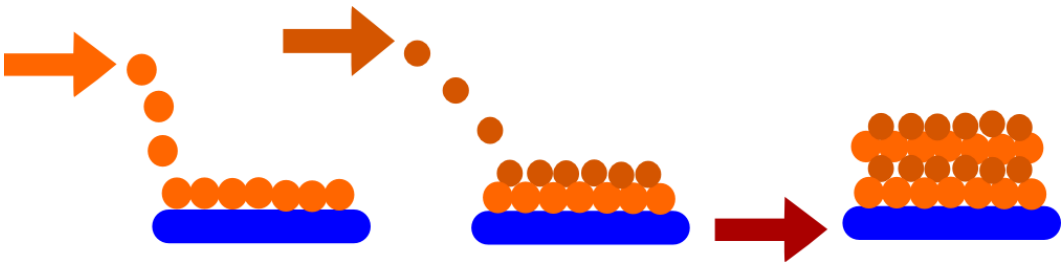


Figure 3.3: A scheme of ALD process. The first precursor will be chemisorbed on the surface, as the surface saturates the second precursor is introduced reacting with the new surface until saturation. This process is repeated in order to get the desired thickness.

3.2 Electrical and structural characterization.

Electrical characterization was performed using three different systems, a room temperature probe station, a low temperature probe station and a magnetic cryo system. The electrical measurements performed were capacitance-voltage (CV), current-voltage (IV), Hall and magneto-resistance. At room temperature the electrical characterization was done using a Karl Suss probe station, this probe station allows 4-point measurements. At low temperature electrical characterization was performed using a Desert Cryogenics TT-Probe Station for temperatures as low as 4 K. To perform the magnetotransport measurements two systems were employed: the closed-cycle cryostat for temperatures in the range 12 K to 300 K and the Heliox AC for temperatures as low as 300 mK to room temperature.

The structural characterization consisted of performing X-ray photoelectron spectroscopy, atomic force microscopy and transmission electron microscopy.

3.2.0.1 Non-magnetic electrical measurement systems

The Suss probe station was designed to probe structures from a few microns to 6" in diameter. It is composed of a chuck stage, which can be moved in the x, y and z directions. In order to ensure the structure to be measured does not move it is possible to switch on the vacuum pump. In order to probe the devices there are 4 probe heads, which can also be moved in x, y and z directions. In order to help in the probing process there is a microscope. The probe needles used were Ti with 10 μm diameter. The probe station was housed in an earthed Faraday cage to avoid electromagnetic interference, which also excluded visible light.

In the Desert Cryogenics TT-Probe Station it is possible to perform up to 4-point electrical measurements. The sample is immobilized on the sample stage with cryogenic tape. The sample stage cannot be moved. The cryogenic refrigerator, is supplied continuously with cryogen through a transfer tube from a dewar. Before inserting the refrigerant the chamber needs to be in high vacuum, 10^{-5} mbar, this prevents the formation of moisture in the chamber. Two different vacuum systems are employed independently, for the chamber and for the cryogenic liquid. On top of the chamber there is a glass window to view the sample. To position the arms on small features on the sample, the system has a optical system with a CCD. The probe needles used were BeCu with 10μm diameter. To reach temperatures between room temperature and 77 K liquid nitrogen is used and for temperatures beloww 77K to 4K liquid He is used.

3.2.0.2 Magnetic electrical measurement systems

A closed-cycle cryostat is used for measurements between 12 K and 300 K. The sample is mounted in a holder with the help of cryo wax to prevent a short between the holder and the sample a glass piece is used. The contacts are done mechanically using Cu pieces. The wires from the close cycle are then soldered to the Cu pieces. To ensure that no wires touch the shield the sample is covered with tape. The system is then put in vacuum. The system needs to be in high vacuum around 10^{-5} mbar before the He3 compressor can be turned on, providing a good thermal shield. Before initializing the temperatures it is necessary to let the system reach the base temperature around 12 K. The system can be warmed up in steps, by a metal film heater, with the temperature being controlled by a Lake Shore temperature controller.

The Heliox AC is a compact ^{3}He system, for temperatures from 300 mK to room temperature. In this system it is possible to perform Hall and Shubnikov de Haas measurements. Prior to loading the samples in the Heliox it is necessary to wire bond the sample in a chip package. Afterwards the sample is glued to the holder with the back of the chip package exposed. The wires are then solder into contacts. In order to guarantee proper shielding, the sample is covered with tape. Two metal shields are used to give further shielding. The samples are loaded and brought to vacuum before the cry-cooler is started. Afterwards, it is necessary to let the second stage reach a temperature below 10K, this will make the sorption pump cool below 20 K and start pumping the ^{3}He. Prior to cooling the ^{3}He pot it is necessary for all the gas to be in the sorb. This is done by switching the heat switch. After 1h the heat switch is switched off and the temperature should go below 7K. When that

temperature is reached, the sorb is heated to 35K. This makes the adsorbed ^{3}He go back into the pot, acting as a thermal link between the PTC$^{2^{nd}}$ stage and the pot, stabilizing the temperature. If we want the temperature to go to base temperature it is necessary to remove the heat from the sorb and close the heat switch.

3.2.1 Current-Voltage measurements

IV measurements consist of sweeping a voltage while measuring a current through a device. The IV sweeps were performed using an Agilent 4156C semiconductor parameter analyser. From IV sweep measurements we can obtain important characteristics, such as the simple device resistance or the threshold voltage of a MOSFET.

While doing IV measurements some considerations should be taken. When we connect the instrument to the device we are adding contributions to the current due to noise, contacts, wires etc. which can be reduced by employing a number of techniques; there will however always be some noise in a measurement that can not be removed. The noise due to wires and electrical connections can be reduced by using coaxial or tri-axial cables to connect the device and the instrument. Also the sample can be put in a box electrically isolated, a Faraday box. By isolating the device in this way we ensure that what we are measuring is not changed by electronics in the room or other sources of noise. When it comes to the contribution due to the device contacts, two courses of action can be taken. The first one is two perform a 4-point measurement, by measuring separately the current and voltage it eliminates the wires and contact contribution to the resistance. The second one is to

determine the contact resistance and then removed it from the calculations. The first approach is the easiest and more reliable but not always viable with the equipment available, since when measuring MOSFETs all 4 probes are needed, for the drain, source, gate and substrate.

3.2.2 Capacitance-Voltage measurement

CV measurement consists of applying a voltage across a capacitor while simultaneously applying an AC signal. The CV sweeps were performed using an Agilent E4980A precision LCR meter, capable of frequencies from 20 Hz to 2 MHz. The measurements performed were most commonly performed at frequencies between 100 Hz and 2 MHz. CV measurements are widely used to study the quality of a device, from a simple capacitor to a more complicated MOSFET.

In order to determine the effective mobility of a MOSFET the split-CV technique was used. In this technique the gate-to-channel and the gate-to-body components of the capacitance are separately measured. For the gate-to-channel capacitance, the capacitance between the gate to source/drain is measured while a voltage is applied to the gate. For the gate-to-body capacitance, the capacitance is measured across the body of the device, the source and drain grounded and a voltage applied to the gate (see Figure 3.4).

When performing a CV measurement some considerations should be taken. If the capacitance is too small it becomes difficult to measure, and higher frequencies are necessary. If the capacitor is leaky it means that the resistance in parallel with the capacitor is too low. In this case, the resistive impedance is higher than the capacitive impedance and the capacitance gets

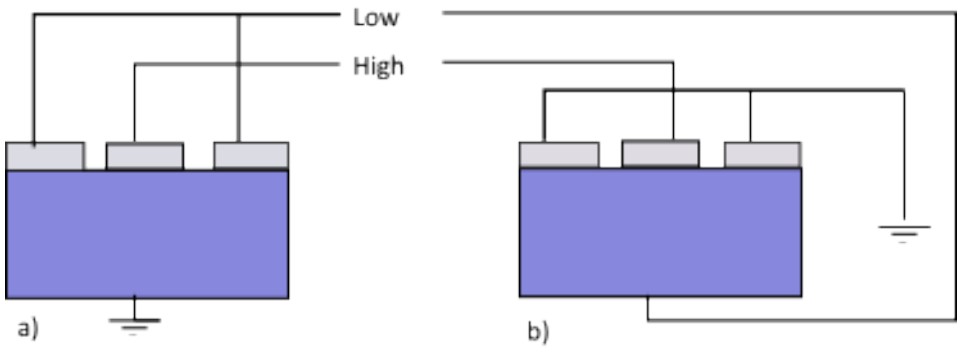


Figure 3.4: Diagrams for measuring MOSFETs capacitances using the split-CV method exhibiting both branches: gate-channel (a) and gate-body (b).

lost in the noise. Again, it is necessary to use high frequencies because then the capacitive impedence will increase whereas the parallel resistive impedance remains constant. Connections are also a concern so it is necessary to perform corrections, a combination of open and short circuit corrections are usually used.

3.2.3 Resistivity and Hall measurements.

From resistivity and Hall measurements it is possible to determine the transport properties of samples, including carrier density, carrier type and the carrier mobility. A simplified outline of the resistivity and Hall measurement set up is given in Figure 3.5. It can be seen the surface of the sample is perpendicular to the magnetic field. In measuring resistivity the longitudinal (V_{xx}) voltage is taken as a function of the current without applying a magnetic field. The transversal voltage, V_{xy}, or Hall voltage is taken across the sample as a function of the current in the presence of a magnetic field. In order to understand the behaviour of the carriers it is necessary to measure this quantities

as a function of temperature.

It is also possible to determine the effective mass of the carriers from Shubnikov-de Haas measurements. These measurements differ from standard Hall measurement in that the voltages are taken while the magnetic field is ramped.

Care should be taken while doing resistivity and Hall measurements to

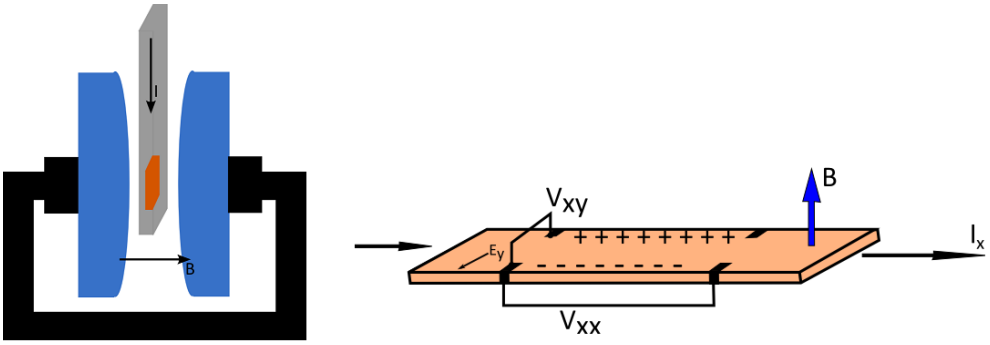


Figure 3.5: Hall measurement set up (**left**) and in plane view of the sample (**right**) for resistivity and Hall effect measurements.

avoid galvanomagnetic and thermoelectric effects. These effects can be minimized by putting the sample in a cryogenic bath and controlling the bath temperature. During the measurement, the lowest current should be used in order to avoid increasing the sample temperature. By performing measurements in forward and reverse current and/or magnetic field directions, and averaging the results, intrinsic and geometric problems with the sample can be diminished and cancelled out.

The most popular geometries for performing Hall measurements are the Van der Pauw and Hall bar geometries; in Figure 3.6 both geometries are shown. The Van der Pauw structure is simpler to process, it only requires the evaporation of metal contacts in the corners of a square sample. To obtain

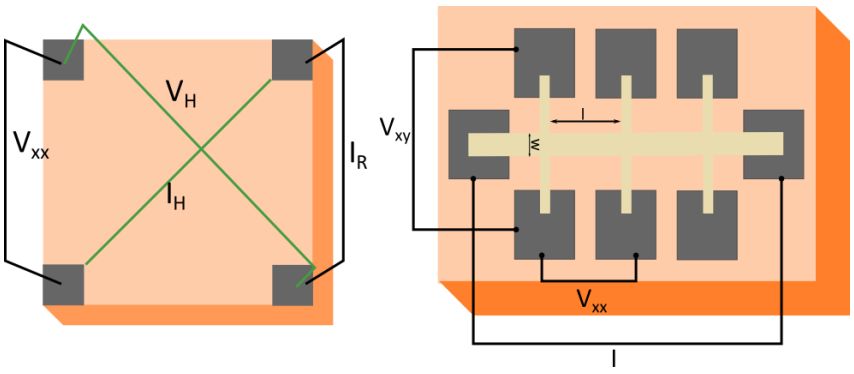


Figure 3.6: Measurement configuration for measuring the Hall effect. On the left the Van der Pauw structure and on the right the Hall bar geometry.

better results, it is necessary to ensure that we have small enough contacts, the contacts are placed at the edge of the sample, and that we have a uniform sample. The Hall bar geometry used has eight contacts and for measurements a minimum of six contacts are necessary. In this geometry it is necessary to ensure a good alignment of the contact arms and it is necessary to ensure a minimum l/w ratio of 4 to avoid shorting of the edges.

3.2.3.1 Magnetotransport measurements

The previous measurements provide us with information at a set field and temperature. To have a better understanding of the sample behaviour it is necessary to perform these measurements at different temperatures at each magnetic field. Looking at the curves as a function of temperature gives us information considering the ionization energies of the donors and acceptors present. In Shubnikov-de Haas measurements transversal voltage (V_H) and longitudinal voltage (V_{xx}) are taken while performing a sweep in magnetic field at a set temperature. The sample should have a high mobility in order to observe these SdH oscillations over a range of temperatures, so that the

effective mass and scattering times can be extracted (see below).

3.2.4 X-Ray Photoemission Spectroscopy.

In X-ray photoemission spectroscopy (XPS) the photoelectric effect is used to give surface composition, layer thickness and surface behaviour of the sample. The sample is bombarded by X-rays that interact with the core electrons, releasing a photoelectron from a bound state and creating ionized states [73]. The photoelectrons are ejected with an energy

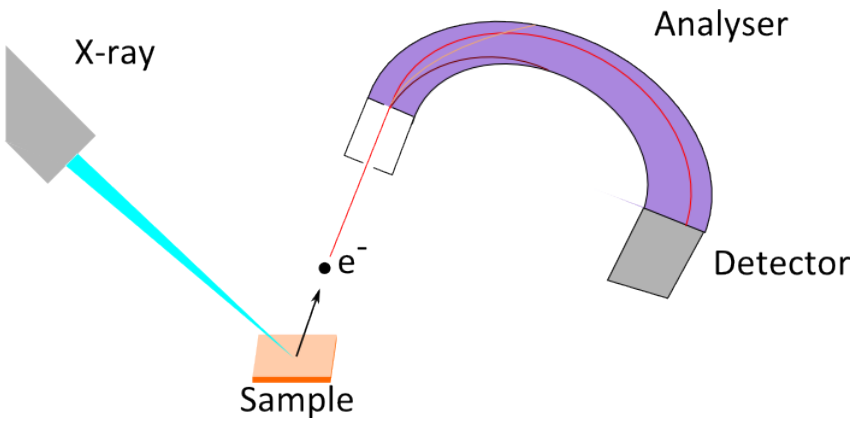


Figure 3.7: Diagram of a XPS measurement.

$$E_K = h\nu - E_b - \Phi \tag{3.8}$$

where E_K is the kinetic energy, $h\nu$ is the energy of the incoming photon, E_b the binding energy of the electron and Φ is the work function of the material. Usually, both the sample and the spectrometer are grounded making the Fermi level of both at the same energy level so that only the spectrometer work function, Φ_{sp}, is needed for determining the kinetic energy [74].

In Figure 3.7 a simplified diagram of an X-ray photoemission spec-

troscopy measurement is given. The electrons are ejected to a hemispherical analyser where a potential difference is used to select the energy of the electrons that reach the detector.

As the binding energy of the different levels are unique for each element it is possible to find out which element is present from the photoelectron energy spectrum. It is also possible to determine the oxidation state of the element by observing shifts in the photoelectron energy. These shifts occur due to a change in the binding energy of a core electron of an element due to changes in the chemical bonding of the same element. In addition, from the intensity peaks of the elements present it is possible to determine the overlayer thickness.

3.3 Data analyses techniques

3.3.1 Threshold Voltage

The threshold voltage V_t is usually defined as the voltage at which a device is switched on. From the threshold voltage measurements it is possible to calculate other parameters, such as channel length and width. Moreover it is a useful comparison parameter between different devices. There are various methods to determine the threshold voltage, using both current-voltage and capacitance-voltage measurements. For MOSFET analysis the threshold voltage is most commonly calculated from IV measurements. The threshold voltage is usually taken by extrapolating the drain current (I_D) curves to zero in the linear region.

There are several methods that use linear extrapolation techniques [75]

such as: i) linear extrapolation, ii) transconductance, iii) constant drain current iv) transconductance derivative, among others. Methods i) and ii) will now be analysed in more detail.

The extrapolation in the linear region method uses the drain current

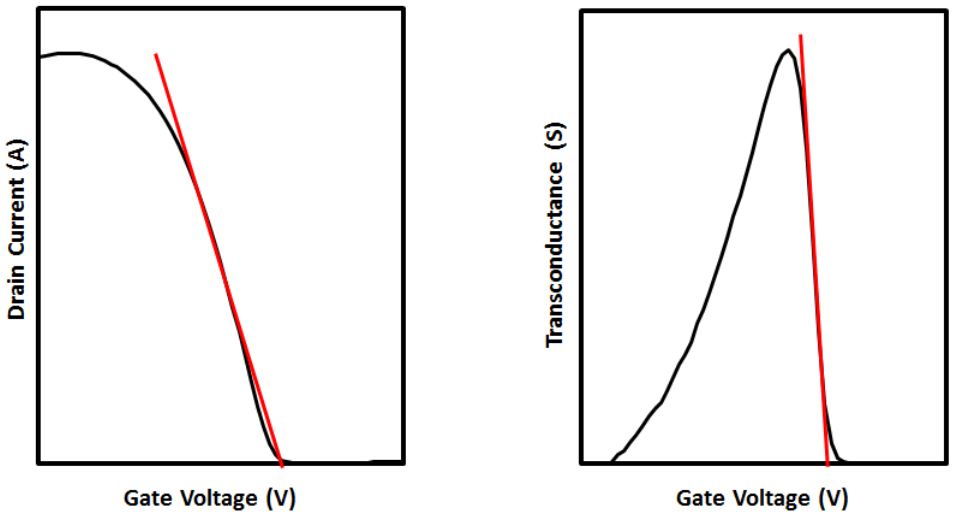


Figure 3.8: Drain current (**left**) and transconductance (**right**) curves of a pMOSFET for the determination of threshold voltage. In both methods an extrapolation of the linear region to the voltage axis gives the threshold voltage.

versus the gate voltage curve in the linear region. An extrapolation of the curve is performed and the threshold voltage will be the voltage value at which the drain current is zero, as it can be seen on the left of Figure 3.8. This technique assumes a very small series resistance, which is true for the majority of the devices.

The transconductance method uses the transconductance versus the gate voltage curve. The transconductance g_m is a measure of how much the

drain current changes when the gate voltage changes and is given by:

$$g_m = \frac{dI_D}{dV_G} \tag{3.9}$$

The extrapolation will be taken from the point where the transconductance is at maximum, as seen on the right of Figure 3.8. This technique assumes a linearly dependence of the transconductance with the gate voltage when the device goes from weak to strong inversion.

3.3.2 Subthreshold Slope

A figure of merit for MOSFETs is the subthreshold slope. By applying a high or low voltage to the gate, the device can be switched between its on-state (current flow) and off-state (current does not flow), between the source and drain contact. In real devices in the the off-state a small current can flow between the contacts. While for long channel devices this current is negligible, as the channel length is decreased the off-current starts to increase. The subthreshold slope is taken from the inverse of the slope of $\log_{10}(I_D)$ vs V_G for gate voltages below the threshold voltage and is given in units of mV/dec. We have

$$I_D = \exp(qV/nk_BT) \tag{3.10}$$

where k_B is the Boltzmann constant, q the electron charge, T the temperature and n the subthreshold ideality factor, is defined as

$$n = 1 + \frac{C_B}{C_G} \tag{3.11}$$

with n greater than 1. With C_B the bulk capacitance and C_G the gate capacitance. Ideally n should equal to unity which leads to a subthreshold slope, S, of

$$S = 2.3\frac{k_B T}{q} \approx 60\text{mV/dec} \tag{3.12}$$

60mV/dec is the theoretical limit at room temperature. Typical values, at room temperature are between 70mV/dec and 100mV/dec. High values on the subthreshold slope are an indication of high interface trap density.

3.3.3 Parasitic Resistance and Resistivity

Parasitic resistances are present in all devices and while they may be reduced, they are very difficult to eliminate. Parasitic resistance diminishes the current drive of a device. This reduction in drive current becomes an issue as device scaling continues.

3.3.3.1 Transmission line model.

A simple way to determine the contact resistance is to use transmission line model (TLM) test structures [76]. A TLM line (see Figure 3.9 consist of metal contacts spaced at different distances L_i. In this method resistance is measured between the first contact and all other contacts along the length of the bar:

$$R_i = R_{ci} + R_{ch} + R_{c_{i+1}} \tag{3.13}$$

with R_i the total resistance, $R_{c_{i+1}}$ the contact resistance and R_{ch} the channel resistance. Since $R_{ci} = R_{c_{i+1}}$ and $R_{ch} = \rho_s L_i/W$ we have

$$R_i = 2R_c + \frac{\rho_s L_i}{W} \tag{3.14}$$

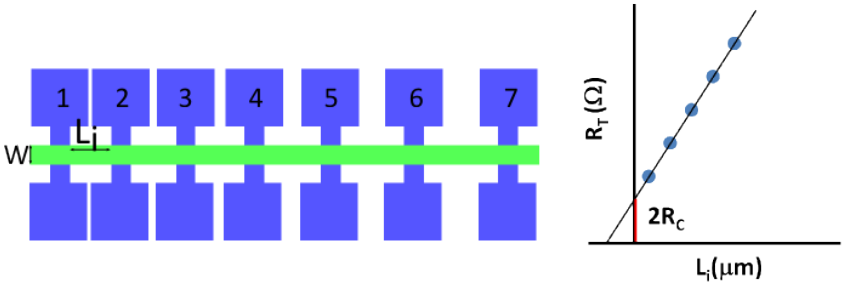


Figure 3.9: Transmission line model test structure (TLM) and method to extract the contact resistance (right).

Where ρ_s is the contact resistivity. Plotting the total resistance versus the distance between contacts, the intercept on the y-axis gives $2R_C$ and the slope is ρ_s/W.

3.3.3.2 Source-Drain Resistance

In a MOSFET the source-drain resistance contributes to the drive current so cannot be neglected [75, 77]. The major contributors are the metal contacts and the doped regions under them. In Figure 3.10 a MOSFET is represented together with the different contributions to the resistance. In order to

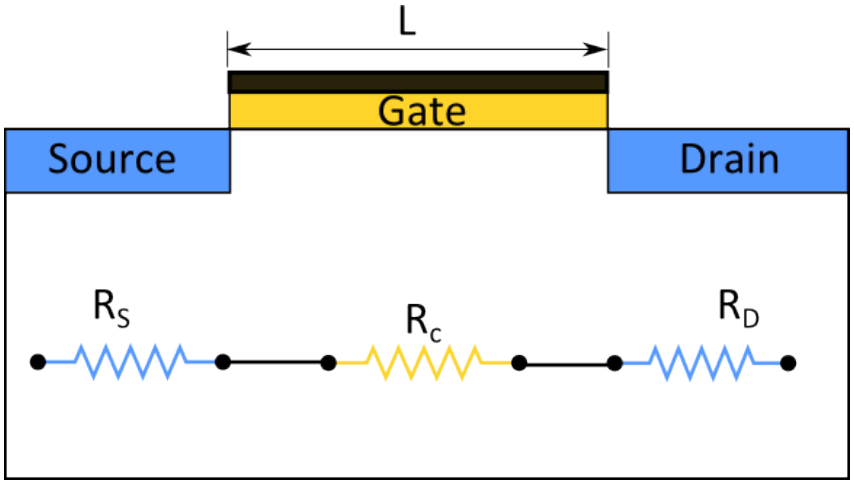


Figure 3.10: Different contributions to the resistance in a MOSFET.

evaluate the source-drain resistance, R_{SD}, various methods can be employed. The drain current $I_D$in the linear region can be written as [77]

$$I_D = Q_{inv}\mu_{eff}\frac{W_{eff}}{L_{eff}}(V_{SD}^{'}) \tag{3.15}$$

with

$$V_{SD}^{'} = V_{SD} - IR_{SD} \tag{3.16a}$$

$$L_{eff} = L - \Delta L \tag{3.16b}$$

$$W_{eff} = W - \Delta W \tag{3.16c}$$

Where Q_{inv} is the inversion charge, μ_{eff} the effective mobility, W_{eff} the efective width and L_{eff} the effective length.

A widely used method to measure the soure-drain resistance requires a set of devices with channels of different lengths but with the same width. Taking $R_m = V_{DS}/I_D = R_{ch} + R_{SD}$ we have

$$R_m = \frac{V_{DS}^{'}}{I_D} + R_{SD} \tag{3.17a}$$

$$R_m = \frac{L_{eff}}{Q_{inv}\mu_{eff}W_{eff}} + R_{SD} \tag{3.17b}$$

It is, now, necessary to measure R_m, the total resistance, for different gate voltages. These values are then plotted versus the channel length. This should give straight lines that intersect at a single point. This point corresponds to $R_m = R_{SD}$ and to $L = \Delta L$. If the lines do not intersect at one point

the following correction must be applied:

$$R_m = R_{SD} + AL_{eff} = (R_{SD} - A\Delta L) + AL = B + AL \tag{3.18}$$

where A and B are determined from the slope and intersect of the previous lines. Plotting B against A then gives R_{SD} from the slope and ΔL from the intersept. In both methods it is assumed a weak dependence of R_{SD} and channel length on the gate voltage. Since both methods depend on the gate overdrive, $V_G - V_{th}$, an accurate value of V_{th} must have been obtained.

Another method involves measuring a set of devices with $L = 0$ and different widths [78, 79]. If we then plot the resistance measured as a function of $1/W$ the intersection with the y-axis gives the R_{SD}. However, this method gives an under estimation of the value of the resistance since real MOSFET possess a finite total contact length.

The real channel length of a device differs from the channel length fabricated; this can be due to lithography and the diffusion of dopant into the source and the drain. Bias conditions can also affect the channel length. The effective channel length relates to the mask length by 3.16c and can be extracted by applying the previous methods.

3.3.3.3 Van der Pauw technique

The resistivity can be measured by the Van der Pauw technique. The resistivity for the Van der Pauw structure given on the left of Figure 3.6 will be given by [62]

$$\rho = \frac{\pi t}{\ln 2} . \frac{V_R}{I} . f \tag{3.19}$$

where V_R is an average of the V_{xx} through all contacts, I is the current, t the thickness and f is a geometry dependent correction factor. For samples with geometric symmetry $f = 1$, otherwise f is calculated by solving

$$\frac{R_r - 1}{R_r + 1} = \frac{f}{ln2} arcosh \left[\frac{exp(ln2/f)}{2} \right] \tag{3.20}$$

It is also possible to extract resistivity from a Hall bar geometry, this is given by

$$\rho = \frac{w}{l} . \frac{V_R}{I} \tag{3.21}$$

now V_R is the average between both arms of the bar and w/l is the width to length ratio of the channel.

3.3.4 Oxide Capacitance and Equivalent Oxide Thickness

The oxide capacitance is determined by

$$C_{ox} = \frac{\epsilon_0 . \kappa_s . A}{t_{ox}} \tag{3.22}$$

where ϵ_0 is the permittivity in free space, κ_s the dielectric constant of the material, A the area of the capacitor and t_{ox} the oxide thickness. When the device is in accumulation $C_{ox} = C_{max}$. This value can be used to determine the equivalent oxide thickness, EOT, which is defined as the thickness a SiO_2 layer would have in order to have the same characteristics of a high$-\kappa$ layer.

$$\text{EOT} = \frac{3.9}{\kappa_{high-\kappa}} . t_{high-\kappa} \tag{3.23}$$

where 3.9 is the dielectric constant for SiO_2.

3.3.5 Flatband Voltage

Due to the difference in the band structure of metals and semiconductors, when they are in contact there is an adjustment of the conduction and valence bands so that the Fermi levels of both materials align. In order to eliminate this band bending it is necessary to apply a certain voltage to the device. This voltage is called as flatband voltage and is defined as

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \tag{3.24}$$

where ϕ_{ms} is the metal-semiconductor work function, C_{ox} the oxide capacitance and Q_{ox} the different contributions to the oxide charge. At the flatband condition the carrier concentration is in equilibrium. The flatband voltage can be determined from the flatband capacitance $C_{fb}$from

$$C_{fb} = \frac{\kappa_s}{L_D} \tag{3.25}$$

where $\kappa_s$is the relative permittivity and L_D is the Debye length.

In the case of uniform doping and thick wafers it is possible to use 3.25; however, in the case of non-uniformity it is necessary to determine the flatband voltage by other means. One method consists of plotting the inverse of the square of a high-frequency capacitance curve versus the gate voltage and subsequently differentiating the curve. The maximum slope of this curve occurs at the flatband voltage [14, 75].

3.3.6 Effective mobility and effective field

In order to calculate effective mobility we need to perform both current-voltage and capacitance-voltage measurements. It can be determined from

$$\mu_{eff} = \frac{I_D.L}{WV_{ds}.Q_{Inv}} \tag{3.26}$$

where I_D is the drain current, L the channel length, W the channel width, V_{ds} the drain-source voltage and Q_{Inv} is the inversion charge. The inversion charge is determined by integrating the gate-channel branch of the CV curve, see Figure 3.11:

Figure 3.11: Split-CV characteristics for a pMOSFET. The green curve show the gate-to-channel branch, by integrating the area under the curve the inversion charge is obtain. The red curve represents the gate-to-body branch, by integrating the area under the curve the depletion charge is obtain.

$$Q_{Inv}(V_G) = \int_{\infty}^{V_G} C_{GC}(V_G)dV_G \tag{3.27}$$

The effective field is determined from

$$E_{eff} = \frac{Q_{Inv} + \eta.Q_{Dep}}{\epsilon_0.\kappa_s} \tag{3.28}$$

where η is an empirical factor, which was found to be 1/2 for electrons and 1/3 for holes and Q_{dep} is the depletion charge. The depletion charge is evaluated from the gate-to-body branch of the split-CV by

$$Q_{Dep}(V_G) = \int_{V_{FB}}^{\infty} C_{GB}(V_G)dV_G \tag{3.29}$$

When considering the drain current both the diffusion and drift contributions should be taken into consideration

$$I_D = Q.Q_{Inv}.\mu_{eff}.E_x - WD_p.\frac{dQ_{Inv}}{dx} \tag{3.30}$$

here E_x is the longitudinal electric field and D_p the diffusion coefficient given by

$$D_p = \frac{k_B.T}{q}.\mu_{eff} \tag{3.31}$$

Putting this in equation 3.26 gives us

$$\mu_{eff} = \frac{L}{W}.\frac{I_D}{V_{ds}}\frac{1}{Q_{Inv} - D_p.C_{GC}(V_(G))} \tag{3.32}$$

3.3.7 Hall mobility and effective mass.

The Hall mobility is extracted from Hall measurements and arises from the Hall effect. As mentioned previously (see 3.2.3) the Hall voltage is measured in both Van der Pauw and Hall bar configurations. In the Van der Pauw configuration the Hall coefficient is calculated from [80]:

$$R_H = \frac{t}{B}\frac{V_H}{I} \tag{3.33}$$

where V_H is the average V_{xy} and B is the magnetic field. For the Hall bar geometry this gives

$$R_H = \frac{1}{B}\frac{V_{xy}}{I} \tag{3.34}$$

With the resistivity and Hall coefficient it is possible to determine the carrier density (p_s) and Hall mobility (μ_H):

$$p_s = \frac{1}{R_H e} \tag{3.35a}$$

$$\mu_H = \frac{R_H}{\rho} \tag{3.35b}$$

Shubnikov-de Haas (SdH) measurements also provide us with Hall mobility and carrier density. The Hall coefficient is taken from the slope of the magnetoresistance (ρ_{xx}) versus the magnetic field in the linear region. Substituting, afterwards, in equations 3.35 for magnetoresistance at zero field $\rho_{xx}(0)$ the carrier density and mobility is given.

The magnetoresistance has a periodicity that is proportional to the inverse magnetic field. By knowing this period it is possible to determine the sheet carrier density p_s, which can either be done by inspection or by plotting magnetoresistance versus the inverse of magnetic field and performing a Fast Fourier Transform, FFT. This is then used to obtain

$$p_{_{SdH}} = \frac{e}{\pi\hbar\Delta(B^{-1})} \tag{3.36}$$

where $p_{_{SdH}}$ is the carrier density extracted from the SdH oscillations.

The SdH oscillations are describe by [62, 81]

$$\frac{\Delta\rho_{xx}(B)}{\rho_{xx}(0)} = \exp\left(-\frac{\pi\alpha}{\omega_c\tau_t}\right)\cos\left(\frac{2\pi E_F}{\hbar\omega_c}\right)\frac{\Psi}{\sinh\Psi} \tag{3.37}$$

with

$$\Psi = \frac{2\pi^2 k_B T}{\hbar\omega_c} \tag{3.38a}$$

$$\omega_c = \frac{eB}{m^*} \tag{3.38b}$$

$$\alpha = \frac{\tau_t}{\tau_q} \tag{3.38c}$$

with $\rho_{xx}(0)$ as the magnetoresistance at zero magnetic field, τ_t the transport scattering time, τ_q the quantum scattering time, $\Delta\rho_{xx}(B)$ the amplitude of the SdH oscillations, and E_F the Fermi energy. The ratio of transport to quantum lifetimes (α) is a useful parameter for interpreting the origin of the dominant scattering mechanism. While the quantum scattering time is a measure of the rate of all scattring events, the transport scattering time depends on momentum relaxation and so the ratio will be large when only small angle scattering is involved (such as from remote ionised impurities) and the ratio will be closer to unity for scattering from background impurities. The Fermi energy of a 2DHG is given by

$$E_F = \frac{\pi\hbar^2 p_s}{m^*} \tag{3.39}$$

In order to determine m^* it is necessary to perform a iterative method. First it is necessary to take the magnetoresistance magnitude for each temperature. Secondly, we plot

$$\ln\left(\frac{\Delta\rho_{xx}(T)}{\rho_{xx}(0)}.\frac{\sinh\left(\Psi(T)\right)}{\Psi(T)}\right) \text{versus} \frac{1}{(\mu B)} \tag{3.40}$$

for a initial value of m^*. This plot will provides a gradient of $-\pi\alpha$ from where the value of α is taken. Knowing this value a new plot is made of

$$\ln\left(\frac{\Delta\rho_{xx}(B)}{\rho_{xx}(0)}\right) \text{versus} \ln\left(\frac{\Psi(B)}{\sinh\left(\Psi(B)\right)}\right) - \left[\frac{\pi\alpha}{\mu B}\right] \tag{3.41}$$

This plot should give a slope of 1. If the slope is different from 1 then we take another value for m^* and repeat the process.

Chapter 4

Germanium pMOSFETs

The transistors in production nowadays, have a gate length of approximately 22 nm. Devices with this dimensions need to address several issues: high leakage currents, band-to-band tunnelling, gate stack reliability, channel mobility degradation, etc. In order to keep up with Moore's law new device geometries have been developed: from planar to non-planar geometries, like finFETs, tunnelFET; as well as new materials such as high-κ gate dielectrics, Ge and III-V as channel materials [82].

The recent development in non-planar designs has been made possible by the improvements in short channel behaviour on this type of devices, as well as improving the scalability. Tri-gate devices are fully depleted, which improves the subthreshold slope. If the channel length to channel width ratio is kept above 0.5 then it is possible to reduce the channel doping and consequently reduce scattering from impurities, hence achieving better performance.

Aggressive MOSFET scaling has required the thickness of the SiO_2 layer used as a gate dielectric to be reduced below 1nm. However, scaling below this point makes the gate leakage current increase dramatically due to tunnelling through the oxide, as well as devices being more susceptible to failure due to imperfections causing oxide breakdown in these very thin layers. The use of

high-κ dielectrics has allowed for a reduction of the gate leakage current, since the dielectric layer can be physically thicker than the SiO_2 layer that would produce the equivalent electric field int he channel. Special attention has been given to metal oxides as a replacement for SiO_2, such as HfO_2, ZrO_2 and TiO_2. Of these, HfO_2 is considered to be the best candidate, because it has a large band gap and high dielectric constant [9, 83]. However, the electronic properties of devices are affected by defects in these metal oxides, especially charges trapped within the layers and modification of the Si (or Ge) surface states at the high-κ interface. When growing a layer of HfO_2 on Si a very thin interfacial layer is usually created that can be SiO_2, the ternary $HfSiO_2$ or a nitride. When putting a dielectric layer on Ge there are further complications due to the need to passivate the Ge surface and avoid forming mixtures of Ge sub-oxides. (This topic will be further explored in Chapter 6.) The electrical properties of the interfacial layer change with the deposition method, with ALD currently presenting the best results with a leakage current of 10^{-9} A for an EOT of 0.5 nm and a dielectric constant of 20-25.

Despite multi-gate devices having seen an increase in research activity, planar designs are still the back bone of CMOS. Much progress has been made with Si-high-κ devices, but integrating the use of high-κ dielectrics with high mobility material, such as Ge, for the channel has been shown to be an alternative with excellent future prospects [84].

This chapter presents results on Ge MOSFETs that were fabricated in IMEC using strained Ge-on-Si(100) epi-wafers grown in Warwick.

4.1 Device description

The batch consist of two wafers of relaxed Germanium (rGe), grown directly on a silicon substrate, and six wafers of strained Germanium (sGe) layers that were grown on reverse graded virtual substrates, as seen in Figure 4.1 and Figure 4.2, respectively.

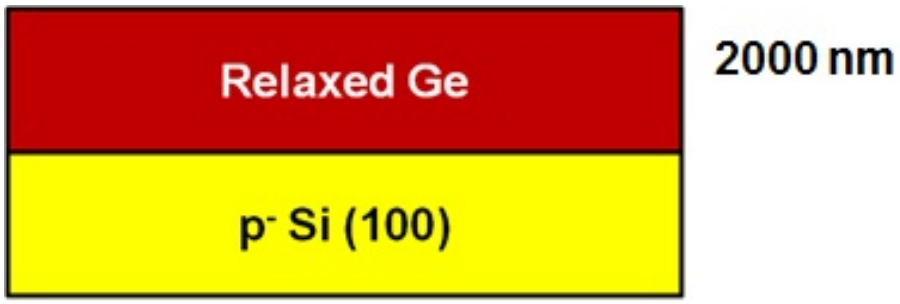


Figure 4.1: Schematic diagram of the structures for relaxed germanium layers. The rGe layers consisted of a thick Ge layer growm directly on a Si substrate.

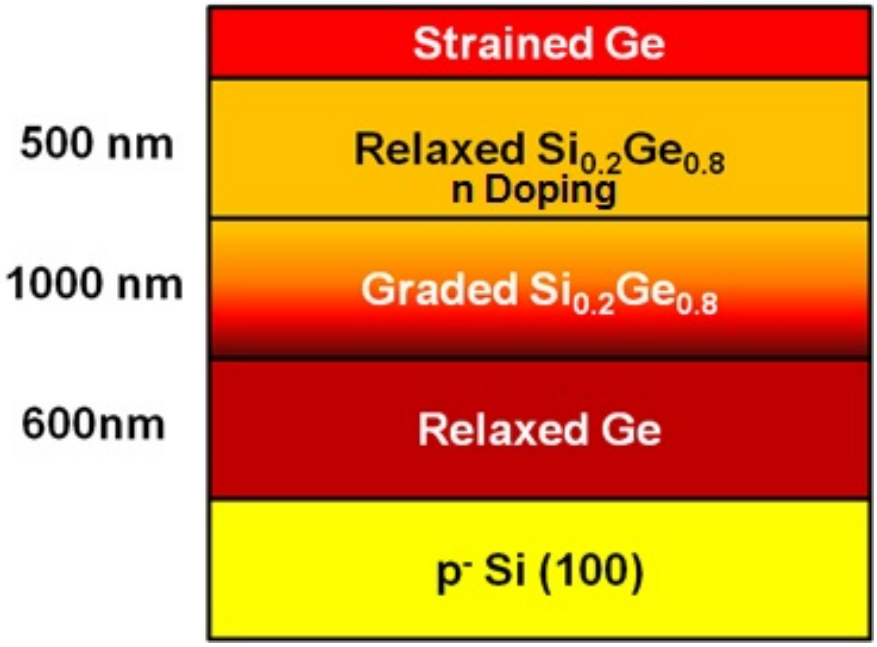


Figure 4.2: Schematic diagram of the structures for strained germanium layers. The sGe layers were grown on a reverse graded virtual substrate.

The rGe layers have 2 μm nominal thickness and were epitaxially grown at IMEC with a TDD of approximately 2×10^7 cm^{-2}. For the sGe wafers, 600 nm of relaxed Ge was first grown at Warwick on a Si(100) wafer. Afterwards, a 1 μm $Si_{0.2}Ge_{0.8}$ reverse graded virtual substrate [25] was grown terminating in a 500 nm constant composition $Si_{0.2}Ge_{0.8}$ layer. On the top a thin layer of strained Ge was grown, the thickness of this and its doping concentration were varied. Both rGe and sGe wafers are n doped with boron and possess a base doping concentration of 5×10^{17}cm^{-3}. The layer thickness and composition, as well as doping concentration are reported in previous studies [85–87].

The final crucial layer was a silicon cap to passivate the Ge surface before high-κ deposition. Two Si cap passivation schemes were employed. For the rGe wafers, one was passivated by growing Si with SiH_4 at 500° C and another with Si_3H_8 at 350° C. All the sGe wafers were passivated using Si_3H_8.

The devices were fabricated at IMEC by Atomic Laser Deposition. The gate stack (Figure 4.3) consist of passivating the Si cap at high temperature (350° C or 500° C) afterwards a 4nm layer of HfO_2 with gate metallisation of 10nm TaN followed by 70 nm of TiN was deposited.

Figure 4.4 shows the design of the transistors measured. The gate width of the devices was varied between 10 μm and 80 μm, and the gate length between 3 to 100 μm.

The majority of the characterization was performed on devices with a gate length and width of 10 μm. Table 4.1 summarizes the various wafers studied, including variations in the channel thickness and doping density.

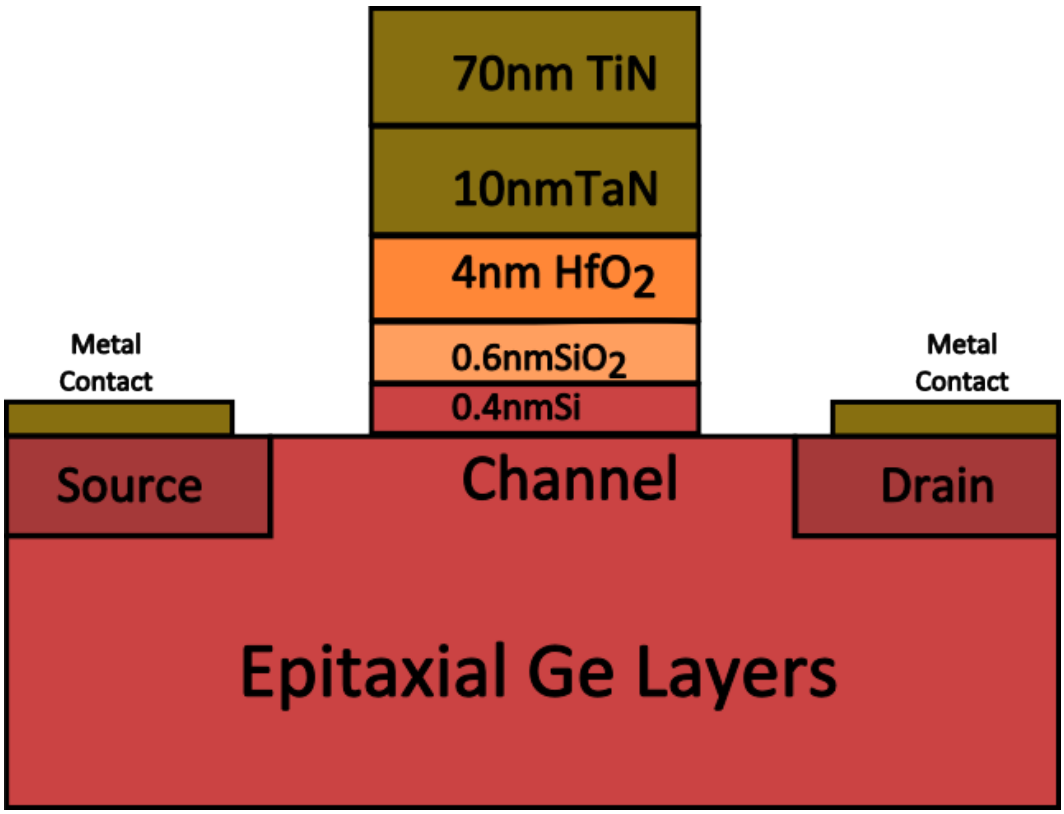


Figure 4.3: Gate stack implemented by Atomic Laser Deposition at IMEC. The gate stack consists of a SiO_2 interlayer on top of the Si cap, HfO_2 and for metal gate TiN and TaN.

4.2 Device characteristics

The characterization started by performing a uniformity test in selected areas of the wafer with strained layers, a 10 nm channel thickness and a doping of 5×10^{-17} cm^{-3}. All the measurements were taken from chips in the top 1/3 of the wafer, chips from different sites in the wafer were chosen to performed IV measurements as shown in Figure 4.5. In Figure 4.5 six devices were chosen, however, only four are shown in Figures 4.6 and 4.7, because some were destroyed during measurements. Since no post-metallization treatment was carried on, charge carriers induced by light will contribute to the current. As

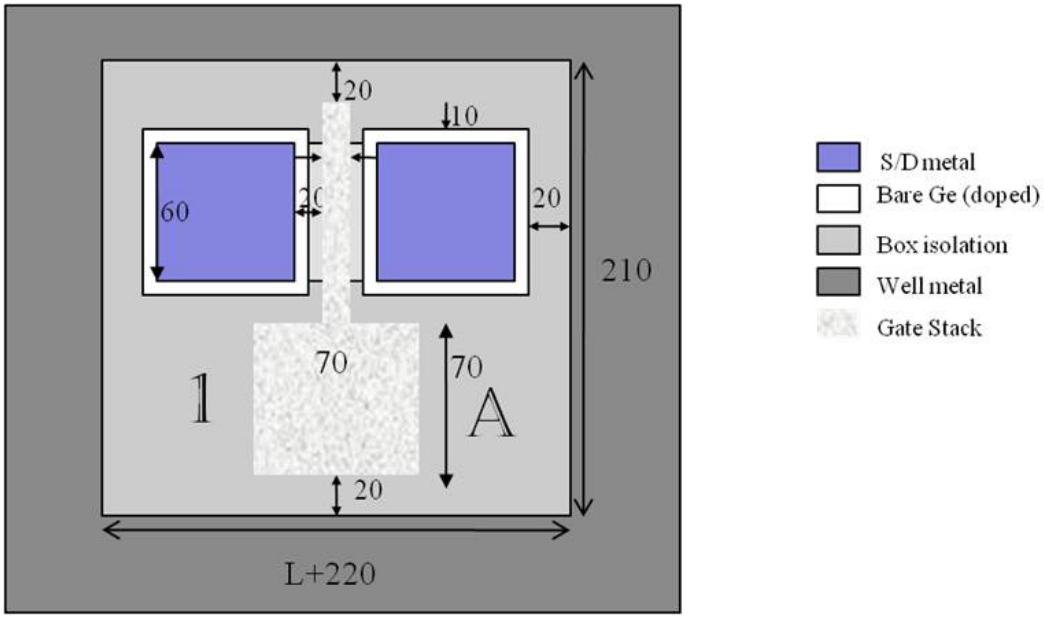


Figure 4.4: Devices schematic (dimensions in μm).

Wafer Number	Strained or Relaxed	Channel Thickness (nm)	Doping ($\times 10^{17}$cm^{-3})	Si Cap Passivation	
				350°C Si_3H_8	500°C SiH_4
DO4	relaxed	–	–	x	
DO5	relaxed	–	–		x
DO6	strained	10	0	x	
DO7	strained	10	1	x	
DO8	strained	10	5	x	
D11	strained	20	0	x	
D16	strained	30	0	x	
D21	strained	40	0	x	

Table 4.1: Label of the different wafers, according to passivation type, thickness and doping.

a solution the devices were probed in dim light. The IV measurements consisted of sweeping the gate voltage (V_G) of the MOSFETs and measuring the drain current (I_D). Figures 4.6 and 4.7 show that the processing was extremely

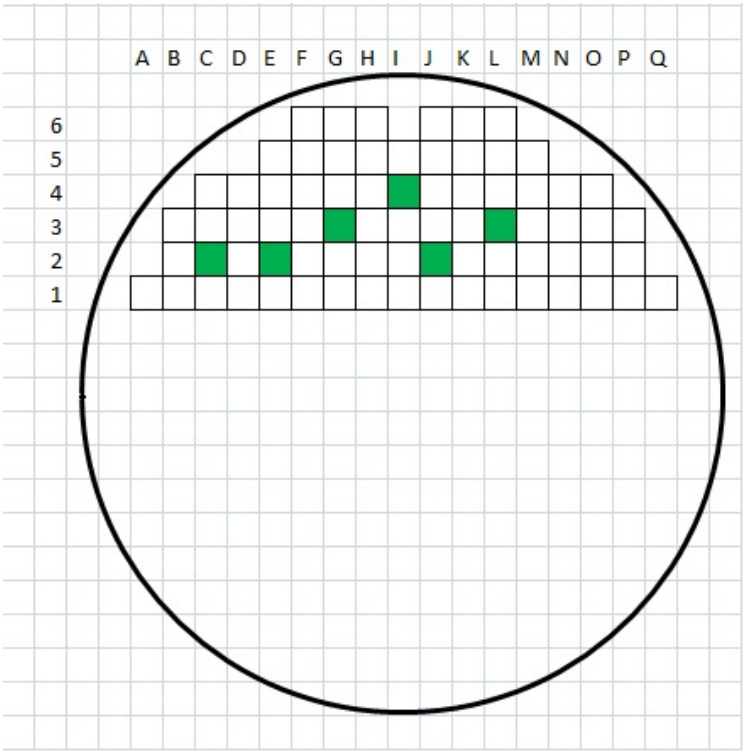


Figure 4.5: Wafer map for uniformity study. The devices study have a channel length of (10 μm).

uniform with all the I_D-V_G curves being essentially identical. Processing of the other wafers was similarly uniform.

In the following sections we will look at different factors that are responsible for mobility degradation in devices, such as the effect of the Si cap passivation, the effect of the thickness of the strained Ge channel and the effect of the doping. This study will be carried out at room temperature and 77 K to extract the hole mobility, using the split CV method for selected devices. The measurements at low temperatures reduce phonon scattering, leading to a higher mobility and allowing the effect of other scattering mechanisms to be identified. The results shown in the following section, using devices with a gate length of 10 μm, are representative of the results obtained on devices

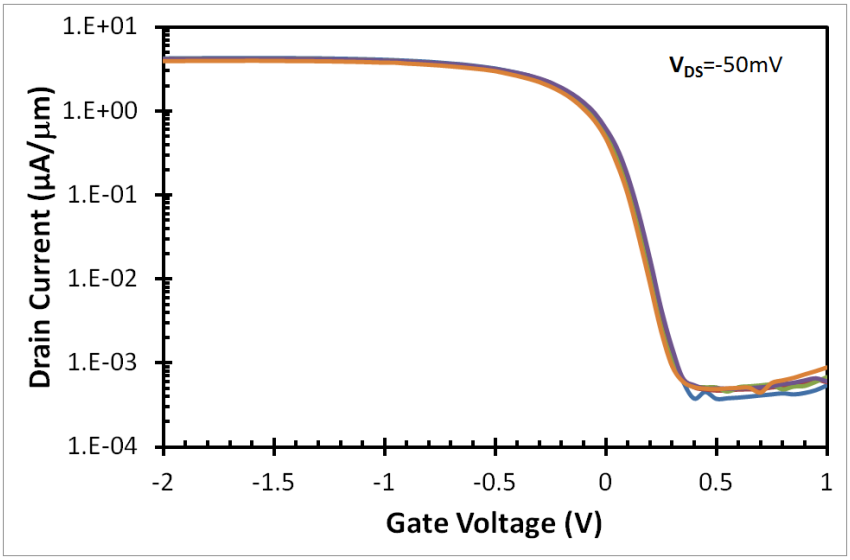


Figure 4.6: Drain current curves for four devices, with the same dimensions taken from different positions on the wafer, at room temperature. The wafer consisted of sGe layers, with a channel thickness of 10 nm and a channel doping of $5 \times 10^{-17}\text{cm}^{-3}$.

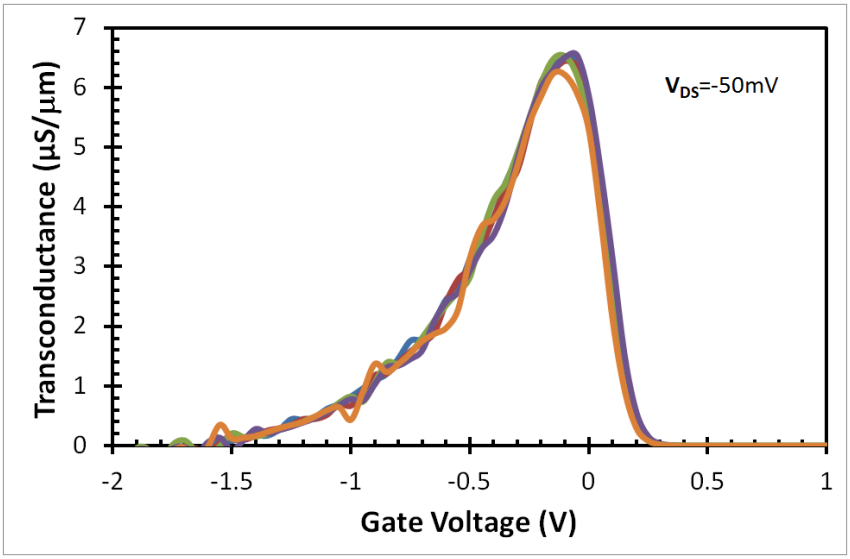


Figure 4.7: Transconductance curves for the four devices shown in the previous figure. The wafer consisted of sGe layers, with a channel thickness of 10 nm and a channel doping of $5 \times 10^{-17}\text{cm}^{-3}$.

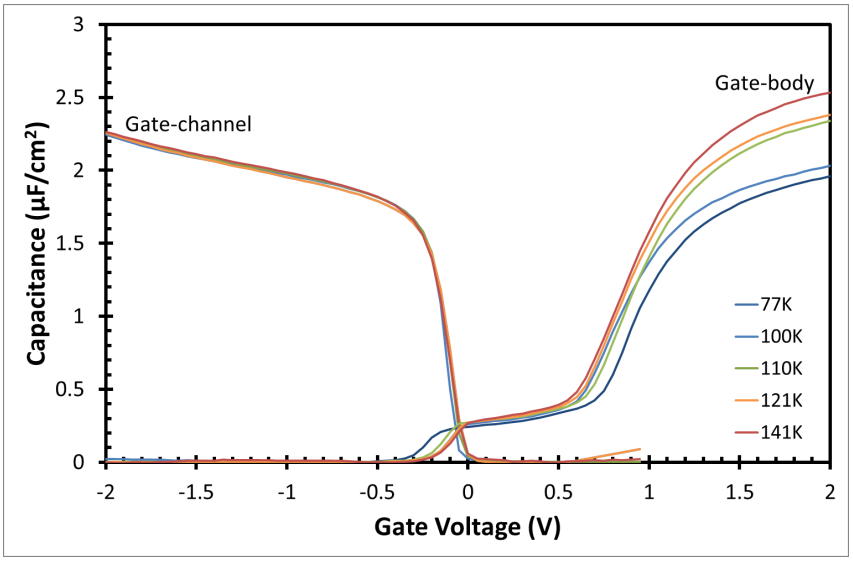


Figure 4.8: Capacitance characteristics used to extract the oxide thickness at different temperatures. The CV curves were obtained using the split-CV techniques.

with these dimensions, for all the wafers measured.

The mobility was extracted using the split CV technique see Figure 4.8. We found difficult to extract good gate-body CV characteristics at 77 K. Figure 4.9 shows the variation of the oxide capacitance for the gate-body and gate-channel branches with temperature. The oxide thickness were extracted from the curves in Figure 4.8. The measurements were taken from 77 K up tp 140 K, since at 110 K it is possible to observe a change in the gate-to-body capacitance. The freeze-out of carriers in the body (substrate) occurs between 100 K and 110 K. The capacitance value of $C_{ox} = 2.3$ μFcm^{-2} means that the devices have been fabricated with an EOT of 1.5 nm, which is close to the design specification of 1.2 nm shown in Figure 4.3. The slight discrepancy may be due to slightly thicker layers having been deposited or due to some mixing between the SiO_2 and HfO_2 at their interface to produce a region of $HfSiO_4$ with a dielectric constant of around 11 instead of 25.

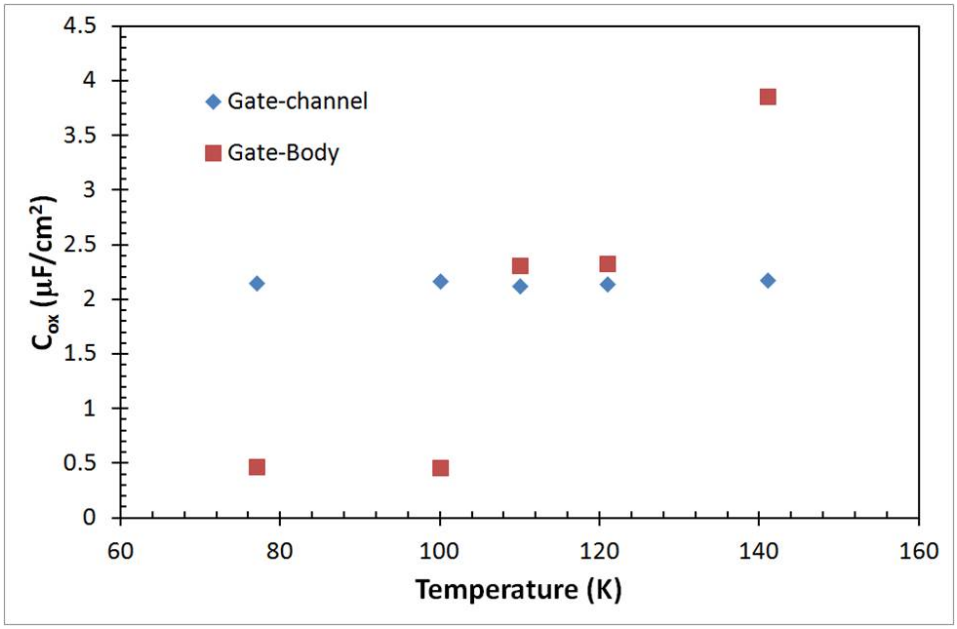


Figure 4.9: Oxide capacitance extracted from the gate-channel and gate-body branches of the split CV taken at different temperatures.

From the gate-to-body is extracted the depletion charge used in calculating the effective field. Since it is not possible to obtain reliable C_{GB} curves, in the next sections the mobility will be plotted as function od inversion charge.

4.2.1 Effect of passivation.

First, the effect of surface passivation will be studied on the relaxed Ge wafers. Mitard *et al.* [88] has shown that reducing the passivation temperature from 500° C to 350° C reduces the incorporation of Ge in the Si cap, so from the point of view of scalability this passivation scheme is favourable [42]. Also, the Si cap thickness plays an important role, it has been shown that for a thickness lower than 8 MLs the peak mobility increases with the thickness and this is independent of the precursor used. [89]. In addition, low process temperatures avoid the strain relaxation expected at 500° C.

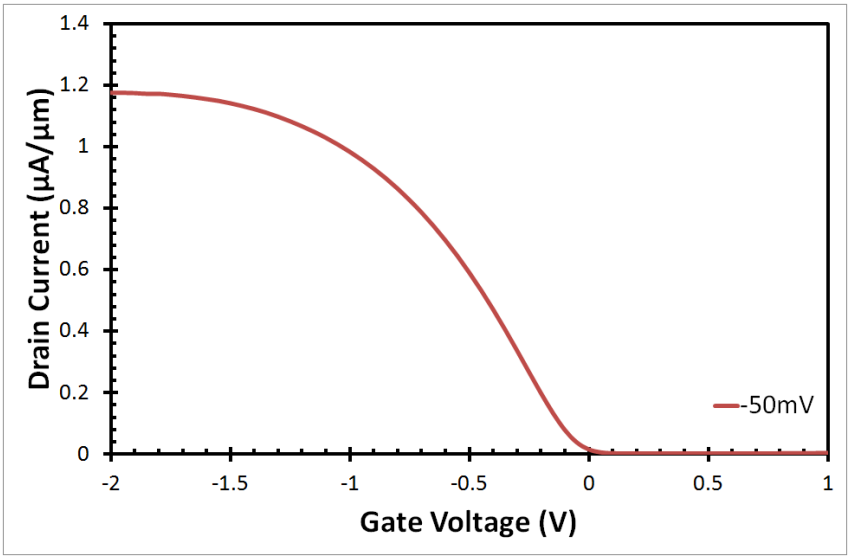


Figure 4.10: Linear drain current taken for wafer with rGe layers and Si_3H_8 passivation scheme. The measurements were taken at room temperature.

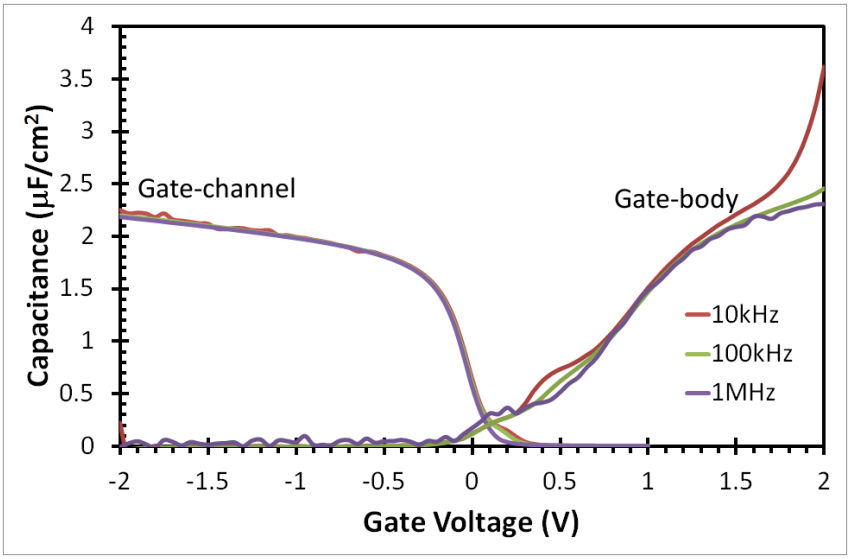


Figure 4.11: Capacitance characteristics in function of frequency for wafer with rGe layers and Si_3H_8 passivation scheme. Both the gate-channel and gate-body branch are shown. A small bump can be seen in the depletion region as indicated by the arrow. The measurements were taken at room temperature.

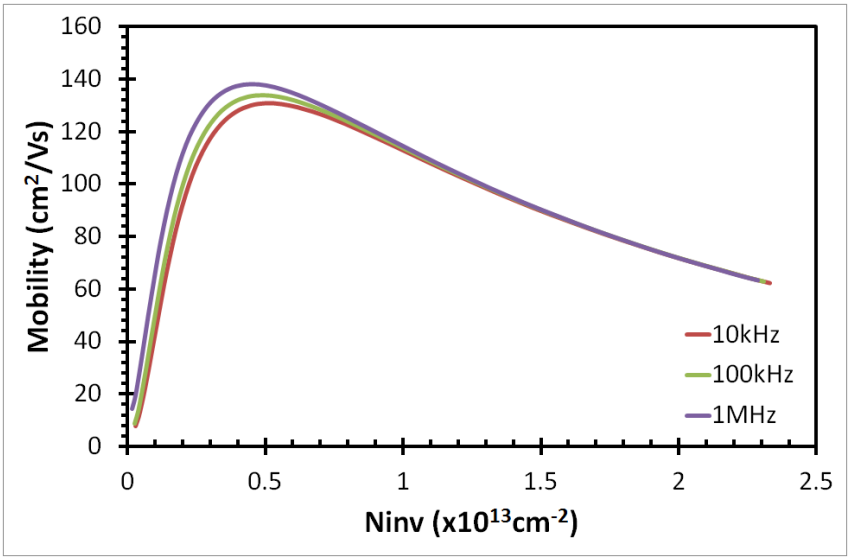


Figure 4.12: Effective mobility extracted for wafer with rGe layers and Si_3H_8 passivation scheme. The measurements were taken at room temperature.

The effective mobility was calculated using CV curves taken applying a constant drain voltage, V_{DS}, equal to -50 mV.

Figures 4.10, 4.11 and 4.12 show the typical room temperature behaviour for a device in wafer DO4 which consists of rGe layers with the Si_3H_8 passivation scheme. For the gate-channel branch of the capacitance, see Figure 4.11, there is no observable frequency dispersion, although at low frequencies it is possible to observe a bump in the depletion region. The bump disappears at higher frequencies, indicating the presence of interface traps.

Figures 4.13, 4.14 and 4.15 show the typical room temperature behaviour for devices passivated with SiH_4 (Wafer D05). No frequency dispersion is observed in accumulation; also in the depletion region we do not observe a bump which is an indication of a well passivated surface, see Figure 4.14. The gate-body branch of the capacitance shows more noise than for the rGe wafer with Si_3H_8 passivation scheme at lower frequencies. It is possible to observe

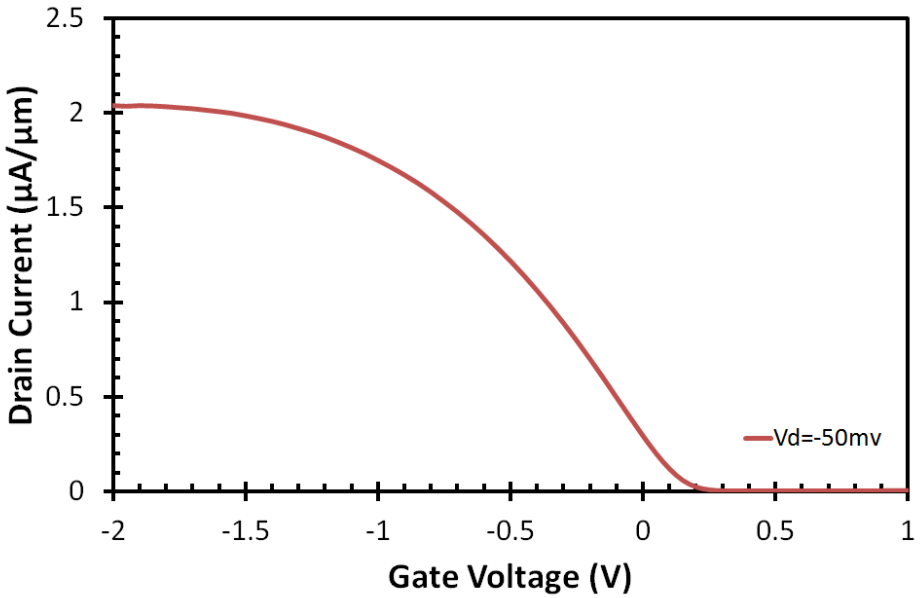


Figure 4.13: Linear drain current taken for wafer with rGe layers and SiH_4 passivation scheme. The measurements were taken at room temperature.

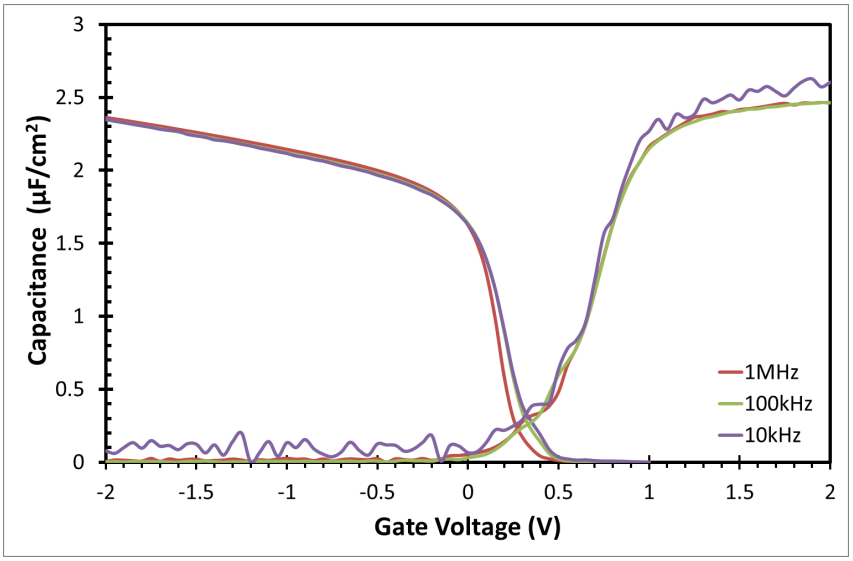


Figure 4.14: Capacitance characteristics in function of frequency for wafer with rGe layers and SiH_4 passivation scheme. The measurements were taken at room temperature.

frequency dispersion in the extracted mobility at low inversion charge density.

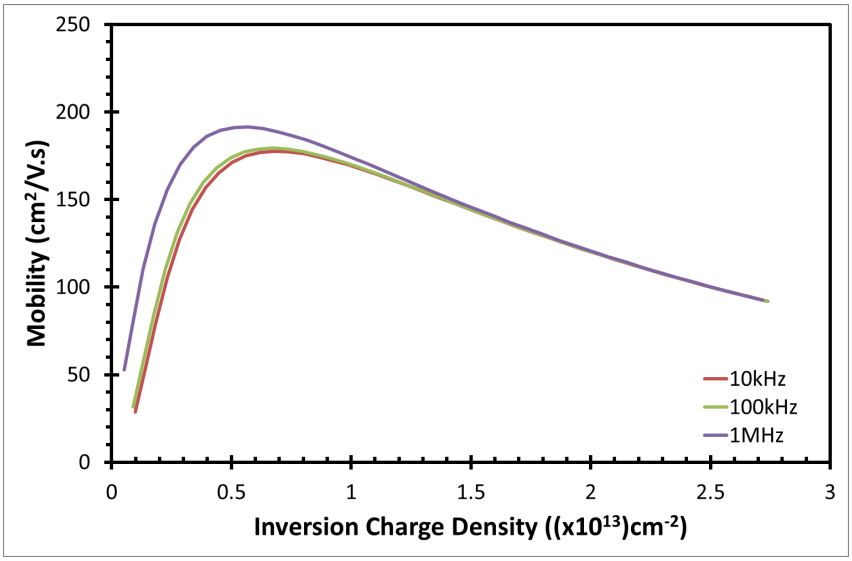


Figure 4.15: Effective mobility extracted for wafer with rGe layers and SiH_4 passivation scheme. The measurements were taken at room temperature.

From a comparison of the room temperature results for wafer DO4 and DO5, taken for a drain voltage of -50 mV and 1 MHz, we see that passivation with SiH_4 shows a 74% higher drain current at a gate voltage of -2 V. This translates into an enhancement in mobility both at low and higher charge density, see Figure 4.16, with a 36% enhancement for the SiH_4 passivated wafers at the peak mobility. This higher mobility may be a result of more effecitve passivation of the surface states in the higher temperature process. It should also be borne in mind that the SiH_4 passivation process is very well established, whereas the Si_3H_8 process was fairly recently developed in IMEC at the time these devices were fabricated so may not have been fully optimised.

At 77 K, the difference in mobility becomes more pronounced, reaching 50% higher at the peak for SiH_4 passivation. Figure 4.17 shows the drain current at room temperature and 77 K for the two types of wafer on a logarithmic scale that allows the subthreshold region to be seen more clearly

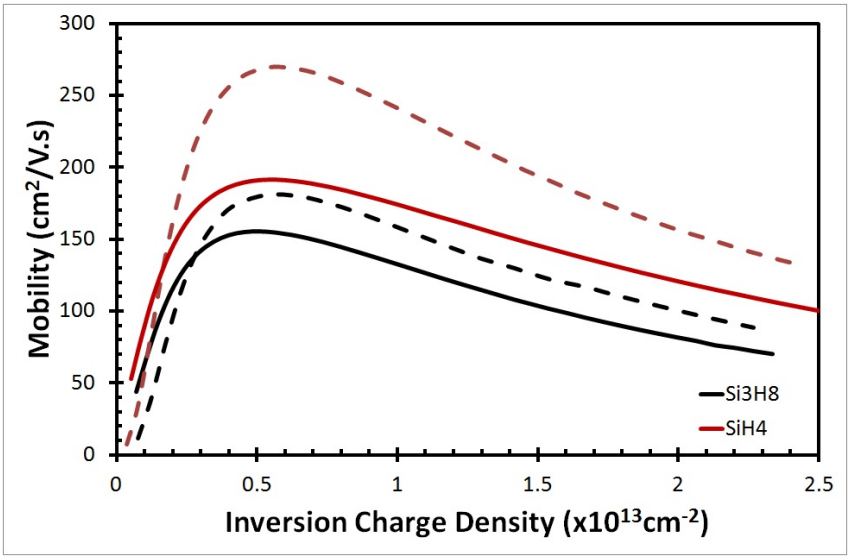


Figure 4.16: Effective mobility in function of the inversion charge for devices with different passivation methods. Solid lines represent room temperature data and dashed lines represent data taken at 77 K.

than in the linear plots. The I_{on}/I_{off} ratio is observed to increase for both devices as they are cooled and a decrease in subthreshold slope is seen, as expected. At 77 K, the off-current for the Si_3H_8 passivated devices is lower then for the SiH_4 passivation and the subthreshold slope is marginally better at 28 mV/dec, compared to 36 mV/dec (at 77 K the ideal slope is 15 mV/dec). At 300 K both devices show significant leakage and only manage subthreshold slopes of 121 mV/dec and 117 mV/dec, respectively (compared to the ideal of 60 mV/dec).

The remaining results reported in this Chapter are for Si_3H8 passivated devices, because they include strained Ge layers for which the lower thermal budget of 350°C used in this passivation scheme compared to 500°C for SiH_4 passivation will be less likely to initiate strain relaxation. However, it should be remembered that this scheme did produce devices with a significantly lower mobility, so the actual mobility values reported in the following may represent

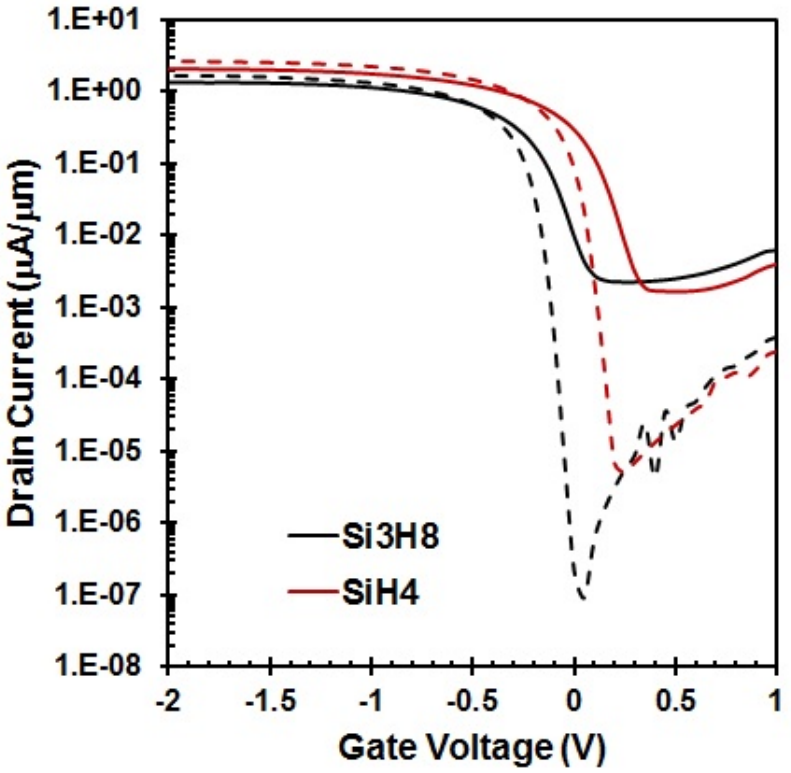


Figure 4.17: Drain current as a function of gate voltage for devices with different passivation methods. Solid lines represent room temperature data and dashed lines represent data taken at 77 K.

a lower limit of what is possible in a fully optimised passivation scheme.

4.2.2 Effect of sGe channel thickness.

The devices used to obtain the following results differ in the thickness of their strained Ge channel: 10 nm, 20 nm, 30 nm and 40 nm. The graphs also show devices from the control wafer: relaxed Ge with the same Si_3H_8 cap passivation.

Figure 4.18 shows the drain current for devices with different sGe channel thickness, measured at room temperature. The drain current curves show that all the strained Ge devices performed better than the relaxed Ge control,

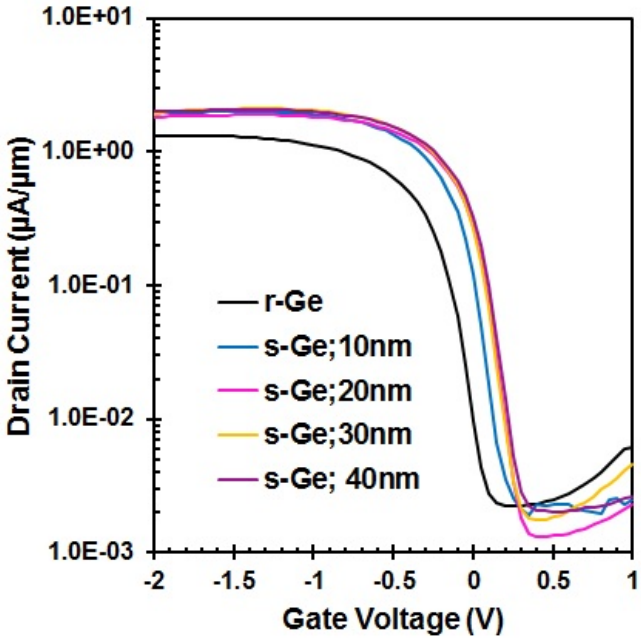


Figure 4.18: Drain current for different channel thickness taken at room temperature.

with higher I_{on} and lower I_{off} leading a slightly improved subthreshold slope of 100 mV/dec and a threshold voltage shift of +0.2 V. There is not a significant difference between the different channel thickness, although the I_{on}/I_{off} ratio is highest for a channel thickness of 20 nm; similarly, the variation in threshold voltage and subthreshold slope is small. The peak mobility (Figure 4.21) is highest for devices with higher channel thickness, namely 30 nm and 40 nm, and reaches 316 cm^2/Vs.

Decreasing the temperature to 77 K leads to a diminished subthreshold slope, but again the variation between the different channel thickness is not significant. Decreasing the temperature leads to an increase in mobility of almost 50%, although this increases diminishes for higher charge densities, see Figure 4.21. An increase in mobility of up to a factor of 3.7 is observed for the strained Ge devices when compared with the relaxed Ge. The mobility

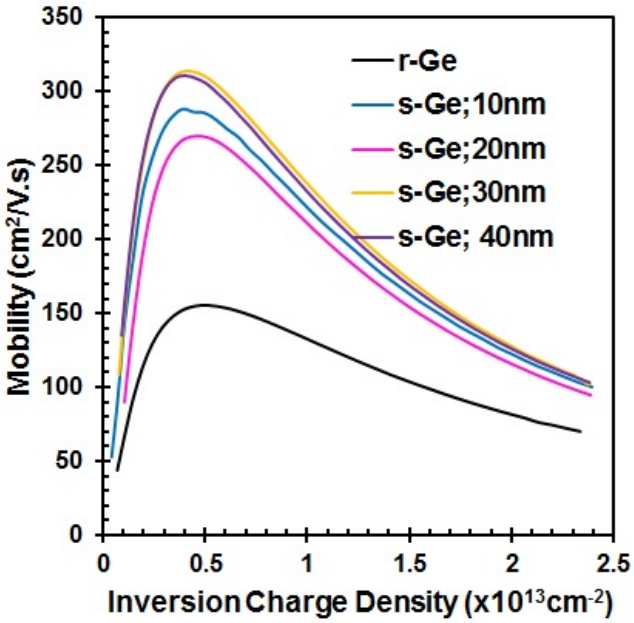


Figure 4.19: Effective mobility for different channel thickness taken at room temperature.

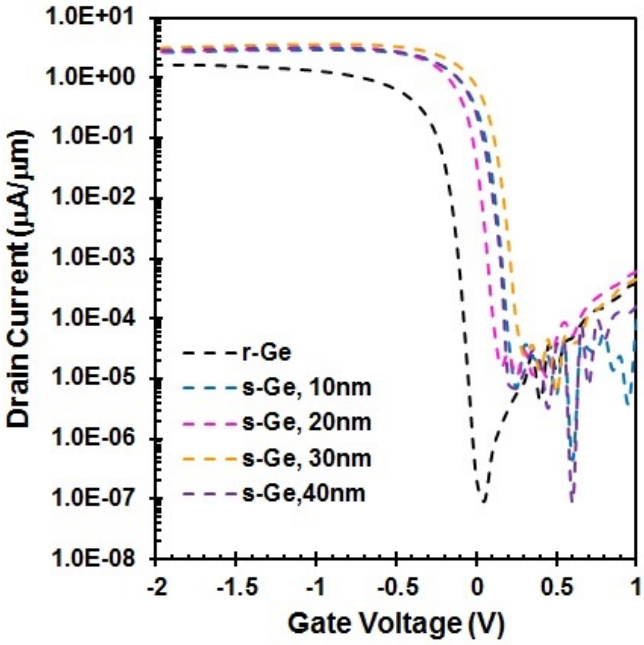


Figure 4.20: Drain current for different channel thickness at 77 K.

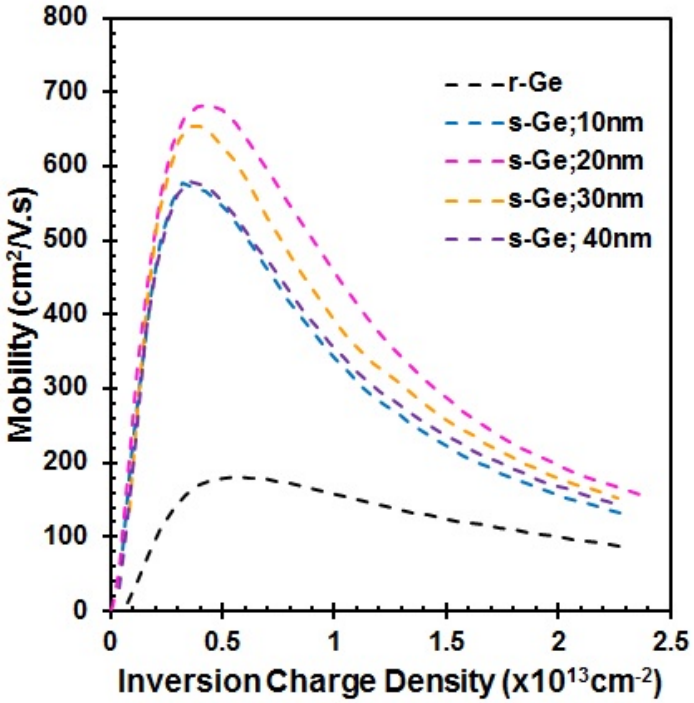


Figure 4.21: Effective mobility for different channel thickness at 77 K.

increase is again observed both at low and high charge densities. At a charge density of 5×10^{12} cm^{-2} a mobility of around 660 cm^2/Vs is obtained for devices grown with a channel thickness of 30 nm.

The equilibrium critical thickness for a sGe channel grown on a $Si_0.2Ge_{0.8}$ buffer is 20 nm [90]. For sGe thickness much greater than the critical thickness mobility degradation might be expected due to dislocations formed during relaxation. However, from this data the mobility in the 40n m channel is only slightly less than in the 20 nm channel. This suggests that within these devices the Ge remains fully strained in a metastable condition. For narrower sGe layers the mobility might also be expected to reduce due to greater scattering off the lower interface, and for very thin layers the carrier confinement would be weaker. Again there is only a small drop in mobility for the 10 nm

layer, which suggests that these mobility reducing effects are not too serious for this thickness.

4.2.3 Effect of doping.

The devices used in this section have a channel thickness of 10 nm and vary in the level of doping in the relaxed SiGe layer below the channel: no doping, 1×10^{17} cm^{-3} and 5×10^{17} cm^{-3}. Also, devices from control wafer were employed, having the Si cap passivated with Si_3H_8. Only room temperature measurements were taken for these samples.

Figure 4.22 shows the drain current for devices with different doping. The curve for the device with highest doping shows a marginally higher I_{on}/I_{off} ratio. However, the subthreshold slope does not vary much with the doping. Again, it is above the ideal 60 mV/dec. The threshold voltage increases slightly with doping concentration.

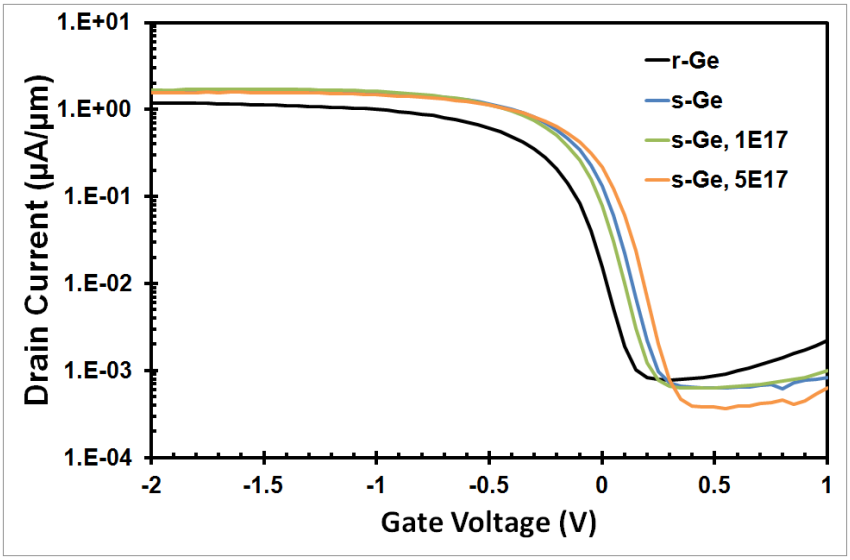


Figure 4.22: Drain current for different doping concentrations taken at room temperature.

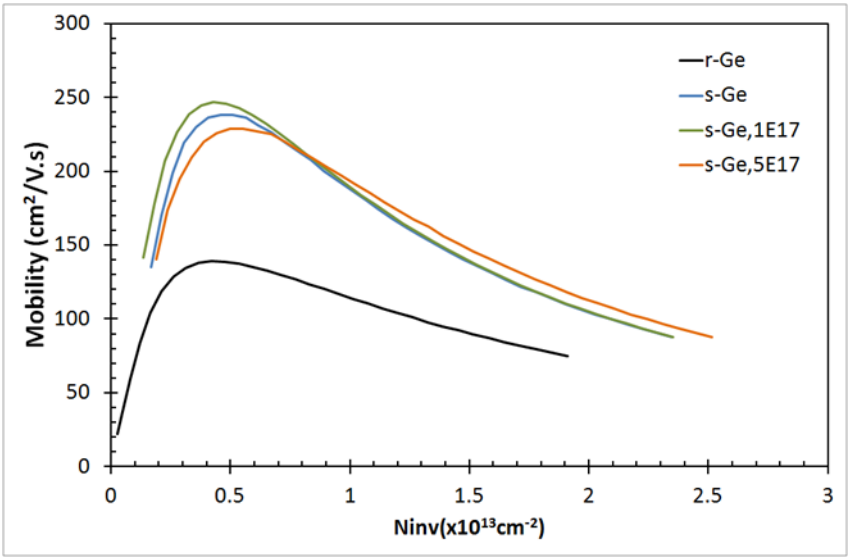


Figure 4.23: Effective mobility for different doping concentrations taken at room temperature.

Figure 4.23 shows that the sGe device doped at 1×10^{13} cm^{-3} has a 4% higher mobility than the undoped sGe device at low carrier concentration, peaking at around 250 cm^2/V.s, and its mobility remains at least as high over the full density range studied. By contrast, the more highly doped sample, at 5×10^{17} cm^{-3}, has a lower peak mobility, but at high charge densities the mobility is slightly higher which would be advantageous for increased on-current.

4.3 Series Resistance

Measurements of the mobility for the devices discussed in Section 4.2.2 were also made at 4 K, but there was no significant increase in mobility over the values measured at 77 K. This may be a consequence of a high series resistance. In order to determine this series resistance, the method described in section 3.3.3.2 was applied. As can be seen from Figure 4.24 it was not possible to find a point where all the lines intercept. After applying the correction the

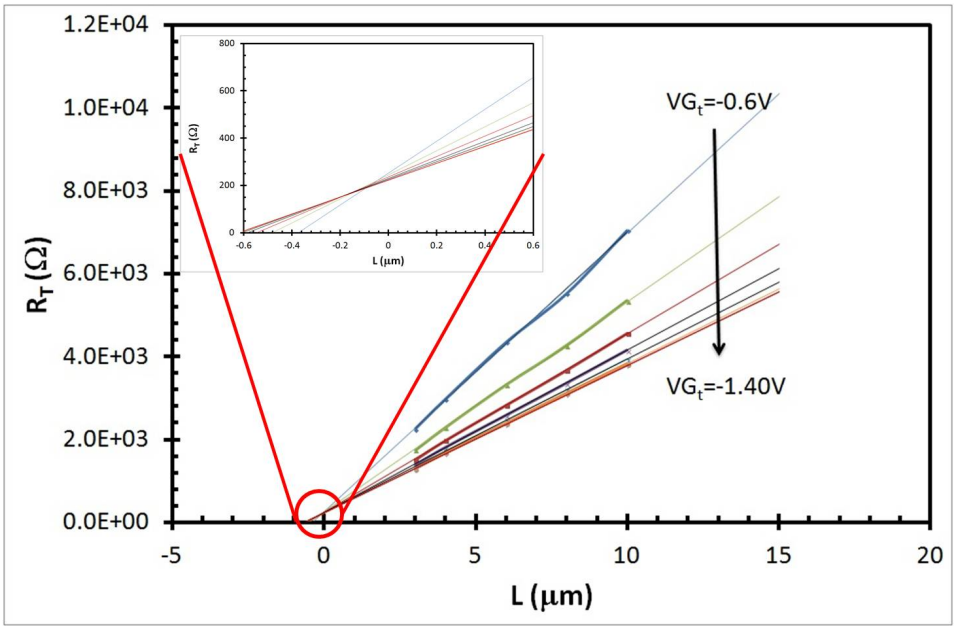


Figure 4.24: Determination of series resistance by the method described in section 3.3.3.2.

linear extrapolation of the lines does not allow ΔL and R_{SD} to be determined accurately.

Therefore, another method is necessary to determine the series resistance. Assuming the device is in strong inversion the drain current can be defined by

$$I_D = \frac{WC_{ox}}{L}.\frac{\mu_0}{[1+\theta\,(V_G - V_t)]}.\,(V_G - V_t)\,.V_D \tag{4.1}$$

where W and L are the effective channel width and length, C_{ox} is the gate oxide capacitance, μ_0 is the low field mobility, θ is the mobility reduction coefficient, V_t is the threshold voltage. The transconductance can be obtained by differentiating equation 4.1:

$$g_m = \frac{W}{L}.C_{ox}\frac{\mu_0}{[1+\theta.\,(V_G - V_t)]^2}.V_D \tag{4.2}$$

Ghibaudo developed a model in which the mobility dependence with gate voltage is eliminated [91]. This can be achieved by creating a new function Y which is constructed using the above equations:

$$Y = \frac{I_D}{\sqrt{g_m}} = \left(\frac{W}{L} C_{ox} \mu_0 V_D\right)^{1/2} (V_D - V_t) \tag{4.3}$$

According to [91], the new Y-function is linear with gate voltage, so by plotting the function against gate voltage it should be possible to determine the low field mobility from the slope and the threshold voltage by the intercept. However, the Y-function is not linear, in devices with thin oxides the effect of surface roughness is always present which breaks the linearity of the Y-function. An attenuation factor, Θ_2, needs to be introduced. Fleury *et al˙* [92] took this into consideration and redefined the Y-function as

$$Y = \sqrt{\frac{\beta V_D}{1 - \Theta_2 V_{Gt}^2}} V_{Gt} \tag{4.4}$$

with Θ_2 defined as

$$\Theta_2 = \frac{\theta_2}{1 + \theta \Delta V_{th}^2} \tag{4.5}$$

Based on this new model Fleury *et al.* developed an iterative method to extracted device parameters. The extraction is done in three steps: 1) a recursive method to extract β and V_{th}, 2) determination of Θ_1 and Θ_2, 3) extraction of ΔV_{th}.

Since the standard method did not give reliable results, this new method was tested. The initial parameter given, V_{th} was determined using the method described in section 3.3.1 to be $(0.06 \pm 0.0.3)$ V for devices in wafer D04. This, also, did not give us a reliable result since the final threshold voltage given by

the recursive method converged on a higher value than initial input, that is 0.11 V, thus invalidating the method.

Since the previous methods did not gave reliable result for the threshold voltage, the zero-length transistors in the chip were employed, see section 3.3.3.2. Applying this method it was possible to obtain a straight line, see Figure 4.25. However this method does not take into consideration the contribution of the highly doped regions, so the values obtained are an under estimation of the series resistance.

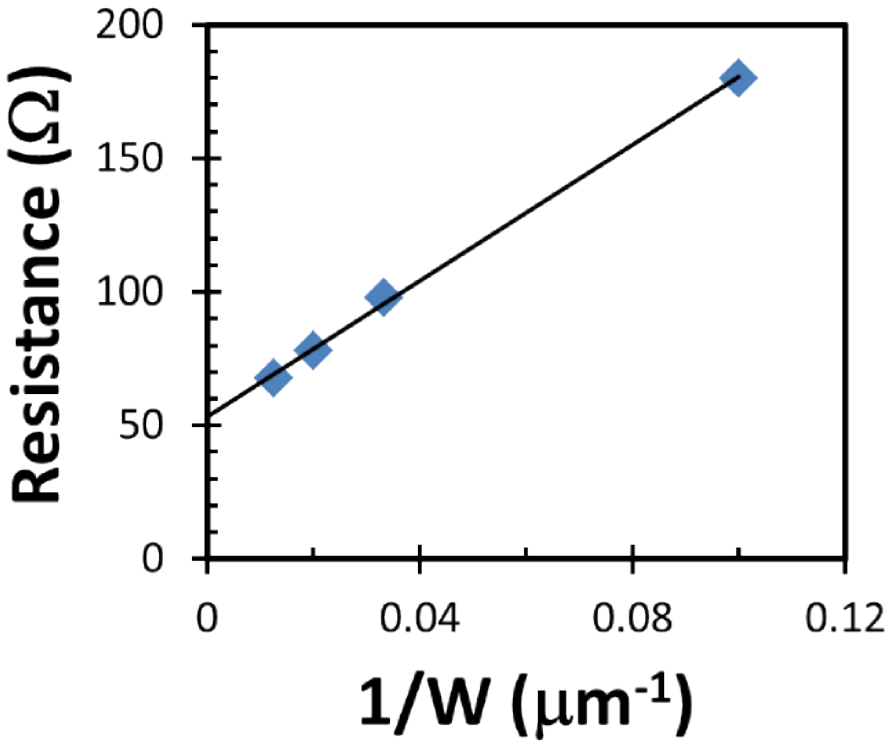


Figure 4.25: Plot for series resistance determination from W^{-1} method for devices in wafer D04 at room temperature.

4.4 Conclusion

In summary, the effects on the performance of Ge pMOSFET of passivation scheme, channel thickness and doping were studied in this chapter.

The passivation scheme with SiH_4 presented better results than using Si_3H_8, showing an enhancement in mobility at both low and high charge density of factors 1.3 to 1.7. However, from the point of view of scalability, Si_3H_8 is still a passivation scheme to consider. The lower process temperatures allow for limiting the Ge segregation in the Si cap, on the other hand it is the low temperatures that are responsible for generating the defects which causing the lower performance observed [93].

There is a large increase in mobility when comparing between relaxed and strained Ge, which is approximately 50% at low charge density and at high charge density decreases to around 30%. However, we do not observe a significant variation with channel thickness for the sGe devices. Since the mobility change in this channel thickness region is not significant it can be deduced that surface roughness is the limiting factor in mobility [94]. Again, a significant difference is not observed with different doping levels of the sGe devices, although there is a slight increase when the doping is increased. For higher doping concentrations the mobility limiting factor is Coulomb scattering [95].

When calculating the series resistance of the devices, traditional methods failed. So, the zero-length transistor method was used. However, this method does not take into consideration the highly doped regions which contribute to the resistance.

Our results show, for these devices, that mobility improvement is sig-

nificant when comparing strained and unstrained Ge layers but that doping level and channel thickness have little impact. A reason for this can be related with defects originating from the formation of source and drain. Also, these devices do not have any source/drain extensions or halo doping to prevent the diffusion of dopants into the channel, which causes poor device performance. In order to improve device performances it would be necessary to better define the source and drain, by implementing halo doping and extensions to the drain and source. Also, germination of the surface has been shown to improve device characteristics.

Chapter 5

High mobility strained Ge QW heterostructures.

Applying strain to Ge layers can improve the performance of devices, both by splitting the heavy-hole and light-hole bands which reduces the carrier scattering rate [96] and by the changed bandstructure leading to a reduced effective mass. The effective mass m^* of charge carriers is an important parameter in determining the kinetic and thermodynamic properties of the conduction system as the carrier mobility is inversely proportional to m^* and it affects the density of states, which in a 2D system is $n_{2D} = m^*/(\pi\hbar^2)$ [97]. The effective mass can be determined from the temperature dependence of the amplitude of Shubnikov-de-Haas (SdH) oscillations [2].

In this work, modulation doped (MOD) heterostructures will be studied, which enable the material properties to be studied in simple devices without the need to create an elaborate gated structure. Modulation doped structures typically consist of an undoped quantum well embedded in layers of semiconductor material with carriers supplied to the quantum well from a doped region that is physically seperated by an undoped spacer layer. A low temperature

hole mobility of above 10^6 cm^2/V.s at a sheet density of 2×10^{11}cm^{-2} has been accomplished in such structures with strained Ge quantum wells [98]. In order to study these structures, magnetotransport measurements were performed in the temperature range 0.3-300 K, with a magnetic field swept from 0 to 12 T in both directions of the field.

5.1 2DHG grown by CVD and MBE.

The first structure studied was a pGeQW/$Si_{0.2}Ge_{0.8}$/Ge/Si(100) MOD heterostructure grown by RP-CVD and SS-MBE, see Figure 5.1, sample 12-28. The reason behind this hybrid growth was to use MBE to create a delta-doped supply layer, because at the time this process could not be done by CVD.

The epitaxial layers from the substrate through the strain tuning buffer and Ge quantum well to the undoped spacer layer were grown using an ASM Epsilon 2000 CVD system in Warwick. A reverse linearly graded (RLG) layer $Si_{0.2}Ge_{0.8}$ buffer of 2.5 μm was grown on a Si substrate, followed by an undoped compressive strained Ge QW layer (20 nm) and undoped $Si_{0.2}Ge_{0.8}$ spacer layer (20 nm). The precursor used was germane (GeH_4).

The B doped δ-layer, the 30 nm undoped $Si_{0.2}Ge_{0.8}$ layer and the undoped Si cap layer (1 nm) were grown in Tokyo using a VG Semicon V80 UHV SS-MBE system.

The epitaxial layers show good structural properties with low RMS surface roughness $\sim$ 2 nm and low TDD $\sim 2 \times 10^6$cm^{-2}. For this structure, a Hall mobility of $90,000$ cm^{2}V^{-1}s^{-1} and carrier density of 5×10^{11}cm^{-2} were recorded at 3 K [85, 99].

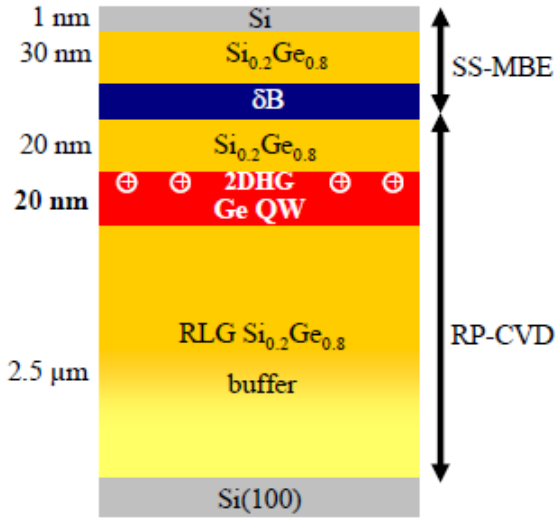


Figure 5.1: Schematic diagram of sample 12-28. The epitaxial layers were grown by CVD and the delta layer doping was grown by SS-MBE. Figure taken from [99]

The magnetic field dependence of the magnetoresistance at for the lowest temperature, 0.316 K is shown as a black line in Figure 5.2, the blue line corresponds to the transverse resistivity or Hall resistivity. The SdH oscillations appear at magnetic fields above 1 T and the oscillation amplitude increases with increasing magnetic field. There is a single series of SdH oscillations, with minima appearing at even integer filling factor ν. From the period of these oscillations, there is a fundamental field of 20.9 T, which corresponds to a hole density of $5.06 \times 10^{11}\text{cm}^{-2}$ (equation 2.28) in agreement with the previous measurements, see Figure 5.3. Figure 5.4 shows the behaviour of the magnetoresistance for different temperatures, as the temperature increases the amplitude of the oscillations decreases and the oscillations start at higher fields. For example, at 7.4 K the first oscillations start at fields around 2.3 T. At 40 K no oscillations are observed. Figure 5.4(b) shows a detail of the SdH oscillations up to 3 T.

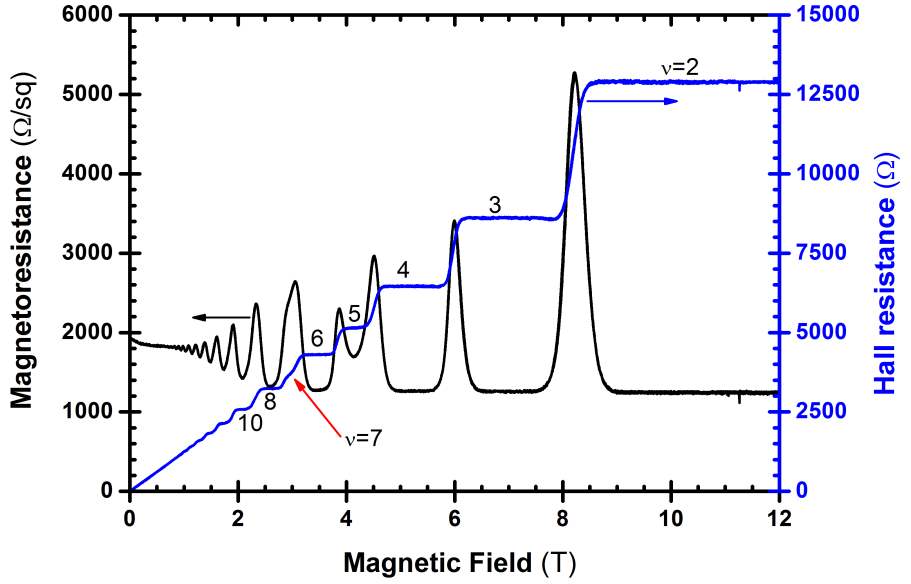


Figure 5.2: Shubnikovde Haas and Quantum Hall Effects at a temperature of 316 mK. Minima in resistivity are labelled with their corresponding filling factors.

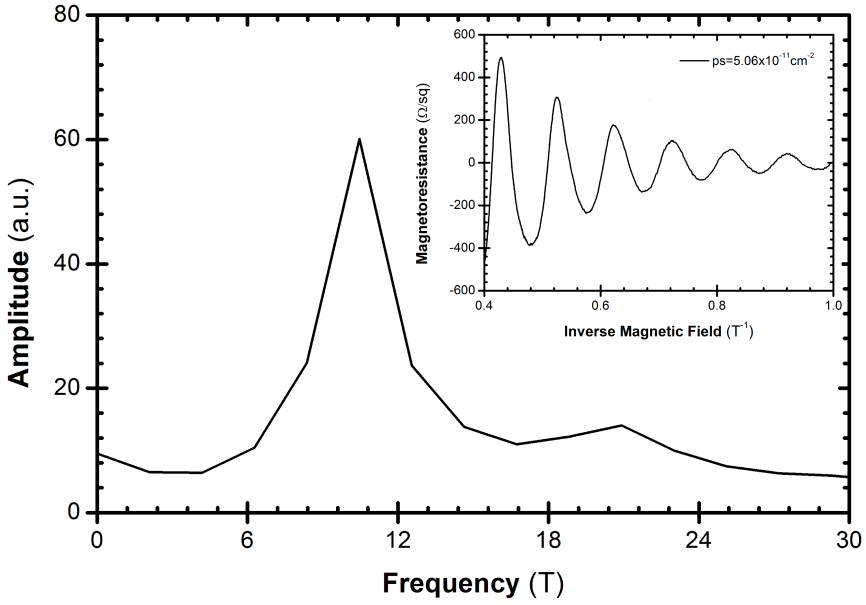
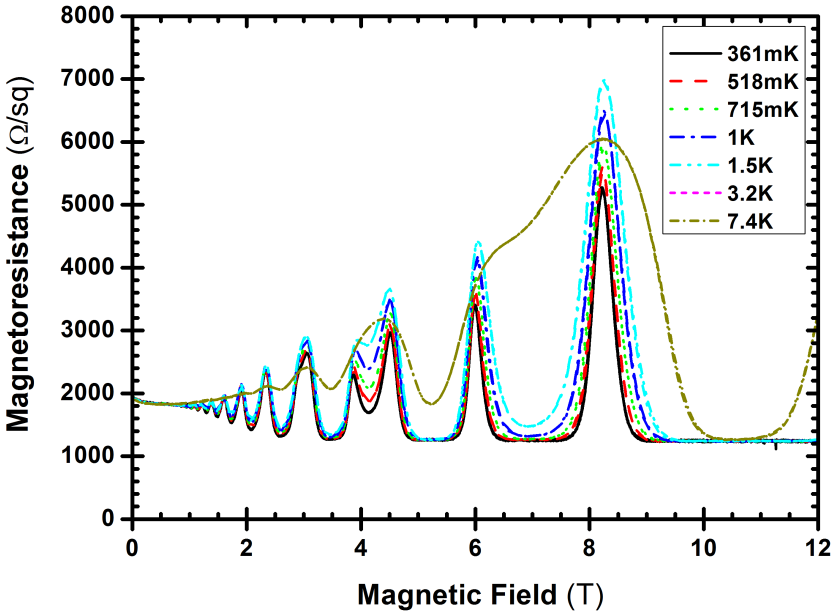
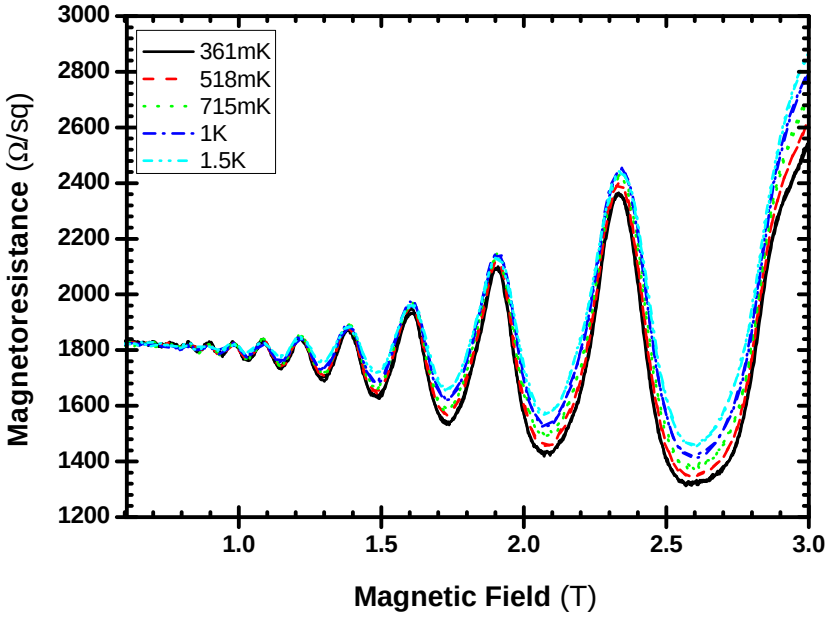


Figure 5.3: SdH oscillations in inverse magnetic field (inset) and their FFT spectrum for sample 12-28 at 316 mK



(a) Magnetoresistance for fields up to 12 T .



(b) Magnetoresistance for fields up to 3 T.

Figure 5.4: Magnetic field dependence of magnetoresistance and spin-splitting dependence with temperature.

At $B > 4\ T$ (Figure 5.5) spin-splitting is observable in the SdH oscillations, with SdH minima now also appearing at odd integer filling factors. As the temperature increases the effect becomes less pronounced, at T = 3.2 K the spin-split minima are no longer observable (not shown).

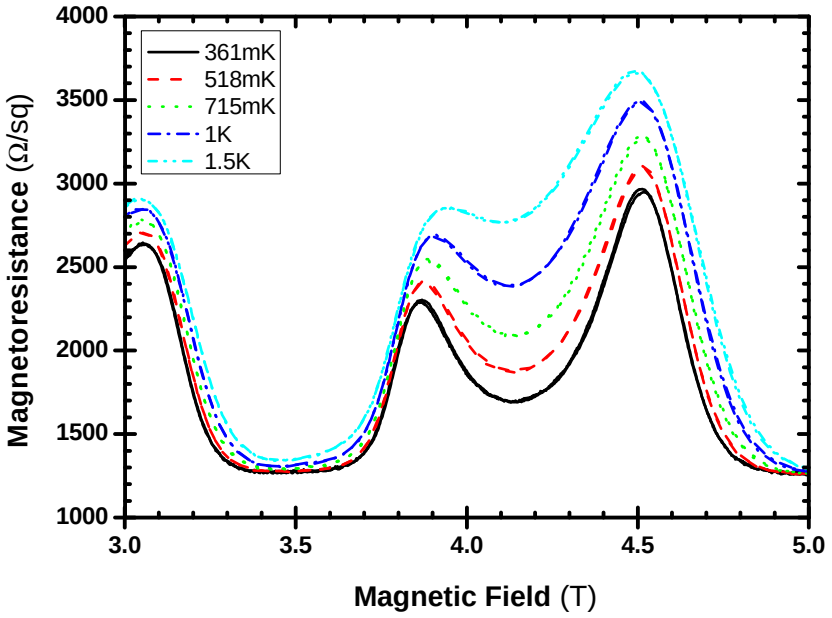


Figure 5.5: Spin-splitting dependence on temperature with temperature.

Figure 5.6 shows the Hall resistance as a function of magnetic field and temperature. Very clear quantum Hall effect plateaus are seen at integer filling factors ν with resistance values of R_k/ν, where $R_k = h/e^2$ is the Klitzing constant of $25,813\ \Omega$, named after the discoverer of the integer quantum Hall effect. At the highest magnetic fields the spin-degeneracy of the Landau level energy spectrum is resolved, with odd-integer plateaus seen around 4.2 T and 7 T, corresponding to $\nu = 5$ and $\nu = 3$ respectively. There is also an inflexion seen at $\nu = 7$, but no clear plateau. At lower magnetic field the spin-degeneracy is not resolved and only even integer plateaus are seen. The

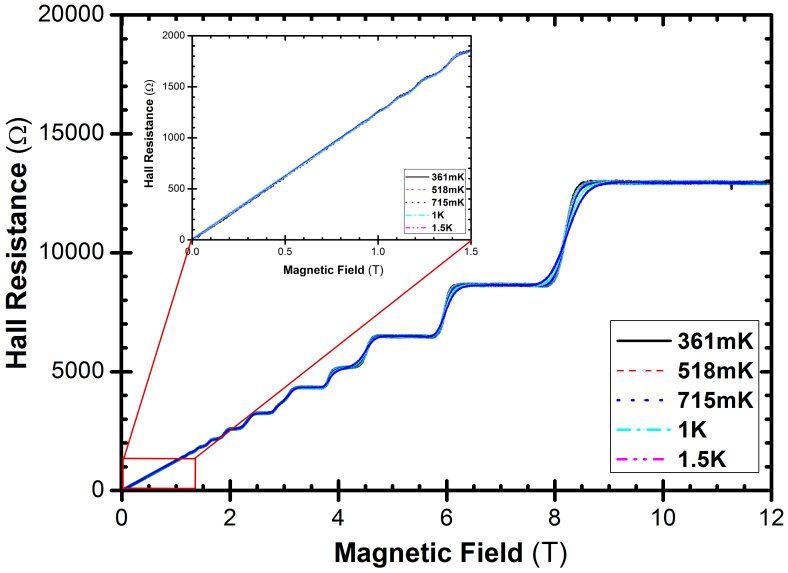
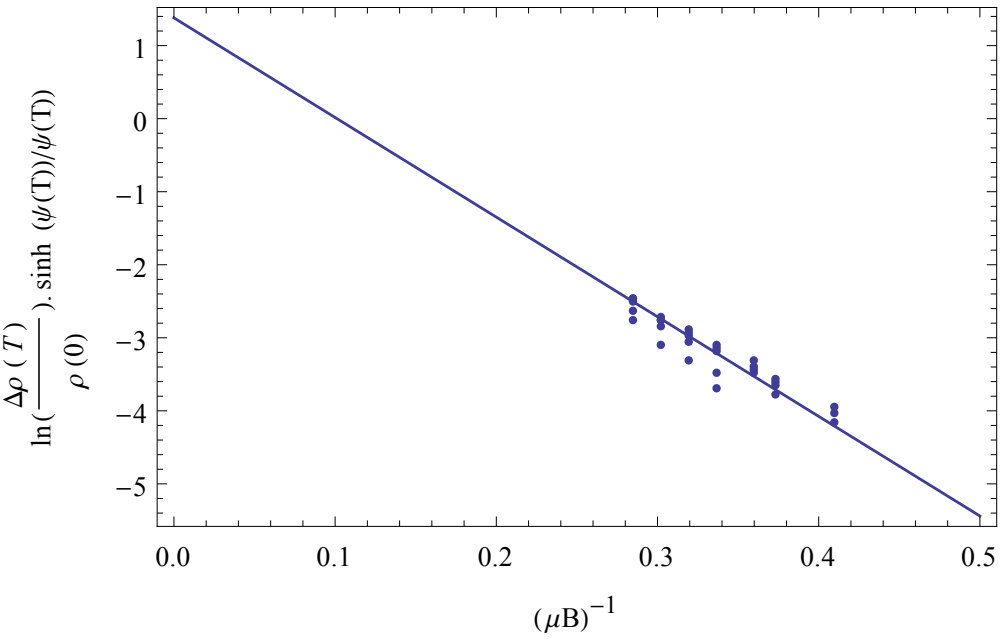


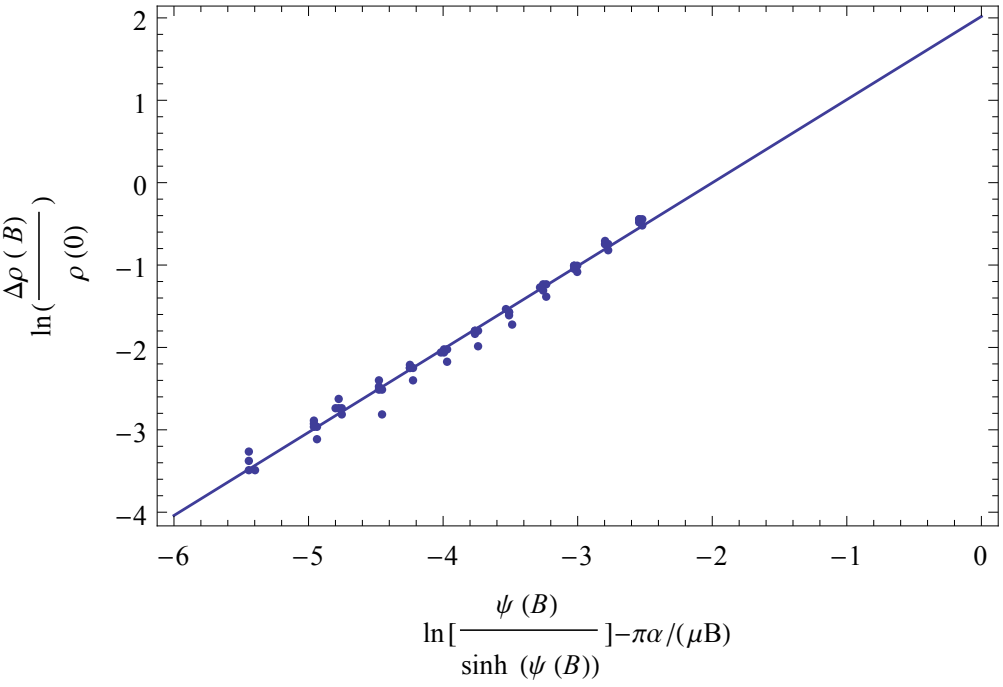
Figure 5.6: Magnetic field dependences of Hall resistance measured at different temperatures. In the inset is shown the linear region of the Hall resistance.

plateaus observed disappear with increasing temperature in a similar way to the SdH oscillations. The inset of figure 5.6 shows that the linear region of the Hall resistance goes up to B=1 T. By performing a linear fit on this region is possible to determine the Hall coefficient $R_H = 1251\ \Omega/T$, which corresponds to a density of $5.00 \times 10^{11}\text{cm}^{-2}$, as found from the SdH positions.

The linear variation of Hall resistance at low magnetic field, well developed quantum Hall plateaus at high magnetic field, and single series of SdH minima at integer filling factor all point to conduction from a single 2D channel of high mobility charge carriers. The excellent quality of the data also show that the Hall bar geometry is well constrained and the contacts are do not introduce any spurious signals - this was ensured by inspection of the sample under a microscope and scratching to remove possible leakage paths round the contacts.



(a)



(b)

Figure 5.7: Plots for self-consistent extraction of effective mass m^* and parameter α for different temperatures (a) and magnetic fields (b).

From the magnetoresistance measurements, a value for the hole effective mass can be extracted using the self consistent method described in Section 3.3.7 [81]. For this method, only SdH oscillations that are approximately sinusoidal can be used, which restricts the analysis to lower B/T before peak sharpening and spin-splitting occur. Figure 5.7 shows the plots with the best fit for an effective mass of $m^* = (0.085 \pm 0.02)\ m_0$ (equation 3.40) and a transport to quantum scattering time ratio α of 4.34 ± 0.02 (equation 3.41). The Dingle plot shows a straight line with an intercept at 1.38 ($\log 4$) which is in accordance with the theory [61]; this is related to the broadening of the Landau levels.

5.2 Heterostructures grown by CVD.

Heterostructures grown entirely by CVD have also been studied. A typical layer configuration for these structures is shown in figure 5.8.

Si cap	2 nm
$SiGe_{0.8}$ cap	30
B (2e18 cm^{-3}) :$SiGe_{0.8}$	10
$SiGe_{0.8}$ spacer	20
Ge QW	20
$SiGe_{0.80}$	600
$SiGe_{0.85\text{-}0.80}$	250
$SiGe_{0.90\text{-}0.85}$	250
$SiGe_{0.95\text{-}0.90}$	250
$SiGe_{1.0\text{-}0.95}$	250
Ge	600
Si (100)	

Figure 5.8: Schematic cross-section of sample 12-131.

The different epilayers were grown using the ASM Epsilon 2000 CVD

system in Warwick. A relaxed Ge layer of approximately 600 nm was first grown on a Si(100) wafer, followed by a reverse linearly graded strain relaxed $Si_{1-x}Ge_x$ buffer, an undoped constant composition layer of $Si_{1-x}Ge_x$, an undoped compressive strained Ge quantum well (QW) layer, an undoped $Si_{1-x}Ge_x$ spacer layer, a Boron doped $Si_{1-x}Ge_x$ supply layer, an undoped $Si_{1-x}Ge_x$ cap layer and finally a Si cap at the surface. In order to grow the layers the standard precursors GeH_4 and Si_2H_6 were used.

5.2.1 Structural analysis.

The grown structures present a relatively low RMS surface roughness of around 2nm and low threading dislocation density at the top surface of around $2 \times 10^6 cm^{-2}$ [25].

Figure 5.9: Cross-section TEM of sample 12-447.

Figure 5.9 shows a cross-section TEM of one of these Ge QW MOD

heterostructures, wafer 12-447. It can be seen that dislocations stop at the top of the reverse linearly graded buffer layer with the remaining layers being smooth and defect-free. The Ge QW was measured to be 22 nm and does not show a rough interface.

5.2.2 Hall Bar fabrication.

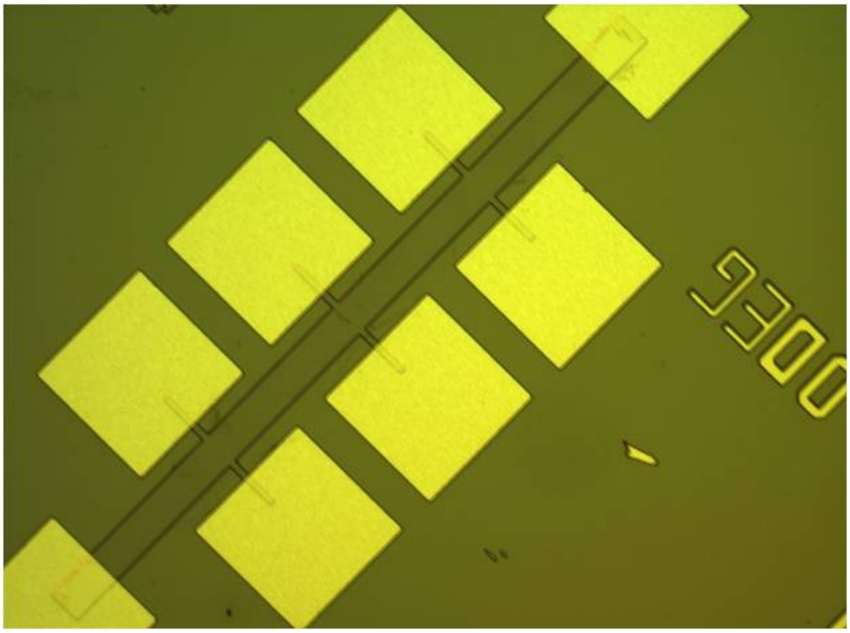


Figure 5.10: Hall bar fabricated for magnetoresistance measurements.

In order to study the magneto-transport properties of these structures Hall bar devices were fabricated in a clean room using optical lithography following the process described in subsection Section 3.1.3 (see Figure 5.10). In order to clean the sample, the surface is cover with primer for 10 s. Next it was+ covered with negative photoresist (AZ5124E) and spun for 35 s at 4000 rpm followed by a spread at 0.1 s at 1600 rpm. The sample is then baked for 1 minute at 115°C. It then undergoes an exposure of 6s followed by a reverse bake at 120°C for 2 minutes and a flood exposure of 10 s. The developer used

was MF319 for 1 min and a 10 s rinse. Prior to Al evaporation, the sample undergoes plasma ashing so as to remove leftover photoresist followed by a 2% HF dip. The Al evaporated should cover all the sample and then lift-off is performed in order to reveal the pattern. In a second phase, positive photoresist is applied (S1813), spun for 2 s at 500 rpm and spread for 7 s at 4000 rpm. It undergoes a 10 s exposure and is developed to leave the Hall bar defined in resist. The final step of the lithography process is etching to isolate the Hall bar. Dry etching is used for these samples to give an anisotropic profile, it shows good results for small features. These samples were etched right down to the substrate, to avoid parasitic conduction paths through the virtual substrate, as confirmed by the height profile shown in Figure 5.11.

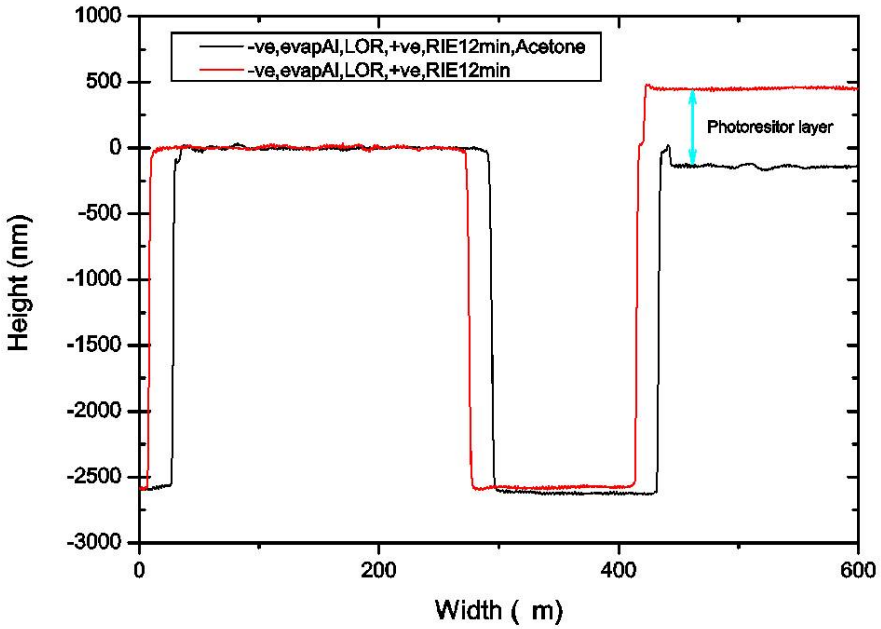


Figure 5.11: Profilemeter graph after samples undergo dry etching.

5.2.3 Mobility measurements.

The samples were measured in the closed-cycled cryostat by performing Hall and resistivity in the temperature range 10 K to 300 K. At low temperatures the values for Hall mobility and sheet carrier density are related to carriers in the 2DHG located in the quantum well [100], whilst at higher temperatures other parallel conducting channels appear.

Figure 5.12 shows the Hall mobility and carrier sheet density of sample 12-131 as function of temperature. Below 77 K, the hole density starts to saturates at $\sim 3 \times 10^{11}\text{cm}^{-2}$ indicating the presence of a 2DHG in the strained Ge channel. The Hall mobility increases with decreasing temperature to a maximum of $4.8 \times 10^{5}\text{cm}^{2}/\text{Vs}$.

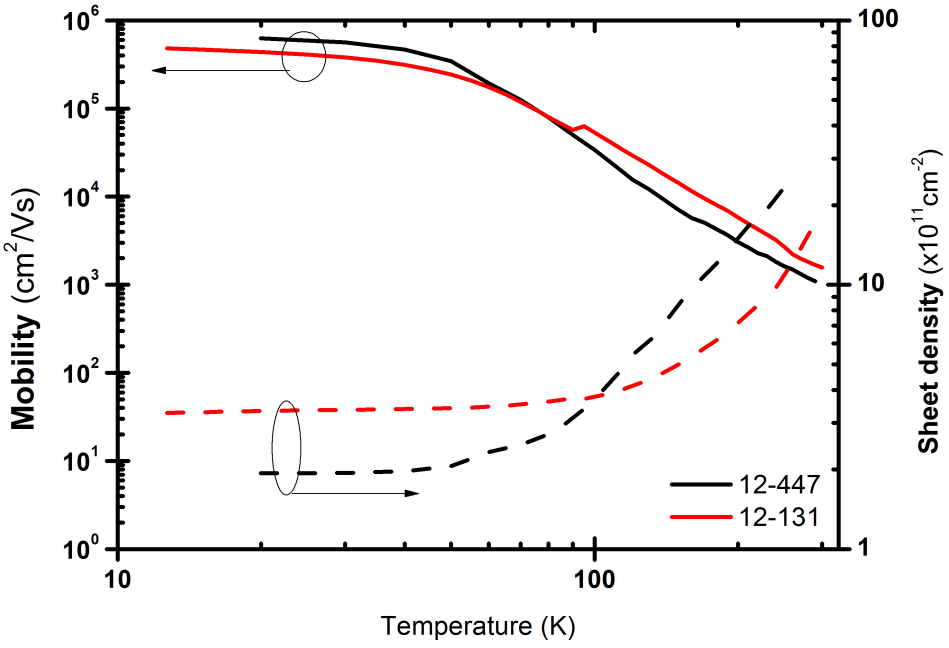


Figure 5.12: Hall mobility (solid lines) and sheet density (dash lines) as a function of temperature for sample 12-131 and 12-447. Both samples were etched until the substrate.

Similar measurements for sample 12-447 are also shown in figure 5.12. In this case, the carrier sheet density saturates, below 77 K, at $1.9 \times 10^{11}\text{cm}^{-2}$ again indicating the presence of a 2DHG in the strained Ge channel. The mobility increases with decreasing temperature to a maximum value of $6.3 \times 10^5\text{cm}^2/\text{Vs}$, but without reaching saturation indicating the possibility of even higher mobility at lower temperatures.

Although the two samples have the same intended layer structure, 12-447 has a 30% lower hole density in the QW than 12-131 and an approximately 30% higher hole mobility. This decrease of mobility with increasing hole density suggests that the mobility in these samples is limited by remote impurity or interface roughness scattering, rather than by background impurity scattering for which the reverse trend would have been seen. The carrier density difference in the quantum well arise from small differences in the actual layer thickness and doping density of the two samples.

At higher temperatures the mobility decreases due to phonon scattering and parallel conduction in the sample, reaching 1093 cm^2/Vs at a total hole density of $30 \times 10^{11}\text{cm}^{-2}$ at 300 K.

5.2.4 Magnetotransport measurements.

The higher mobility sample (12-447) was then measured at lower temperatures, down to 300 mK, in a cryomagnetic system. For a set temperature the field was continuously swept from 0 to 12 T in both directions. Shubnikov-de-Haas were observed from these measurements and several parameters were extracted by applying the method describe in section 3.3.7 [81].

Figure 5.13 shows the magnetoresistance and Hall resistance as a func-

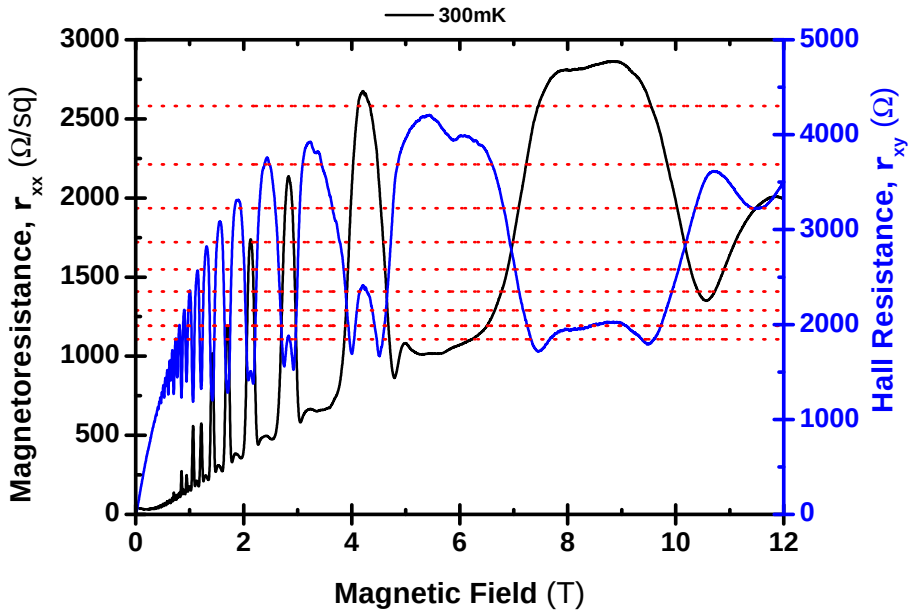


Figure 5.13: Magnetic field dependences of magnetoresistance and Hall Resistance for a measurement at 300 mK. The landau levels are represented in red dotted lines.

tion of magnetic field taken at 300mK. The presence of SdH oscillations are an indication of 2D carrier confinement; however, the shape of these magnetoresistance curves are quite different from those observed in Figures 5.4(a) and 5.6 from sample 12-28: the Hall resistance is not linear in magnetic field, plateaus do not appear for the quantum Hall effect, there is an increasing linear baseline to the magnetoresistance oscillations, and a simple series of integers cannot be applied to all the minima seen. These issues could indicate that there is parallel conduction in this sample, possibly through the B-doped supply layer, or arise from issues of sample or contact geometry that mix the two components of magnetoresistance ρ_{xx} and ρ_{xy}.

The magnetoresistance measurements were made at a range of temperatures. In the low field region, Figure 5.14 shows SdH oscillations are observed

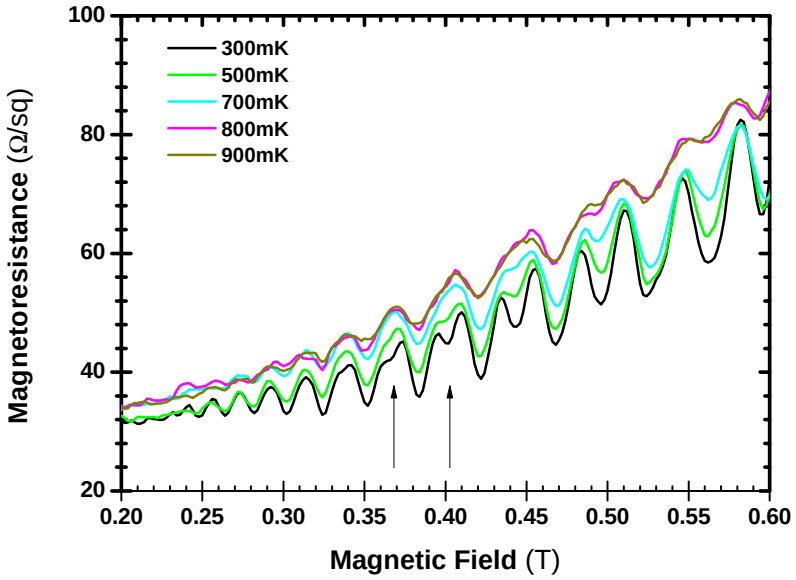


Figure 5.14: Low field SdH oscilations for sample 12-447, measured at temperatures from 300 mK to 900 mK.

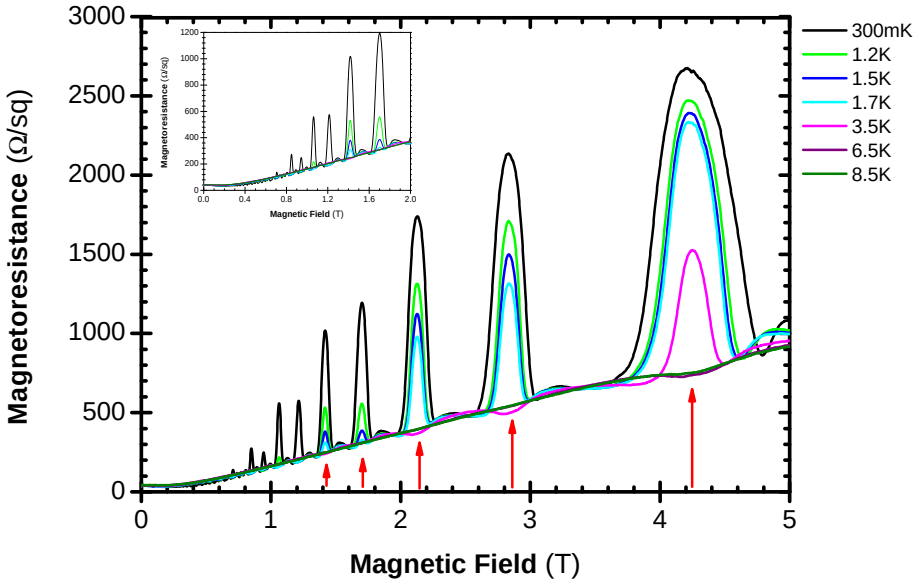


Figure 5.15: Temperature dependence characteristics of the magnetoresistance, measured at different temperatures.

at fields as low as $B = 0.235$ T for the measurement at 300 mK, with spin splitting appearing above $B = 0.36$ T (as indicated by the arrows in Figure 5.14). As the temperature increases the oscillation amplitude decreases in the usual way and the field at which spin-splitting is resolved increases. The magnetoresistance behaviour at higher fields are shown in Figure 5.15 for different temperatures. The main feature of this data is a set of peaks that start to appear at around $B = 0.6$ T at 300 mK (with red arrows on Figure 5.15). As the temperature increases, it is the peak amplitude that decreases against a temperature independent background between them. This is the complete opposite to the SdH behaviour usually observed for high mobility samples, where the depth of minima vary with temperature and eventually reach zero at integer filling factors for low enough temperature. At higher temperatures these peaks also only start to appear at higher magnetic fields. In the inter-

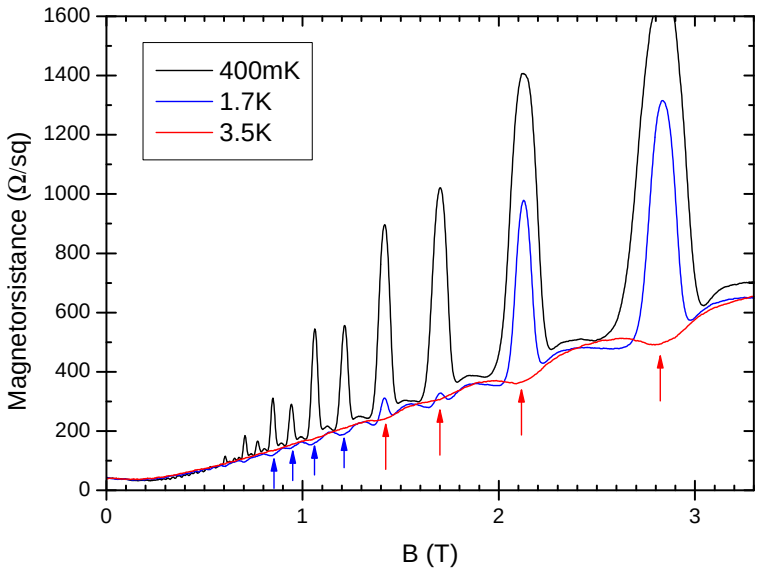


Figure 5.16: Magnetoresistance of sample 12-447 at intermediate temperature and field showing the emergence of peaks from SdH minima.

mediate temperature and field range, shown in Figure 5.16 it can be seen that the SdH minima at higher temperatures (indicated by arrows coloured to the 1.7 K and 3.5 K data) transform into peaks at lower temperatures.

Using this knowledge, the filling factor for each feature in the SdH data can be identified. Figure 5.17 shows the filling factor plotted against inverse magnetic field up to $\nu = 36$, with the filled points coming from the positions of SdH minima, including those at higher temperatures, and the open points from the sharp peaks seen at the lowest temperatures. The fact that these points all fit to a straight line through the origin demonstrates that this is the correct assignment of filling factors and gives a fundamental field of 8.45 T, which corresponds to a 2DHG density of $2.04 \times 10^{11}\text{cm}^{-2}$.

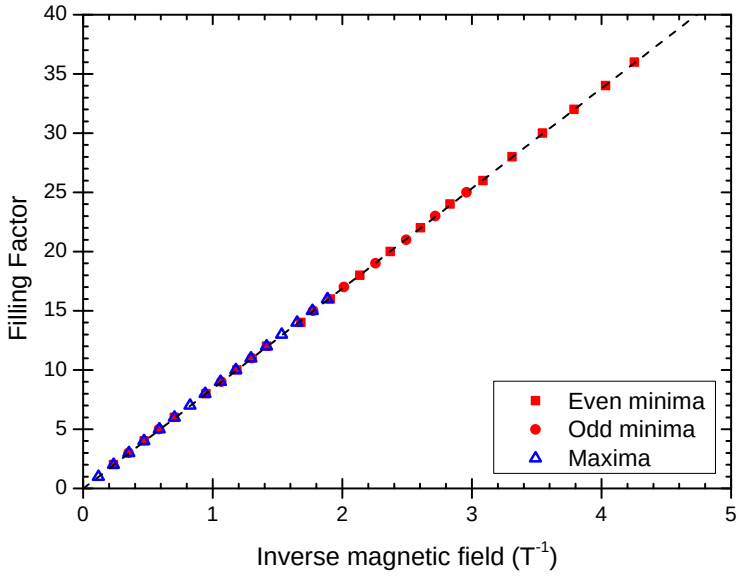


Figure 5.17: Filling factor as a function of inverse magnetic field for sample 12-447. Filled points are taken at SdH minima (from a range of temperatures), open points are for peaks in resistivity seen at lowest temperature. The straight line through the origin shows that the filling factors have been correctly assigned.

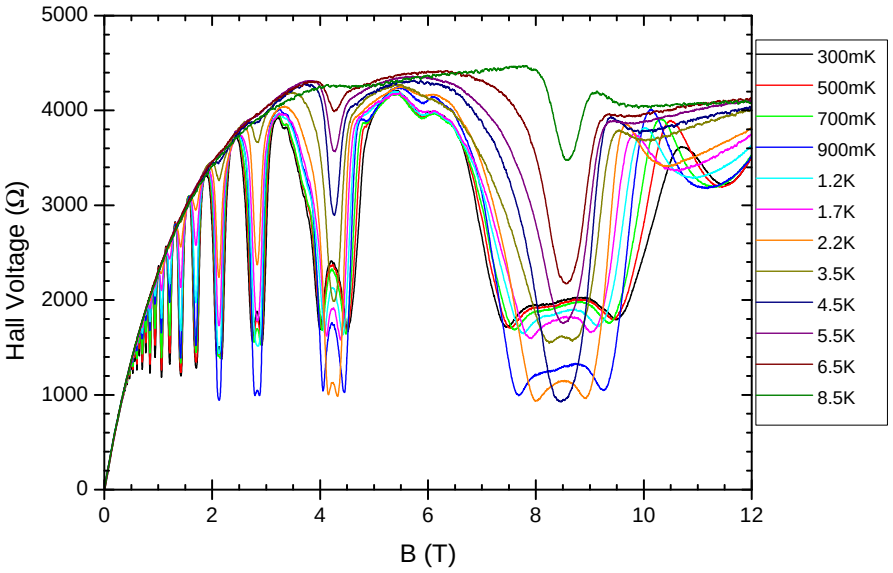


Figure 5.18: Temperature dependence of the Hall resistance for sample 12-447.

The Hall resistance curves, shown in Figure 5.18, do not show the typical quantum Hall effect plateaus. In their place there are minima that have a dependence with temperature like the peaks in the magnetoresistance. The higher temperature background to the Hall resistance is also sub-linear in magnetic field, which is a possible indication of parallel conduction. However, there is a linear region until approximately 0.2 T. By performing a linear fit on this region is possible to determine the Hall coefficient $R_H = 3162\ \Omega/T$, which corresponds to a carrier density of $1.98 \times 10^{11}\text{cm}^{-2}$. This value appears in complete agreement with the value obtained from the filling factors of the SdH oscillations (to within the experimental uncertainty) which would suggest that all the carriers involved in conduction are those in the quantum well and that there is therefore no parallel conducting channel.

In a further attempt to understand this sample, the conductivity σ_{xx}

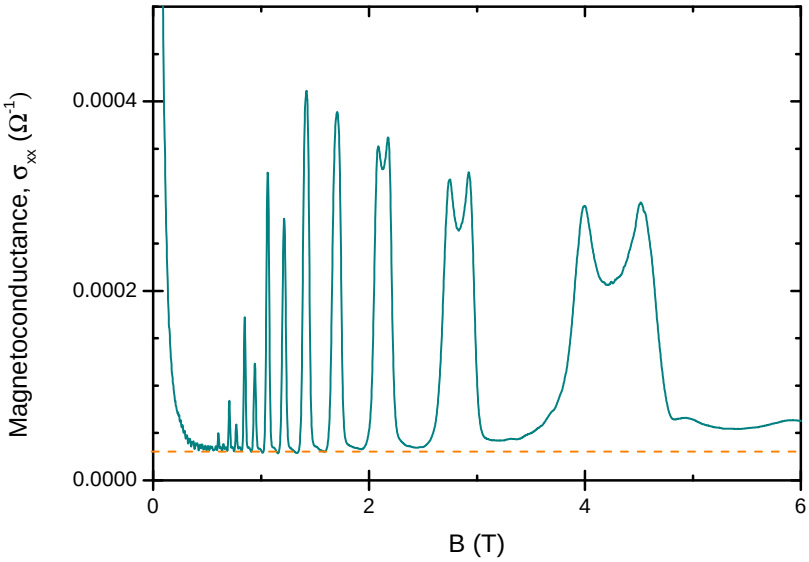
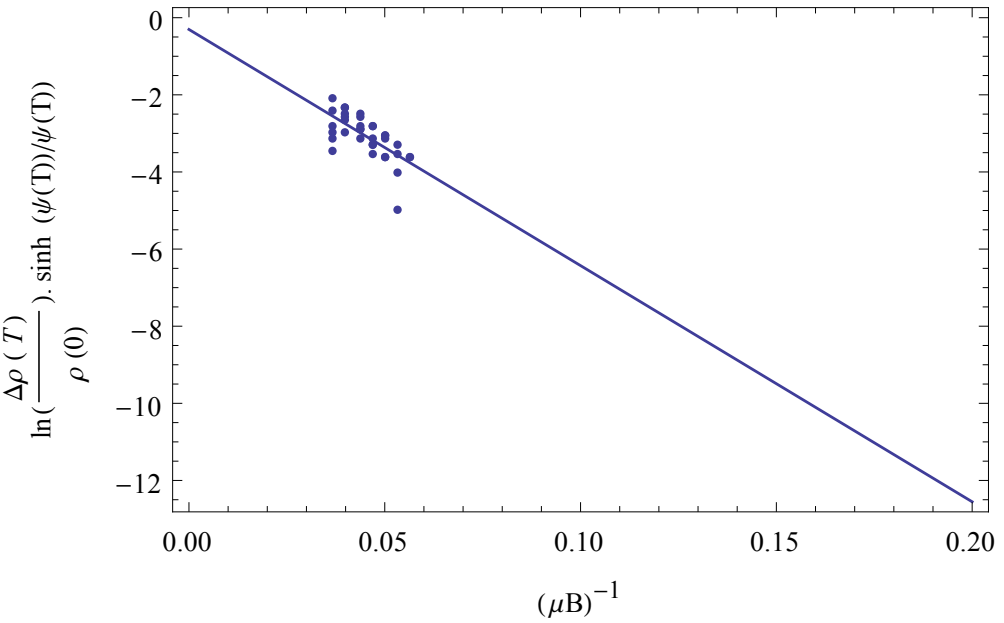


Figure 5.19: Magnetoconductivity for sample 12-447 at 300 mK.

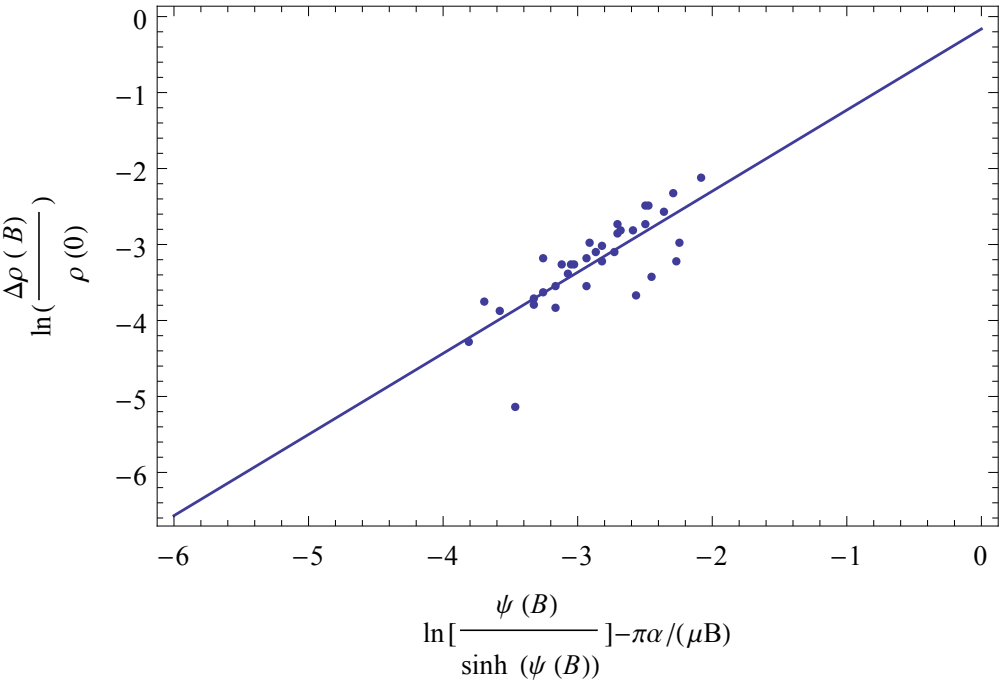
was calculated from the resistivity components at 300 mK and is shown in Figure 5.19. This shows that the rising background in ρ_{xx} has been replaced by a constant background in σ_{xx}. Such a constant background does suggest a parallel conducting channel with a conductivity of $3 \times 10^{-5}\Omega^{-1}$/sq, but is still inconsistent with the Hall effect data and does not explain the appearance of temperature dependent peaks in ρ_{xx}. The magnetoresistance of this sample therefore remains a mystery and in need of further investigation!

Despite the strange behaviour described in the previous paragraphs, the low field magnetoresistance behaves relatively normally and can be used to extract an effective mass value.

To determined the effective mass a small range of magnetic field was chosen in order to avoid the spin-splitting part or any regions where minima become maxima with decreasing temperature. In Figure 5.20 are shown



(a)



(b)

Figure 5.20: Plots for self-consistent extraction of effective mass m^* and parameter α for different temperatures (a) and magnetic fields (b).

the plots for a magnetic field range of 0.2 to 0.4 T. From these an effective mass value of 0.085 m_0 is obtained, although the plot has a negative intercept rather than the expected $\log 4$. This displaced intercept could be due to the anomalous value for the absolute resistance (because of factors unknown in the conduction in this sample), but the field and temperature dependence of the oscillations can still give a reasonably trustworthy value for the effective mass. A transport to quantum scattering times ratio α of 19.5 is also found. By reducing the magnetic field range a little more, an effective mass of 0.081 m_0 and an α of 26.5 result. This difference in values is due to the complexity of the magnetoresistance curve and gives an indication of the uncertainty in the values obtained. Nevertheless, the effective mass is found to be very similar to that measured for the more simple sample 12-28 earlier in the chapter. The α value is about five times higher in 12-447 than the 4.3 recorded for that sample, which is consistent with 12-447 having a much higher mobility of 700,000 cm^2/Vs as opposed to 90,000 cm^2/Vs. This indicates that background impurity scattering has been reduced in 12-447 to leave the mobility more affected by the small angle scattering from remote impurities.

5.3 Conclusion

In this section the magnetotransport properties were determined for holes in the 2DHG found in strained Ge quantum wells of different heterostructures. The first set of samples were heterostructures grown partially by CVD and partially by MBE, and the second set of samples were grown exclusively by CVD. The magnetic field dependences of magnetoresistance and Hall resistance were measured at temperatures in the range 0.3 to 300 K and in

magnetic fields up to 12 T.

The SdH oscillations were observed at low magnetic fields, spin splitting was also seen in both samples. The carrier sheet density was determined from the SdH oscillations and from the magnetic field dependence of Hall resistance, agreeing well in both cases. From the temperature dependence of the SdH oscillations effective mass values of $(0.083 \pm 0.002)\ m_0$ were found for the holes in both of these 20% strained Ge quantum wells.

Despite fabricating a Hall bar to ensure that parallel conduction is diminished, the magnetoresistance of sample 12-447 had an odd behaviour with temperature dependent resistance maxima at high magnetic fields where temperature dependent minima would be expected. There was also a field dependent background to the magnetoresistance that appeared to indicate different paths for carries to go, but this is inconsistent with carrier density obtained from the SdH oscillation period and Hall voltage slope at low fields being the same.

Chapter 6

Germanium Oxide

6.1 Introduction

This chapter describes the growth of GeO_2 on epitaxial grown Ge on Si(100) substrates. All the fabrication and characterization was performed at Warwick. The samples were characterized electrically and/or structurally.

Germanium oxide is the natural oxide of Ge. Despite showing good device performance, GeO_2 still presents some challenges due to its hygroscopic nature, solubility in water and thermal instability at temperatures used during device fabrication [101]. These lead to the degradation of the Ge-GeO_2 interface and consequently to poor device performance. Also when grown at lower temperatures a combination of GeO_2 and GeO is produced. Furthermore, GeO can desorb from the surface at temperatures as low as 500°C [102]. This desorption of GeO from the surface is related to degradation of the buried Ge-GeO_2 interface and consequently to poor device performance [49]. In [49, 102–108], it is shown that the GeO desorption occurs from the interaction of the GeO_2 with the Ge by

$$GeO_2 + Ge \longrightarrow 2GeO. \tag{6.1}$$

This was observed in Wang *et al.* [49], where lines were patterned in GeO_2/Ge structures. The samples were afterwards annealed and the Ge layer under the GeO_2 layer was measured by AFM and a reduction in the layer thickness was observed, leading to the conclusion that Ge is consumed during GeO formation and consequently the cause for interface degradation. This results was obtain for different GeO_2 thicknesses.

A model of oxygen vacancy diffusion has been proposed as the basis for Ge consumption [106], since a flux of O vacancies from the interface to the bulk should occur. In order to validate the model Wang *et al.* [106] grow a sample of $Ge^{16}O_2$ (40 nm)/$Ge^{18}O_2$(15 nm)/Ge by thermal oxidation at 530°C in $^{18}O_2$ ambient followed by sputtering $Ge^{16}O_2$. The structure was then partially covered with Si. The samples where then annealed at 550°C and measured by SIMS and a sharper diffusion slope was observed for the sample without Si. The O vacancies are consumed at the surface, making the concentration of vacancies lower in this sample, and consequently the exchange rate between O and GeO_2 is lower.

In order to control the GeO desorption it is necessary to choose a reliable method to passivate the surface. Lee *et al.* [44] have demonstrated control of GeO desorption by performing a high pressure oxidation (HPO) followed by low temperature oxidation annealing (LOA). For GeO_2 grown at 70 atm they measured interface trap densities (D_{it}) of $2 \times 10^{11} eV^{-1}cm^{-2}$ and a peak mobility in Ge(110) of 1100 $cm^2V^{-1}s^{-1}$ at room temperature. Bellenger *et al.* [46] performed thermal oxidation at low temperatures between 350°C and 450°C, and at an O_2 partial pressure of 1 atm, this gave a $D_{it} \approx 10^{11} eV^{-1}cm^{-2}$. Kutsuki *et al.* [109] passivated the surface with nitrogen and found that the current leakage was suppressed by a factor of 4 to 6 times, but at the ex-

pense of the EOT. However, they did not observe an improvement in the D_{it} ($D_{it_{min}} \approx 3.3 \times 10^{11}$ and $3.4 \times 10^{11}\text{eV}^{-1}\text{cm}^{-2}$). An improvement in device characteristics was also observed by Koumo *et al.* [110] while performing a two-step oxidation, the first oxidation was done at 500°C at 1 atm for 30 min followed by the second oxidation at 400°C 1 atm for another 30 mins. For a one step oxidization process at 500°C and 1 atm they observed a significant shift in the flatband voltage (V_{FB}), as well as a large hysteresis. With the two-step oxidation the hysteresis was reduced significantly, but still with the V_{FB} shift. In order to reduce this shift they performed an annealing in UHV. Another method of surface passivation used is ozone passivation [47] In this method it was found that the optimized oxidation temperature is 400°C with a D_{it} of $3\times10^{11}\text{eV}^{-1}\text{cm}^{-2}$. At higher temperatures, $GeO_2(4+)$ transforms into $GeO_2(2+)$ which favours the formation of GeO leading to degradation of the D_{it}. Yet another method is to thermally oxidise the Ge substrate [48, 49, 111]. It was found that D_{it} diminishes for higher temperatures, but at 600°C the surface GeO starts to desorb leading to formation of pin holes at the surface. It was found that the optimized oxidation temperature range is between 450°C and 575°C.

Nakakita *el al.* [112] have shown a 2.0x enhancement in mobility compared to the universal Si mobility-field curve for an $Al_2O_3/GeO_2/Ge$ device with GeO_2 thermally grown at 500°C, with the mobility limiting factor at low N_s being Coulomb scattering. However, this enhancement was obtained for a relatively thick GeO_2 layer. In order to reduce this layer, a gate stack employing high-κ dielectrics was sought [6]. This paper showed high mobilities $\mu = 515$ cm^2/V.s, and $D_{it} = 1.6 \times 10^{12}\text{cm}^{-2}\text{eV}^{-1}$ for devices with EOT=1.4 nm. The GeO_x interfacial layer was grown by plasma post oxi-

dation (PPO) by oxidizing the Ge layer using electron cyclotron resonance (ECR), after ALD deposition of Al_2O_3. Zhang *et al.* [7] were able to increase the mobility while reducing the EOT even further for gate stacks of $HfO_2/Al_2O_3/GeO_x/Ge$. Again the GeO_x IL was formed by PPO; it was shown that good performances can be reached even with subspecies of GeO_2. The Al_2O_3 layer is needed to prevent the intermixing between HfO_2 and GeO_x layers, which is responsible for interface degradation and consequently poor device performance. They reported an electron mobility of 754 $cm^2/V.s$ and a hole mobility of 596 $cm^2/V.s$ for an EOT of 0.82 nm.

6.2 Epitaxial Ge layer growth

The Ge epilayers were grown using the two-step technique [113]. In this technique a Ge 'seed' is grown at lower temperature, between 330°C and

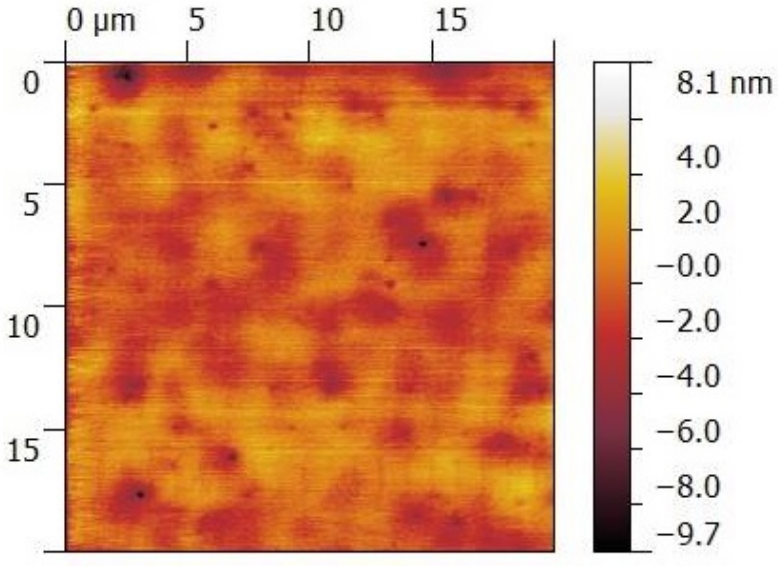


Figure 6.1: An AFM schematic representation of the surface morphology of sample of Ge grown by CVD, prior to oxidation.

450°C, followed by another layer deposition at higher temperature, 600°C to 850°C. The second Ge layer was grown with a final temperature of 670°C with a nominal thickness of 1 μm. Using low temperatures for the first Ge layer relaxes the strain and avoids the formation of islands. The high temperatures employed in the second layer reduces the dislocation density, by encouraging dislocation glide and annihilation, and reduces the deposition time. A typical image of the surface grown by this method is shown in Figure 6.1. The surface morphology was measured by AFM in tapping mode, giving a low RMS surface roughness of ~ 0.6 nm.

6.3 GeO_2 oxidation formation

6.3.1 GeO_2 Oxidation System

The GeO_2 was grown thermally in a furnace using a tube quartz, see Figure 6.2. The gases were controlled by using mass flow controllers. The quartz tube is only used for oxidation and only for GeO_2 to minimise the risk of contamination. Prior to the first oxidation the tube was cleaned with isopropanol and dried with a N_2 gun. After inserting the tube, the furnace was heated to 900°C for 1 hour, this will remove any remaining particles and moisture. The heating is done at a low flux of N_2. In order to reduce the temperature the N_2 is increased to maximum and the furnace is set to a lower temperature. Prior to oxidation the wafers are kept in a clean environment. In order to perform the oxidation it is necessary to cleave the sample into small pieces, between (1×1) cm^2 and (1×2) cm^2, in order to fit a ceramic boat that will be pushed to the middle of the furnace. For each oxidation 3 pieces are

cut. After oxidation, one piece is used for electrical measurements and has Al dots evaporated on to it, a second piece is covered with Al for TEM analysis, and the third is kept for other types of analysis.

In Figure 6.2 it is possible to see the four main components of the system: the gas inlet, the furnace, the quartz tube and the extraction of gases. After oxidation the samples were kept in a box purged with a constant flux of N_2.

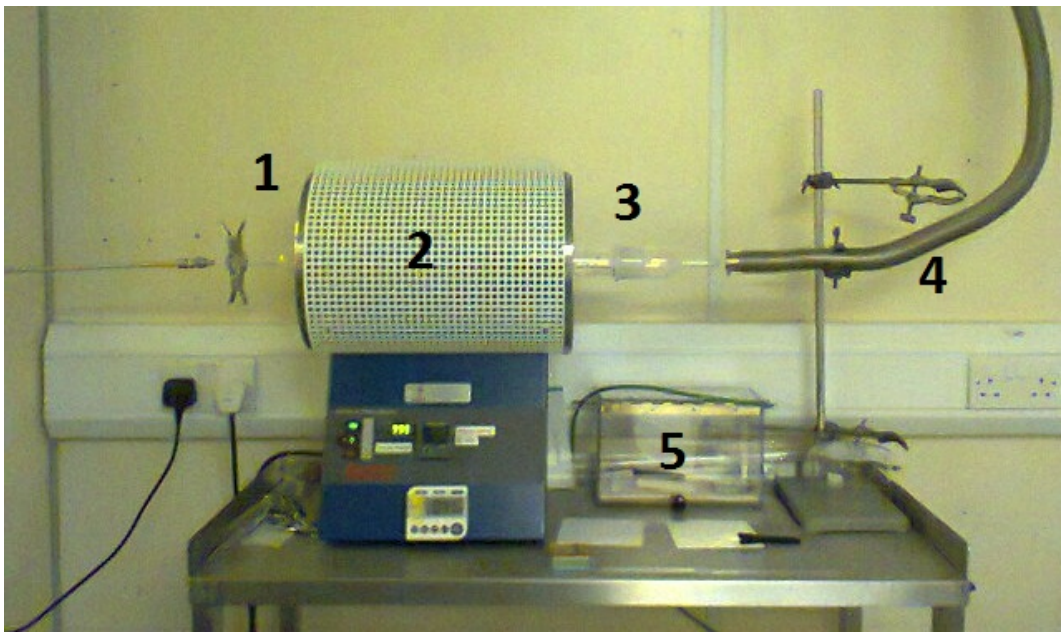


Figure 6.2: System used to perform the oxidation. it is composed of an inlet for the gases (1), a furnace (2), a quartz tube (3), gases extraction tube (4) and box to storage the samples (5). N_2 is constantly passing through the box.

6.3.2 Ge surface preparation and GeO_2 growth.

Natural oxides are responsible for degradation in devices, through increasing the contact resistance and increasing the interface roughness which causes mobility degradation [114]. Hence, it is necessary to remove the natural

oxide. The native oxide might include contamination such as particles, metals and organics. Although GeO_2 is soluble in water, GeO is not, so cleaning with DI is not the correct method. HF treatment of a Ge surface leads to a surface terminated with hydrogen, but when left in ambient conditions for 5 minutes re-oxidation occurs. If left in N_2 ambient re-oxidation takes longer to occur. HCl passivation of a Ge surface leaves a Cl terminated surface. If left in ambient conditions re-oxidation occurs after about 10 minutes [114]. Various other process have been employed in order to remove the oxide, in [6] the cleaning was performed using deionized water, acetone,and HF aqueous solution. Bellenger *et al.* [46] the cleaning was done using $NH_4OH/H_2O_2/H_2O$ followed by a 2% HF dip. However, there is always a risk that chemical cleaning can introduce further impurities. In this work, we chose instead to rely on thermal desorption of the native oxide and avoid using a chemical cleaning process for all the samples. The wafer used in this study are kept in a clean environment so it is expected that only a small layer of natural oxide to be present at the surface. The temperatures used for oxidation are enough for starting GeO desortion from the surface leaving a surface clean. The first oxidation was done in order to test the system. This resulted, in layers with good structural and electrical characterization, to be seen in the next sections. So a simple method for growing GeO_2 will be shown.

6.3.3 Oxidation process

In order to perform oxidation it is necessary to set the furnace temperature to the desired temperature at a flux 1000 sscm N_2. In order to ensure only O_2 is present in the tube during the oxidation, 1000 sccm of O_2

is sent through before inserting the sample. The samples are put in a ceramic boat at the entrance of the tube for 5 min prior to oxidation to gently heat the sample and reduce thermal shock. To start the oxidation, the sample is moved to the middle of the tube, where the temperature is believed to be at its maximum. The oxidation is performed at 1000 sccm. Before removing the sample, it was cooled at the entrance for 5 min at 500 sccm. The parameters varied are oxidation time and oxidation temperature. The set of oxidation temperatures chosen was between 450°C and 600°C. Below 450°C the surface is too rough and above 600°C the formation of pin holes occurs [103, 115, 116]. After oxidation Al dots were evaporated.

6.4 Characterization of Oxide layers

6.4.1 XPS analysis

In order to carry out an XPS study, a spectrum is first taken of an as-grown sample. Then the sample is annealed in-situ and a new spectrum is taken for each anneal temperature. The temperature interval at which annealing occurred was between 300°C and 500°C, with spectra taken of samples for which the anneal temperature increased in steps of 50°C.

Figure 6.3 shows a spectrum of a sample prior to oxidation, which has been kept outside of a clean environment, which as mentioned previously leads to natural oxidation. Looking at the data, two peaks can be clearly distinguished; however, by fitting the peaks with Voigt functions it is possible to differentiate four curves that contribute to the spectrum. At lower energies a peak can be identified at 30.12 eV corresponding to the elemental Ge peak

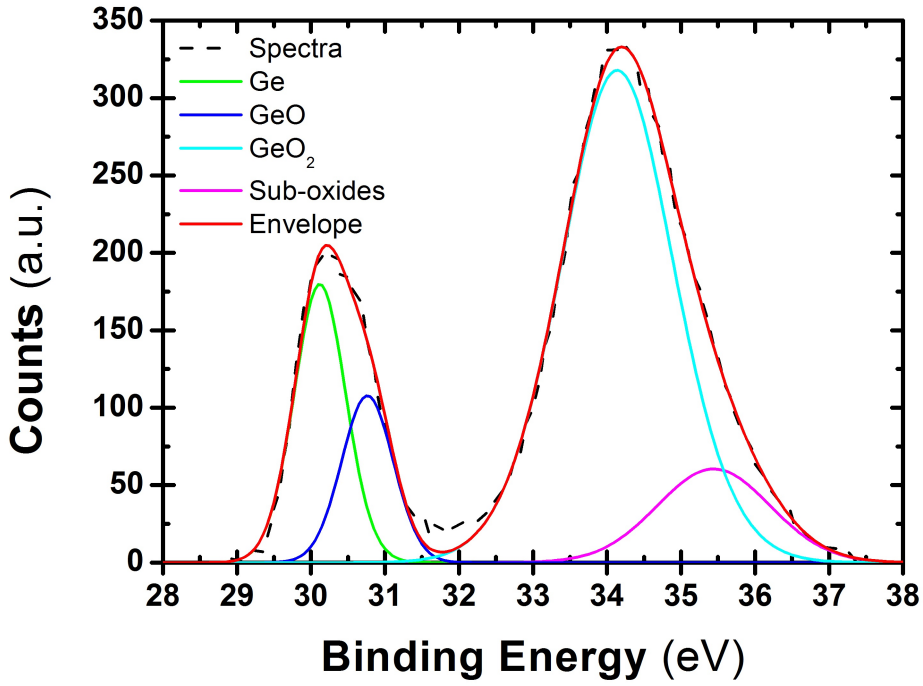


Figure 6.3: XPS Ge $3d$ spectra for the sample with natural oxide as-grown

(green). A second peak is shifted by 0.64 eV corresponding to the Ge^{1+} oxidation state (blue). A third peak is shifted by 3.37 eV which corresponds to oxidation state Ge^{4+} (cyan), the final peak (magenta) is shifted by more than 5 eV which is attributed to oxides from the bulk. The different oxidation states corresponds to the different Ge sub-oxides, for instance, Ge^{1+} corresponds to the Ge_2O oxide, Ge^{2+} to GeO, Ge^{3+} to Ge_2O_3 and Ge^{4+} to GeO_2 [117, 118].

In Figure 6.4 is shown the envelope spectra taken for different anneal temperatures, the annealing occurred in vacuum. The shift to lower binding energies of the GeO_x peak can be observed with increasing temperature which is associated with the desorption of GeO. At 500°C only the elemental Ge peak is observed.

The thickness of the layer can be estimated from the XPS spectra, by applying the thickogram method [119] (see Figure 6.5), to be around 2.1 nm.

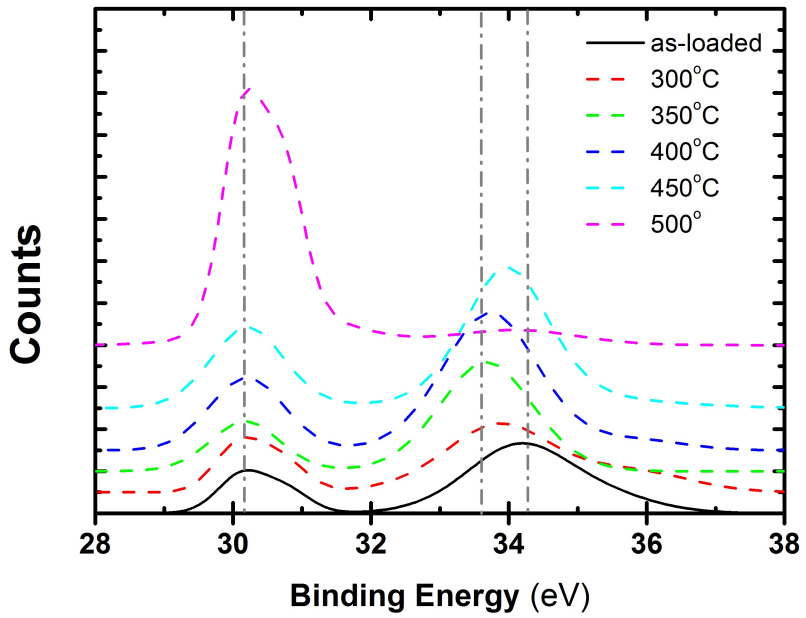


Figure 6.4: XPS Ge 3d spectra for the sample with natural oxide as function of annealed temperature.

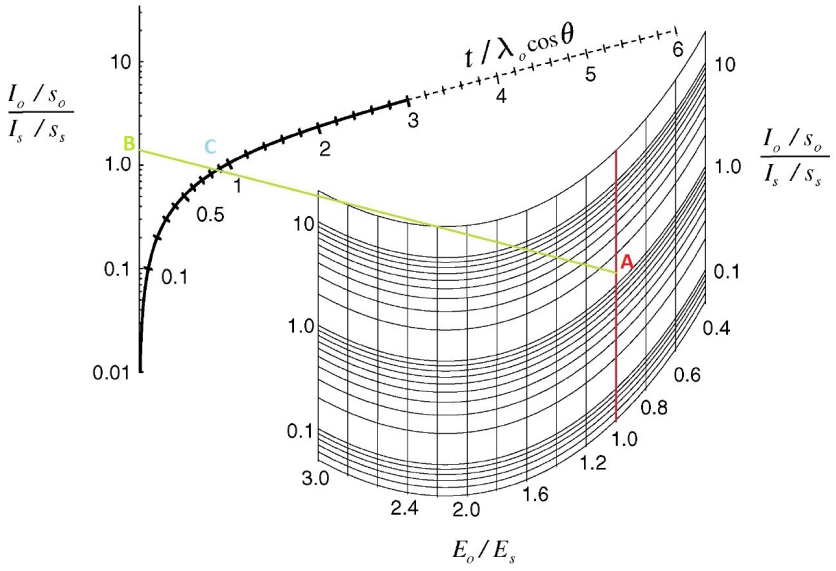


Figure 6.5: Thickogram for determining the Germanium Oxide thickness. The ratio of kinetic energy of overlayer and substrate peaks is 1. The intensity ratios is 1.53. This gives an intersection for C=0.9.

6.5 Results of the GeO_x layers.

6.5.1 Preliminary studies.

In order to test the tube furnace a set of samples, which have not gone through any cleaning treatment, were oxidised at 450°C for 30 minutes and at 475°C for 30 and 60 minutes. Both n-and p-type substrates were used. The samples were characterized by depositing an Al surface contact and performing CV measurements.

For the first set oxidised at 450°C it is possible to observe a small bump in the CV profile (see Figure 6.6) at low frequencies indicating the presence of interface traps. However, it is not possible to observe the inversion layer for low frequencies.

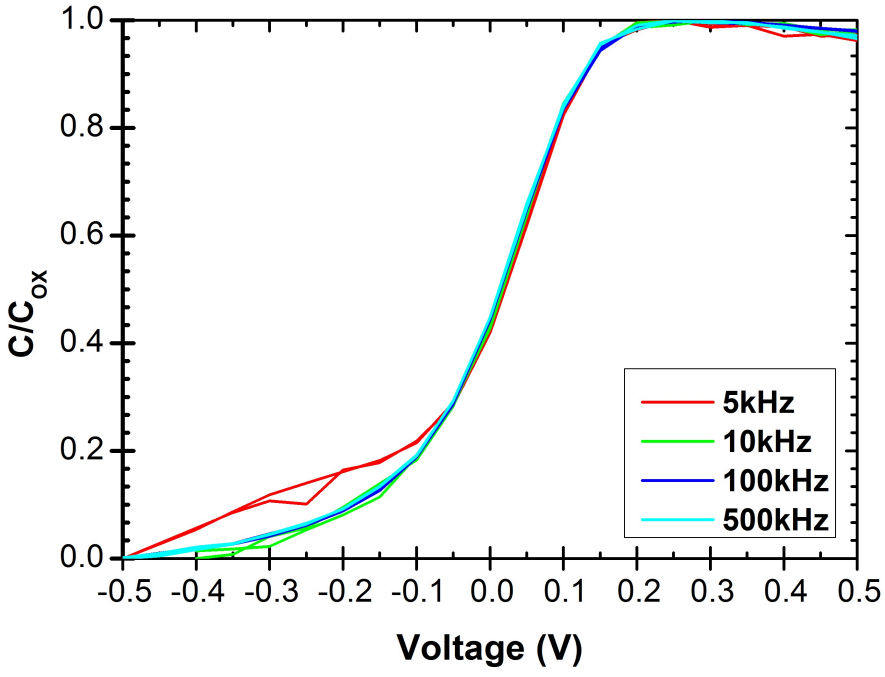
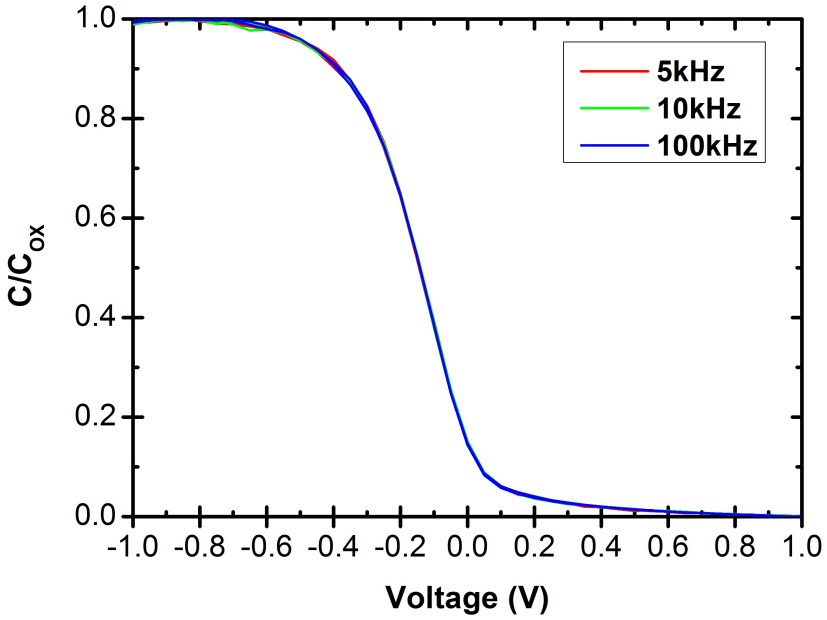
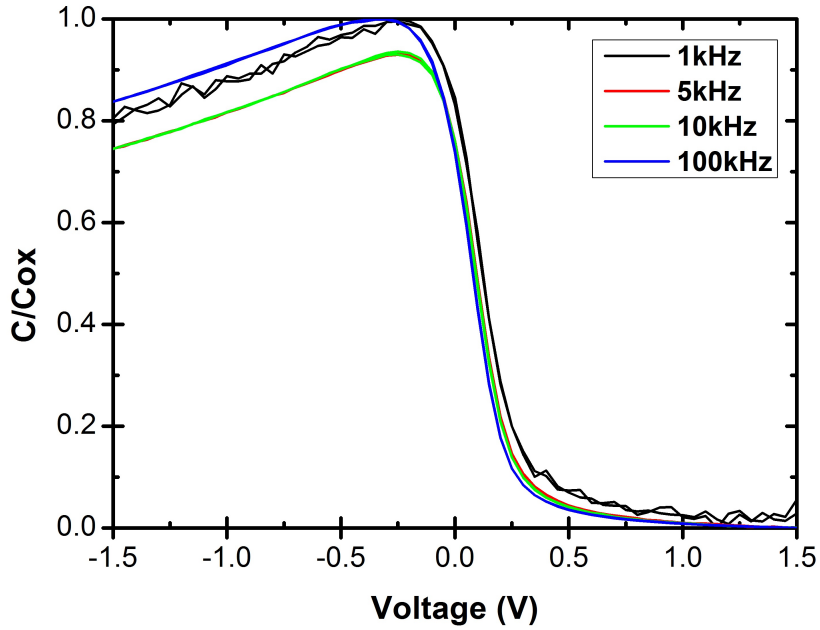


Figure 6.6: C-V characteristics of Al/GeO_2/Ge capacitors at frequencies of 5k-500 kHz for samples grown at 450°C for an oxidation time of 30 minutes. $N_D = 2.8 \times 10^{18}$ cm^{-3}, $t_{ox} = 272.5$ nm as measured by the CV curve.



(a) Oxidation at 475°C for 30 minutes.



(b) Oxidation at 475°C for 60 minutes.

Figure 6.7: C-V characteristics of Al/GeO_2/Ge capacitors at frequencies of 1k - 100 kHz for samples grown at: a) 475°C for 30 minutes, $N_A = 4.5 \times 10^{15}$ cm^{-3}, t_{ox} = 58.4 nm as measured by CV curves; and b) at 475°C for 60 minutes, $N_A = 9.8 \times 10^{14}$ cm^{-3}, t_{ox} = 47.9 nm as measured by CV curves.

	Electrical (CV)			Structural (TEM)		
	450^{o}C	475^{o}C		450^{o}C	475^{o}C	
	30min	30min	1h	30min	30min	1h
V_{FB} (mV)	-88	-50	-113	–	–	–
t_{ox} (nm)	272.5	58.4	47.9	1200	58	82
EOT (nm)	204.3	43.8	35.9	–	–	–

Table 6.1: Selected electrical parameters for the capacitors in test batch.

For the devices grown at 475°C we no longer see the bump in CV at low frequencies, which suggest interface traps have been eliminated. The frequency dispersion is non-existent for 30 minutes of oxidation time. The device quality for capacitors grown at 475°C for 1 h is poor (see Figure 6.7(b)), showing a dispersion in frequency, but no bump for high frequencies. The sharp slopes shown in the CV curves are an indication of low interface state density. In this batch we cannot see formation of the inversion layer at low frequencies.

In Table 6.1 we can see parameters extracted from the CV measurements, with the oxide thickness calculated using equation 3.22 and the EOT using equation 3.23, as well as the thickness extracted from TEM. Comparing the oxide thickness obtained by the CV and TEM we can see that the values only agree for the sample grown at 475°C for 30 minutes. From Figure 6.8 we can see that it is difficult to differentiate the oxide from the Ge layer. The poor quality of the oxide contributed to the poor performance of the device, see Figure 6.6.

In Figures 6.9 and 6.10 it is possible to observe a good Ge-GeO_2 interface for the samples grown at 475°C. Considering both the CV measurements and the TEM images it is possible to say that oxidation occurred for both temperatures; however, from a device point of view, the lower temperature is

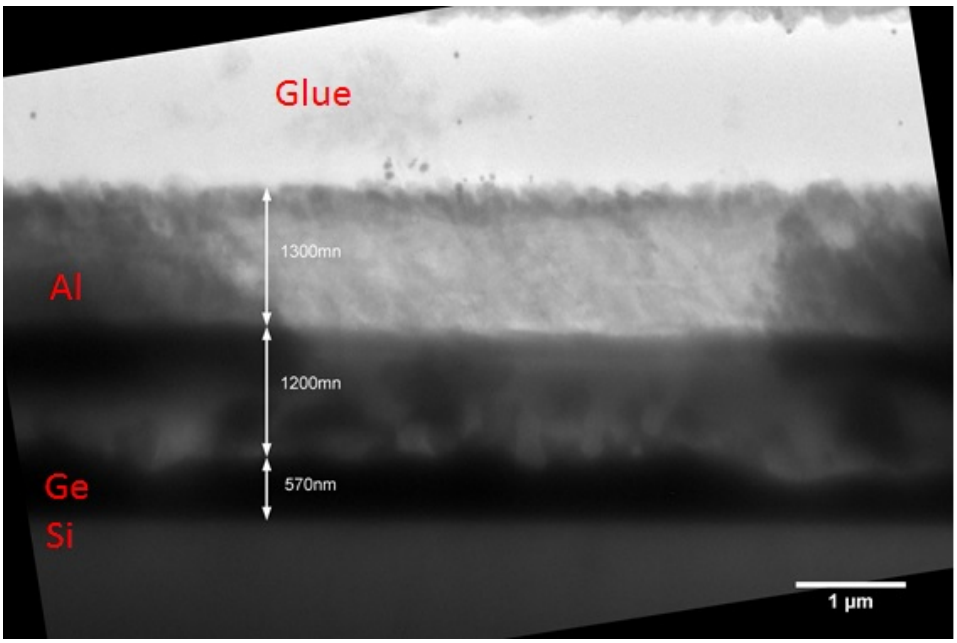


Figure 6.8: Oxidation at 450°C for 30 minutes.

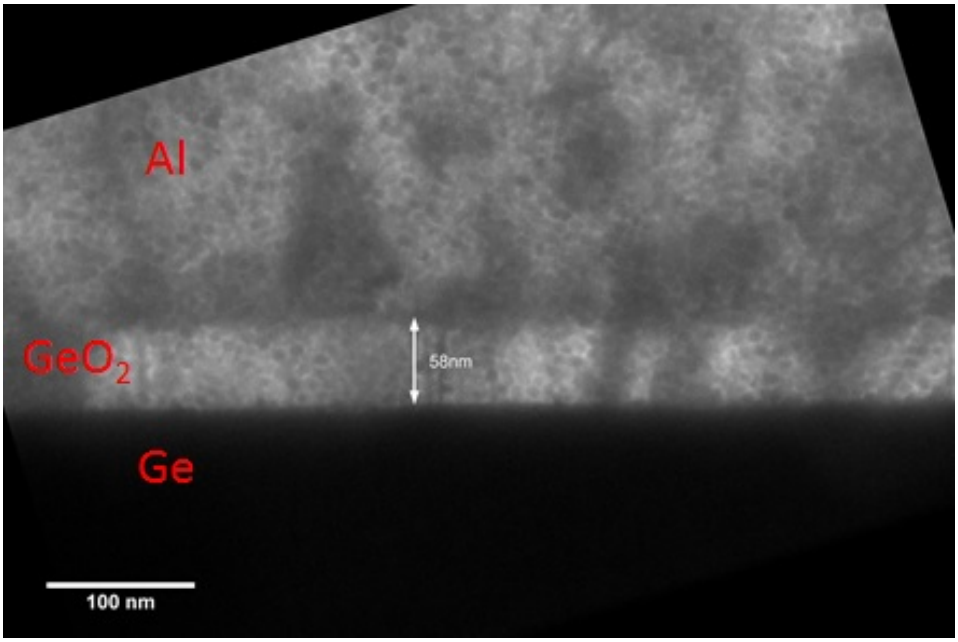


Figure 6.9: Cross-sectional TEM images of the oxidized samples for samples grown at 475°C for 30 minutes.

not adequate, there is no clear distinction between Ge and the GeO_2, making it difficult to determine the layer thickness. In order to have CMOS quality devices it is necessary to reduce the oxide thickness while maintaining the good quality interface, so in the second batch of oxidation the oxidation temperature started at 475°C and the oxidation time was reduced.

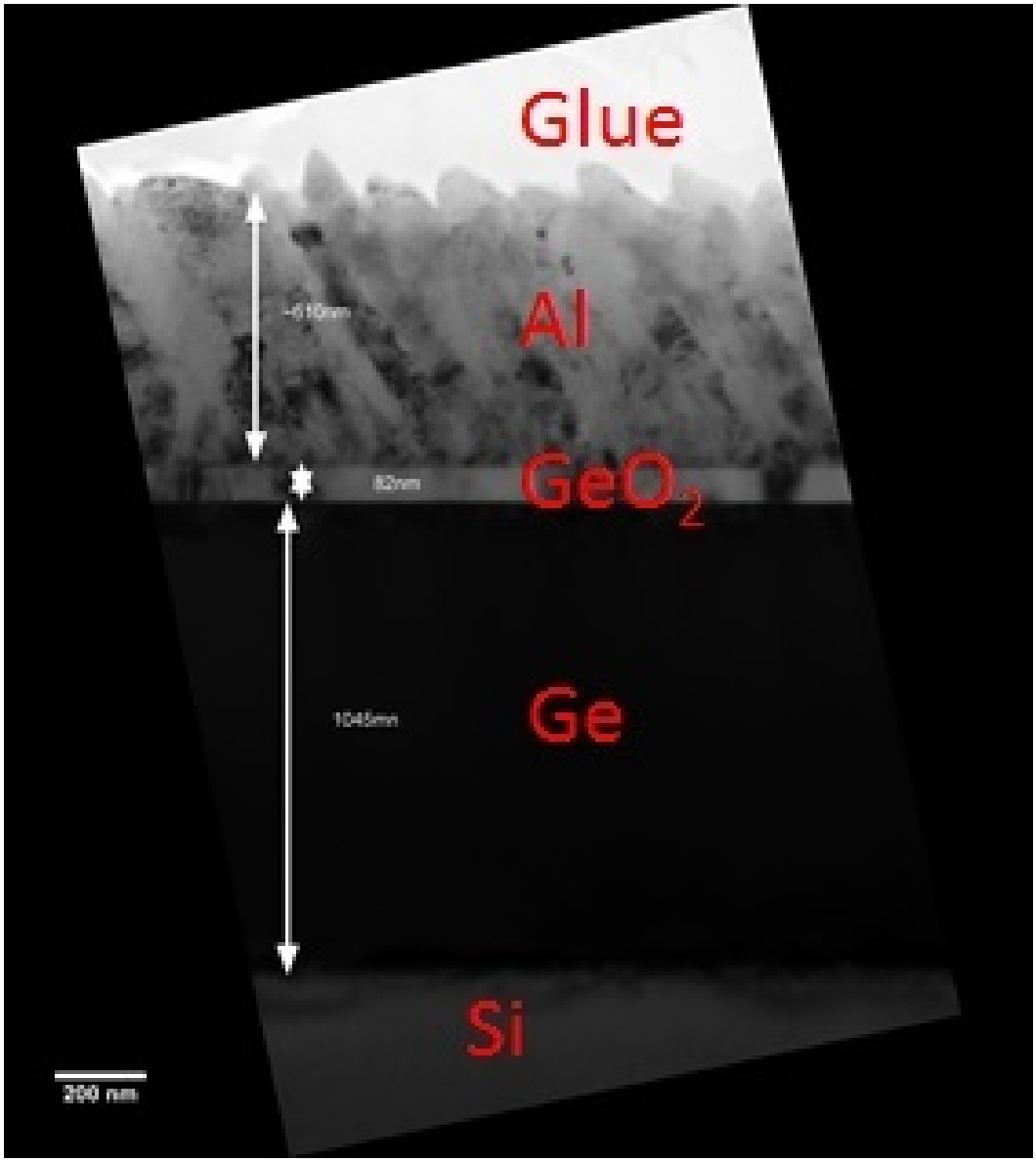


Figure 6.10: Cross-sectional TEM images of the oxidized samples for samples grown at 475°C for 60 minutes.

A second oxidation was performed in order to test the repeatability of the process, however, this oxidation failed. The position of the samples in the tube is crucial so it is necessary to find the position at which the temperature is at maximum. The maximum in temperature can be found in the middle of tube with the temperature decreasing quite rapidly towards the ends. Therefore positioning the sample exactly in the middle of the oxidation furnace is critical. With this information a third oxidation was performed.

6.5.2 Oxidation results.

The new oxidations were carried out at 475°C, 500°C, 550°C and 600°C. Table 6.2 shows the oxidation times for each oxidation temperature.

CV characteristics for the new oxidation batch are shown in Figures 6.11 to 6.18. This time it was not possible to obtain good devices for the samples oxidized at 475°C; we were not able to reproduce the results obtained in the first oxidation. The voltage sweep was performed in both directions lead to the dislocation of the curve by small amount, hysteresis. This hysteresis is present in the CV curves for all the oxidations performed, which is between 40 mV and 80 mV (see Table 6.3). The curves show noise at low frequencies independently of the oxidation temperature and oxidation time. Nevertheless,

	Temperature (°C)			
	475°C	500°C	550°C	600°C
Time	45	30	15	15
	60	45	30	30
	75	60	45	45

Table 6.2: Matrix of oxidation times and oxidation temperatures used.

we were able to measure CV curves at frequencies as low as 500 Hz (which indicates a good quality oxide without significant leakage) for oxidation performed at 500°C and 550°C, see Figure 6.13, Figure 6.14 and Figure 6.15. Figure 6.15 shows noise even at 1 kHz being the noisiest figure, with noise even in the depletion region.

Figure 6.12 shows the CV curve for sample grown at 500°C for 45 minutes. In accumulation it is possible to observe a frequency dispersion, this frequency dispersion is associated to a high carriers concentration [120]. Also, at high frequency a stretch-out of the curve is observed, indicating the presence of trapped charge at the interface. Figures 6.15 to Figure 6.18 show small inversion even at high frequencies.

For an oxidation temperature of 500°C, as the oxidation time increases we are able to measure at lower frequencies showing that the oxide

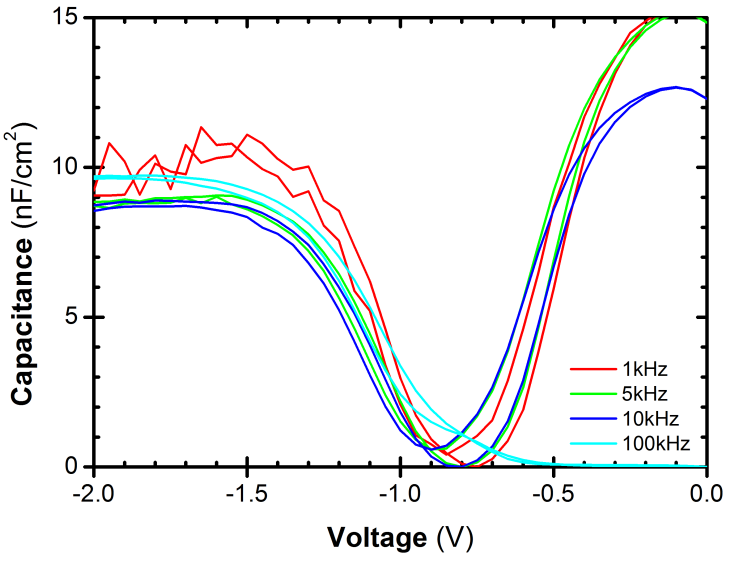


Figure 6.11: C-V characteristics of Al/GeO_2/Ge capacitors at frequencies of 1k-100 kHz for samples grown at 500°C for 30 minutes. $N_A = 4.7 \times 10^{14}$ cm^{-3}, $t_{ox} = 7.2$ nm as measured by CV curves.

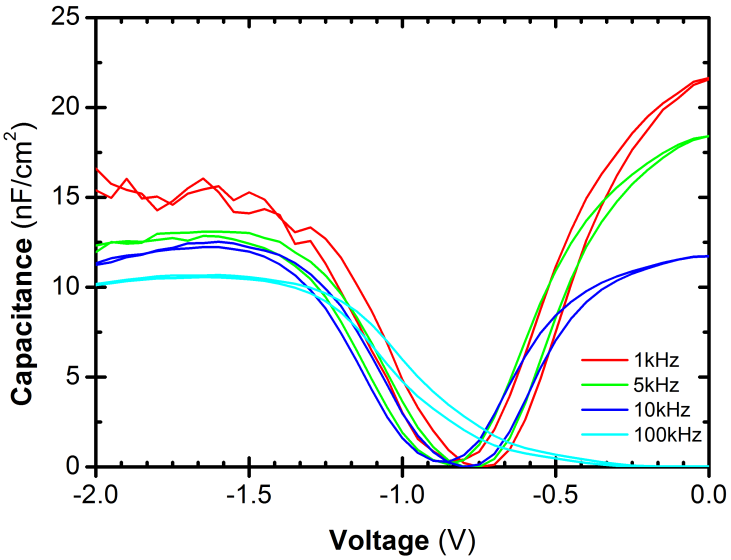


Figure 6.12: C-V characteristics of Al/GeO_2/Ge capacitors at frequencies of $1k-100$ kHz for samples grown at 500°C for 45 minutes. $N_A = 4.1\times10^{14}$ cm^{-3}, $t_{ox} = 6.7$ nm as measured by CV curves.

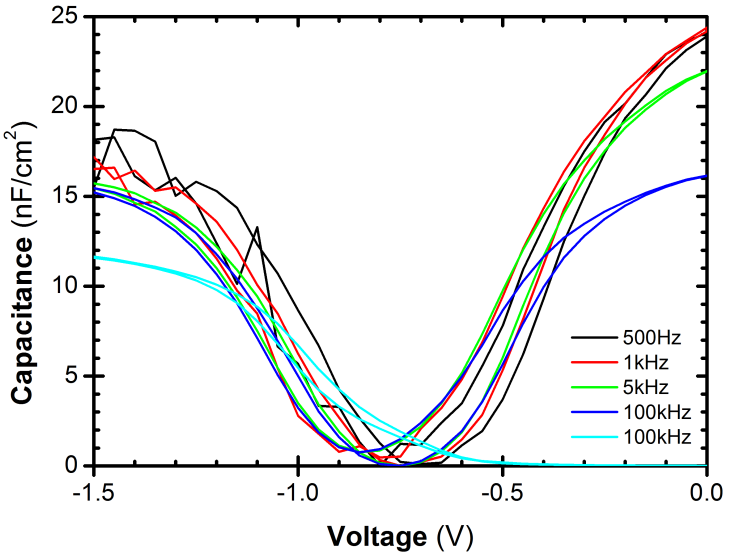


Figure 6.13: C-V characteristics of Al/GeO_2/Ge capacitors at frequencies of 500 - 100 kHz for samples grown at 500°C for 60 minutes. $N_A = 2.9\times10^{14}$ cm^{-3}, $t_{ox} = 5.8$ nm as measured by CV curves.

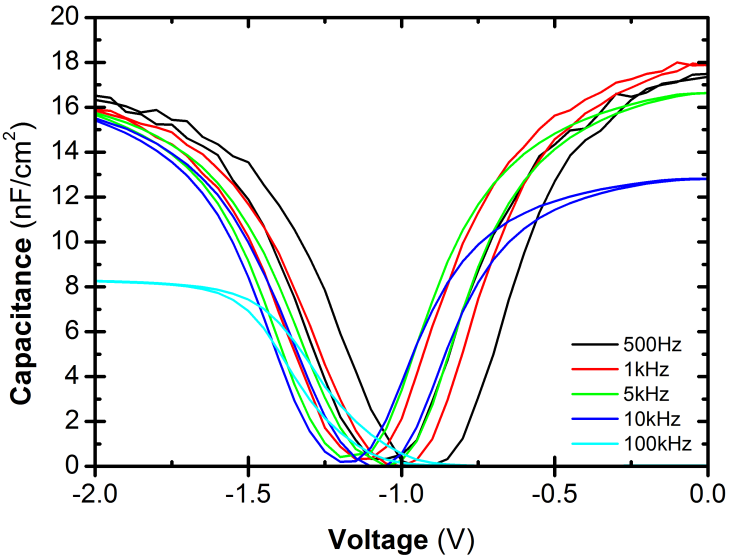


Figure 6.14: C-V characteristics of Al/GeO_2/Ge capacitors at frequencies of 500 - 100 kHz for samples grown at 550°C for 30 minutes. $N_A = 1.3\times10^{14}$ cm^{-3}, $t_{ox} = 8.7$ nm as measured by CV curves.

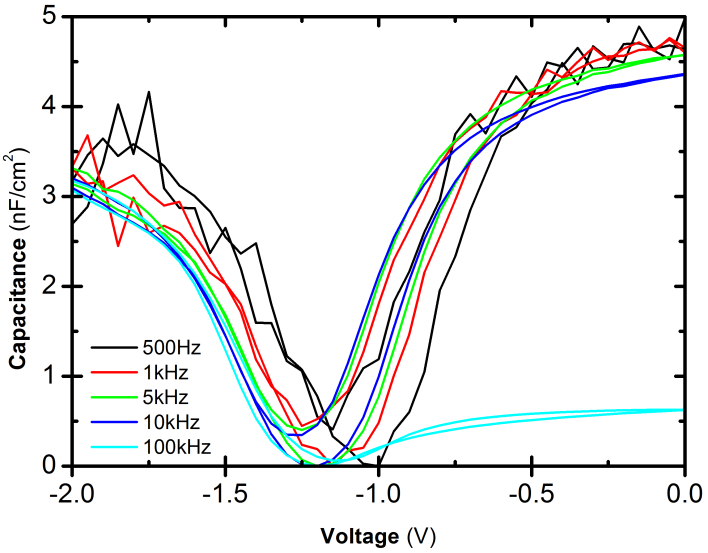


Figure 6.15: C-V characteristics of Al/GeO_2/Ge capacitors at frequencies of 500 - 100 kHz for samples grown at 550°C for 45 minutes. $N_A = 4.0\times10^{14}$ cm^{-3}, $t_{ox} = 22.6$ nm as measured by CV curves.

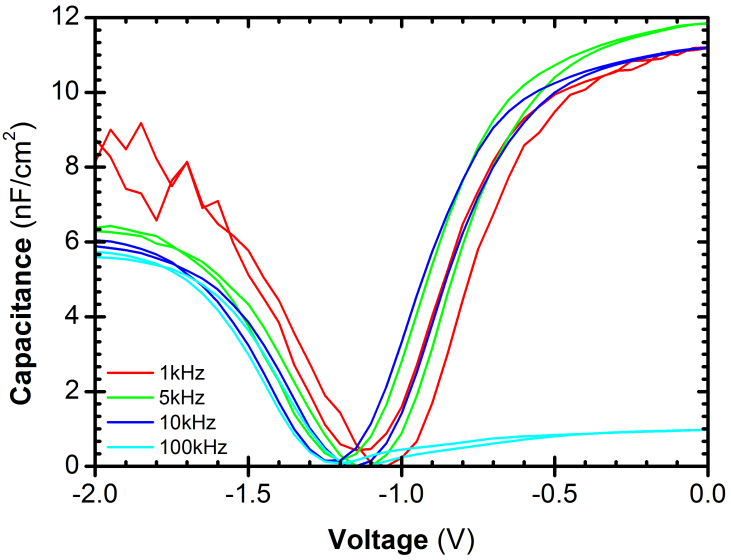


Figure 6.16: C-V characteristics of Al/GeO_2/Ge capacitors at frequencies of 1k - 100 kHz for samples grown at 600°C for 15 minutes. $N_A = 4.2 \times 10^{14}$ cm^{-3}, t_{ox} = 13.0 nm as measured by CV curves

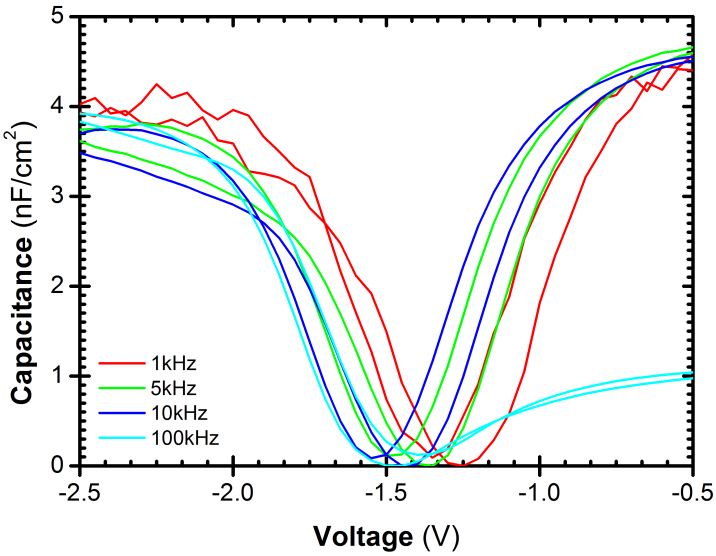


Figure 6.17: C-V characteristics of Al/GeO_2/Ge capacitors at frequencies of 1k - 100kHz for samples grown at 600°C for 30 minutes. $N_A = 6.8 \times 10^{14}$ cm^{-3}, t_{ox} = 11.9 nm as measured by CV curves

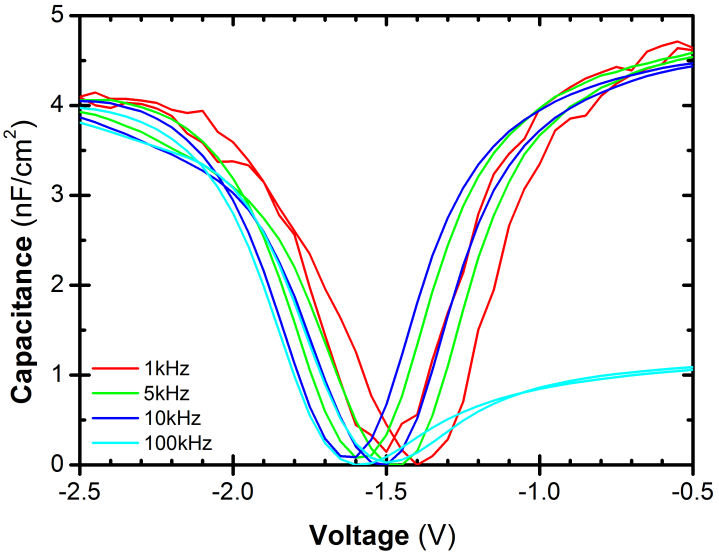


Figure 6.18: C-V characteristics of $Al/GeO_2/Ge$ capacitors at frequencies of 1k - 100kHz for samples grown at 600°C for 45 minutes. $N_A = 5.6 \times 10^{14}$ cm^{-3}, $t_{ox} = 17.0$ nm as measured by CV curves

film quality improves as it grows. Also, with increasing oxidation time the frequency dispersion in accumulation increases.

The sample grown at 550°C for 30 minutes shows in accumulation higher frequency dispersion but better CV characteristics. For higher oxidation time the 100 kHz curve shows small inversion due to minority carriers response. This curve shows more noise.

At an oxidation temperature of 600°C, with an oxidation time of 45 minutes, the 100 kHz curve shows small inversion, but the frequency dispersion is small. Also, we observe a decrease in the difference between accumulation and depletion capacitance. For the sample grown for 30 minutes, it is still possible to observe a small inversion for 100 kHz. The inversion is smaller for the sample grown for 15 minutes; however, the difference between accumulation and depletion is greater.

		Electrical (CV)					Structural (TEM)
Temperatura	Time (min)	ΔV (mV)	V_{FB} (V)	C_{ox} (nF)	EOT (nm)	t_{ox} (nm)	
500°C	30	56	-0.83	1.2	5.6	7.2	6.0
	45	62	-0.63	1.3	5.3	6.7	-
	60	46	-0.73	1.5	4.5	5.8	9.0
550°C	15	-	-	-	-	-	5.5
	30	65	-1.3	1.0	6.8	8.7	9.5
	45	54	-1.5	0.4	17.7	22.6	5.5
600°C	15	53	-1.4	0.7	10.1	13.0	6.5
	30	100	-1.7	0.7	9.3	11.9	5.7
	45	80	-1.8	0.5	13.3	17.0	35

Table 6.3: Selected electrical parameters for the Al/GeO_2Ge capacitors from the third oxidation and a comparison of oxide thickness measured by CV and TEM. The t_{ox} values were calculated assuming a dielectric constant of 5.

Table 6.3 shows parameters extracted from the CV characteristics for the last oxidation. The parameters extracted were capacitance in accumulation (C_{ox}), oxide layer thickness (t_{ox}), hysteresis (ΔV) and flatband voltage (V_{FB}). The flatband voltage is negative for all oxidation temperatures, with the shift increasing with oxidation temperature. Also, the hysteresis can be seen to increase with oxidation time, but does not exceed 100 mV.

Figure 6.20 to Figure 6.26 shows cross-sectional TEM images of the samples oxidized. In all figures it is possible to distinguish the GeO_2 layer, and observe the good quality of the Ge-GeO_2 interface. The images allow the oxide thickness to be determined as can be seen in Table 6.3. As expected, the thickness increases with the oxidation time and temperature. Moreover, we see that layer quality increases with increasing oxidation time.

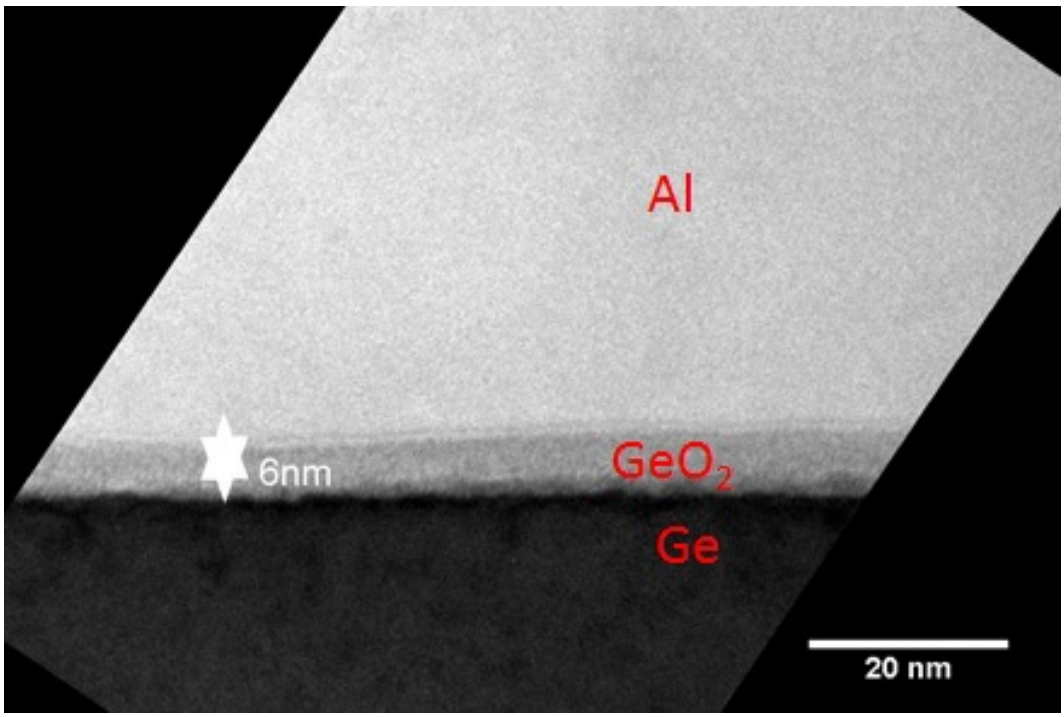


Figure 6.19: Cross-sectional TEM images of the sample oxidized at 500°C for 30 minutes.

There are discrepancies between the values obtained from the TEM images and the CV curves (see Table 6.3). According to the cross-sectional TEM, oxide thicknesses are less than 10 nm with the exception for the sample grown at 600°C, while extraction from electrical characterization gives higher thickness for the majority of samples. The discrepancy in the values may be due to non-uniformity of the oxidation across the samples.

In Figure 6.27 an XPS spectrum for a sample oxidised at 500°C for 45 minutes is shown; after fitting two peaks are observed. The first peak shows a chemical shift of 3.5 eV and the second 4.1 eV associated to the oxidation state Ge^{+4} and to sub-oxides from the bulk-oxides [117, 118]. A sample oxidised at 550°C for 30 minutes was also analysed by XPS. In the as-grown sample no Ge peak can be distinguished (see Figure 6.29). After annealing at 500°C for

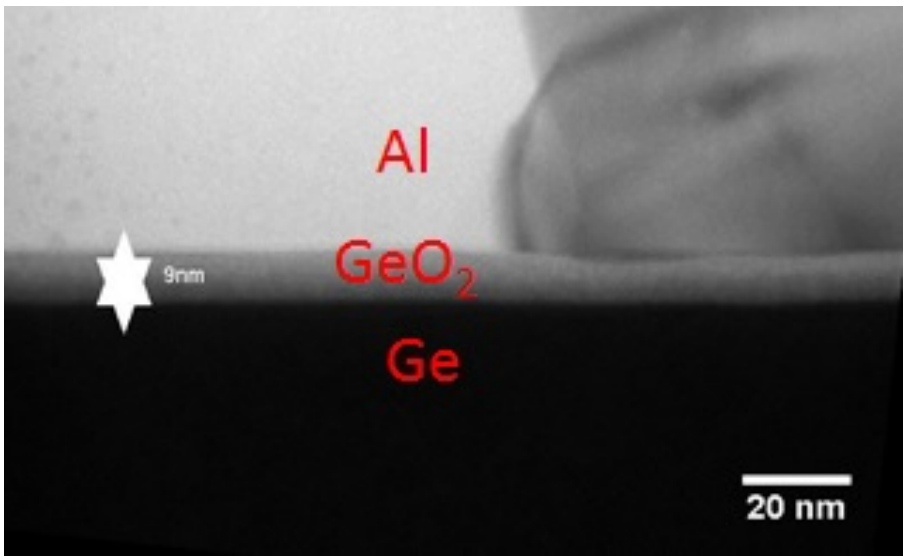


Figure 6.20: Cross-sectional TEM images of the sample oxidized at 500°C for 60 minutes.

30 minutes the oxide composition changes for both samples. Figure 6.28 and Figure 6.30 shows the spectrum for samples grown at 500°C for 45 minutes and grown at 550°C for 30 minutes after annealing at 500°C. In Figure 6.28 a

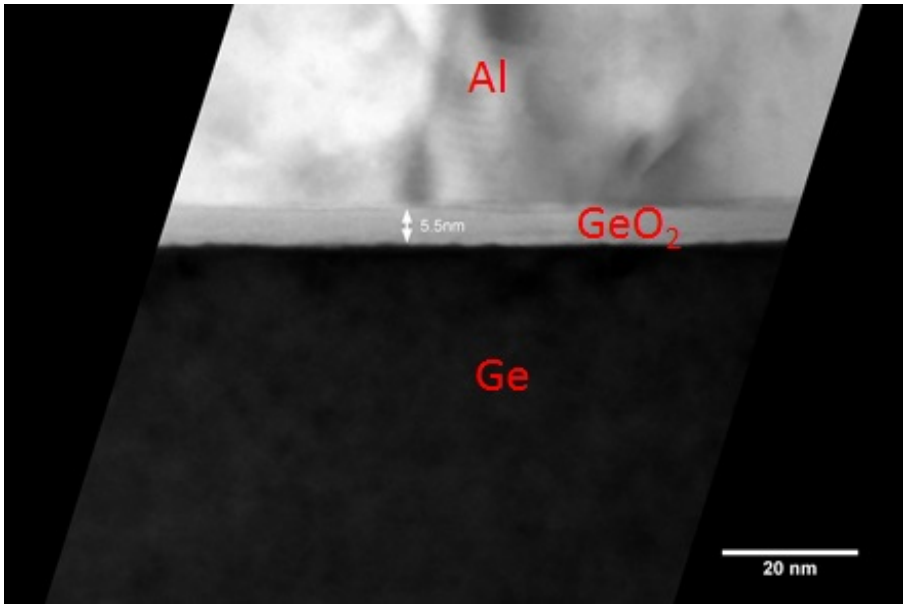


Figure 6.21: Cross-sectional TEM images of the sample oxidized at 550°C for 15 minutes.

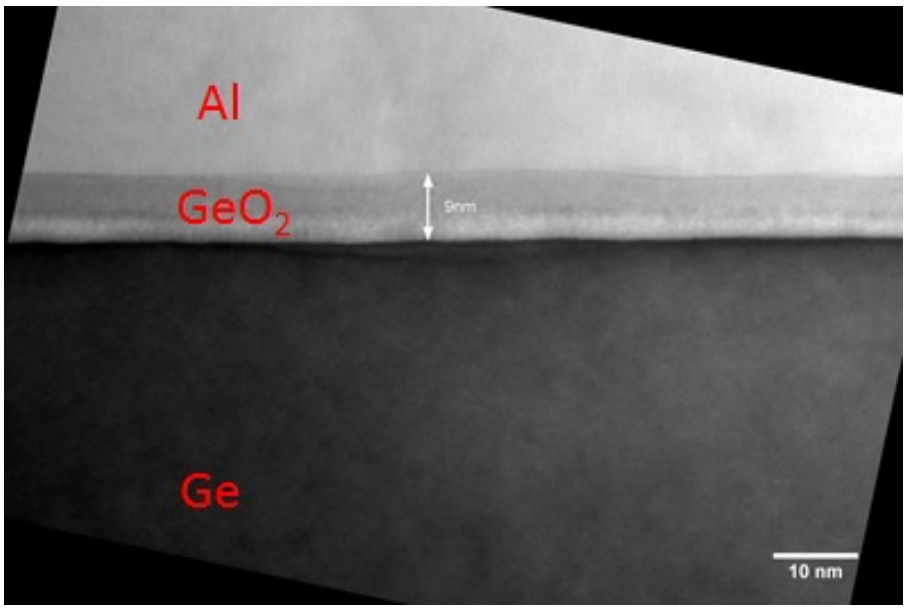


Figure 6.22: Cross-sectional TEM images of the sample oxidized at 550°C for 30 minutes.

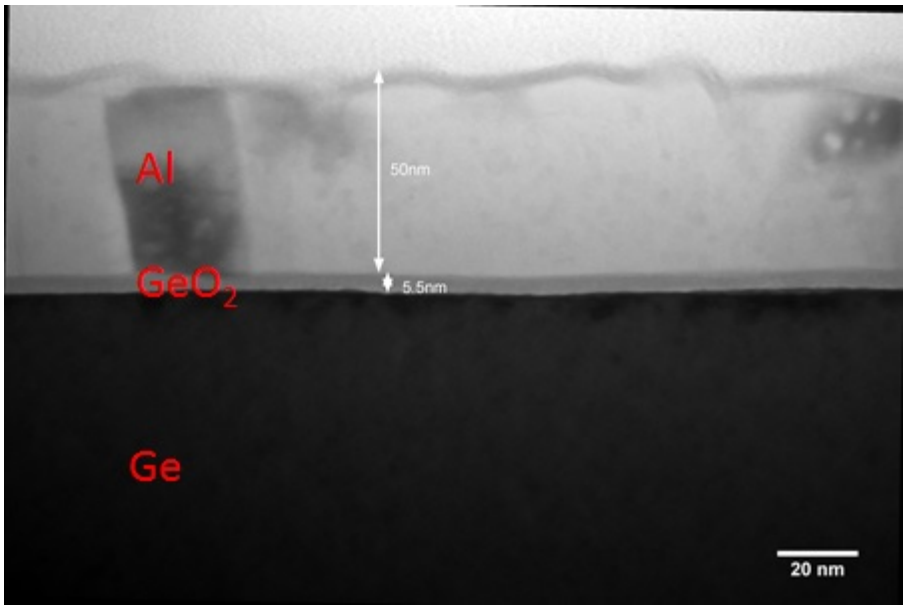


Figure 6.23: Cross-sectional TEM images of the sample oxidized at 550°C for 45 minutes.

single peak is observable. In order to fit the peak, Voigt functions are used, as a result two peaks can be distinguished, the elemental Ge peak at 29.5 eV and

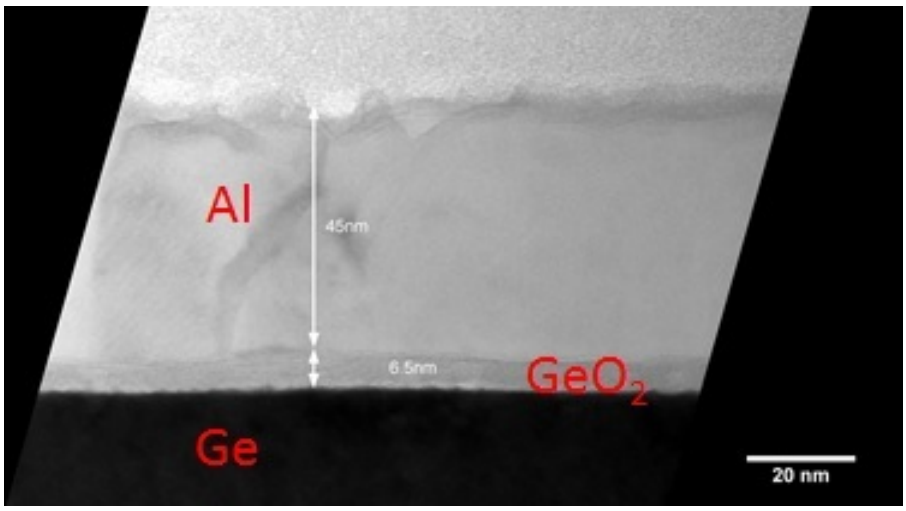


Figure 6.24: Cross-sectional TEM images of the sample oxidized at 600^{o}C for 15 minutes.

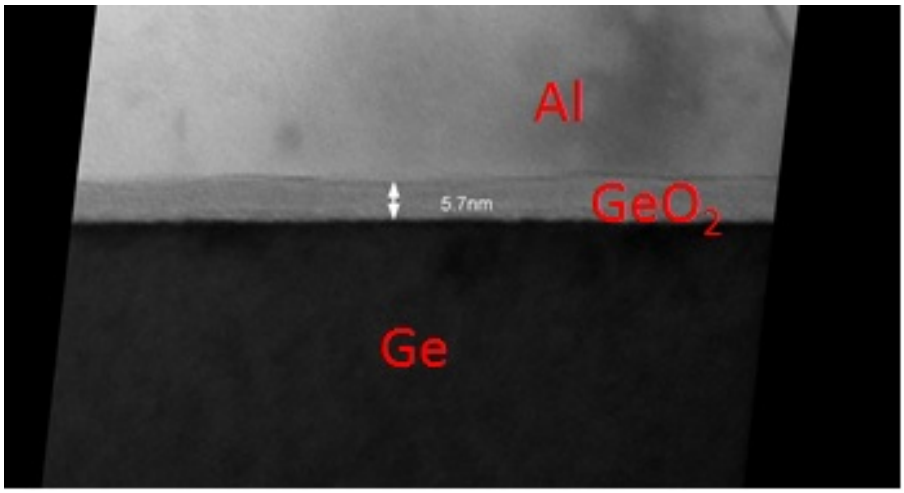


Figure 6.25: Cross-sectional TEM images of the sample oxidized at 600°C for 30 minutes.

a second peak at 30.1 eV corresponding to the oxidation state Ge^{+1}. In Figure 6.30 it is possible to observe the Ge peak at 28.8 eV. Three other peaks are observable, after fitting with Voigt functions, the Ge^{+1}, the Ge^{+4} and states related to oxides from the bulk.

Figure 6.27 and Figure 6.28 represent the XPS spectra for the sample oxidised at 500°C for 45 minutes, before and after additional annealing, respec-

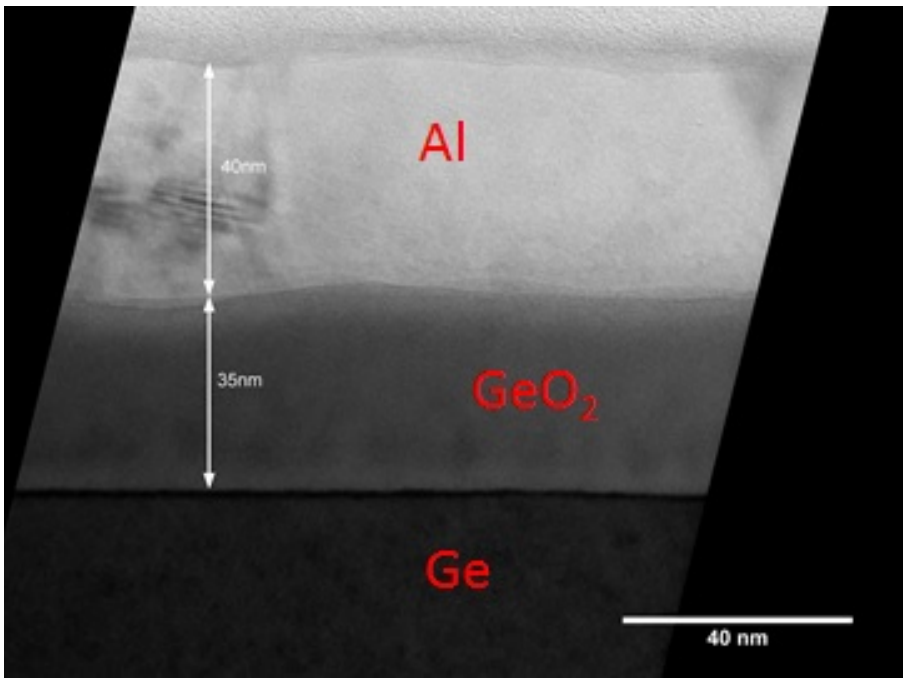


Figure 6.26: Cross-sectional TEM images of the sample oxidized at 600°C for 45 minutes.

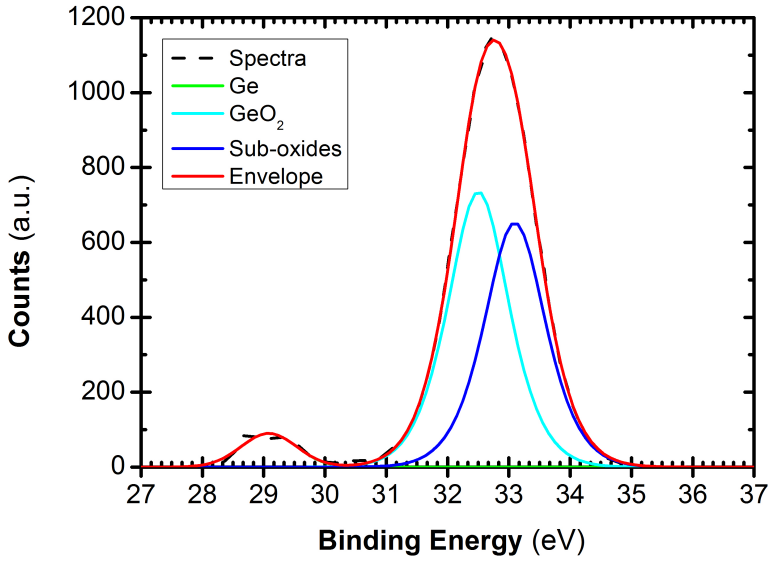


Figure 6.27: XPS Ge *3d* spectra for the as-grown sample oxidized at 500°C for 45 minutes.

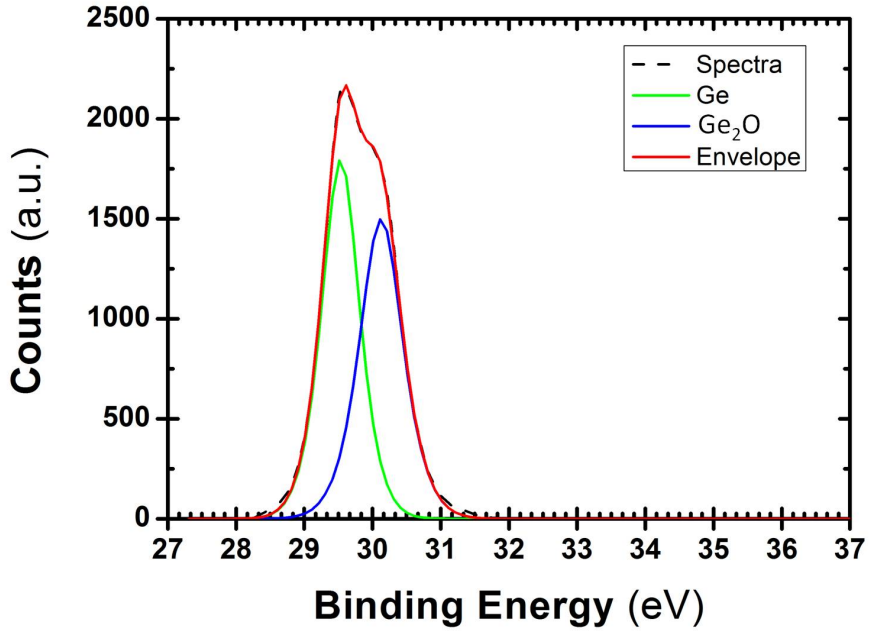


Figure 6.28: XPS Ge *3d* spectra for sample oxidized at 500°C for 45 minutes after annealing at 500°C.

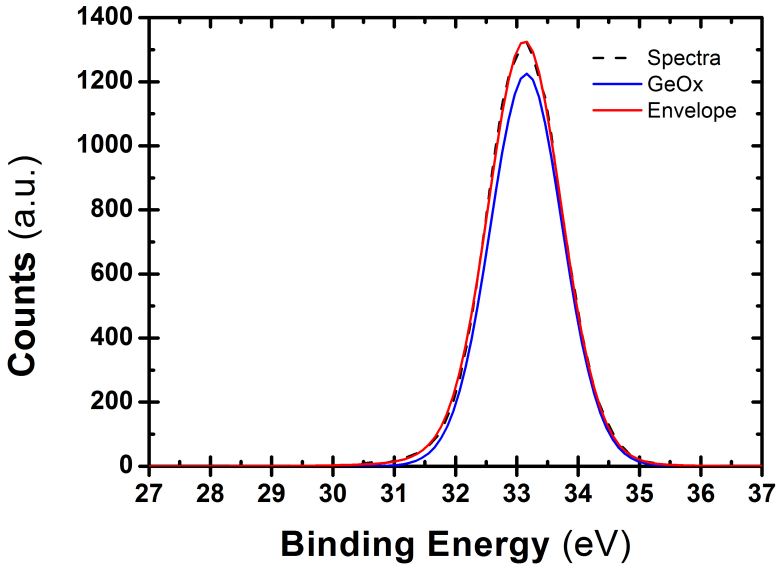


Figure 6.29: XPS Ge *3d* spectra for the as-grown sample oxidized at 550°C for 30 minutes.

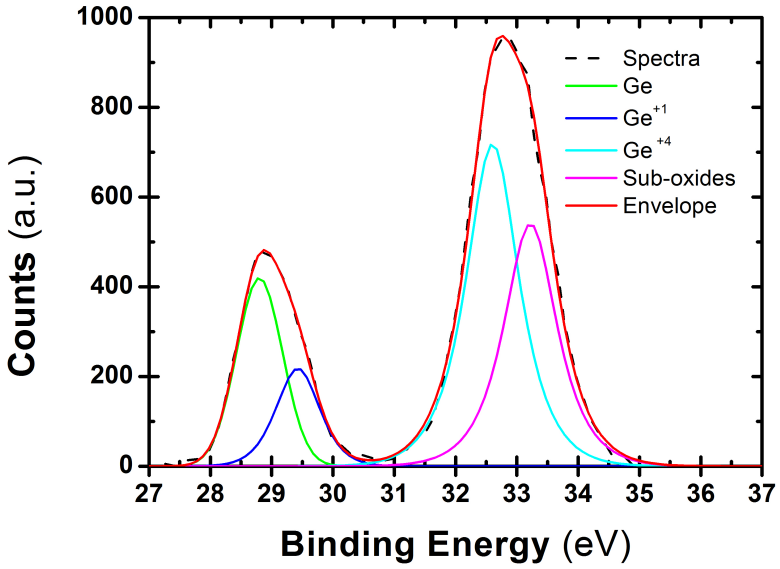


Figure 6.30: XPS Ge *3d* spectra for the sample oxidized at 550°C for 30 minutes after annealing at 550°C.

tively. The CV curves show good behaviour even though the XPS indicates that two sub species of germanium oxide are present in the oxide. In the sample grown at 550°C it is not possible to observe the Ge peak for the as-grown sample (Figure 6.29) and only the GeO_2 peak is present. With increasing annealing temperature for both samples, see Figure 6.31 and Figure 6.32, it is possible to observe a shift towards lower binding energies of the GeO_x peak indicating desorption of the GeO.

Figure 6.31 and Figure 6.32 shows the XPS spectra taken after each annealing for samples grown at 500°C and 550°C. It is possible to observe the behaviour of GeO_2 with temperature. In Figure 6.32 only after annealing at 500°C it is possible to observe the Ge peak.

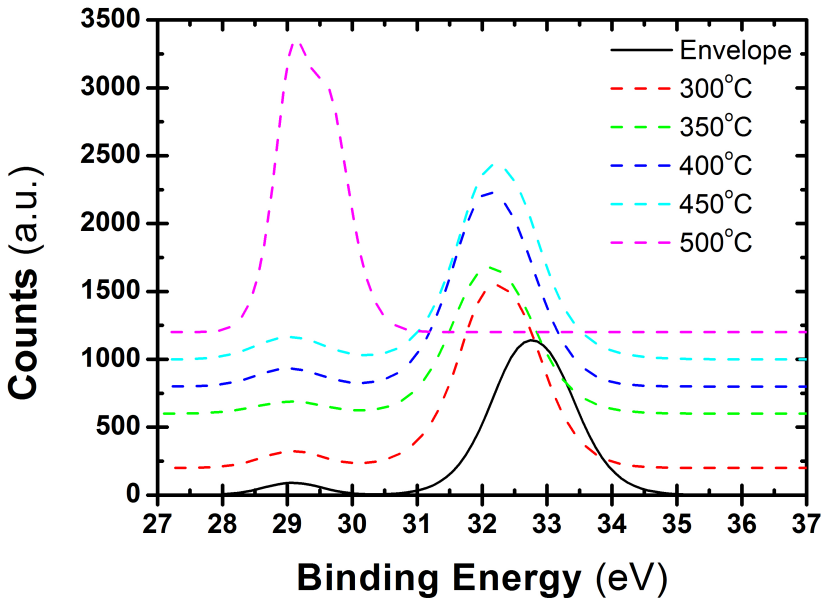


Figure 6.31: XPS Ge *3d* spectra as function of anneal temperature for samples oxidised at 500°C for 45 minutes.

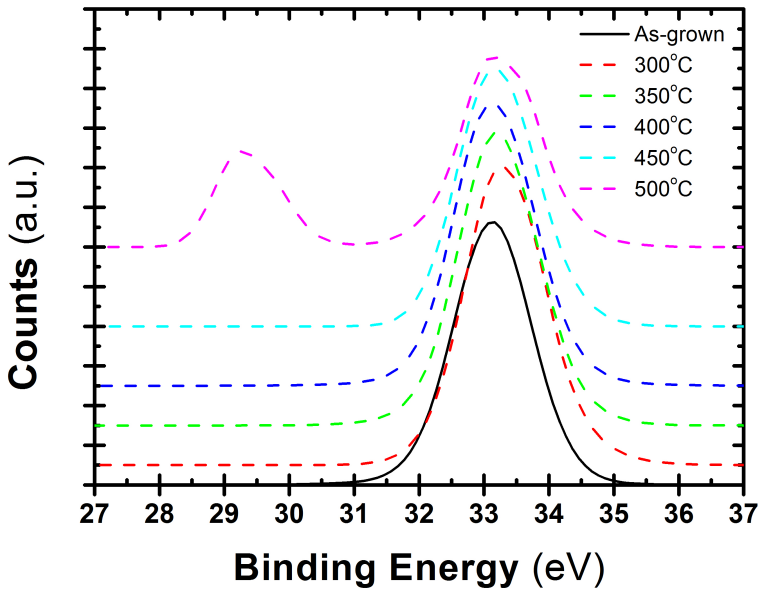


Figure 6.32: XPS Ge *3d* spectra as function of anneal temperature for samples oxidised at 550°C for 30 minutes.

6.6 Discussion

In the test oxidation, see Figure 6.6 and Figure 6.7, we obtained very good electrical characteristics especially for the sample grown at 475°C for 30 minutes, with negligible frequency dispersion. However, at 450°C a bump can be seen in the depletion region indicating the presence of interface traps. The interface trap density, D_{it}, was estimated by the high-low frequency method to be of the order of $10^{10}\text{cm}^{-2}\text{eV}^{-1}$ for the three samples. Looking at the TEM images the GeO_2 layer is not very well defined, not being possible to exactly say where the layer starts. Looking at the samples grown at 475°C it is possible to observe an improvement in the quality of the GeO_2, see Figure 6.8, Figure 6.9 and Figure 6.10. The frequency dispersion observed for the sample oxidised at 475°C for 60 minutes (Figure 6.7(b)) can be attributed to a bad capacitor which can explain the discrepancy between the oxide thickness values obtained by electrical and physical measurements. The flatland voltage for the three devices shows a small shift from the ideal curve.

In the second oxidation, the oxidation failed and it was not possible to obtain good device characteristics except for the sample treated at 500°C for 10 minutes. It was not possible to observe any oxide layers in the TEM images. The lack of oxidation can be attributed to a bad position of the sample in the tube since, as it was shown, at the ends of the tube the temperature is much lower. Also, for this batch the oxidation times used were smaller, and presumably too short for an oxide to be formed at the low temperatures used in the tube. Instead all the characterisation measurements will be of a low quality native oxide layer, either pre-existing or formed during the time between (non-)oxidation and characterisation. Looking at Figure 1.8 no bump

is observed, also a negligibility frequency dispersion is observed. The interface trap density was estimated to be in the order of $10^{10}\text{cm}^{-2}\text{eV}^{-1}$, by the high-low frequency method. The significant characteristic is the hysteresis which increases frequency. This hysteresis reaches 363 mV for 10 kHz demonstrating just how poor this oxide layer is.

In the next oxidation batch, it was possible to obtain good quality GeO_2 layers. No bumps in the depletion region and no frequency dispersion is observed for any of the samples. However, the stretch out of the high frequency curve is an indication of the presence of interface traps in significant densities. The D_{it} was estimated, from the high-low frequency method, to be around $10^{10}\text{cm}^{-2}\text{eV}^{-1}$. Hysteresis is observable for all samples, being highest for the sample grown at 600°C. There is some discrepancy between the oxide thickness values obtained from electrical and physical characterization. The values are general higher when obtained from the CV curves. It is expected to have an increase in thickness with increasing oxidation temperature and oxidation time, and this trend is partial seen if the values considered are the ones determined from the CV curves. The TEM images show good quality layers for all the samples measured, but the thickness values obtained must be considered to be less reliable.

6.7 Summary

In summary, GeO_2 have been thermally grown on an epitaxial Ge-on-Si(001) substrate. We have shown a simple method to grow GeO_2 while achieving good electrical characteristics. The values of D_{it} estimated in this work are of the same order as in previous works with more complicated pro-

cesses. Lee *et al.* [44] has obtained a $D_{it} = 2 \times 10^{11}\text{eV}^{-1}\text{cm}^{-2}$ by performing high pressure oxidation, Zhang *et al.* [6] obtained a $D_{it} = 1.7 \times 10^{11}\text{eV}^{-1}\text{cm}^{-2}$ for an EOT of 1.2 nm. The samples were grown by Plasma Post Oxidation. In [7] Zhang *et al.* maintained these values for lower values of EOT (0.8 nm).

From the TEM images taken of the oxide, it is clear that the layer quality is good, as it does not show irregularities at the interface. The layers appear to be smooth and no diffusion is observed.

The XPS data shows the presence of GeO_2 on the layers grown, as well as other sub-oxides that don't seem to contribute to the device degradation. After annealing it is possible to observe the peak shifts for lower binding energies showing the oxide desorption, with peaks due to lower oxidation states, and consequently, different oxide peaks, appear. The difference in oxide thickness measured by TEM and CV characterisation may be explained by the non-uniformity of growth and the consumption of GeO_2 during sample preparation.

In order to obtain a more reliable value for D_{it}, the full conductance method should be employed. Also, there are still issues with reproducibility of the results. The difference in oxide thickness between the different oxidations can be due to the cleanliness of the quartz tube. Some residues from previous oxidation might remain in the tube after purging and warming of tube. This issue should also be addressed in future growths.

Chapter 7

Conclusion

In this investigation different types of Ge devices have been studied.

The epilayers for the devices were grown at Warwick by RPCVD, except for the control relaxed wafer which was grown at IMEC. The devices investigated in chapter 4 were deposited by ALD the dielectric used in these devices was HfO_2. For chapter 6, the GeO_2 layers were grown at Warwick by thermal oxidation, on top of the GeO_2 Al was deposited. The samples were characterised both electrically and physically.

In chapter 4, the effect of different growth parameters on the mobility of holes in Ge MOSFETs was investigated: Ge passivation scheme, channel thickness and doping concentration. For these devices, the SiH_4 passivation scheme showed better device performance, mobility for this passivation scheme being 1.3 times higher than observed for the Si_3H_8 passivation scheme. The devices with different channel thickness did not show a significant difference in mobility. The same was observed for devices with different doping concentrations. However, an enhancement of 50% in mobility was observed for strained germanium devices relatively to the relaxed germanium ones. For the devices under study the parameter that has most influenced device performance was strain. This can be explained by the fact that these devices were fabricated

without extensions and halos that are used to prevent the diffusion of Ge to the channel, which is a factor known to degrade mobility.

In chapter 5, strained Ge heterostructures grown with different processes were studied using magnetotransport measurements. The first sample was an heterostructure grown partially by CVD and partially by MBE. The mobility obtained for this sample was lower than expected, this can be due to the fact that the contacts show some defects at the surface. Nevertheless, it was possible to observe SdH oscillation until 7.4 K indicating good quality layers. The second sample was completely grown by CVD and the device was fabricated by etching all the layers until the substrate in order to minimize parallel conduction due to the fabrication process. From the magnetoresistance curves it is possible to observe a background, almost, linear dependence with field. For these sample it was possible to observe the SdH oscillations at lower fields, around 0.2 T at 300 mK. There seems to have two different set of peaks appearing. One at lower field and the second at higher fields. However, the behaviour of these peaks is not the same at different temperatures. It seems there are more than one path through which carrier can move; however, the carrier density obtain by SdH oscillations and Hall voltage slope is the same which contradicts this idea.

In chapter 6, GeO_2 was thermally grown on epitaxial Ge-on-Si(100) substrates. TEM images show good quality GeO_2 layers, with a smooth Ge-GeO_2 interface. The CV characteristics do not show frequency dispersion and the hysteresis was not significant, indicating a lower carrier concentration and lower interface trap density. The XPS study shows the presence of GeO_2 in all samples as well the presence of sub-oxides, GeO_x. The presence of these sub-oxides do not seem to change the layer quality. It was also possible to

observe the desorption of GeO after annealing the sample. With this simple process it was possible to obtain devices with characteristics comparable with early works.

In summary, this investigation has demonstrated many interesting features of hole transport in germanium devices and how this is affected by the sample and device processing. It has shown that strained Ge is an exciting material for future device applications and that further work in this field would be justified. In each section there have been new discoveries and yet also unanswered questions that could be used to guide a future project in this area.

Bibliography

[1] G E Moore. Cramming more components onto integrated circuits. *Electronics*, **38**(8):4, 1965.

[2] Simon M. Sze. *Physics of Semiconductor Devices.* John Wiley and Sons Inc., second edition, 1981.

[3] C. Claeys, J. Mitard, G. Eneman, M. Meuris, and E. Simoen. Si versus Ge for future microelectronics. *Thin Solid Films*, **518**(9):6, 2010.

[4] S. Dutta Gupta, J. Mitard, G. Eneman, B. De Jaeger, M. Meuris, M.M. M Heyns, and S D Gupta. Performance enhancement in Ge pMOSFETs with ¡1 0 0¿ orientation fabricated with a Si-compatible process ow. *Microelectronic Engineering*, **87**(11):4, November 2010.

[5] D. P. Brunco, B. De Jaeger, G. Eneman, J. Mitard, G. Hellings, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, G. Winderickx, E. Vrancken, S. Sioncke, K. Opsomer, G. Nicholas, M. Caymax, A. Stesmans, J. Van Steenbergen, P. W. Mertens, M. Meuris, and M. M. Heyns. Germanium mosfet devices: Advances in materials understanding, process development, and electrical performance. *Journal of The Electrochemical Society*, **155**(7):H552–H561, 2008.

[6] Rui Zhang, Takashi Iwasaki, Noriyuki Taoka, Mitsuru Takenaka, and S Takagi. High-Mobility Ge pMOSFET With 1-nm EOT

Al2O3/GeOx/Ge Gate Stack Fabricated by Plasma Post Oxidation. *IEEE Transactions on Electron Devices*, **59**(2):335–341, 2012.

[7] Rui Zhang, Po-Chin Huang, Ju-Chin Lin, N. Taoka, M. Takenaka, and S. Takagi. High-mobility ge p- and n-mosfets with 0.7-nm eot using $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks fabricated by plasma postoxidation. *Electron Devices, IEEE Transactions on*, **60**(3):927–934, 2013.

[8] Qi Xie, Shaoren Deng, Marc Schaekers, Dennis Lin, Matty Caymax, Annelies Delabie, Xin-ping Qu, Yu-long Jiang, and Davy Deduytsche. Germanium surface passivation and atomic layer deposition of high-k dielectrics a tutorial review on Ge-based MOS capacitors. *Semiconductor Science and Technology*, **27**:074012, 2012.

[9] J.H. H Choi, Y. Mao, and J.P. P Chang. Development of hafnium based high-k materialsA review. *Materials Science and Engineering R*, **72**(6):40, July 2011.

[10] S Takagi, T Irisawa, T Tezuka, T Numata, S Nakaharai, N Hirashita, Y Moriyama, K Usuda, E Toyoda, S Dissanayake, M Shichijo, R Nakane, S Sugahara, M Takenaka, and N Sugiyama. Carrier-Transport-Enhanced Channel CMOS for Improved Power Consumption and Performance. *IEEE Transaction Electron Device Letters*, **55**(1):19, 2008.

[11] S. Takagi and M. Takenaka. Advanced cmos technologies using iii-v/ge channels. In *VLSI Technology, Systems and Applications (VLSI-TSA), 2011 International Symposium on*, pages 1–2, 2011.

[12] S. Takagi, S.-H. Kim, M. Yokoyama, R. Zhang, N. Taoka, Y. Urabe, T. Yasuda, H. Yamada, O. Ichikawa, N. Fukuhara, M. Hata, and M. Tak-

enaka. High mobility {CMOS} technologies using iiiv/ge channels on si platform. *Solid-State Electronics*, **88**(0):2 – 8, 2013.

[13] Chris Beer. *Fabrication and Characterisation of Novel Ge MOSFETs*. PhD thesis, The University of Warwick, 2007.

[14] Andrew Dobbie. *Investigation of the Electrical Properties of $Si_{1-x}Ge_x$ Channel pMOSFETs with High-κ Dielectrics*. PhD thesis, The University of Warwick, 2007.

[15] F Schaffler. High-mobility Si and Ge structures. *Semiconductor Science and Technology*, **12**:1515–1549, 1997.

[16] M V Fischetti and S E Laux. Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys. *Journal of Applied Physics*, **80**(4):2234–2252, 1996.

[17] D W Palmer. Properties of the iii-v compound semiconductors, 2006.

[18] The general properties of si, ge, sige, sio_2 and si_3n_4, 2002.

[19] E. Kasper, A. Schuh, G. Bauer, B. Hollnder, and H. Kibbel. Test of vegard's law in thin epitaxial sige layers. *Journal of Crystal Growth*, **157**(14):68 – 72, 1995.

[20] J. P. Dismukes, L. Ekstrom, and R. J. Paff. Lattice parameter and density in germanium-silicon alloys1. *The Journal of Physical Chemistry*, **68**(10):3021–3027, 1964.

[21] T E Whall and E H C Parker. SiGe heterostructures for FET applications. *Journal of Physics D: Applied Physics*, **31**:1397–1416, 1998.

[22] J.W. Matthews and A.E. Blakeslee. Defects in epitaxial multilayers: I. misfit dislocations. *Journal of Crystal Growth*, **27**(0):118 – 125, 1974.

[23] R. People and J. C. Bean. Calculation of critical layer thickness versus lattice mismatch for gexsi1x/si strainedlayer heterostructures. *Applied Physics Letters*, **47**(3):322–324, 1985.

[24] R. People and J. C. Bean. Erratum: Calculation of critical layer thickness versus lattice mismatch for gexsi1x/si strainedlayer heterostructures [appl. phys. lett. 47, 322 (1985)]. *Applied Physics Letters*, **49**(4):229–229, 1986.

[25] V A Shah, A Dobbie, M Myronov, D J F Fulgoni, L J Nash, and D R Leadley. Reverse graded relaxed buffers for high Ge content SiGe virtual substrates. *Applied Physics Letters*, **93**(19):3, 2008.

[26] Vishal A. Shah. *Reverse Graded High Content (x=0.75)* $Si_{1-x}Ge_x$. PhD thesis, The University of Warwick, 2009.

[27] V. A. Shah, A. Dobbie, M. Myronov, and D. R. Leadley. Reverse graded sige/ge/si buffers for high-composition virtual substrates. *Journal of Applied Physics*, **107**(6):–, 2010.

[28] V. Destefanis, D. Rouchon, J. M. Hartmann, a. M. Papon, L. Baud, a. Crisci, and M. Mermoux. Structural properties of tensily strained Si layers grown on SiGe(100), (110), and (111) virtual substrates. *Journal of Applied Physics*, **106**(4):043508, 2009.

[29] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald. Controlling threading dislocation densities in ge on si using

graded sige layers and chemical-mechanical polishing. *Applied Physics Letters*, **72**(14):1718–1720, 1998.

[30] Y Bogumilowicz, J M Hartmann, R Truche, Y Campidelli, G Rolland, and T Billon. Chemical vapour etching of si, sige and ge with hcl; applications to the formation of thin relaxed sige buffers and to the revelation of threading dislocations. *Semiconductor Science and Technology*, **20**(2):127, 2005.

[31] Y. Bogumilowicz, J.M. Hartmann, F. Laugier, G. Rolland, T. Billon, N. Cherkashin, and A. Claverie. High germanium content sige virtual substrates grown at high temperatures. *Journal of Crystal Growth*, **283**(34):346 – 355, 2005.

[32] C. H. Lee, T. Nishimura, T. Tabata, S. K. Wang, K. Nagashio, K. Kita, and a. Toriumi. Ge MOSFETs Performance: Impact of Ge Interface Passivation. *IDEM 2010*, **2**:4, December 2010.

[33] M Caymax, S Van Elshocht, M Houssa, A Delabie, T Conard, M Meuris, S Van Elshocht, M M Heyns, A Dimoulas, S Spiga, M Fanciulli, J W Seo, and L V Goncharova. HfO2 as gate dielectric on Ge: Interfaces and deposition techniques. *Materials Science and Engineering: B*, **135**(3):256–260, 2006.

[34] P C McIntyre, D. Chi, C O Chui, H. Kim, K.-Ill Seo, K Saraswat, R Sreenivasan, T Sugawara, F S Aguirre-Testado, and R. M. Wallace. Interface Layers for high-k/Ge gate stacks:are they necessary? *ECS Transactions*, **3**(7):519–530, 2006.

[35] John Robertson. High dielectric constant gate oxides for metal oxide si transistors. *Reports on Progress in Physics*, **69**(2):327, 2006.

[36] Chi On Chui, Fumitoshi Ito, and Krishna C Saraswat. Nanoscale Germanium MOS DielectricsPart I: Germanium Oxynitrides. *IEEE ELECTRON DEVICE LETTERS*, **53**(7):8, 2006.

[37] C O Chui, H Kim, D Chi, P C McIntyre, and K C Saraswat. Nanoscale Germanium MOS DielectricsPart II: High-κ Gate Dielectrics. *IEEE TRansaction Electron device Letters*, **53**(7):8, 2006.

[38] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi. Impact of GeOx interfacial layer thickness on Al2O3/Ge MOS interface properties. *Microelectronic Engineering*, **88**(7):4, July 2011.

[39] R Zhang, T Iwasaki, N Taoka, M Takenaka, and S Takagi. Suppression of ALD-Induced Degradation of Ge MOS Interface Properties by Low Power Plasma Nitridation of GeO2. *Journal of Electrochemical Society*, **158**(8):7, 2011.

[40] M Caymax, F Leys, J Mitard, K Martens, L J Yang, G Pourtois, W Vandervorst, M Meuris, and R Loo. The Influence of the Epitaxial Growth Process Parameters on Layer Characteristics and Device Performance in Si-Passivated Ge pMOSFETs. *Journal of the Electrochemical Society*, **156**(12):H979–H985, 2009.

[41] O S Yoo, J Oh, K S Min, C Y Kang, B H Lee, K T Lee, M K Na, H M Kwon, P Majhi, H H Tseng, R Jammy, J S Wang, and H D Lee. Effect of Si capping layer on the interface quality and NBTI of high mobility

channel Ge-on-Si pMOSFETs. *Microelectronic Engineering*, **86**(3):259–262, 2009.

[42] B. Vincent, R. Loo, W. Vandervorst, J. Delmotte, B. Douhard, V.K. Valev, M. Vanbel, T. Verbiest, J. Rip, B. Brijs, T. Conard, C. Claypool, S. Takeuchi, S. Zaima, J. Mitard, B. De Jaeger, J. Dekoster, and M. Caymax. Si passivation for ge pmosfets: Impact of si cap growth conditions. *Solid-State Electronics*, **60**(1):116 – 121, 2011. Papers Selected from the 5th International SiGe Technology and Devices Meeting (ISTDM 2010).

[43] Jerome Mitard, Brice De Jaeger, Geert Eneman, Andrew Dobbie, Maksym Myronov, Masaharu Kobayashi, Jef Geypen, Hugo Bender, Benjamin Vincent, Raymond Krom, Jacopo Franco, Gillis Winderickx, Evi Vrancken, Wendy Vanherle, Wei-e W.-E. Wei-E. Wang, Joshua Tseng, Roger Loo, Kristin De Meyer, Matty Caymax, Luigi Pantisano, David R. Leadley, Marc Meuris, Philippe P. Absil, Serge Biesemans, Thomas Hoffmann, David R Leadley Ã, and Si Ge. High Hole Mobility in 65 nm Strained Ge p-Channel Field Effect Transistors with HfO 2 Gate Dielectric. *Japanese Journal of Applied Physics*, **50**(4):5, April 2011.

[44] Choong Hyun Lee, Toshiyuki Tabata, Tomonori Nishimura, Kosuke Nagashio, Koji Kita, and Akira Toriumi. Ge/GeO 2 Interface Control with High-Pressure Oxidation for Improving Electrical Characteristics. *Applied Physics Express*, **2**(7):071404, July 2009.

[45] Y Fukuda, Y Yazaki, Y Otani, T Sato, H Toyota, and T Ono. Low-Temperature Formation of High-Quality GeO2 Interlayer for High-kappa

Gate Dielectrics/Ge by Electron-Cyclotron-Resonance Plasma Techniques. *Ieee Transactions on Electron Devices*, **57**(1):282–287, 2010.

[46] F. Bellenger, M. Houssa, a. Delabie, V V Afanas'ev, T. Conard, M. Caymax, M. Meuris, K. De Meyer, M. M. Heyns, and V. Afanasiev. Passivation of Ge(100)/GeO(2)/high-kappa gate stacks using thermal oxide treatments. *Journal of the Electrochemical Society*, **155**(2):G33–G38, 2008.

[47] Duygu Kuzum, Tejas Krishnamohan, Abhijit J. Pethe, Ali K. Okyay, Yasuhiro Oshima, Yun Sun, James P. McVittie, Piero a. Pianetta, Paul C. McIntyre, and Krishna C. Saraswat. Ge-Interface Engineering With Ozone Oxidation for Low Interface-State Density. *IEEE Electron Device Letters*, **29**(4):328–330, April 2008.

[48] Hiroshi Matsubara, Takashi Sasada, Mitsuru Takenaka, and Shinichi Takagi. Evidence of low interface trap density in GeO2 / Ge metal-oxide- semiconductor structures fabricated by thermal oxidation. *Applied Physics Letters*, **93**(3):032104, 2008.

[49] Sheng Kai Wang, Koji Kita, Choong Hyun Lee, Toshiyuki Tabata, Tomonori Nishimura, Kosuke Nagashio, and Akira Toriumi. Desorption kinetics of GeO from GeO_2/Ge structure. *Journal of Applied Physics*, **108**(5):054104, 2010.

[50] Charles Hawkins and Jaume Segura. *Introduction to Digital Electronics*. Scitech Pub Inc, first edition, 2010.

[51] Stephen Michael Thomas. *Electrical Characterisation of Novel Silicon MOSFETs and finFETs*. PhD thesis, The University of Warwick, 2011.

[52] J.R. Brews. A charge-sheet model of the {MOSFET}. *Solid-State Electronics*, **21**(2):345 – 355, 1978.

[53] Simon M. Sze and Kwok K. Ng. *Physics of Semiconductor Devices.* John Wiley and Sons Inc., third edition, 1981.

[54] Gareth Nicholas. *Investigation of the electronic properties of tensile strained silicon MOSFETs.* PhD thesis, The University of Warwick, 2004.

[55] Mark Lundstrom. *Fundamentals of carrier transport.* Cambridge University Press, second edition, 2000.

[56] B. Laikhtman and R. A. Kiehl. Theoretical hole mobility in a narrow si/sige quantum well. *Physical Review B*, **47**:10515–10527, Apr 1993.

[57] Tsuneya Ando, B Fowler, Frank Stern, I B M Thomas J, and B Devices. Electronic properties of two-dimensional systems. *Reviews of Modern Physics*, **54**(2):437–672, 1982.

[58] D R Leadley, M J Kearney, A I Horrell, H Fischer, L Risch, E H C Parker, and T E Whall. Analysis of hole mobility and strain in a si/si 0.5 ge 0.5 /si metal oxide semiconductor field effect transistor. *Semiconductor Science and Technology*, **17**(7):708, 2002.

[59] Daniel Chrastina. *Transport in Silicon-Germanium Heterostructures.* PhD thesis, University of Warwick, 2001.

[60] John H. Davies. *The Physics of Low-Dimensional Semiconductors.* Cambridge University Press, first edition, 2006.

[61] A Isihara and L Smrcka. Density and magnetic field dependences of the conductivity of two-dimensional electron systems. *Journal of Physics C: Solid State Physics*, **19**(34):6777, 1986.

[62] Maksym Myronov. *Magnetotransport, structural and optical characterization of p-type modulation doped heterostructures with high Ge content $Si_{1x}Ge_x$ channel grown by SS-MBE on $Si_{1y}Ge_y$/Si(001) virtual substrates*. PhD thesis, The University of Warwick, 2001.

[63] K. Y. Suh and Hong H. Lee. Ge composition in si1xgex films grown from sih2cl2/geh4 precursors. *Journal of Applied Physics*, **88**(7):4044–4047, 2000.

[64] B. A. Ferguson, C. T. Reeves, D. J. Safarik, and C. B. Mullins. Silicon deposition from disilane on si(100)-21: Microscopic model including adsorption. *Journal of Applied Physics*, **90**(10):4981–4989, 2001.

[65] Arash Salemi. Low temperature epitaxy growth and kinetic modeling of sige for bicmos application. Master's thesis, KTH, Royal Institute of technology, 2011.

[66] Sami Franssila. *Introduction to microfabrication.* John Wiley and Sons Inc., second edition, 2010.

[67] Annelies Delabie, David P. Brunco, Thierry Conard, Paola Favia, Hugo Bender, Alexis Franquet, Sonja Sioncke, Wilfried Vandervorst, Sven Van Elshocht, Marc Heyns, Marc Meuris, Eunji Kim, Paul C. McIntyre, Krishna C. Saraswat, James M. LeBeau, Joel Cagnon, Susanne Stemmer, and Wilman Tsai. Atomic Layer Deposition of Hafnium Oxide on Ge

and GaAs Substrates: Precursors and Surface Preparation. *Journal of The Electrochemical Society*, **155**(12):H937, 2008.

[68] Takuya Sugawara, Yasuhiro Oshima, Raghavasimhan Sreenivasan, and Paul C McIntyre. Electrical properties of germanium/metal-oxide gate stacks with atomic layer deposition grown hafnium-dioxide and plasma-synthesized interface layers. *Applied Physics Letters*, **90**(11), 2007.

[69] Paul C McIntyre, Yasuhiro Oshima, Eunji Kim, and Krishna C Saraswat. Interface studies of ALD-grown metal oxide insulators on Ge and III-V semiconductors. *Microelectronic Engineering*, **86**(7-9):1536–1539, 2009.

[70] G D Wilk, M L Green, M.-Y. Hot, B W Busch, T W Sorsch, F P Klemens, B Brijs, R B van Dover, A Komblit, T Gustafsson, E Garfunkel, S Hillenius, D Monroe, P Kalavade, and J M Hergenrother. Improved Film Growth and Flatband Voltage (Control of ALD Hf02 and Hf-AI-0 with n+ poly-Si Gates using Chemical Oxides and Optimized Post-Annealing. In *Symposium on VLSI Technology Digest of Technical Papers*, page 2, 2002.

[71] Annelies Delabie, Riikka L. Puurunen, Bert Brijs, Matty Caymax, Thierry Conard, Bart Onsia, Olivier Richard, Wilfried Vandervorst, Chao Zhao, Marc M. Heyns, Marc Meuris, Minna M. Viitanen, Hidde H. Brongersma, Marco de Ridder, Lyudmila V. Goncharova, Eric Garfunkel, Torgny Gustafsson, and Wilman Tsai. Atomic layer deposition of hafnium oxide on germanium substrates. *Journal of Applied Physics*, **97**(6), 2005.

[72] A Delabie, A Alian, F Bellenger, M Caymax, T Conard, A Franquet,

S Sioncke, S Van Elshocht, M M Heyns, and M Meuris. H2O- and O3 -Based Atomic Layer Deposition of High-k Dielectric Films on GeO2 Passivation Layers. *Journal of Electrochemical Society*, **156**(10):5, 2009.

[73] Siegfried Hofmann. *Auger- and X-ray Photoelectron Spectroscopy in Material Science.* Springer., first edition, 2013.

[74] John C. Vickerman and Ian S. Gilmore. *Surface Analysis The Principal Techniques.* John Wiley and Sons Inc., second edition, 2009.

[75] Dieter K. Schroeder. *Semiconductor Material and Device Characterization.* John Wiley and Sons Inc., third edition, 2006.

[76] Safa Kasap and Peter Capper. *Springer Handbook of Electronic and Photonic Materials.* Springer, first edition, 2006.

[77] Tak H Taur and Ning Yang. *Fundamentals of Modern VLSI Devices.* Cambridge University Press, first edition, 1998.

[78] Martin J. Palmer. *Investigation of high mobility pseudomorphic SiGe p-channels in Si MOSFETs at low and high electric fields.* PhD thesis, The University of Warwick, 2001.

[79] P. Zimmerman, G Nicholas, B De Jaeger, B Kaczer, A Stesmans, L- Ragnarsson, D P Brunco, F E Leys, M Caymax, G Winderickx, K Opsomer, M Meuris, and M M Heyns. High performance Ge pMOS devices using a Si-compatible process flow. In *IEEE International Electron Devices Meeting*, 2006.

[80] Lake Shore Inc. *Lake Shore 7500/9500 Series Hall System Users Manual.*

[81] Y F Komnik, V V Andrievskii, I B Berkutov, S S Kryachko, M Myronov, and T E Whall. Quantum effects in hole-type Si/SiGe heterojunctions. *Low Temperature Physics*, **26**(8):609–614, 2000.

[82] Suman Datta. Recent advances in high performance cmos transistors: From planar to non-planar. *The Electrochemical Society Interface*, **41**(1):41–46, 2013.

[83] S Desgreniers and K Lagarec. High-density ZrO2 and HfO2 : Crystalline structures and equations of state. *Physical Review B*, **59**(13):6, 1999.

[84] G Nicholas, T J Grasby, D J F Fulgoni, C S Beer, J Parsons, M Meuris, and M M Heyns. High Mobility Strained Ge pMOSFETs With High-κ/Metal Gate. *IEEE Electron Device Letters*, **28**(9):3, 2007.

[85] V. A. Shah, A. Dobbie, M. Myronov, D. J. F. Fulgoni, L. J. Nash, and D. R. Leadley. Reverse graded relaxed buffers for high ge content sige virtual substrates. *Applied Physics Letters*, **93**(19):–, 2008.

[86] Maksym Myronov, Andy Dobbie, Vishal a. Shah, Xue-Chao Liu, Van H. Nguyen, and David R. Leadley. High Quality Strained Ge Epilayers on a Si[sub 0.2]Ge[sub 0.8]/Ge/Si(100) Global Strain-Tuning Platform. *Electrochemical and Solid-State Letters*, **13**(11):H388, 2010.

[87] G. Eneman, M. Wiot, Antoine Brugere, O.S.I. Casain, S. Sonde, D.P. Brunco, B. De Jaeger, Alessandra Satta, G. Hellings, K. De Meyer, C. Claeys, M. Meuris, Marc M. Heyns, and E. Simoen. Impact of donor concentration, electric field, and temperature effects on the leakage current in germanium p +/ n junctions. *Electron Devices, IEEE Transactions on*, **55**(9):2287–2296, Sept 2008.

[88] J. Mitard, B. De Jaeger, F. E. Leys, G. Hellings, K. Martens, G. Eneman, D.P. Brunco, R. Loo, J.C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C. H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M.M. Heyns. Record ion/ioff performance for 65nm ge pmosfet and novel si passivation scheme for improved eot scalability. In *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pages 1–4, 2008.

[89] J. Mitard, C. Shea, B. DeJaeger, A. Pristera, G. Wang, M. Houssa, G. Eneman, G. Hellings, W. E Wang, J.C. Lin, F. E. Leys, R. Loo, G. Winderickx, E. Vrancken, A. Stesmans, K. DeMeyer, M. Caymax, L. Pantisano, M. Meuris, and M. Heyns. Impact of eot scaling down to 0.85nm on 70nm ge-pfets technology with sti. In *VLSI Technology, 2009 Symposium on*, pages 82–83, 2009.

[90] A. Dobbie, Van Huy Nguyen, R. J. H. Morris, Xue-Chao Liu, M. Myronov, and D. R. Leadley. Thermal Stability of Thin Compressively Strained Ge Surface Channels Grown on Relaxed Si0.2Ge0.8 Reverse-Graded Buffers. *Journal of The Electrochemical Society*, **159**(5):H490, 2012.

[91] G Ghibaudo. New method for the extraction of MOSFET parameters. *Electronic Letters*, **24**(9):13, 1988.

[92] D Fleury, A Cros, H Brut, and G Ghibaudo. New Y -Function-Based Methodology for Accurate Extraction of Electrical Parameters on Nano-Scaled MOSFETs. page 6, 2008.

[93] B. Vincent, R. Loo, W. Vandervorst, G. Brammertz, and M. Caymax.

Low temperature si homo-epitaxy by reduced pressure chemical vapor deposition using dichlorosilane, silane and trisilane. *Journal of Crystal Growth*, **312**(19):2671 – 2676, 2010.

[94] Toshifumi Irisawa, Hidetoshi Miura, Tetsuji Ueno, and Yasuhiro Shiraki. Channel width dependence of mobility in ge channel modulation-doped structures. *Japanese Journal of Applied Physics*, **40**(Part 1, No. 4B):2694–2696, 2001.

[95] Hasan M. Nayfeh, Christopher W. Leitz, Arthur J. Pitera, E.A. Fitzgerald, J.L. Hoyt, and D.A. Antoniadis. Influence of high channel doping on the inversion layer electron mobility in strained silicon n-mosfets. *Electron Device Letters, IEEE*, **24**(4):248–250, 2003.

[96] K Sawano, K Toyama, R Masutomi, T Okamoto, N Usami, K Arimoto, K Nakagawa, and Y Shiraki. Strain dependence of hole effective mass and scattering mechanism in strained Ge channel structures. *Applied Physics Letters*, **95**(12), 2009.

[97] I. B. Berkutov, V. V. Andrievskii, Yu. F. Komnik, Yu. A. Kolesnichenko, R. J. H. Morris, D. R. Leadley, and O. A. Mironov. Magnetotransport studies of sige-based p-type heterostructures: Problems with the determination of effective mass. *Low Temperature Physics*, **38**(12):1145–1152, 2012.

[98] A. Dobbie, M. Myronov, R. J. H. Morris, a. H. a. Hassan, M. J. Prest, V. a. Shah, E. H. C. Parker, T. E. Whall, and D. R. Leadley. Ultra-high hole mobility exceeding one million in a strained germanium quantum well. *Applied Physics Letters*, **101**(17):172108, 2012.

[99] M. Myronov, K. Sawano, D. R. Leadley, and Y. Shiraki. Very high mobility 2d holes in strained ge quantum well epilayers grown by reduced pressure chemical vapor deposition. In *International Conference on Solid State Devices and Materials*, volume 4, 2009.

[100] M. Myronov, T. Irisawa, S. Koh, O. a. Mironov, T. E. Whall, E. H. C. Parker, and Y. Shiraki. Temperature dependence of transport properties of high mobility holes in Ge quantum wells. *Journal of Applied Physics*, **97**(8):083701, 2005.

[101] S. R. M. da Silva, G. K. Rolim, G. V. Soares, I. J. R. Baumvol, C. Krug, L. Miotti, F. L. Freire, M. E. H. M. da Costa, and C. Radtke. Oxygen transport and GeO2 stability during thermal oxidation of Ge. *Applied Physics Letters*, **100**(19):191907, 2012.

[102] Koji Kita and Akira Toriumi. Origin of electric dipoles formed at high-k/SiO(2) interface. *Applied Physics Letters*, **94**(13):29–32, 2009.

[103] Koji Kita, Sho Suzuki, Hideyuki Nomura, Toshitake Takahashi, Tomonori Nishimura, Akira Toriumi, Koji K I T A Ã, Sho S Uzuki, Hideyuki N Omura, and Toshitake T Akahashi. Direct evidence of GeO volatilization from GeO(2)/Ge and impact of its suppression on GeO(2)/Ge metal-insulator-semiconductor characteristics. *Japanese Journal of Applied Physics*, **47**(4):2349–2353, April 2008.

[104] Wenwu Wang, Koji Akiyama, Wataru Mizubayashi, Toshihide Nabatame, Hiroyuki Ota, and Akira Toriumi. Effect of Al-diffusion-induced positive flatband voltage shift on the electrical characteristics of

Al-incorporated high-k metal-oxide-semiconductor field-effective transistor. *Journal of Applied Physics*, **105**(6), 2009.

[105] Sheng Kai Wang, Koji Kita, Tomonori Nishimura, Kosuke Nagashio, and Akira Toriumi. Kinetic Effects of O-Vacancy Generated by GeO$_{2}$/Ge Interfacial Reaction. *Japanese Journal of Applied Physics*, **50**(10):10PE04, October 2011.

[106] Sheng Kai Wang, Koji Kita, Tomonori Nishimura, Kosuke Nagashio, and Akira Toriumi. Isotope Tracing Study of GeO Desorption Mechanism from GeO(2)/Ge Stack Using (73)Ge and (18)O. *Japanese Journal of Applied Physics*, **50**(4), 2011.

[107] K Prabhakaran, F Maeda, Y Watanabe, and T Ogino. Thermal decomposition pathway of Ge and Si oxides: observation of a distinct difference. *Thin Solid Films*, **369**(1-2):289–292, July 2000.

[108] Jungwoo Oh and JoeC. Campbell. Thermal desorption of ge native oxides and the loss of ge from the surface. *Journal of Electronic Materials*, **33**(4):364–367, 2004.

[109] K Kutsuki, G Okamoto, T Hosoi, T Shimura, and H Watanabe. Germanium oxynitride gate dielectrics formed by plasma nitridation of ultrathin thermal oxides on Ge(100). *Applied Physics Letters*, **95**:3, 2009.

[110] H Koumo, Y Oniki, Y Iwazaki, and T Ueno. Effects of Structural Transformation of Metal-GeO2 Interface on Electrical Properties. *Journal of the Electrochemical Society*, **158**(6):5, 2011.

[111] Hiroshi Matsubara and Shinichi Takagi. Interface-controlled self-align

source/drain Ge pMOSFETs using thermally-oxidized GeO¡inf¿2¡/inf¿ interfacial layers. *2008 IEEE International Electron Devices Meeting*, **2**:1–4, December 2008.

[112] Yosuke Nakakita, Ryosho Nakakne, Takashi Sasada, Mitsuru Takenaka, and Shinichi Takagi. Interface-Controlled Self-Align Source/Drain Ge p-Channel MetalOxideSemiconductor Field-Effect Transistors Fabricated Using Thermally Oxidized GeO 2 Interfacial Layers. *Japanese Journal of Applied Physics*, **50**:010109, January 2011.

[113] J. M. Hartmann. Reduced pressurechemical vapor deposition of Ge thick layers on Si(001) for 1.31.55-μm photodetection. *Journal of Applied Physics*, **95**(10):5905, 2004.

[114] Jungyup Kim. *Germanium Surface Preparation Methods*. VDM Verlag Dr. Muller Aktiengesellschaft and Co. KG, first edition, 2008.

[115] K Kita, S K Wang, M Yoshida, C H Lee, K Nagashio, T Nishimura, A Toriumi, and Ieee. Comprehensive Study of GeO(2) Oxidation, GeO Desorption and GeO(2)-Metal Interaction - Understanding of Ge Processing Kinetics for Perfect Interface Control. In *2009 Ieee International Electron Devices Meeting*, pages 649–652, 2009.

[116] Shengkai K Wang, Koji Kita, Tomonori Nishimura, Kosuke Nagashio, and Akira Toriumi. 18O isotope tracing study of GeO Desorption from GeO2/Ge Structure. In *International Conference on Solid State Devices and Materials*, volume 4, pages 1002–1003, 2009.

[117] D Schmeisser, R D Schnell, A Bogen, F J Himpsel, Rieger. D., G Land-

gren, and J F Morar. Surface Oxidation States of Germanium. *Surface Science*, **172**:11, 1986.

[118] Alessandro Molle, Md. Nurul Kabir Bhuiyan, Grazia Tallarida, and Marco Fanciulli. In situ chemical and structural investigations of the oxidation of ge(001) substrates by atomic oxygen. *Applied Physics Letters*, **89**(8):083504, 2006.

[119] P. J. Cumpson. The thickogram: a method for easy film thickness measurement in xps. *Surface and Interface Analysis*, **29**(6):4, 2000.

[120] A. Dimoulas, G. Vellianitis, G. Mavrou, E. K. Evangelou, and A. Sotiropoulos. Intrinsic carrier effects in HfO2Ge metal insulator semiconductor capacitors. *Applied Physics Letters*, **86**(22):223507, 2005.