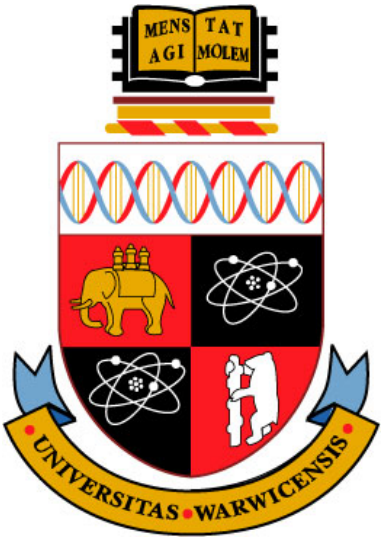

Electrical Characterisation and Modelling of Schottky barrier metal source/drain MOSFETs

by

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Thesis

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Declarations

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. Except where stated, all of the work described in this thesis was carried out by the author or under his direction. None of the work presented has been submitted for examination at any other institution.

Publications

The following publications contain material included in this thesis:

D. J. Pearman, G. Pailloncy, J.-P. Raskin, J. M. Larson, E. H. C. Parker, T. E. Whall, *"Static and High-frequency behavior and performance of Schottky Barrier p-MOSFET devices"*, accepted for publication in *IEEE Transactions on Electron Devices*.

D. J. Pearman, G. Pailloncy, J.-P. Raskin, J. M. Larson, E. H. C. Parker, T. E. Whall, *"High-frequency performance of Schottky Source/Drain Silicon pMOS devices"*, to be published.

Further publications arising from this work are currently in preparation.

Abstract

The motivation for the work presented in this thesis originates in the semiconductor industry's drive to create increasingly scaled transistors. In view of current device dimensions approaching fundamental atomic scales, the industry is looking to alternative structures to provide continued scaling capabilities.

The use of metal, usually silicide, source and drain regions to create Schottky barrier (SB-)MOSFETs is one such approach. Previous work on static and RF electrical characterisation as well as simulations has shown this device to provide a number of scaling benefits to the planar MOSFET structure. In addition, it provides simpler and more cost effective fabrication.

In this work, the electrical properties under DC bias conditions of p-channel SB-MOSFETs with PtSi sources and drains are explored at room temperature and down to 80 K. High room temperature ON currents up to 545 mA/mm and transconductances up to 640 mS/mm for 85 nm gate length devices are measured and performance factors are found to satisfy ITRS recommendations. Increasing silicide anneal temperatures lead to increases in Schottky barrier height and corresponding decreases in drain current are observed.

The radio-frequency performance at frequencies up to 110 GHz is studied using a novel measurement deembedding technique. High unity-gain cutoff frequencies up to 71 GHz are extracted. Finally, two-dimensional simulations using the drift-diffusion simulator MEDICI are performed and fitted to the measured electrical characteristics.

Chapter 1

Introduction

1.1 Background

Since its invention in 1947, the solid state transistor has revolutionised just about every aspect of our daily lives, be it work, home, entertainment, travel or communications, and has done so on a global scale. The transistor, in particular its predominant realisation in the form of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), has enabled the fabrication of devices ranging from the microscopic, such as the electronics in medical implants, to the vastly integrated, such as present in modern computer systems capable of mind-boggling calculations. This enourmous potential has been harnessed in many ways to provide machines capable of performing a wide range of operations, such as precise control of manufacturing equipment, storage of incredible amounts of information in vast databases, near instantaneous provision of information anywhere in the world or the creation life-like animated videos, to name a few.

Despite the incredible increase in performance of electronic hardware, both its size and price have dropped continuously and, more often than not, has become outdated within months. This phenomenal development has been the result of continual improvements in the fabrication techniques of integrated circuit (IC) packages, so-called chips. The

by far most common incarnation of the transistor is in the form of a MOSFET, a simple electronic switch. Its simple structure, the abundance of its fabrication material, silicon, and the ability to precisely define its processing steps have enabled incredible chip packing densities and circuit complexity levels to be achieved, thereby providing the basis for the fabrication of extremely complex electronic devices.

1.2 Scaling

The primary driver for the continual performance increases has been the scaling of the MOSFET from larger to smaller dimensions, thereby gaining both speed and integration level improvements [Wong, 2002]. This process involves the modification of MOSFET parameters, such as gate length, supply voltage and gate oxide thickness, by a factor commonly referred to as the *scaling factor* λ to gain corresponding speed and packing density improvements of λ. For nearly 40 years since its first statement in 1965 by George Moore, this development of IC performance and packing density has closely followed the so-called *Moore's Law* [Moore, 1965], which states that the number of devices per unit area on a chip as well as its performance double every 18 months. Indeed, this prediction has been followed so closely over several decades that the Semiconductor Industry Association (SIA) has regularly published roadmaps outlining future developments [International Technology Roadmap for Semiconductors, 2000 Update, 2001 Edition, 2003 Edition] with respect to various MOSFET parameters.

As transistors are continuously scaled, parasitic effects, so-called short channel effects (SCE), begin to diminish performance improvements and can lead to device failures. The most prevalent limitations observed to date are tunneling of carriers though the thin gate oxide, tunneling of carriers from drain to source and substrate, loss of control over doping profiles in channel, source and drain, leading to consequent reduction in ON-OFF current ratio, and finite subthreshold slope [Keyes, 2001, Packan, 1999, Wong, 2002].

Moreover, once these problems are solved, the next, and, as most scientists working in the area agree, final limit of fundamental atomic sizes looms. Scaling devices to sub-nm dimensions means that atomic scales are being approached and classical physics gives way to quantum mechanics. Given that the operation of a MOSFET is based on classical physics, this essentially spells the end of the conventional transistor. Current technology operates at scales of 45 - 90 nm, still well above the quantum physics regime and estimates predict another 5 to 10 years worth of scaling capability left in MOSFETs [International Technology Roadmap for Semiconductors, 2003 Edition].

1.3 Schottky Barrier Source/Drain Transistors

One proposed solution to the problematics relating to source and drain junctions is the introduction of metallic materials in place of conventional doped semiconductor regions. Rectifying metal-semiconductor junctions, so-called *Schottky barriers*, have very similar electrical characteristics to doped pn junctions and thus represent a simple replacement for the source and drain regions of a MOSFET. These so-called *Schottky barrier MOSFETs* provide a number of scaling benefits. Throughout this text, the acronym *SB-MOSFET* will be used when referring to Schottky barrier source/drain MOSFETs.

As junction depths are scaled to below 50 nm, source and drain series resistances become increasingly significant due to the reduction in cross-sectional area. This reduces drive current and counteracts benefits offered by scaling. Thompson et al. [1998] showed that scaling junctions to below 30 nm results in little or no performance benefits, since increases in source/drain resistance offset any improvements gained by scaling device.

By replacing the doped source and drain regions with a metal, their resistance is significantly reduced, even for very shallow junctions. Doing so makes the metal-semiconductor junction an integral part of the transistor. The reduction of source/drain resistances was

the original factor for investigating Schottky barrier MOSFETs for highly scaled devices, and subsequently other benefits were also discovered.

Benefits

As gate lengths are scaled down, the requirements for source/drain to channel junction abruptness become more stringent and require ever-increasing doping concentrations. Silicide-silicon junctions are inherently atomically abrupt, thus directly solving this problem and allowing very short physical channel lengths to be defined. As well as that, the Schottky barrier present at the interface between metallic source/drain and semiconducting channel provides a potential barrier to carriers in the OFF state, thus providing greater control over the OFF-state leakage current in short channel devices [Larson and Snyder, 2006]. Together with the low resistivity, these two factors represent the main benefits of Schottky barrier metal sources and drains to highly scaled MOSFET devices, though there are additional benefits, as described in the following.

Conventional doped source/drain (DSD) MOSFETs require a gate-to-source/drain overlap to prevent current from spreading to lower doping locations in the source/drain extensions, thereby increasing accumulation and spreading resistance. Thompson, Packan, and Bohr [1998] showed that reducing this overlap results in a degradation of saturation current.

SB-MOSFETs do not require these overlaps - in fact, the presence of an *underlap*, a gap between the edge of the gate and source/drain electrodes, is beneficial to SB-MOSFET performance [Koeneke et al., 1981]. The absence of gate-to-source/drain overlaps eliminates corresponding parasitic capacitances, which is of great importance for high-frequency applications. Because of this, SB-MOSFETs are thought to promise performance benefits for radio-frequency operation, as will be investigated in this work.

One problem in DSD MOSFETs is parasitic bipolar latchup between adjacent devices. For example, p-type source or drain and the n-type substrate of a p-channel device and the p-well of an adjacent n-channel transistor form a bipolar transistor and lead to parasitic conduction. Both npn and pnp parasitic bipolar latchup is entirely eliminated in SB-MOSFETs due to the presence of metallic materials in source and drain [Larson and Snyder, 2004, Sugoni et al., 1982].

Doped source/drain devices require high temperature RTAs of about 900 °C for dopant activation in source and drain implants. This is incompatible with proposed high-κ gate dielectrics required for further gate oxide scaling, which are damaged by such high temperature treatment. Silicides, such as PtSi or ErSi, form at much lower temperatures of 500 °C and lower, thereby maintaining compatibility with fabrication requirements for high-κ dielectrics.

In addition to lowering thermal budgets, SB-MOSFETs require fewer processing steps by not requiring source/drain extension and halo implants, dopant activation anneals and associated masking and cleaning steps [Larson and Snyder, 2004]. This is achieved with processes fully compatible with current CMOS fabrication technologies.

Challenges

Despite aforementioned benefits, there are a few issues preventing widespread adoption of SB-MOSFETs. The first concerns n-channel devices.

While most studies of SB-MOSFETs have centred around p-channel devices, relatively few investigations into n-channel devices have been made. Currently, the major obstacle for n-channel SB-MOSFETs is the lack of a suitable source/drain silicide for n-channel devices due to Fermi level pinning at the metal-semiconductor interface, a result of interface states.

The concept of the neutral level Φ_0 is introduced in section 2.3.4, around which the Fermi level in a metal-semiconductor junction is pinned. Experimentally, it has been determined that Φ_0 is generally located about one-third of the band gap above the valence band [Cowley and Sze, 1965]. While this results in relatively low hole Schottky barrier heights, it conversely also pins the electron Schottky barrier height at considerably higher values, generally about twice the hole barrier height. Consequently, electron transport across a contact between a metal and a n-type semiconductor is more restricted than hole transport for a metal on a p-type semiconductor. Despite the use of a wide variety of metals as suitable silicides, such as Iridium, Erbium or Ybitterium, the performance of n-channel SB-MOSFETs has remained inferior to p-channel devices. The recently proposed use of interfacial layers to *de-pin* the Fermi level in the semiconductor holds some promise to solving this problem, though at the expense of additional fabrication steps [Connelly et al., 2004, 2006]. In addition, the use of dopant segregation techniques to create a layer of highly doped semiconductor close to the metal-semiconductor interface has been shown to reduce the effective Schottky barrier height and may be able to sufficiently reduce the electron Schottky barrier height [Knoch et al., 2005].

Secondly, the silicidation process is a very energetic one. Semiconductor bonds are broken and replaced with metal-semiconductor bonds that, although being covalent, are not entirely non-polar. Differences in electronegativity between metal and semiconductor create slightly polarised bonds that act as a dipole layer at the interface. Furthermore, the crystal structures differ, for example, silicon and germanium are arrenged in a diamond lattice, whereas silicides generally have a different crystal lattice, such as an orthorhombic arrangement for PtSi. Depending on their alignment during the silicidation process, the properties of the Schottky contact, specifically the barrier height, may vary from junction to junction.

1.4 Current Work

This work focuses on the electrical characterisation of SB-MOSFETs provided by Spinnaker Semiconductor to gain further understanding of their operation. The devices operate in p-channel mode with PtSi used in the source and drain regaions, fabricated on bulk Si substrates. Measurements at DC and RF frequencies have been performed to analyse device performance under various conditions and compared to literature results. DC characterisation includes room temperature and low-temperature measurements down to 77K, while RF measurements were all performed at room temperature. In addition, 2-D device simulations using MEDICI have been performed in an attempt to fit simulations to experimental results.

Chapter 2

Theoretical Considerations

This chapter discusses the most important topics pertinent to the operation of SB-MOSFET devices. The operation of long-channel conventional doped source/drain (abbreviated as DSD) MOSFETs is outlined as a basis for understanding device operation. Then, short-channel devices are introduced and their operation contrasted to the ideal behaviour of long-channel counterparts.

Following that, the physical and electrical properties of metal-semiconductor junctions are presented. Lastly, the incorporation of Schottky contacts as the sources and drains of MOSFETs to form SB-MOSFETs is discussed and contrasted to the behaviour of conventional DSD devices.

2.1 The Metal-Oxide-Semiconductor Field-Effect-Transistor

The Metal-Oxide-Semiconductor Field-Effect Transistor is the basic building block of all digital electronic circuits, such as microprocessors and dynamic memories. It is unipolar in operation, meaning that only one type of carrier, holes in the case of p-channel MOSFETs, contribute to current flow. For this discussion, all devices are assumed to be situated on bulk silicon substrates, unless stated otherwise.

Since the devices characterised in this work are p-type, the theory of operation will focus on p-channel MOSFETs, in which holes are the majority carrier. The principles are applicable to n-type devices by reversing polarities and exchanging dopant types. To begin with, the characteristics of a MOSFET will be described based on an ideal long-channel device. This will serve as the basis for understanding the more complicated behaviour of short-channel devices.

2.1.1 Structure

The MOSFET is a simple four-terminal device, shown schematically in Fig. 2.1, with terminals designated in accordance with common convention as gate (subscript g), source (s), drain (d) and substrate or body (b). All voltages and currents associated with the corresponding terminals will be labelled using the indicated subscripts.

A p-channel MOSFET comprises an n-doped silicon substrate in which two highly p-doped regions have been created, usually by ion implantation, to form source and drain. A heavily doped polysilicon or metal gate electrode is resides on top of an insulating layer, typically silicon dioxide, and is situated directly above the substrate region between source and drain with some overlap to the source and drain regions. The sidewall spacers isolate the gate from the metal source and drain contacts. The surface region of the substrate immediately beneath the gate electrode is called the *channel*. Surrounding each individual MOSFET is an insulating layer, again usually made up of silicon dioxide, called the field oxide (FOX in Fig. 2.1). Its purpose is to electrically isolate adjacent devices and prevent operation of one influencing the state of another.

2.1.2 Principle of Operation

Gate, oxide and semiconductor substrate of a MOSFET act as a parallel plate capacitor. In the OFF state, the channel region below the gate is in accumulation and the series combination of source, substrate and drain act like two back-to-back diodes,

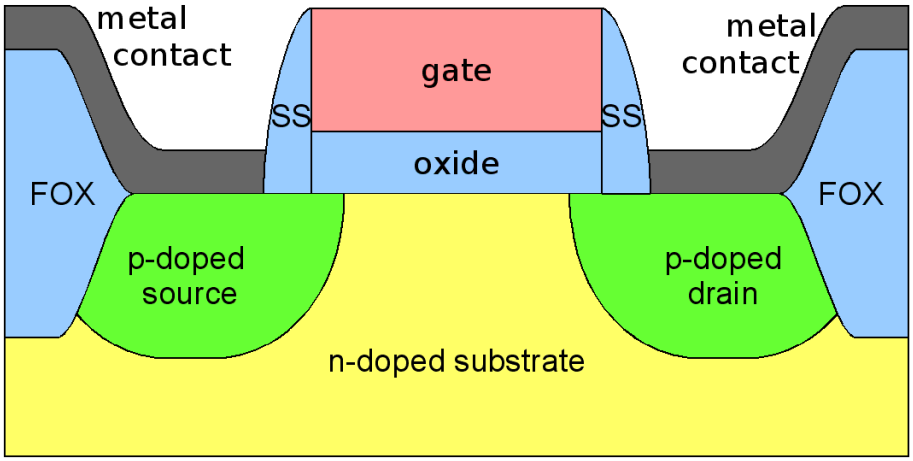

Figure 2.1: Cross-sectional schematic of a Metal-Oxide-Semiconductor Field-Effect-Transistor. SS: sidewall spacer; FOX: field oxide.

presenting the holes in source and drain with a large potential barrier and preventing carriers from traversing the channel.

Applying a negative voltage to the gate electrode with respect to source and substrate repels electrons from the oxide-channel interface, leaving behind fixed positively charged donor atoms in a *depletion region*. Increasing the negative gate voltage further induces a layer of positively charged holes in the channel, creating a so-called *inversion region or layer*, as shown in Fig. 2.2. Mobile holes in the inversion layer are of the same polarity as majority carriers the source and drain regions, thus creating a conducting channel between the two. If a voltage is applied at the drain, then carriers drift from source to drain via the channel. The MOSFET is a symmetric device in that source and drain terminals are interchangeable.

In an ideal MOSFET, the gate electrode is electrically insulated from the channel and thus no DC current will flow when a gate voltage is applied. This has the benefit that a MOSFET dissipates no power in a quiescent state. Current will only flow into or out of the gate during switching. The principle of operation is based on the capacitive coupling

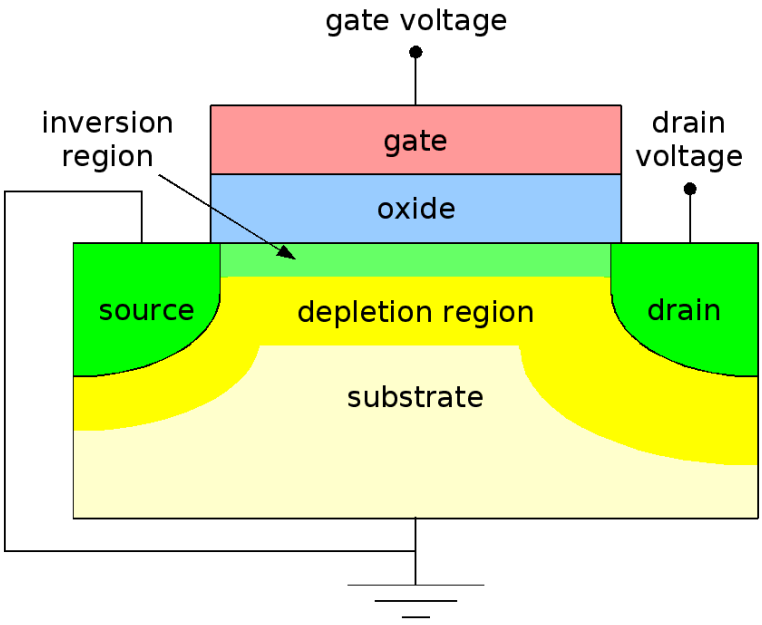

Figure 2.2: MOSFET channel inversion under applied gate voltage.

between gate and channel via the electric field in the oxide, hence the nomenclature of *field-effect transistor*.

2.1.3 Carrier Transport

The gradual channel approximation (GCA) [Pao and Sah, 1966], which assumes the gradient of the horizontal electric field along the channel to be negligible compared to the vertical electric field caused by a voltage applied to the gate, enables one-dimensional models to be applied to the description of the channel current. This assumption is valid for long channel devices and channel regions up to the pinch-off point. Together with the charge-sheet approximation [Brews, 1978], which assumes the thickness of the inversion charge layer to be zero, the drain-to-source current I_{ds} can be expressed as [Taur and Ning, 1998]

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} [(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}], \tag{2.1}$$

where μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, W and L the device width and length respectively, V_{gs} the gate voltage with respect to the source terminal, V_t the threshold voltage and V_{ds} the drain-to-source voltage.

The drain-to-source current given by eqn. 2.1 has a maximum at $V_{ds} = V_{gs}$ - V_t. Beyond this point, the MOSFET enters *saturation*, in which further increases in drain voltage result in no further increases in current. The inversion charge density at the drain end of the channel reaches zero and *pinch-off* occurs. With increasing drain voltage, this pinch-off point is moved towards the source and the remaining voltage is dropped across the high resistance region between it and the drain. By substituting $V_{ds} = V_{gs}$ - V_t into eqn. 2.1, the saturation drain current can be expressed as [Sze, 1981, Taur and Ning, 1998]

$$I_{dsat} = \mu_{eff} C_{ox} \frac{W}{2L} (V_{gs} - V_t)^2. \tag{2.2}$$

2.2 Short Channel MOSFETs

While the scaling of MOSFETs provides performance enhancements by reducing switching times and increasing packing density, there are several aspects in which short-channel MOSFETs differ from the ideal long-channel mode of operation. These effects are discussed in the following sections.

2.2.1 Velocity Saturation

In a long-channel MOSFET the drain current increases with drain voltage until pinch-off occurs towards the drain end of the channel and the current remains constant at the saturation value I_{dsat}. This is due to the linear dependence of carrier velocity on horizontal electric field. However, carrier velocities begin to deviate from this linear dependence above electric fields of about 10^4 V/cm [Taur and Ning, 1998]. Due to non-scaling factors, the electric field present in a MOSFET increases with decreasing gate

length. In very short channel devices, it is possible to achieve electric fields in excess of 10^4 V/cm prior to the onset of pinch-off and cause the drain current to saturate prematurely at a value lower than I_{dsat} as a result of carrier velocity saturation [Sze, 1981, Taur and Ning, 1998].

2.2.2 Short-Channel Effect

The short-channel effect (SCE) is defined as the decrease of MOSFET threshold voltage as the channel length is scaled down [Sze, 1981, Taur and Ning, 1998]. It is especially pronounced at high drain biases. In a short-channel MOSFET, the electric field pattern in the depletion region is no longer one-, but two-dimensional. The closer proximity of source and drain means that their influence over depletion charge extends over a greater portion of the channel. Both source and drain terminals control charge in a depletion region surrounding them, as shown in Fig. 2.3 a). As the gate length is reduced, a larger proportion of the depletion charge beneath the gate is controlled by source and drain potentials, as in Fig. 2.3 b). Less depletion charge is controlled by the gate electrode, as evident by the reduced area of the trapezoid in Fig. 2.3 b). Thus, a lower gate bias is required to achieve channel inversion and turn the device on [Sze, 1981, Taur and Ning, 1998]. This reduction in threshold voltage is detrimental to the ability of MOSFETs to turn off properly.

An alternative way of considering this effect is that the source and drain potentials have an appreciable impact on band bending over a significant portion of the device under the gate. Under the charge sharing model, field lines terminating on fixed charges in the depletion region either originate from gate or from source or drain. With decreasing gate lengths, a larger proportion of field lines terminating on depletion charge under the gate originate from source and drain [Sze, 1981, Taur and Ning, 1998].

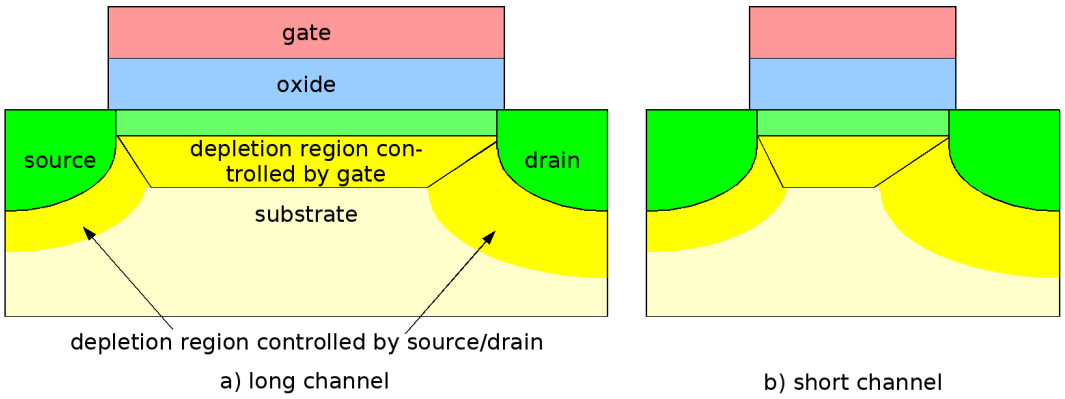

Figure 2.3: Schematic illustration of the Short Channel Effect. The proportion of depletion charge controlled by the gate electrode is reduced with channel length.

2.2.3 Channel Length Modulation

Channel length modulation occurs in short-channel MOSFETs when the drain bias is increased beyond the onset of pinch-off. At the pinch-off point, the horizontal electric field becomes comparable to the vertical field and thus, the gradual channel approximation is no longer applicable. The inversion layer vanishes at the pinch-off point, leaving a high resistance region to the drain.

As the drain bias is increased, the pinch-off point is moved away from the drain end of the channel. The voltage at the pinch-off point remains constant at V_{dsat} and the voltage difference V_{ds} - V_{dsat} to the drain terminal is dropped across the region between drain and pinch-off point. Carriers are injected from the inversion layer into this region at saturation velocity and travel to the drain. The device acts as if its channel length had been reduced by the length of the region between pinch-off point and drain terminal, ΔL, and the drain current increases by a factor of $\frac{1}{1-\frac{\Delta L}{L}}$. Since ΔL increases with drain bias beyond V_{dsat}, so does the drain current [Taur and Ning, 1998].

2.2.4 Drain Induced Barrier Lowering

As channel lengths are reduced, vertical and horizontal transistor dimensions become comparable and the two electric fields begin to interact. Specifically, the charge in the channel is no longer entirely controlled by the gate (as under gradual channel approximation), but to a certain degree by the drain bias as well. In long-channel devices, the potential barrier is flat along most of channel, as illustrated in Fig. 2.4. The drain depletion region acts to reduce this barrier at the drain end of the channel. For short-channel devices, the extent of this influence may extend over a significant portion of the channel, thus reducing the potential barrier that carriers mus surmount in the OFF state and leading to higher leakage currents [Taur and Ning, 1998].

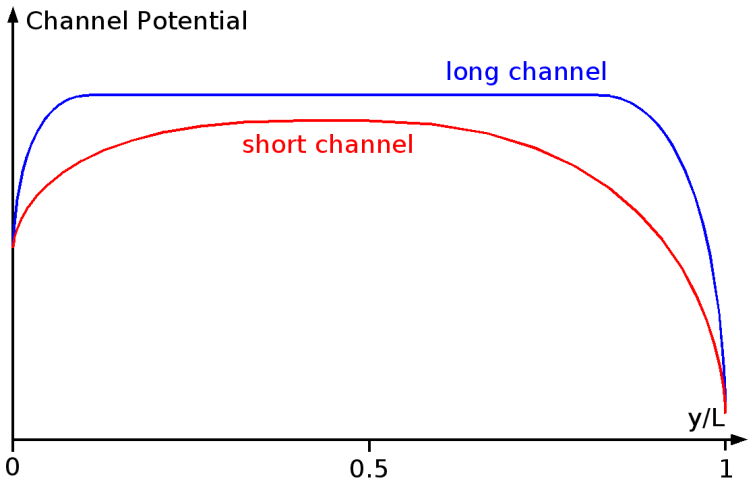

Figure 2.4: Channel potential (arbitrary units) versus lateral distance y along the channel from source to drain (normalised by channel length L) for long and short channel MOSFETs.

The net effect of drain induced barrier lowering (commonly abbreviated as DIBL) is a reduction in threshold voltage with increasing drain bias. This makes it harder for devices to fully turn off and can result in significant leakage currents in their OFF state. DIBL can be alleviated by increasing the channel doping concentration.

Punchthrough is an extreme case of DIBL in which the source and drain depletion regions overlap and create a conduction path independent of gate bias. This can either occur at the surface or in the bulk and renders a MOSFET useless, since the gate no longer has any influence over the channel.

2.2.5 Source-Drain Series Resistance

In a long-channel device, the resistance of source and drain regions is negligible compared to the resistance of the channel. In a short-channel MOSFET, however, the channel resistance is substantially lowered by the decrease in gate length whereas source and drain resistances are increased by the reduced junction depth x_j required to reduce charge sharing and counteract the short channel effects. The impact on the drain current begins to become appreciable at short gate lengths and can lead to drive current degradation [Taur and Ning, 1998]. The effect of source/drain series resistance on drain current can be expressed as

$$V_{ds} = V_{ds,app} - I_{ds}R_{sd}, \tag{2.3}$$

where V_{ds} is the voltage between source and drain. $V_{ds,app}$ the voltage applied across the source and drain terminals and R_{sd} is the source/drain series resistance. Large source and drain resistances will lead to reduced drain currents because it is V_{ds}, not $V_{ds,app}$, that determines the drain current in eqn. 2.1.

The series resistance of source and drain consists of four components [Taur and Ning, 1998], illustrated in Fig. 2.5. The accumulation layer resistance R_{ac} represents the resistance in the gate-to-source or gate-to-drain overlap regions where carriers remain confined to the surface. The spreading resistance R_{sp} is associated with carriers spreading from the surface under the overlaps uniformly into the entire depth of the junction. The sheet resistance R_{sh} is related to the uniform transport of carriers through the

source or drain region. Finally, the contact resistance R_{co} is present at the interface between the source or drain and the metal contact lines.

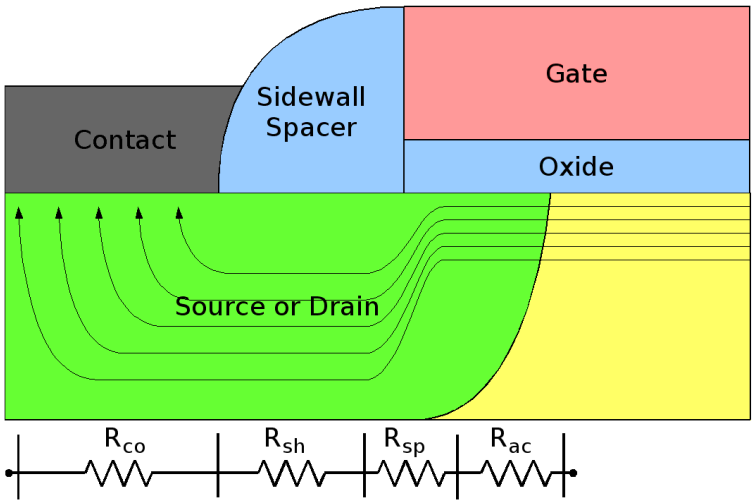

Figure 2.5: Cross-sectional illustration of the four components contributing to source and drain series resistances in a MOSFET.

Accumulation and spreading resistance are dependent on the doping profile gradient between source or drain and the channel, so their contribution can be curtailed by the use of abrupter junction profiles and higher doping concentrations. In modern devices with self-aligned silicides (so-called *salicides*), the impact of sheet and contact resistances has been significantly reduced, mainly by making the interface between doped source or drain region and metallic contact very large, i.e. the entire length of source or drain.

2.3 Metal-Semiconductor Junctions

A metal-semiconductor junction is formed at the interface between a metallic and a semiconducting material and may contain additional interfacial layers, such as a native oxide. Depending on material properties, metal-semiconductor junctions can be ohmic or rectifying. In order to simplify matters without losing relevance to the devices investigated in this work, the following assumptions about metal-semiconductor junctions will

be made.

Firstly, since the sources and drains of the SB-MOSFETs under investigation in this work were formed by silicidation, no interfacial layers between metal and semiconductor will be present and the junction can be assumed atomically abrupt. Therefore, the presence of interfacial layers and their impact on electrical properties will be omitted in this discussion and all metal-semiconductor junctions will be assumed to be intimate.

Secondly, the semiconductor is assumed to be a covalently bonded group IV material (silicon or germanium), since the SB-MOSFETs investigated in this work were fabricated on bulk silicon substrates. The properties of metal-semiconductor junctions with group III-V and II-VI semiconductors are a lot more complex, due to the multitude of possible materials, work functions and band gaps and the non-covalent nature of many of the semicondcutor materials' bonds.

2.3.1 Formation

A metal-semiconductor junction is generally formed in one of two ways: Either by deposition of a metal on a semiconductor surface or by silicidation of a portion of semiconductor to form a metal. While the former usually contains some interfacial layer, such as a native oxide, the latter creates an intimate contact between metal and semiconductor and is the type of greater interest to this work.

In order to silicide a portion of semiconductor, a suitable metal for forming the compound, e.g. Platinum on silicon, is deposited on the semiconductor surface, as shown in Fig. 2.6. The material is then heated in a furnace and the silicide will begin forming at the interface between the deposited metal and the semiconductor substrate. The silicidation process consumes both the metal and part of the semiconductor regions, until the entire layer of deposited metal is consumed to form the final silicide layer.

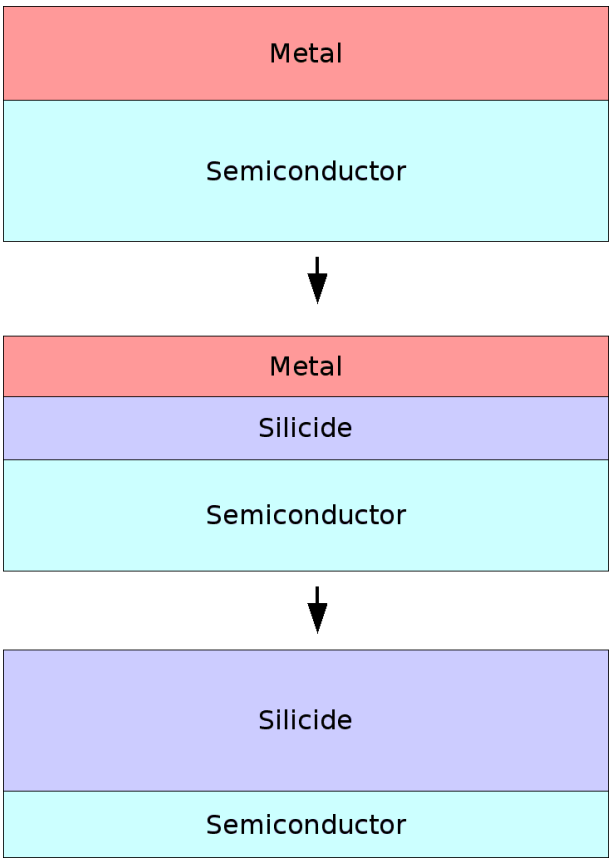

Figure 2.6: Metal-semiconductor formation by silicidation of a portion of semiconductor with a metal.

The growth kinetics are a function of annealing temperature and time as well as the thickness of the deposited metal. Therefore, the three factors cannot be separated and must always be considered together. Moreover, they are also a strong function of the material properties of both metal and semiconductor.

The silicidation process for platinum on silicon consists of two steps in series. Initially, Pt_2Si forms with Pt atoms migrating into silicon. This first step occurs at temperatures as low as 180 - 200 °C [Franco et al., 2003]. Once all the platinum has been consumed, PtSi begins to form with Si diffusing into the existing Pt_2Si layer, until the entire layer has been converted to PtSi. This second step requires temperatures of at least 280 -

400 °C [Franco et al., 2003].

2.3.2 Electrostatics

The band structure of a metal-semiconductor junction depends on the material properties, in particular the workfunction of the metal and the doping and workfunction of the semiconductor [Rhoderick and Williams, 1988]. Conduction and valence band in a metal partially overlap, whilst they are separated by a band gap in a semiconductor in which no carrers can be present. When put into intimate contact, the Fermi levels in both metal and semiconductor under thermal equilibrium must align, so a transfer of charge from one side to the other takes place.

There are four possible combinations of metal-semiconductor junctions, illustrated in Fig. 2.7 - two on n- and two on p-doped substrates. For each substrate type, the relative magnitudes of metal and silicon workfunctions determine whether a rectifying or an ohmic contact is formed. A rectifying junction is referred to as a *Schottky barrier*, named after the German physicist Walter Schottky who is credited with developing their initial theory of operation.

The band structure for the formation of a rectifying Schottky barrier on silicon is shown in Fig. 2.8 for a metal with a workfunction larger than that of the n-type silicon substrate. No interface states are assumed to be present. Fig. 2.8 a) depicts the situation for electrically neutral and separated materials. Since the Fermi level in the silicon is higher than in the metal, once the two are electrically connected, as shown in Fig. 2.8 b), electrons from the semiconductor will flow into the metal until the two Fermi levels align. This leaves behind positively charged donor atoms in a depletion region in the semiconductor, similar to the case of a p-n junction, and accumulates negative charges on the surface of the metal. The separation of charge leads to the formation of an electric field in the junction region and causes the energy bands in the silicon to

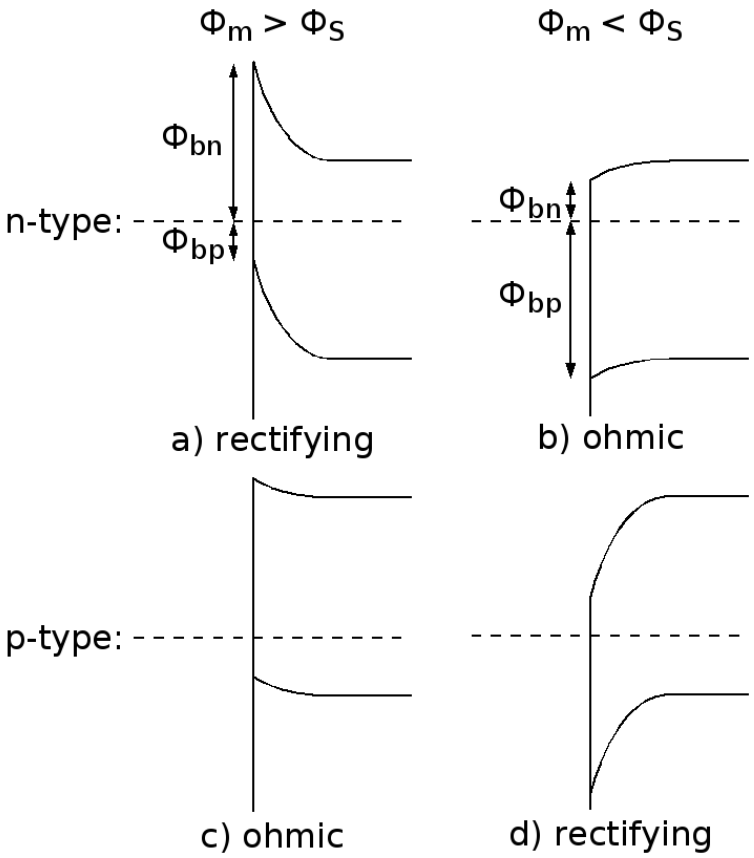

Figure 2.7: Band structures of metal-semiconductor contacts on semiconductors of different doping polarities and with varying metal workfunctions. The formation of rectifying or ohmic contacts is dependent on the substrate doping and the relative workfunctions of metal and semiconductor, as indicated.

bend upwards at the surface. Once the two materials are in perfectly intimate contact, the situation pictured in Fig. 2.8 c) is attained.

2.3.3 Barrier Height

The band bending at the interface establishes a built-in potential or Schottky barrier height for electrons, Φ_{bn}, which according to the simple Schottky-Mott theory is given by [Rhoderick and Williams, 1988]

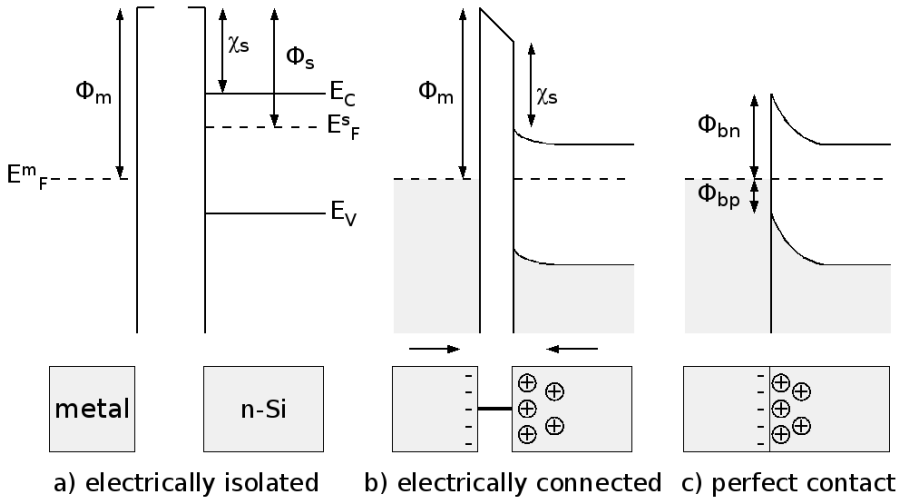

Figure 2.8: Band structures of a metal-semiconductor junction for $\phi_M > \phi_S$: a) electrical isolation; b) electrical contact but some separation; and c) intimate contact.

$$\Phi_{bn} = \Phi_m - \chi_s, \tag{2.4}$$

where Φ_m is the metal workfunction and χ_s the semiconductor electron affinity. The corresponding hole barrer height Φ_{bp} is

$$\Phi_{bp} = \frac{1}{q}E_g - (\Phi_m - \chi_s,) \tag{2.5}$$

where E_g is the semiconductor bandgap.

These simple equations are only valid in an ideal scenario where the influence of interface states is assumed to be negligible or non-existent. However, in practice, this assumption (the so-called *Mott barrier*) is never encountered. The reason for this is the presence of a large interface state density, due to dangling bonds, imperfections at the interface and the fact that the crystal lattices of metal and semiconductor don't match up perfectly. Dangling bonds at the interface significantly alter electrical properties and can lead to *Fermi-level pinning*, which causes the barrier height to be largely independent

of metal [Rhoderick and Williams, 1988]. Schottky barriers encountered in real devices are generally found to behave in a manner between the two extremes of the Mott and a pinned barrier.

2.3.4 Interface States

According to eqn. 2.4, electron and hole Schottky barrier heights should depend on the metal workfunction. However, in practice, the barrier height is found to be a less sensitive function of the metal workfunction and may be almost independent of the choice of metal [Mead and Spitzer, 1964]. Bardeen [1947] suggests that this discrepancy is due to the presence of surface states at the interface between metal and semiconductor.

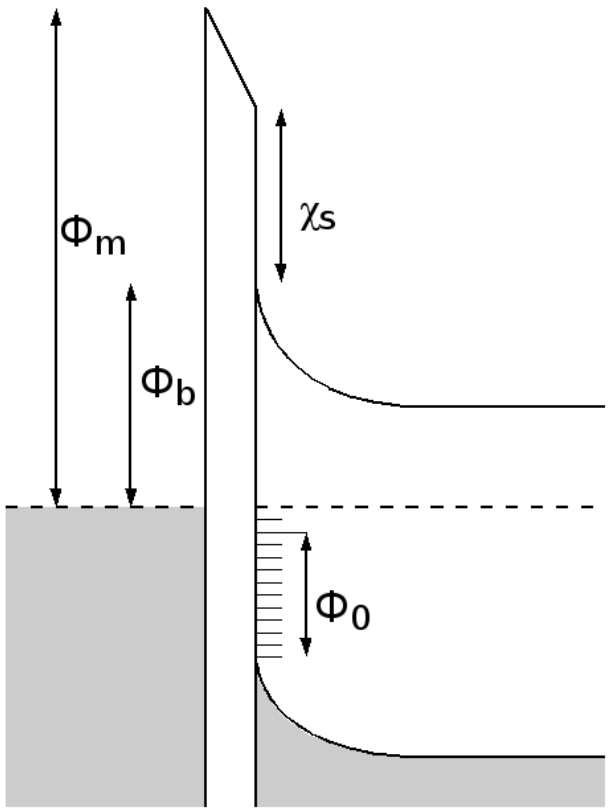

Figure 2.9: Interface states cause the metal Fermi level to be pinned at a value around the neutral level Φ_0.

If a continuous distribution of interface states characterised by a neutral level Φ_0 (measured from the valence band edge) is present at the semiconductor surface, as depicted in Fig. 2.9, the Fermi level will be pinned at or around this neutral level. In the absence of interface states, the depletion charge, Q_d, in the semiconductor must be equal and opposite to the charge on the metal surface, Q_m. In the presence of interface states, however, there is an additional charge at the interface, Q_{ss}, and the charge neutrality condition becomes $Q_m = -(Q_d + Q_{ss})$. Depending on whether the neutral level is above or below the semiconductor Fermi level, the net result will be a reduction or increase in electron Schottky barrier height, respectively. In the limit, when the density of interface states is very high, the barrier is said to be *pinned* and is given by

$$\Phi_b = E_g - \Phi_0. \tag{2.6}$$

Experimentally, it has been found that the neutral level Φ_0 is generally one third of the energy band gap E_g, pinning the electron and hole barrier heights at around 0.75 and 0.37 eV, repectively [Cowley and Sze, 1965]. The workfunction difference between metal and semiconductor then serves to manipulate the barrier height around the neutral level.

2.3.5 Barrier Lowering

The electrostatics outlined in Fig. 2.8 c) are valid for equilibrium, i.e. when no voltages are applied. Once voltages are applied to a Schottky barrier junction, the electrostatics change. Specificially, the shape and height of the barrier are altered. The barrier becomes more rounded, as depicted in Fig. 2.10, and the height is reduced with increasing electric field [Sze, 1981].

There are two components that serve to reduce the barrier height, so-called barrier lowering mechanisms - image force lowering and dipole lowering. Both impact carrier

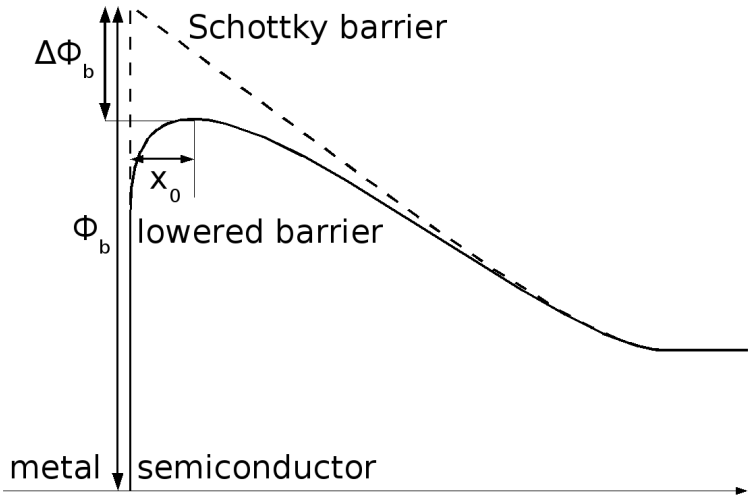

Figure 2.10: Barrier lowering mechanisms reduce a Schottky barrier from its initial profile (dotted line) to an effective height (solid line).

transport at a metal-semiconductor junction by reducing the effective barrier height, which in turn increases carrier transport, since both thermionic emission and field emission are inversely proportional to the barrier height.

Image Force Lowering

When an electric field is applied to a metal-semiconductor junction, an electron with charge -q located a distance x from the metal surface in the semiconductor establishes electric field lines that terminate normally on the metal surface. These field lines act as if a positive charge +q were located at distance -x from the metal surface, i.e. the mirror image of the electron charge, and the force acting on the electron is the same if the metal surface were replaced by an image charge +q at -x [Yang, 1988]. Using Coulomb's force of attraction, the amount of barrier lowering due to this image force, $\Delta\Phi_{b,ifl}$ under an applied external electric field $E_{applied}$ can be expressed as

$$\Delta\Phi_{b,ifl} = \sqrt{\frac{qE_{applied}}{4\pi\epsilon_s}}, \tag{2.7}$$

where ϵ_s is the semiconductor permittivity. From eqn. 2.7, the amount of barrier lowering is seen to be proportional to the square root of the applied electric field. In addition, the location of the maximum potential barrier x_o is altered according to

$$x_o = \sqrt{\frac{q}{16\pi\epsilon_s E_{applied}}}. \tag{2.8}$$

With increasing applied electric field, the effective barrier height is continually reduced and the maximum of the potential barrier is moved closer to the metal surface.

Dipole Lowering

Image force lowering alone is often not sufficient to explain experimentally observed barrier lowering. Additional barrier lowering is attributable to the presence of a dipole layer at intimate metal-semiconductor interfaces. The wave functions of electrons in the metal penetrate into the semiconductor forming metal-induced gap states (MIGS), which form a static dipole layer at the interface. This layer causes the barrier height to vary approximately linearly with electric field [Sze, 1981]

$$\Delta\Phi_{b,dl} \simeq \alpha E_m, \tag{2.9}$$

where $\Delta\Phi_{b,dl}$ represents dipole barrier lowering, α the rate of change of barrier height with electric field and E_m is the electric field perpendicular to the interface. The impact of dipole lowering can be as large as image force lowering [Andrews and Lepselter, 1970].

2.3.6 Carrier Transport

Due to the abrupt nature of Schottky barriers, carrier transport across them differs from conventional pn junctions, where drift and diffusion as well as thermionic emission of carriers constitute the current. In Schottky barriers, an abrupt barrier is present that carriers must surmount in order to contribute to current flow. The three components contributing to carrier transport, illustrated in Fig. 2.11, are thermionic emission of

carriers over the barrier, thermionic-field emission of high energy carriers through the upper part of the barrier and field emission of carriers through the barrier at the Fermi level. Depending on the bias conditions at the junction, one or more of these components will dominate carrier transport, though the total current will be the sum of all three. In addition, barrier lowering occurs at high electric fields which, while not being a carrier transport mechanism, enhances carrier transport by altering the size and shape of the Schottky barrier.

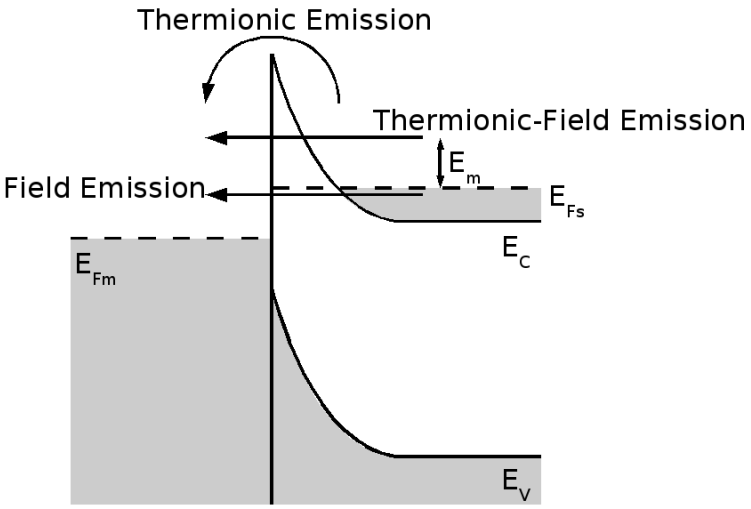

Figure 2.11: Illustration of carrier transport mechanisms for a Schottky barrier on n-doped silicon under an applied forward bias.

Schottky barriers are *majority carrier* devices in that only majority carriers contribute to current flow, i.e. holes for a p-type semiconductor. In comparison, pn junction current is due to both minority and majority carriers.

Thermionic Emission

Thermionic emission (TE) of carriers consists of two basic mechanisms in series. Before being emitted over the barrier, carriers must be transported from the semiconductor to the metal interface by traversing the depletion region, where their motion is subject

to drift and diffusion. Once at the barrier, the emission is determined by the rate of transfer across the boundary. These two transport mechanisms are in series and the current is determined by whichever process causes the larger impediment to carrier flow.

According to the diffusion theory for Schottky barriers by Wagner (1931) and Schottky and Spenke (1939), drift and diffusion in the semiconductor are thought to dominate, whereas the thermionic emission theory of Bethe (1942) proposes that the current is limited by thermionic emission at the interface [Rhoderick and Williams, 1988]. For semiconductors with fairly high mobility, such as silicon and germanium, experimental work on Schottky barriers has determined the thermionic emission theory to be applicable [Padovani and Stratton, 1966, Rhoderick and Williams, 1988, Sze, 1981]. Crowell and Sze [1966] combined diffusion and thermionic emission theories and according to their work, the thermionic emission current can be expressed as [Crowell and Sze, 1966, Rhoderick and Williams, 1988, Sze, 1981]

$$J = J_R(e^{\frac{qV}{kT}} - 1) \tag{2.10}$$

with

$$J_R = A^{**}T^2 e^{\frac{-q\Phi_{bn}}{kT}}, \tag{2.11}$$

where J_R represents the reverse current density, A^{**} the effective Richardson's constant, V the applied bias voltage and the rest take their usual meanings. It must be noted that due to the bias dependence of the barrier height Φ_{bn}, the reverse current density J_R does not saturate as in the case of a pn junction and shows some dependence on the reverse bias voltage [Andrews and Lepselter, 1970, Padovani and Stratton, 1966, Rhoderick and Williams, 1988, Sze, 1981]. Equations 2.10 and 2.11 can be applied to hole barriers on p-type substrates by replacing Φ_{bn} with Φ_{bp}.

Carriers thermally emitted from the semiconductor are not in thermal equilibrium with carriers in the metal, having an energy exceeding the metal Fermi energy by at least the barrier height. They can be loosely described as *hot carriers* and as they penetrate into the metal, they lose energy by collisions with other carriers and lattice atoms. Carrier transport in the reverse direction under opposite bias conditions is governed by the same equations.

Field and Thermionic-Field Emission

It is possible for carriers with energies below the top of the barrier to traverse the barrier by quantum-mechanical tunneling through the barrier. This modifies the thermionic process in two ways, as illustrated in Fig. 2.11. Carriers with energies close to the Fermi energy in the semiconductor can tunnel through the barrier into the metal. This is called *field emission* (abbreviated as FE) [Padovani and Stratton, 1966, Rhoderick and Williams, 1988, Sze, 1981].

Additionally, thermally excited carriers with energies between the Fermi energy and the top of the barrier in the semiconductor have an increased tunneling probability since the barrier between them and the metal becomes increasingly thinner towards the top of the barrier. However, the number of electrons decreases rapidly with increasing energy and there will be a maximum contribution to the current from electrons with an energy E_m. This contribution is called *thermionic-field emission* (TFE) [Rhoderick and Williams, 1988].

Thermionic-field emission is highly temperature dependent because, as the temperature in the semiconductor is increased, the number of carriers at higher energies is increased. In the limit, virtually all carriers have sufficient energy to go over the top of the barrier and pure thermionic emission is achieved. As such, there is a smooth transition with temperature from field emission through thermionic-field emission to pure thermionic emission. In practice, however, due to the very high temperatures necessary,

pure thermionic emission is not encountered.

The theory behind tunneling through Schottky barriers has been developed by Padovani and Stratton [1966] and Crowell and Rideout [1969] and is very mathematical. The essential conclusions, however, can be summarised as follows.

The tunneling current-voltage relationship, encompassing both field and thermionic-field emission is of the form [Rhoderick and Williams, 1988, Sze, 1981]

$$J = J_S(e^{\frac{qV}{nkT}} - 1), \tag{2.12}$$

with the saturation current density J_S approximated by [Sze, 1981]

$$J_S \sim e^{\frac{-q\Phi_{bn}}{E_{00}}}, \tag{2.13}$$

where n represents the ideality factor and the reduced energy E_{00} is a parameter of great importance in tunneling theory and is a function of the semiconductor doping density, effective mass and permittivity [Rhoderick and Williams, 1988, Sze, 1981]. The relationship presented in eqn. 2.12 and 2.13 is a very simplified approximation of the tunneling current. For detailed analysis and derivation, the reader is referred to the original paper of Padovani and Stratton [Padovani and Stratton, 1966]. Nevertheless, for the purpose of understanding the tunneling behaviour at a Schottky barrier, some very general observations with regards to tunneling can be made.

Firstly, field emission from semiconductor to metal only occurs in degenerate semiconductors and the current density of field emission in the reverse direction governed by eqn. 2.13 is exponentially dependent on both bias voltage and barrier height. Thus, the reverse currents for both thermionic and field emission, given in eqn. 2.11 and 2.13, respectively, are both exponentially dependent on the Schottky barrier height.

Secondly, the ratio kT/qE_{00} is a measure of the relative importance of thermionic emission and tunneling. For $kT \ll qE_{00}$, field emission should dominate, for $kT \approx qE_{00}$ thermionic-field emission and for $kT \gg qE_{00}$ thermionic emission [Rhoderick and Williams, 1988].

Total Current

The total current in a metal-semiconductor junction is always made up of the sum of the three contributions by thermionic, thermionic-field and field emission. If the conduction band in the semiconductor is raised above the peak of the Schottky barrier, no tunneling is possible and carrier transport is dominated by thermionic emission. Thermionic-field emission begins to contribute once the conduction band in the semiconductor is below the Schottky barrier height and its contribution increases as the conduction band is lowered. Finally, thermionic emission can only contribute once the conduction band in the semiconductor passes below the Fermi level of the metal.

2.4 Schottky barrier source/drain MOSFETs

2.4.1 Overview

In a Schottky barrier source/drain MOSFET, the doped source and drain regions are replaced by a metal, usually a metal-silicide for process reasons. Appropriate metal-semiconductor combinations form rectifying junctions with very similar transport properties to doped pn junctions, though the physical mechanisms they are based on differ. Thus, a transistor with Schottky barrier metal source and drain behaves, in terms of externally measurable currents, in a very similar manner to a conventional doped source/drain (DSD) counterpart.

The use of metal source and drain regions was first published by Lepselter and Sze in 1968 [Lepselter and Sze, 1968], though the device exhibited poor performance in

comparison to contemporary DSD MOSFETs. SB-MOSFETs were further investigated in the 1980's, beginning with Koeneke's investigation into the performance impact of a lateral gap between gate and source and drain electrodes [Koeneke et al., 1981]. Most of this early work established proof of the concept, but device performance was still inferior to doped source/drain devices.

In 1994 and 1995, Tucker et al. [1994] and Snyder et al. [1995] published on the advantages of SB-MOSFETs for device scaling. Since then, the investigation of Schottky barrier MOSFETs has received increased attention. Electrical characteristics of p-channel [Calvet et al., 2000, 2002, Dubois and Larrieu, 2002, 2004, Fritze et al., 2004, Ikeda et al., 2002, Kudzierski et al., 2000b, Larrieu and Dubois, 2005, Wang et al., 1999, Zhu and Li, 2005] and n-channel devices [Jang et al., 2003b,c, 2004a,b, Zhu et al., 2004] with a variety of different source/drain silicides have been investigated. The use of barrier height modification techniques to improve device performance has recently been proposed [Connelly et al., 2004, 2006, Kinoshita et al., 2006, Knoch et al., 2005, Zhang et al., 2005b,a, Zhao et al., 2005] and a number of simulations have been performed [Guo and Lundstrom, 2002, Jang et al., 2003a, Vega, 2006a,b, Winstead and Ravaioli, 2000]. The wide variety of possible source/drain silicide materials as well as the need for a suitable silicide with low electron barrier for n-channel devices provide for a large variety of devices with differing properties.

The following discussion of the operation of SB-MOSFETs will be based on a p-channel device on a silicon substrate with source and drain metals exhibiting larger electron than hole Schottky barriers, i.e. $\Phi_{bn} > \Phi_{bp}$. The schematic cross section of a SB-MOSFET is illustrated in Fig. 2.12.

2.4.2 Principle of Operation

The energy band diagrams illustrating four states of operation of a p-channel SB-MOSFET along the line from A to B of Fig. 2.12 are shown in Fig. 2.13. Whilst still

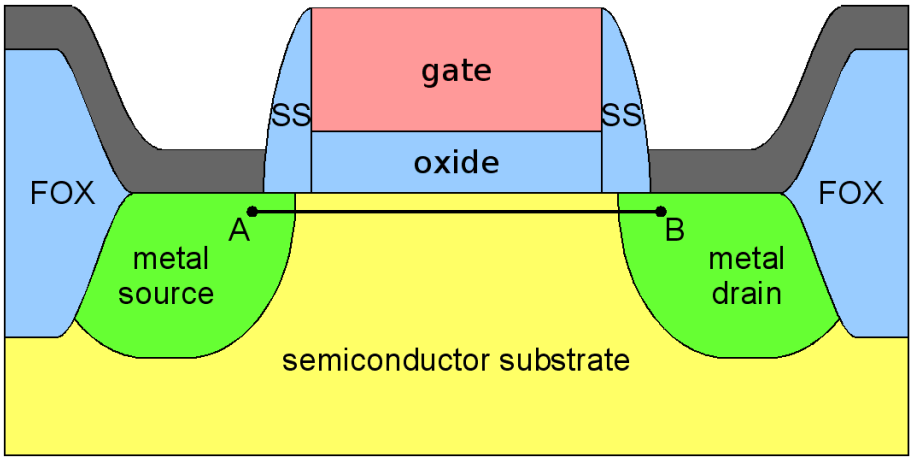

Figure 2.12: Schematic cross section of a SB-MOSFET. Except for the metallic source and drain, it is identical to a conventional MOSFET.

based on the *field-effect principle* of the capacitive coupling between gate and channel, the SB-MOSFET differs in the manner in which carriers enter and exit the channel.

Instead of the continuous energy band profiles present in conventional MOSFETs, valence and conduction bands in a SB-MOSFET contain abrupt junctions between metallic and semiconducting materials at either end of the channel. In traversing the length of the MOSFET, carriers must travel through metal, then semiconductor, then metal again. In the metal source, carriers drift under the influence of the applied horizontal electric field until they reach the source-to-channel interface. Depending on the bias conditions, carriers are either thermally emitted from the source over or tunnel through the potential barrier into the channel. The details of these emission processes are discussed in section 2.3.6.

In the channel, carrier motion is governed by drift and diffusion until the the channel-to-drain interface is reached. Under all but the lowest drain voltages, this junction acts like a forward-biased diode and carriers exit from the channel into the metal drain.

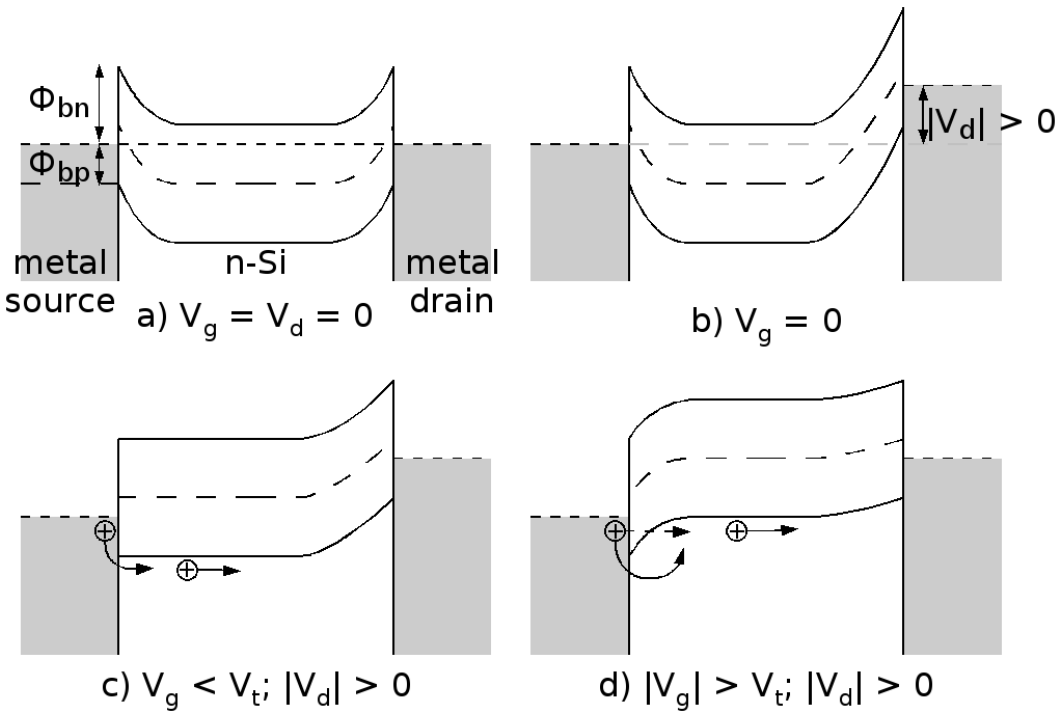

Figure 2.13: Energy band diagrams for a p-channel SB-MOSFET illustrating four states of operation: a) OFF state - no drain bias; b) OFF state - with drain bias; c) threshold; d) ON state

From there, they drift to the drain terminal under the influence of the applied horizontal electric field created by the drain bias. The carrier transport processes for various bias conditions illustrated in Fig. 2.13 will be explained in the following.

2.4.3 Carrier Transport

Carrier transport in a SB-MOSFET is more complex than for a conventional doped source/drain device, due to the added complication of Schottky barriers at source and drain. In a conventional MOSFET, the energy bands are continuous throughout the device and carrier transport is governed by drift and diffusion processes as well as thermionic emission. While these are still applicable in the channel region of SB-MOSFETs, the processes that inject carriers into and out of the channel are different - namely thermionic and field emission at an abrupt metal-semiconductor interface. In a SB-MOSFET, control of carrier transport is highly dependent on bias conditions and is a balance of thermionic emission and tunneling from source to channel and drift and diffusion in the channel. Ultimately, the process posing the greatest hindrance to carrier transport controls current flow.

The transfer characteristic of a 85 nm gate length SB-MOSFET annealed at 550 °C at a drain bias of $|V_{ds}| = 1.0$ V is depicted in Fig. 2.14 to illustrate the tri-slope characteristic that typifies SB-MOSFET drain currents. The presence of a n-type polysilicon gate on these devices instead of the usual p-type shifts the threshold voltage by approximately 1.1 V and must be taken into account during analysis. The approximate regions in which thermionic emission, thermionic-field and field emission are the dominant contributors to the forward drain current as well as the reverse leakage regime are labelled and will be used to describe the different regions.

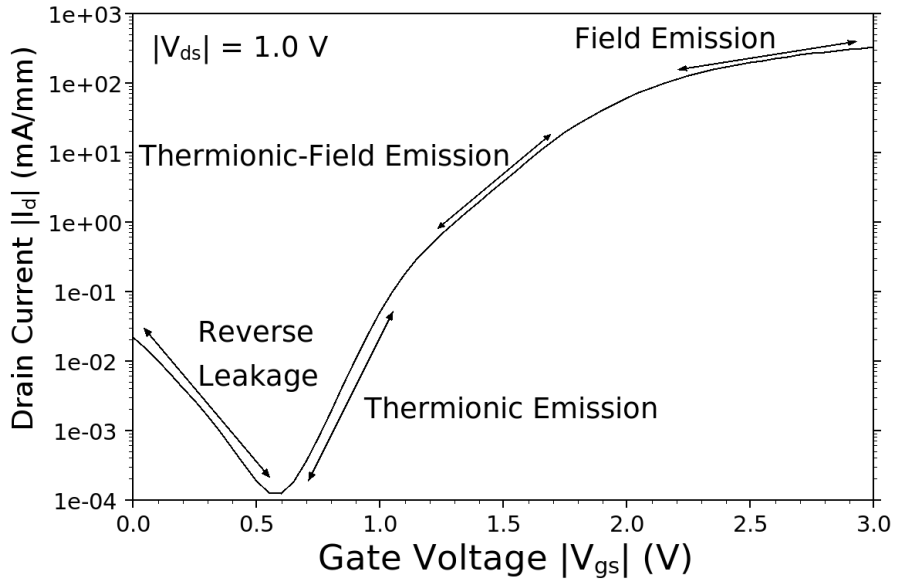

Figure 2.14: Transfer characteristics at a drain bias of 1.0 V of a 85 nm SB-MOSFET annealed at 550 °C. Regions of carrier transport domination are labelled.

Reverse Leakage

At gate voltages below 0.6 V in Fig. 2.14, the channel is in accumulation, due to the n-poly gate, and reverse junction leakage of electrons from drain to source is responsible for significant current flow. The band diagram shown in Fig. 2.15 illustrates its origin in a SB-MOSFET and corresponds to Fig. 2.13 b).

Electrons in the drain electrode possess a finite probablity of tunneling through the large electron Schottky barrier Φ_{bn} into the channel region. This effect will be especially pronounced if the quasi-Fermi level in the drain is raised above the conduction band in the channel, as this enables field emission in addition to thermionic-field emission to contribute. Therefore, this reverse leakage current is highly dependent on drain bias. The high electron barrier ensures that this leakage current is considerably smaller than the hole current in the foward direction, but nevertheless it is an observable feature of SB-MOSFETs with highly doped channels. In addition, the large electron barrier ensures

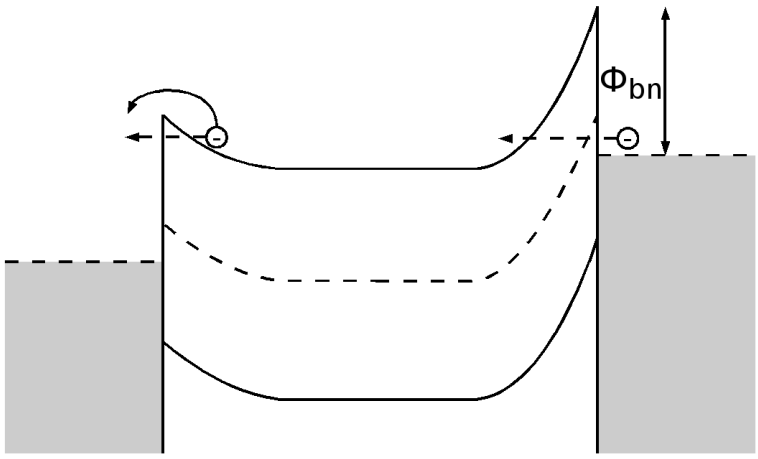

Figure 2.15: Band diagram illustrating the origin of reverse leakage in the OFF state of an SB-MOSFET.

that the contribution by thermionic emission remains very small.

Once in the channel, electrons drift to the source-to-channel interface, where they must surmount a second Schottky barrier to exit via the source. However, since this barrier poses a smaller hindrance to carriers, reverse leakage current is thought to be controlled by field emission from the drain into the channel.

The presence of reverse leakage currents poses a problem to SB-MOSFET device performance, since this reverse leakage severely degrades the ability of SB-MOSFET devices to switch off under very high drain biases.

Thermionic Emission

In the subthreshold regime between $|V_{gs}| = 0.6$ and 1.2 V, corresponding to band diagram situations between those depicted in Fig. 2.13 b) and c), the drain current is entirely due to thermionic emission of holes over the source-to-channel hole Schottky barrier into the channel [Snyder et al., 1995]. The valence band in the channel remains below the tip of the Schottky contact, preventing any form of tunneling current contribution. Once emitted into the channel, holes drift under the horizontal electric field,

where they exit via the drain. The linear appearance on the logarithmic scale is evidence of the exponential dependence of thermionic emission on gate voltage, as predicted by eqn. 2.10, and gives rise to the subthreshold slope.

Once the valence band at the source-to-channel interface coincides with the height of the hole Schottky barrier, corresponding to the band diagram shown in Fig. 2.13 c), the thermionic emission current reaches its maximum contribution. Raising the valence band beyond this level leads to no further increase in thermionic emission, but field and thermionic-field emission begin to contribute to the drain current [Snyder et al., 1995]. Theoretically, the thermionic emission current should increase with gate voltage due to barrier lowering mechanisms reducing the Schottky barrier height under large horizontal electric fields. Experimentally, however, this cannot be verified, since tunneling of carriers becomes larger than thermionic emission under high gate voltages and masks the latter's contribution.

Thermionic-Field Emission

Increasing the gate voltage beyond the situation of Fig. 2.13 c) raises the valence band in the channel above the peak of the hole Schottky barrier. The source-to-channel barrier becomes reverse-biased and increasingly thinned by the raising of the channel potential, as depicted in Fig. 2.13 d). Thermionic-field emission of carriers from source through the barrier into channel dominates the drain current. As well as that, image force and dipole barrier lowering mechanisms serve to reduce the barrier height from its initial zero-bias height with increasing horizontal electric field between source and channel.

The extent of this regime is highlighted in Fig. 2.14 and is evident by the second linear region on the logarithmic scale. This signifies the exponential dependence of tunneling on gate voltage, as described by eqn. 2.12.

Field Emission

With increasing gate voltages, the source-to-channel Schottky barrier becomes increasingly transparent to carriers due to a thinning of the barrier as the channel potential is raised and barrier lowering mechanisms as the horizontal electric field is increased. Once the valence band in the channel is raised above the quasi-Fermi level in the source, field emission of holes becomes possible, as illustrated in Fig. 2.13 d), and adds to the thermionic and thermionic-field emission currents.

With increasing carrier injection into the channel, eventually the resistance of the channel will begin to limit current flow. The onset of this is when the channel resistance, i.e. carrier drift and scattering in the channel, pose a greater hindrance to the drain current than the source-to-channel Schottky barrier.

In short-channel SB-MOSFETs, such as the 85 nm gate length ones investigated in this work, no current limitation by the channel is observed. The drain current is seen to be dominated by source-to-channel carrier injection under all bias conditions, with thermionic-field and field emission the major contributions at the highest gate voltages, as will be demonstrated in section 4.7. However, in long-channel devices, the channel resistance is a lot larger and may limit current flow at high gate voltages rather than tunneling [Snyder et al., 1995, Wang et al., 1999].

2.4.4 Comparison to DSD MOSFETs

The main motivation for studying SB-MOSFETs is the inherent low resistivity of the metallic sources and drains, which alleviates source/drain series resistance issues outlined in section 2.2.5. Since self-aligned silicides are commonly used as the metal contact material in modern MOSFETs, the major difference between DSD and SB-MOSFETs is the removal of parasitic resistances related to the doped source/drain regions. Essentially, accumulation, spreading and sheet resistances, outlined in section

2.2.5 and illustrated in Fig. 2.5, are removed and only the contact resistance remains.

However, this contact is now to n- rather than p-type materials for p-channel devices and the metal-semiconductor contact becomes an integral part of SB-MOSFET operation. In both DSD and SB- MOSFETs, the gate electrode modifies the electrostatic potential in the channel, making both types of device *field-effect transistors*.

The drain current of a DSD device is made up of a diffusion contribution that dominates subthreshold conduction and a drift component that dominates once the channel is inverted [Sze, 1981, Taur and Ning, 1998]. In contrast, the drain current of a SB-MOSFET consists of the three carrier emission processes at the source-to-channel Schottky barrier - thermionic emission dominating in the subthreshold regime and thermionic-field and field emission in the remainder. Additionally, long-channel SB-MOSFETs may also be channel-limited.

Because of the presence of Schottky barriers between source/drain and channel, the doping concentration in a SB-MOSFET can be lower than for a comparable doped source/drain device. The Schottky barrier provides an electrostatic potential barrier in the OFF state, limiting current flow [Larson and Snyder, 2006].

Accumulation-mode operation

One interesting possibility unique to SB-MOSFETs is to operate them in so-called *accumulation-mode* by fabricating p-channel devices on p-type rather than the usual n-type substrates. Similarly, n-channel devices may be placed on n-type substrates. This form of operation has been termed the *Accumulation-Low Schottky Barrier* (ALSB)-MOSFETs [Dubois and Larrieu, 2002].

Instead of current flowing when the channel is inverted, the device ON state occurs when the channel is in *accumulation* and the drain current is due to majority rather than

minority carriers in the substrate. Ultimately, this could allow both n- and p-channel devices to be fabricated on the same substrate type (either n- or p-type), with one operating in inversion-mode, the other in accumulation-mode.

Accumulation-mode operation is possible because metal-semiconductor contacts are majority carrier devices and can be formed on both n- and p-type substrates. One implication of this is that any SB-MOSFET can operate in both accumulation- and inversion-mode. The only caveat to this is that if a specific SB-MOSFET is optimised for p-channel operation by creating a small hole Schottky barrier, e.g. by using PtSi source and drain, it will be a very bad n-channel device.

Chapter 3

Electrical Characterisation and Analysis Techniques

This chapter covers the experimental characterisation and analysis techniques used in this work. Static current-voltage (I-V) measurements are used to characterise and analyse SB-MOSFET device performance. The Schottky barrier height for holes of the PtSi-Si source-to-channel junction is extracted using a series of variable temperature I-V measurements. Radio-frequency (RF) measurements under saturation bias conditions assess device performance at high frequencies.

3.1 Static Current-Voltage

3.1.1 Equipment and Setup

Static I-V characterisation was performed on an enclosed Karl Suss probe station using either an Agilent 4145C or Hewlett-Packard 4145B parameter analyser for data acquisition. For low temperature I-V measurements between 77 and 300 K, a Desert Cryogenics TT-Prober System environmental probe station with a liquid nitrogen feed was used together with aforementioned parameter analysers.

All measurements were performed on on-wafer devices and contacting was established by four point probe method, with the four contacts being gate, source, drain and substrate terminals. Needle probes with a fine positioning adjustment together with a microscope were used to establish contact directly to the gate, source and drain contact pads. In absence of surface substrate contact pads, the substrate contact was established via the vacuum chuck on which the wafers were positioned. Needle probes were connected to measurement equipment via triaxial cables.

3.1.2 Measurement Technique

All measurements were taken with SB-MOSFETs biased in the common-source configuration, i.e. source and substrate are grounded with variable voltages applied to gate and drain. The first, and most interesting measurement, is that of the transfer characteristic. A constant drain voltage V_{ds} is applied while the gate voltage V_{gs} is varied and the drain current I_d is acquired. From this, a number of performance parameters can be extracted, which will be outlined subsequently. The transfer characteristic is usually obtained for low and high drain biases, which, based on recommendations by the International Technology Roadmap for Semiconductors [2000 Update] for high-performance logic applications, are chosen as 0.1 and 1.4 V, respectively. In the case of SB-MOSFETs, the low drain voltage of 0.1 V biases the device in the so-called *sublinear regime* rather than the linear regime. Thus, the extracted parameters are not appropriate for use as design parameters, but are nevertheless extracted for completeness.

The second I-V measurement is that of the output characteristic, for which the gate voltage V_{gs} is held constant while the drain voltage V_{ds} is varied. Typically, this measurement is repeated for a wide range of gate voltages.

3.1.3 Threshold Voltage

Definition

The threshold voltage V_t is an important MOSFET parameter that is required for some further measurements and is vital for assessing the operation of a device [Schroeder, 1998]. Despite many definitions of the threshold voltage being in existance, a commonly used definition is [Brown, 1953]

$$\Phi_S = 2\Phi_F, \tag{3.1}$$

where Φ_S is the surface and Φ_F the bulk potential. This definition stems from equating the surface minority carrier density with the bulk majority carrier density, i.e. p(surface) = n(bulk) for a p-channel MOSFET. However, the condition described by 3.1 is impractical, if not impossible, to measure directly and various methods have been developed to extract the threshold voltage in an actual device. A few of these methods as well as their relevance to this work will be discussed in the following subsections.

Threshold Voltage in SB-MOSFETs

Before delving into the threshold voltage methods, it is beneficial to discuss the relevance and accuracy of the threshold voltage concept for the case of SB-MOSFETs. As outlined in section 2.4.3, the operation of a SB-MOSFET is a combination of carrier transport across a Schottky barrier (thermionic and field emission) and through a semiconducting material (drift and diffusion) with the process posing the greatest limitation to current flow being the controlling influence.

The threshold voltage definition as given by eqn. 3.1 was established based on a conventional doped source/drain MOSFET, whose operation is based on drift and diffusion of carriers in a semiconducting material. Essentially, the threshold voltage is defined as

the gate voltage at which the inverion layer charge density is equal but opposite the bulk charge density, i.e. the channel is in inversion.

In SB-MOSFETs, however, there is the added complexity of carrier injection from the source over or through the Schottky barrier into the channel. It may be possible for this barrier to modify the threshold voltage to a condition other than given by eqn. 3.1. For example, if a very large Schottky barrier is present between source and channel, this will limit current injection into the channel and delay the onset of significant current flow, and hence the threshold voltage, to a higher gate voltage. In view of this, Calvet [2001] proposes the definition of threshold in SB-MOSFETs as the change from thermionic emission to field emission as the dominant contribution to the drain current. In the sample SB-MOSFET transfer characteristic shown in Fig. 2.14, this occurs at about $|V_{gs}| = 1.15$ V.

The following subsections discuss three of the most common threshold voltage measurement techniques as well as their merits and applicability to SB-MOSFETs. A comparison of threshold voltages extracted for a sample SB-MOSFET device using the three techniques outlined in the following is illustrated in Fig. 3.1.

Constant Current Method

The first, and simplest method, takes the gate voltage V_{gs} for a low drain bias V_{ds}, typically 50 or 100 mV, at a specified drain current I_{th} as the threshold voltage. Normally, this threshold current is taken to be

$$I_{th} = 20^{-8} \frac{W_m}{L_m} A, \tag{3.2}$$

where W_m and L_m are drawn device width and length respectively. Device width and length are included to make the definition geometry independent and thus applicable to any device. The gate voltage corresponding to the drain current I_{th} is taken as the

threshold voltage, labelled $V_{t,cc}$ in Fig. 3.1. The choice of 20^{-8} A is somewhat arbitrary and has no proper physical reasoning but has significant influence on the deduced threshold voltage [Arora, 1993]. In this work, a value of 20^{-8} A is chosen in order to satisfy the threshold voltage proposition of Calvet [2001].

The main benefit of this approach is its inherent simplicity and the necessity of only a single measurement, hence lending itself well to batch measurements for statistical analysis. The inaccuracies inherent in this technique derive from the basic assumption that device operation scales with geometry, mobility is identical for all devices and leakage currents may be neglected in the off-state [Arora, 1993, Palmer, 2001, Schroeder, 1998]. Furthermore, the fact that I_{th} is open to choice makes the technique prone to manipulation.

Despite these shortcomings, this method was chosen for threshold voltage evaluation because the two techniques outlined next were simply not applicable to SB-MOSFET devices, as will be explained.

Linear Extrapolation Method

A commonly used threshold voltage measurement method is the *linear extrapolation technique*. The drain current is measured as a function of gate voltage for low drain bias, typically 50 - 100 mV to ensure operation in the linear regime. The point of maximum slope on the I_d-V_{gs} curve is determined by obtaining the maximum of the transconductance, $g_m = dI_d/dV_{gs}$, and a straight line is drawn at that slope from there to $I_d = 0$. The intercept with the x-axis determines the threshold voltage, labelled $V_{t,lin.extr.}$ in Fig. 3.1. This method is sensitive to both series resistance and mobility degradation [Schroeder, 1998], but has the benefit of not requiring an arbitrary threshold current.

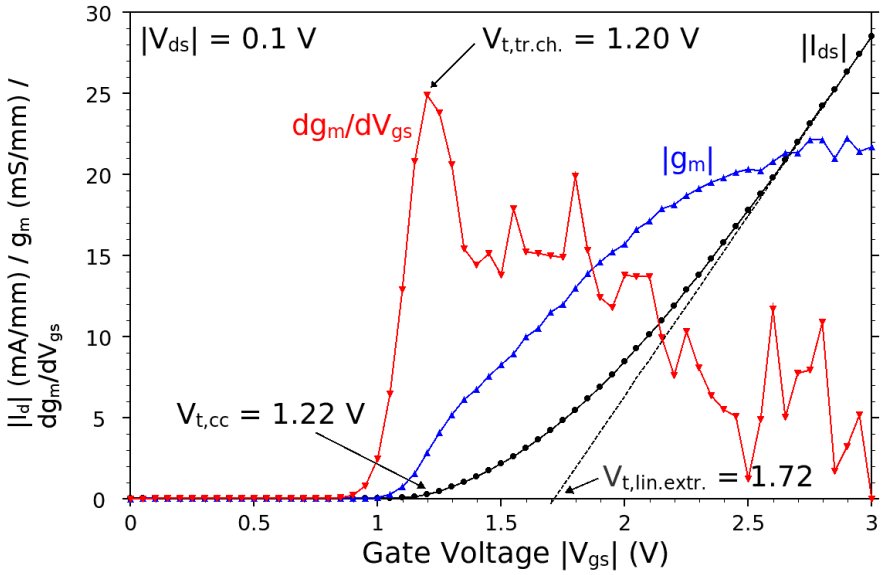

Figure 3.1: Sample threshold voltage extraction using three different techniques on a 85 nm SB-MOSFET undergoing a source/drain silicide anneal of 500 °C.

This method was deemed unsuitable because the transconductance of a SB-MOSFET exhibits a maximum at very high gate voltages, sometimes even at the maximum applied gate voltage. Linear extrapolation of drain current from the point of maximum transconductance results in unreasonably high values for the threshold voltage $V_{t,lin.extr.}$, as evident in Fig. 3.1.

Transconductance Change Method

A superior method, that is immune to series resistance and mobility degradation effects, is the *transconductance change method* [Schroeder, 1998]. By taking the derivative of transconductance with respect to gate voltage, dg_m/dV_{gs}, and determining the maximum, the threshold voltage, labelled $V_{t,tr.ch.}$ in Fig. 3.1, is found. However, as two derivatives of the original measurement data are required, this method is more susceptible to noise in the measurement [Arora, 1993, Schroeder, 1998].

Evaluation

As evident from Fig. 3.1, the threshold voltages for low drain voltage $|V_{ds}| = 0.1$ V extracted using the transconductance change and constant current method with 20 nA agree very well. However, for drain voltages of 0.2 V and above, the transconductance change method became inaccurate, since the derivative of the transconductance, dg_m/dV_{gs}, exhibits a maximum at gate voltages of 1.5 V and higher, clearly in excess of the true threshold voltage.

Therefore, the transconductance change method is used at a low drain voltage of 0.1 V to choose a threshold current of 20 nA. The constant-current method was then applied with the selected threshold current to extract the threshold voltage at other drain voltages at which the transconductance change method no longer returned reasonable values. The constant-current threshold voltage measurement technique is generally used in SB-MOSFET literature [Calvet, 2001, Lousberg et al., 2007].

3.1.4 Subthreshold Slope

As the name implies, the subthreshold current is defined as the current below the threshold voltage and its characteristics are important for MOSFET performance. The subthreshold current depends exponentially on gate voltage V_{gs} and the reciprocal of the slope of $log(I_{ds})$ versus V_{gs} is defined as the subthreshold slope S with units of mV/dec, i.e. Arora [1993]

$$S = \frac{dV_{gs}}{d(logI_{ds})} = 2.3 \left[\frac{dV_{gs}}{d(lnI_{ds})} \right]. \tag{3.3}$$

The subthreshold slope is an important MOSFET parameter, as it determines how quickly a particular MOSFET switches on and off and hence influences its maximum switching speed in digital circuits. In addition, a good subthreshold slope allows low threshold voltage, which is extremely important in low voltage applications.

The subthreshold slope is determined by first measuring the drain current I_{ds0} corresponding to the threshold voltage applied V_t to the gate. Then, the gate voltage V'_{gs} corresponding to a drain current I'_{ds} several decades below I_{ds0} is obtained, i.e. $I'_{ds} = I_{ds0}/10^n$, where n is a positive integer. Linear regression is applied to the intermediate data between I_{ds0} and I'_{ds} and the inverse of the slope is consequently the subthreshold slope [Arora, 1993].

3.1.5 Drain Induced Barrier Lowering (DIBL)

For long channel devices, the threshold voltage is generally assumed to be independent of drain bias. For short channel devices the threshold voltage becomes dependent on drain bias due to Drain Induced Barrier Lowering (DIBL). The higher the drain bias, the lower the threshold voltage, i.e.

$$V_t(V_{ds}) = V_t - \sigma \Delta V_{ds} = V_t - \Delta V_t, \tag{3.4}$$

where V_t is the measured threshold voltage, ΔV_{ds} is the difference in applied drain voltage, ΔV_t is the threshold voltage shift and σ is the DIBL parameter, usually expressed in units of mV/V. Knowing ΔV_t thus allows easy DIBL characterisation [Arora, 1993].

Practically, the DIBL parameter σ is obtained by measuring two transfer characteristics for differing drain voltages. The change in voltage ΔV_t at a fixed drain current I_t is extracted and the DIBL is calculated and usually defined as

$$\sigma = \frac{\Delta V_t}{\Delta V_{ds}}. \tag{3.5}$$

Since the constant-current threshold voltage extraction technique is used, the DIBL can simply be extracted from that available data.

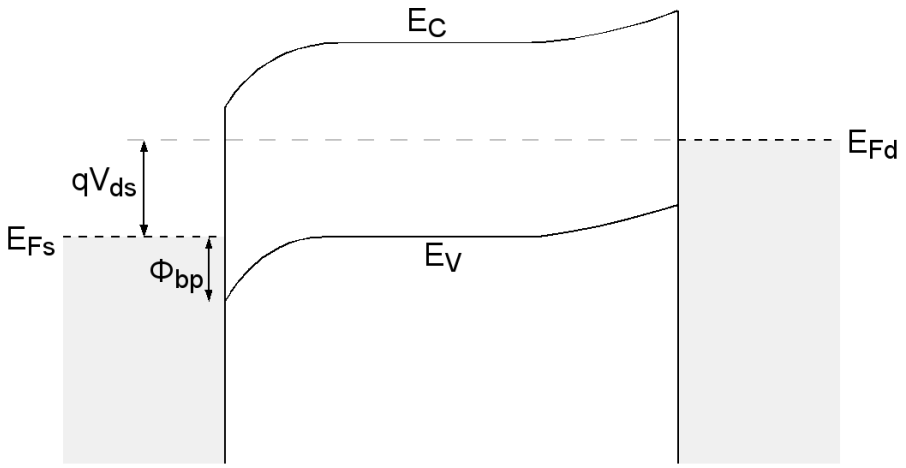

Figure 3.2: Energy band diagram of a SB-MOSFET in the ON state, highlighting the Schottky barrier height for holes.

3.2 Schottky Barrier Height

3.2.1 Overview

One of the critical parameters for understanding, improving and modelling of p-channel SB-MOSFETs is the Schottky barrier height for holes between source and channel, depicted by Φ_{bp} in Fig. 3.2. The method used in this work to experimentally extract this barrier height closely follows the approach of Calvet [2001] and Dubois and Larrieu [2004] using variable temperature measurements and an activation energy (Arrhenius) plot extraction technique.

While other barrier height measurement techniques, such as I-V or C-V measurements on diode structures, are available [Schroeder, 1998], none of these are suitable for use in this because they require knowledge of the electrically active contact area or are inacurate for low barrier heights [Dubois and Larrieu, 2004]. Moreover, it is the Schottky barrier for holes, Φ_{bp}, between source and inverted channel that is of interest. It would not be possible to extract this barrier height from I-V measurements on diode struc-

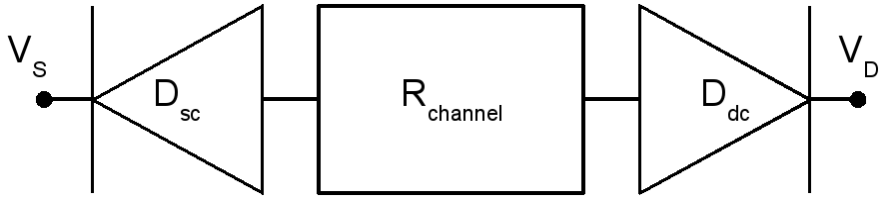

Figure 3.3: Back-to-back diode representation used to approximate the SB-MOSFET source-channel-drain regions for Schottky barrier height extraction.

tures on these wafers, since the substrate is n-type and Schottky barriers are majority carrier devices [Rhoderick and Williams, 1988], thus the current in a Schottky barrier diode would be due to electron flow controlled by the Schottky barrier to electrons. The measurement would extract this barrier, rather than the one for holes.

3.2.2 Method

The series combination of source-to-channel Schottky barrier, channel and drain-to-channel Schottky barrier present in a SB-MOSFET can be modelled by two back-to-back diodes separated by a resistance, as depicted in Fig. 3.2.2. When a negative bias is applied to the drain, the drain-to-channel diode becomes forward biased, whereas the source-to-channel diode is reverse biased. The former, being forward biased, is assumed to be perfectly conducting and the current flow is controlled by the series combination of source-to-channel diode D_{sc} and the channel resistance $R_{channel}$. The control of current flow will pass between source-to-channel diode for low channel resistances and channel resistance for high channel resitances. Therefore, in order to extract the source-to-channel Schottky barrier height for holes Φ_{bp}, the channel resistance must be low, i.e. the channel must be in inversion.

In that case, the current can be entirely described by the reverse diode current of the source-to-channel Schottky barrier. A purely thermionic-emission model is used to approximate the current in this approach, since a full thermionic-field emission model

would be too complex to analyse. This assumption is applicable for weak to moderate channel inversion which occurs at gate voltages around the threshold voltage V_t. The reverse saturation current I_s, introduced in section 2.3.6, of the source-to-channel diode assuming thermionic emission is described by [Rhoderick and Williams, 1988, Schroeder, 1998]

$$I_s = AA^{**}T^2 e^{\frac{-q\Phi_{bp,eff}}{kT}}. \tag{3.6}$$

Solving (3.6) for the effective barrier height for holes $\Phi_{bp,eff}$ gives

$$\Phi_{bp,eff} = \frac{kT}{q}[ln(AA^{**}) - ln(\frac{I_s}{T^2})], \tag{3.7}$$

where the parameters have the meanings outlined in section 2.3.6. Equation 3.7 suggests an activation energy plot of $ln(\frac{I_s}{T^2})$ versus $\frac{1}{kT}$ to determine the effective hole Schottky barrier height. This plot results in a straight line with a slope $q\Phi_{bp,eff}$ and a y-axis intercept of AA^{**}. This technique is equally applicable to n-channel devices to extract the effective Schottky barrier for electrons $\Phi_{bn,eff}$ by substituting it for $\Phi_{bp,eff}$ and reversing bias polarities.

3.2.3 Procedure

Transfer characteristics at a number of temperature points in the range of 77 to 300 K are measured under moderate drain voltage. V_{ds} must be large enough to ensure that the channel-to-drain barrier is forward biased for the technique to be valid. The measured currents I_d are used to calculate $ln(\frac{I_d}{T^2})$ for each bias point and temperature. Their values for a given gate voltage V_{gs} are taken for each temperature point and then plotted versus $\frac{1}{kT}$ to generate the Arrhenius plot. The slope of this plot gives the effective Schottky barrier height for holes $\Phi_{bp,eff}$.

The Arrhenius plot is then repeated for all gate voltages, resulting in a plot of $\Phi_{bp,eff}$ versus V_{gs}. Though these calculations may be performed for all gate voltages, the extracted effective hole barrier heights will only be valid for V_{gs} between OFF state and threshold, where thermionic emission of carriers is the dominant current contribution, as described in section 2.4.3. Additionally, the whole process may be repeated for different drain voltages to investigate the influence that V_{ds} has on the effective barrier height.

3.2.4 Considerations

There are a number of points to be aware of when applying this Schottky barrier height extraction technique. The first is that the reverse saturation current of the source-to-channel diode is approximated by a purely thermionic emission model, which is valid only for gate voltages up to the threshold voltage. At gate voltages above threshold, field emission becomes appreciable, adding to the thermionic emission current and the barrier height extracted using this technique will be considerably lower than the actual value, since field emission will exaggerate the drain current.

Secondly, the choice of drain bias V_{ds} is very important. It must be large enough to ensure that the channel-to-drain Schottky barrier is forward biased and does not impede current flow. If too small a drain bias is applied, the channel-to-drain diode will be reverse biased as well as the source-to-channel diode and the assumption of thermionic emission at a single Schottky barrier, on which this technique is based, is not valid. Typical zero-bias Schottky barrier heights for p-SB-MOSFET devices are in the region of 0.2 to 0.3 V, so a similar drain bias should be applied to ensure a forward biased channel-to-drain junction. At the same time, V_{ds} must be small enough for the horizontal electric field caused by the drain bias not to impact the electric field at the source-to-channel Schottky barrier. At high drain voltages, the large horizontal electric field may induce field emission of carriers from source to channel, thereby distorting the drain current.

Thirdly, the barrier height extracted is an effective barrier, i.e. it includes barrier lowering effects. The electric field at the metal-semiconductor interface serves to lower the actual barrier height to an effective value due to image force and dipole lowering effects. These barrier lowering mechanisms can have a large impact and the extracted values may be considerably lower than common literature values for the zero-bias barrier height.

Finally, under some conditions, in particular when the channel is in depletion or for long-channel devices, the channel resistance may dominate and the current is no longer limited by the source-to-channel Schottky barrier but by drift and diffusion in the channel region. This manifests itself in the Arrhenius plots as an increase in $ln(\frac{I_d}{T^2})$ with decreasing temperature. As temperatures are decreased, the Schottky barrier will begin to dominate and the lower temperature portion of the Arrhenius plot must be used for the barrier height extraction [Dubois and Larrieu, 2004].

3.3 Constant Current Mobility

3.3.1 Overview

In MOSFETs with non-ohmic source/drain-to-channel junctions, such as SB-MOSFETs, the conventional mobility measurement technique using a constant drain voltage [Schroeder, 1998] is no longer applicable, since it implicitly assumes ohmic source/drain-to-channel contacts [Lu and Cooper, 2005]. If the source and drain junctions exhibit some form of non-linear resistance, such as unannealed source/drains or Schottky barriers do, then the relationship between voltage across and current through the contact will vary highly depending on the voltage. As such, the contact properties will have a large impact on the current.

In the case of SB-MOSFETs, the electrostatic potential difference between channel and source controls current flow from the latter to the former. The resistance of the

source-to-channel barrier in the OFF and subthreshold regimes is vastly greater than in the ON state and thus the voltage dropped across it varies greatly with applied gate bias. By forcing a constant drain current instead of a voltage, the voltage dropped at source-to-channel interface remains constant, allowing extraction of effective mobility of carriers in the channel. However, as will be explained subsequently, this approach requires devices of different gate lengths to be applicable.

Though the application of this technique to MOSFETs with unannealed source and drain regions has been published in Lu and Cooper [2005], the derivation and application presented in this work differ slightly and were developed independently from Lu and Cooper [2005] and prior to its publication, so the author lays claim to its novelty.

3.3.2 Theory

The drain current in a conventional MOSFET in the linear regime is given by [Lu and Cooper, 2005, Schroeder, 1998]

$$I_d = \mu_{eff} \frac{W}{L} Q_i V_{ds}, \tag{3.8}$$

where I_d is drain current, μ_{eff} effective mobility, W and L device width and effective length, respectively, Q_i inversion charge per unit area and V_{ds} the drain voltage with respect to source (usually ground). Q_i is dependent on V_{gs} and is either obtained using a split-CV measurement [Koomen, 1973] or calculated using [Sze, 1981, Schroeder, 1998]

$$Q_i = C_{ox}(V_{gs} - V_t), \tag{3.9}$$

where C_{ox} is the oxide capacitance per unit area and V_t is the threshold voltage. The conventional method for extracting the effective mobility in MOSFETs is to apply a fixed drain voltage and acquire the drain current via an I-V measurement and the inversion

charge density using a split-C-V technique [Koomen, 1973]. The measured quantities are then used with eqn. 3.8 to calculate the effective mobility μ_{eff}.

To be more precise, V_{ds} in eqn. 3.8 must be the voltage drop between source and drain ends of the channel, not source and drain contact pads. The difference between the two is the potential drop across the source and drain series resistances. In a DSD MOSFET, source and drain series resistances are either small enough to be neglected or constant at all gate voltages and can be corrected for by accounting for series resistance.

However, a significant portion of the measured drain voltage $V_{ds,meas}$ in a SB-MOSFET is dropped at the source-to-channel Schottky barrier. Moreover, because of the abrupt nature of metal-semiconductor junctions, this voltage drop also changes drastically with gate voltage, making a correction to account for series resistance unfeasible.

These difficulties can be circumvented by applying a constant drain *current* instead of a constant *voltage*. In doing so, the voltage dropped at the source-to-channel Schottky barrier is fixed. Equation 3.8 can be expressed as

$$\mu_{eff} = \frac{I_d}{Q_i W} \frac{1}{\frac{dV_{ds}}{dL}} \tag{3.10}$$

By applying a fixed drain current I_d, measuring the drain voltage V_{ds} and calculating or measuring Q_i for devices of varying gate lengths L, it is possible to extract the effective mobility μ_{eff} using eqn. 3.10.

V_{ds} in eqn. 3.10 refers to the voltage drop between source and drain ends of the channel, not the measured quantity $V_{ds,meas}$. $V_{ds,meas}$ is the sum of three components, i.e.

$$V_{ds,meas} = V_{dj} + V_{ds} + V_{sj}, \tag{3.11}$$

where V_{dj} and V_{sj} are the voltages dropped across the drain and source junctions, respectively. For SB-MOSFETs, these voltage drops are non-linear with respect to applied voltages, but constant with respect to drain current. Taking the derivative of eqn. 3.11 with respect to gate length L gives

$$\frac{dV_{ds,meas}}{dL} = \frac{dV_{dj}}{dL} + \frac{dV_{ds}}{dL} + \frac{dV_{sj}}{dL}. \tag{3.12}$$

Since a constant current is applied to the drain, the voltage drops across source/drain-to-channel junctions are assumed to be constant and their derivatives are zero. Thus, eqn. 3.12 reduces to

$$\frac{dV_{ds,meas}}{dL} = \frac{dV_{ds}}{dL}, \tag{3.13}$$

and the derivative of the measured drain voltage with gate length can simply be used, saving on complicated source/drain resistance extraction techniques. This method hinges strongly on the assumption that, for a constant current, the voltage drop across source/drain-to-channel junctions does not vary with gate length L. In the case of the SB-MOSFETs under investigation in this work, this assumption is thought to be appropriate since all devices were fabricated under the same conditions.

3.3.3 Method

A fixed, small drain current I_d (e.g. 10 nA) is forced at the drain terminal with the source grounded and the drain voltage V_{ds} is measured as a function of gate voltage V_{gs}. This measurement is repeated for devices of different gate lengths L.

A plot of V_{ds} versus gate length L is generated for each gate voltage V_{gs}. The slope of this line is proportional to the effective mobility μ_{eff} according to eqn. 3.10. Together with knowledge of the inversion charge density Q_i, measured or calculated, and the

device width W, the effective mobility is calculated using eqn. 3.10 and plotted against V_{gs}.

3.4 RF Characterisation

3.4.1 Overview

Radio frequency (RF) characterisation of electronic devices is concerned with the measurement of their high frequency characteristics, typically in the GHz range. The most significant figure of merit for this work is the unity-gain cutoff frequency f_T, which represents the frequency at which a transistor no longer amplifies, i.e. it's current gain is greater than unity below and less than unity above this frequency.

High-frequency performance is significant mainly for analog applications in medical, industrial and household appliances, but also implies potentially high switching speeds in digital circuitry. Furthermore, telecommunications benefit from higher frequency ranges as it increases available bandwidths and thus data transfer rates. RF measurements are performed using a network analyser to measure scattering (S-)parameters. As a transistor is a four terminal device, all the following is based on a four-terminal (or two-port) network.

3.4.2 S-Parameters

Such a two-port network is depicted in Fig. 3.4

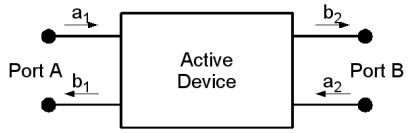

Figure 3.4: Schematic diagram of a two-port electrical network indicating the nomenclature for the incident and reflected waves at both ports.

The corresponding S-parameter matrix is [Agilent, Raskin, 1997]

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}, \tag{3.14}$$

where a_n and b_n are the incident and reflected power waves, respectively, of the two-port model as labelled in Fig. 3.4. The S-parameters describe the scattering and reflection, in terms of power, of travelling electromagnetic waves from a two-port network, such as a transistor, and are a strong function of frequency. They are complex, dimensionless numbers describing both magnitude and phase of the electromagnetic waves. They are closely related to other parameters, such as admittance (Y-)parameters and impedance (Z-)parameters, and it is possible to convert to and from these other parameters. Common descriptions of the four S-parameters of a two-port network as described by eqn. 3.14 are [Agilent]

- S_{11}: input reflection coefficient
- S_{21}: forward transmission coefficient
- S_{12}: reverse transmission coefficient
- S_{22}: output reflection coefficient

The main benefit of using S-parameters is that they are measured with all ports terminated by their nominal impedance, generally 50 Ω. In contrast, Y- and Z-parameter measurements require either currents to be measured or ports to be open or short circuited, both of which are impractical at radio and microwave frequencies. Thus, S-parameter measurements can be performed at much higher frequencies [Agilent]. Furthermore, it is possible to convert between S- and Y-parameters as well as between Y- and Z-parameters, which is necessary for deembedding purposes.

Being complex in nature, S-parameters capture both magnitude and phase information of the network being characterised. With an equivalent circuit of the device under test, it is possible to extract information about the electrical characteristics, with magnitudes (real parts) corresponding to conductances (and hence resistances) and phases (imaginary parts) to capacitances. For example, the magnitude of S_{21} represents the transconductance.

3.4.3 Measurement Setup

RF measurements are taken on dedicated on-wafer RF structures consisting of MOSFET devices embedded in coplanar waveguides. Special radio-frequency probe needles are used for contacting to device contact pads. A network analyser, in this case an Agilent 8510XF, is used to measure S-parameters.

A measurement consists of a frequency sweep with fixed terminal voltages for the duration of a measurement. The bias voltages used in this work were selected based on ITRS recommendations for high-performance logic [International Technology Roadmap for Semiconductors, 2000 Update]. At each frequency, the network analyser measures the four S-parameters outlined previously. However, since the device is embedded in a waveguide, the measured S-parameters contain its high-frequency properties as well as the characteristics of the device itself. It is therefore necessary to extract the intrinsic active device data from the raw measured S-parameters in order to obtain the high-frequency characteristics of the active device alone. This process is called *S-parameter deembedding*.

3.4.4 S-parameter Deembedding

Any measured active device S-parameter data contains parasitics related to the contact and access structures necessary for probing during measurements. These parasitics consist of capacitances and conductances that, while negligible for DC measurements,

cannot be disregarded for RF characterisation. At high frequencies, the capacitances and conductances of the contact pads become more prominent and are detrimental to the extraction of useful information about the device itself and must thus be removed to leave the intrinsic device properties.

There are several common procedures in use, the most common being OPEN and OPEN-SHORT deembedding, that were initially employed in this work. However, due to the properties of the device and its access structure, conventional techniques were deemed inadequate and an improved technique, termed *ColdFET* deembedding [Paillonc y and Raskin, 2006] was applied to these SB-MOSFET devices to circumvent these limitations.

OPEN and OPEN-SHORT Deembedding

Two of the most common S-parameter deembedding techniques the *OPEN* and *OPEN-SHORT* methods, in which access structure parasitics are removed by measuring so-called 'OPEN' and 'SHORT' structures at the same frequencies as the device. The OPEN structure dedicated on-wafer test structure of identical geometry to the access structure of the device under test, but does not contain the transistor itself. The SHORT structure is similar, except that gate and drain terminals are shorted. Both are passive structure whose high-frequency characteristics must accurately reflect the properties of the device access structure in order to be able to deembed measurement data.

Measured S-parameters of device and OPEN deembedding structure are converted to admittances (Y-parameters) and subtracted from each other. This *OPEN deembedding* step removes parasitics related to the access structure and leave only the high-frequency characteristics of the device itself. For *OPEN-SHORT deembedding* an additional step is taken that makes use of the S-parameters measured on the SHORT deembedding structure.

In order for these methods to be accurate, the geometry of the OPEN and SHORT deembedding structures must be identical to the access structure of the device. Also, the electrical characteristics of the deembedding structures, in particular their capacitance and resistance, should be as small as possible compared to the device properties, otherwise small errors in deembedding measurements can lead to large variations in deembedded results. Usually, this is achieved by fabricating devices with large numbers of parallel gate fingers to increase the total device width.

ColdFET Deembedding

In view of contacting problems experienced when attempting to deembed the measured data on the SB-MOSFET devices of this work, a new technique was applied to deembed measured S-parameters. Instead of employing separate measurements on dedicated deembedding structures, such as OPEN and SHORT, a measurement of the device biased in the OFF state is used for deembedding. This approach has several advantages [Paillonc y and Raskin, 2006]:

- No recontacting between deembedding and active measurement is required, thus rendering the technique insensitive to contacting variations.
- No need for separate deembedding structures on wafer.
- Insensitivity to dispersion issues related to the access structures, such as contact variability or field oxide non-uniformity.

The small-signal equivalent circuit (SSEQ) used to model SB-MOSFETs at RF frequencies is depicted in Fig. 3.5. Such a SSEQ is necessary for extraction of specific device capacitances and resistances from S-, Y- or Z-parameters.

The model shown in Fig. 3.5 includes the parasitic elements of the contact pads. The dashed-line rectangle draws the boundary between elements that are intrinsic and

extrinsic to the SB-MOSFET. The intrinsic elements are the ones that are of interest to the measurement, while the extrinsic ones, related to either stray effects within the device or the access structure used for probing to the device, need to be removed in the S-parameter deembedding process.

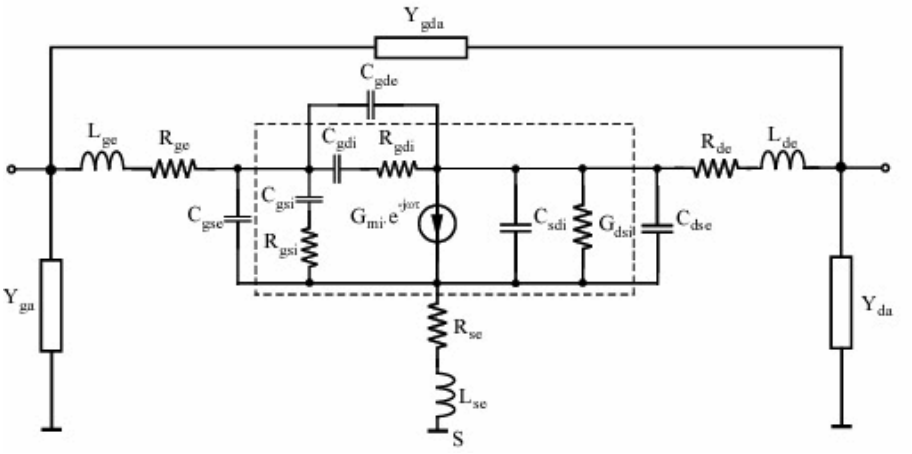

Figure 3.5: Small-signal equivalent circuit used to model the SB-MOSFET devices characterised. The dashed-line rectangle represents the boundary between elements intrinsic to the SB-MOSFET device and extrinsic parasitic contributions.

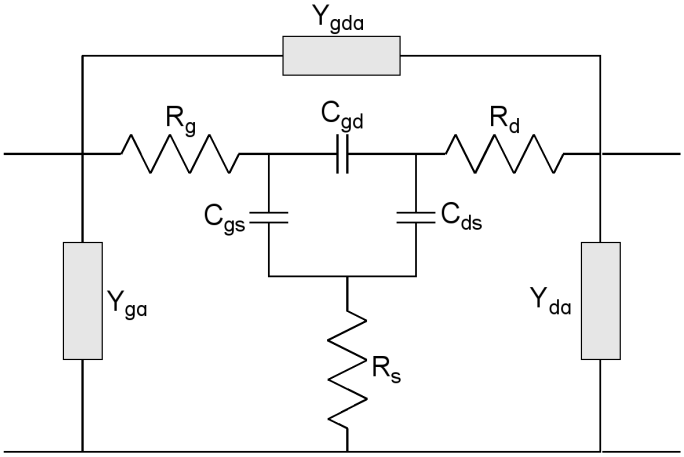

Figure 3.6: Small signal equivalent circuit of a transistor biased in ColdFET conditions

The aim of the deembedding procedure is to withdraw all parasitics related to the device access structure from the measured S-parameter data. When the device is biased well below threshold and in absence of a drain bias, i.e. under so-called *ColdFET* conditions, it can be represented by the small signal equivalent circuit in Fig. 3.6.

Under the assumption that the transistor is symmetrical, i.e. $C_{gs} = C_{gd}$, the three parasitic admittances corresponding to the access structure can be extracted from the total ColdFET Y-matrix Y_{COLD} (which is derived from the measured S-parameters).

$$Y_{ga} = Y_{COLD.11} + 2Y_{COLD.12} \tag{3.15}$$

$$Y_{da} = Y_{COLD.22} + Y_{COLD.12} \tag{3.16}$$

$$Y_{gda} = Y_{COLD.22} - Y_{COLD.11} \tag{3.17}$$

Next, the device is measured under the bias conditions of interest, such as saturation, and converted to an admittance matrix Y_{MOS}. The data can then be deembedded resulting in a deembedded Y-matrix Y_{COR} according to

$$Y_{COR.11} = Y_{MOS.11} - Y_{ga} \tag{3.18}$$

$$Y_{COR.12} = Y_{MOS.12} + Y_{gda} \tag{3.19}$$

$$Y_{COR.21} = Y_{MOS.21} + Y_{gda} \tag{3.20}$$

$$Y_{COR.22} = Y_{MOS.22} - Y_{da} \tag{3.21}$$

The deembedded Y-matrix Y_{COR} is then used for subsequent extraction of RF performance parameters, in particular the unity-gain cutoff frequency. The validity of the ColdFET technique has been established by comparison to results using conventional deembedding techniques on a different wafer [Paillocny and Raskin, 2006]. The comparison was performed by collaborators and is therefore not included in this work. The results presented are the first application of this novel deembedding technique.

3.4.5 Current Gain and Unity-Gain Cutoff Frequency

The high-frequency current gain H_{21} of a transistor can be calculated using Agilent, Raskin [1997]

$$|H_{21}| = \frac{|i_2|}{|i_1|} = \frac{|Y_{21}|}{|Y_{11}|} = \left| \frac{-2_{21}}{(1-2_{11})(1+S_{22}) + S_{12}S_{21}} \right|, \tag{3.22}$$

where Y_{nn} and S_{nn} represent elements of the deembedded Y- and S-parameter matrices, respectively. A plot of H_{21} versus the logarithm of frequency exhibits a slope of -20 dB/dec and the point at which the current gain crosses unity or 0 dB is termed the *unity-gain cutoff frequency* and is commonly denoted by f_T [Agilent, Raskin, 1997]. It represents the point at which the transistor ceases to amplify and is a measure of the potential analog frequency performance of a device.

Chapter 4

DC Characterisation of SB-MOSFETs

This chapter presents all the static (DC) measurement results and analysis obtained on PtSi source/drain SB-MOSFETs. After a description of the samples characterised, measurement of the source-to-channel Schottky barrier height are presented, as it is fundamental to subsequent analysis. Next, the extraction of the effective hole mobility using the constant drain current method is described. Transfer and output characteristics and transconductance curves are presented and analysed for ON and OFF currents, I_{ON}/I_{OFF} ratio, peak transconductance, threshold voltage, drain induced barrier lowering (DIBL) and subthreshold slope. Device performance is then compared for wafers with differing source/drain silicide anneal temperatures and differing channel implant doses. Finally, SB-MOSFET transfer characteristics at ambient temperatures down to 80 K are investigated.

4.1 Sample Description

The SB-MOSFET devices characterised in this work were provided by Spinnaker Semiconductor based in Minneapolis, USA, and their electrical characterisation is part of

ongoing collaborative work. The device structure and properties pertinent to electrical characterisation will briefly be described in the following.

A cross-sectional TEM image of a 25 nm gate length PtSi source/drain SB-MOSFET is shown in Fig. 4.1 to illustrate the device structure. The generalised cross-sectional schematic labelled with the most important device dimensions depicted in Fig. 4.2 summarises the most important dimensional parameters. Other than the channel length and the device width, all dimensions are identical for all characterised devices.

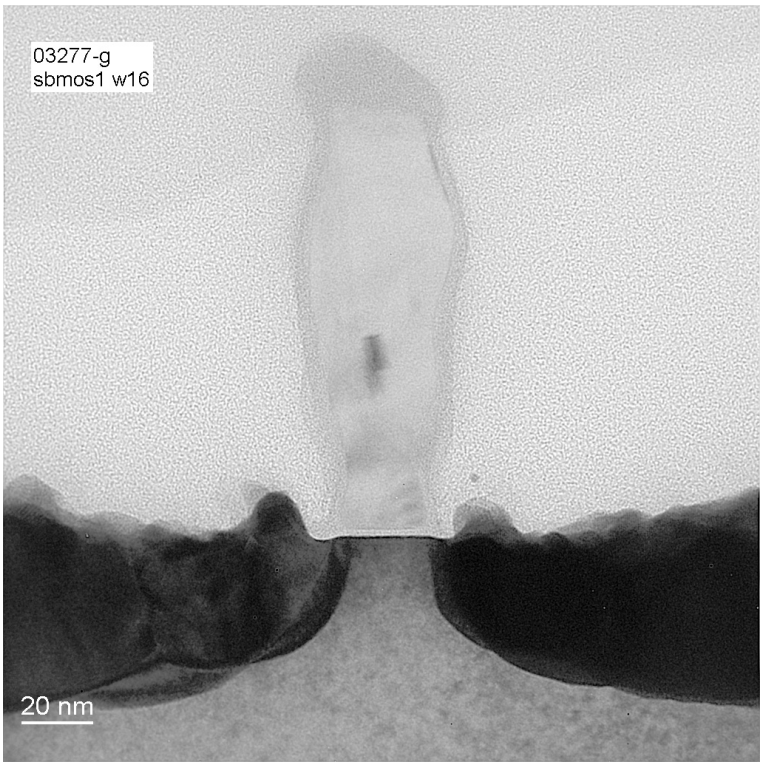

Figure 4.1: Cross-sectional TEM image of a 25 nm SB-MOSFET.

The dark regions on the left and right in Fig. 4.1 are the 50 nm deep PtSi source and drain regions, formed by silicidation of Pt at either 500 or 550 °C for 1 hour. The n-doped, retrograde channel doping profile was created by ion implantation of Arsenic of dose $5 \cdot 10^{12}$ or $1 \cdot 10^{13}$ cm^{-2} into a lightly phosphorous-doped bulk silicon substrate

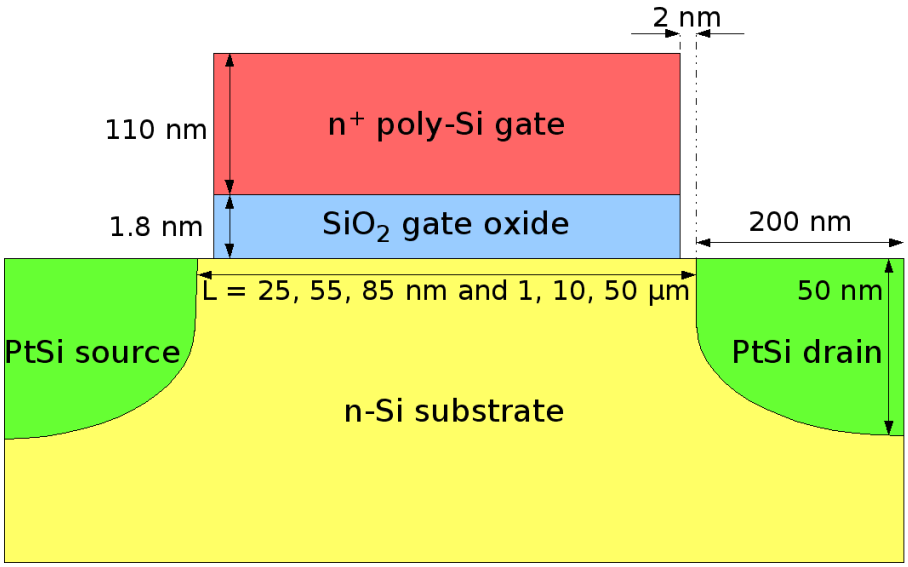

Figure 4.2: Schematic cross-section of a SB-MOSFET device characterised in this work along with labels indicating important dimensions.

followed by two rapid thermal anneals (RTAs) at 1050 and 1100 °C for 10 and 5 seconds, respectively. The first RTA represents the channel implant activation and the second the sidewall spacer anneal. The channel implant doses of $5 \cdot 10^{12}$ and $1 \cdot 10^{13}$ cm^{-2} will be referred to as *half dose* and *full dose*, respectively, throughout the remainder of the work.

The channel implants result in retrograde doping profiles with surface concentrations of 1.5 and $2.8 \cdot 10^{16}$ cm^{-3} for half and full dose implants, respectively. Fig. 4.3 compares measured SIMS data to two simulated doping profiles generated by the author, which will be discussed in detail in chapter 6. The SIMS data (black diamonds in Fig. 4.3) is noisy because the measured concentrations between 10^{16} and 10^{18} cm^{-3} are close to the measurement limitations of the SIMS equipment. As such, data from the simulated curves will be used in the analysis.

The surface concentration in these devices is considerably lower than for conventional DSD MOSFETs, since the large Schottky barrier to electrons acts as a barrier to current

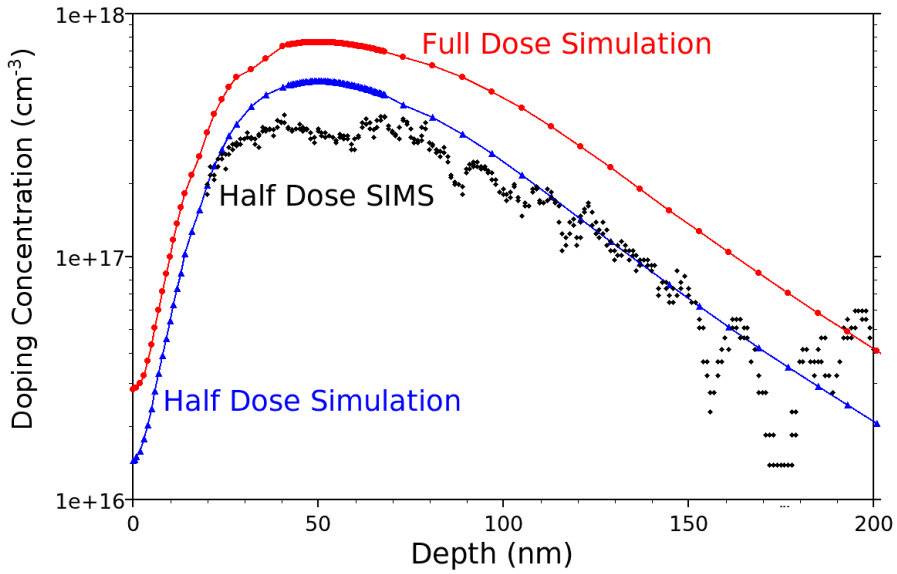

Figure 4.3: Vertical doping concentration profiles in the SB-MOSFET channel. Black diamonds: measured SIMS; Red circles: full dose simulation; Blue triangles: half dose simulation.

flow in the OFF state by permitting only very small thermionic emission currents. The 90 nm gate length 'well-tempered' MOSFET available on the MIT website [Antoniadis, 2001] has a surface concentration of $1 \cdot 10^{17}$ cm^{-3}, which is about 7 and 4 times the surface concentration present in these SB-MOSFETs.

The combination of source/drain silicide anneal temperature and channel implant doses gives a wafer split of four, three of which are characterised in this work. The designations and corresponding properties of the wafers are summarised in Table 4.1. All other device parameters are identical for all three wafers.

	Silicide Anneal Temperature	
Channel Implant Dose	**550 °C**	**500 °C**
Full ($1 \cdot 10^{13}$ cm^{-2})		SBMOS2 #17
Half ($5 \cdot 10^{12}$ cm^{-2})	SBMOS2 #18	SBMOS2 #19

Table 4.1: Designations and process parameters of four wafers available for characterisation.

The gate oxide consists of 1.8 nm thick SiO_2 that isolates the channel from the 110 nm thick, in-situ phosphorous doped, n-type polysilicon gate electrode. An n-type, instead of the usual p-type, polysilicon gate material was used due to process limitations at the time of fabrication. This manifests itself as a 1.12 V shift in all gate voltages from typically expected values for p-channel devices and must be considered when analysing I-V measurements. Aluminium contact pads situated on top of 250 nm SiO_2 field oxide are used for probing to devices. Six device gate lengths, 50, 10 and 1 μm and 85, 65 and 25 nm and two device widths each, 2 and 10 μm, are present on each of the wafers. The mask layout for all three wafers is identical, so the dimensions of corresponding devices on each wafer are assumed to be the same.

Most of this work focuses on the characterisation of devices on wafers SBMOS2 #18 and #19, the two wafers with the *half dose* channel implant. The lower channel implant dose generally results in improved device performance, in terms of both drive current and transconductance. SBMOS2 #17 is characterised to investigate the impact of the higher channel doping on device performance.

High gate leakage currents due to the very thin gate oxide are observed on all devices, which prevents any direct capacitive measurement, whether quasi-static or high-frequency, and prevents quantitative characterisation of the gate oxide and its capacitance. The thin gate oxide thickness additionally impacts device yield and requires any light sources to be switched off when contacting to avoid gate oxide breakdown. The yield among 2 μm wide devices is substantially higher than for 10 μm width. 50 and 10 μm gate length devices are unusable since their gate leakage currents are comparable to drain currents due to their large gate area and the high gate leakage current density as well as the low drain current because of the long channel length.

The bulk of device characterisation is performed on 85 nm gate length devices, since their yield of working devices is considerably higher than any other gate length. Though

25 and 55 nm gate length devices are present on the wafers, the yield of working devices among them was too small to make any conclusive analysis.

No doped source/drain control devices are available either, due to the added complexity that would have been incurred during the fabrication. As such, all performance comparisons must be made with results in the literature. Furthermore, to provide meaningful comparison, only conventional MOSFETs on bulk Si substrates are chosen as controls.

4.2 Schottky Barrier Height

The effective Schottky barrier height for holes between source and channel, $\Phi_{bp,eff}$, is measured using a series of current-voltage measurements at temperatures from 80 to 290 K together with Arrhenius plots for the barrier height extraction, as described in section 3.2. Since these results are fundamental to the analysis performed in the rest of this chapter, they are presented first. The barrier height extraction is performed for two wafers, SBMOS2 # 18 and #19, with the same half-dose channel implant and differing source/drain silicide anneal temperatures of 550 and 500 °C, respectively.

Transfer characteristics of three 85 nm gate length devices on each wafer were measured in a Desert Cryogenics TT-Prober environmental probe station at temperatures of 290, 250, 200, 150, 100 and 80 K using an Agilent 4156C Parameter Analyzer. The gate voltage $|V_{gs}|$ is swept from 0 to 3 V in 50 mV steps for drain biases $|V_{ds}|$ from 0.1 to 0.5 V in 100 mV steps.

Transfer characteristics of wafer SBMOS2 #19 (500 °C anneal) are shown in Fig. 4.4 for a drain bias $|V_{ds}|$ of 0.5 V. The corresponding curves for wafer SBMOS2 #18 (550 °C anneal) are identical in shape, though the current magnitudes are slightly smaller, and are not shown. The noisy data at drain currents of about 10^{-7} mA/mm are an

artifact of the resolution limit of the measurement equipment. Considering a device width of 2 μm, the magnitudes of measured currents are of the order of 100 fA, which is very close to the lower limit of the measurement range of the parameter analyser. Because of this, these data points will be omitted when extracting the barrier height.

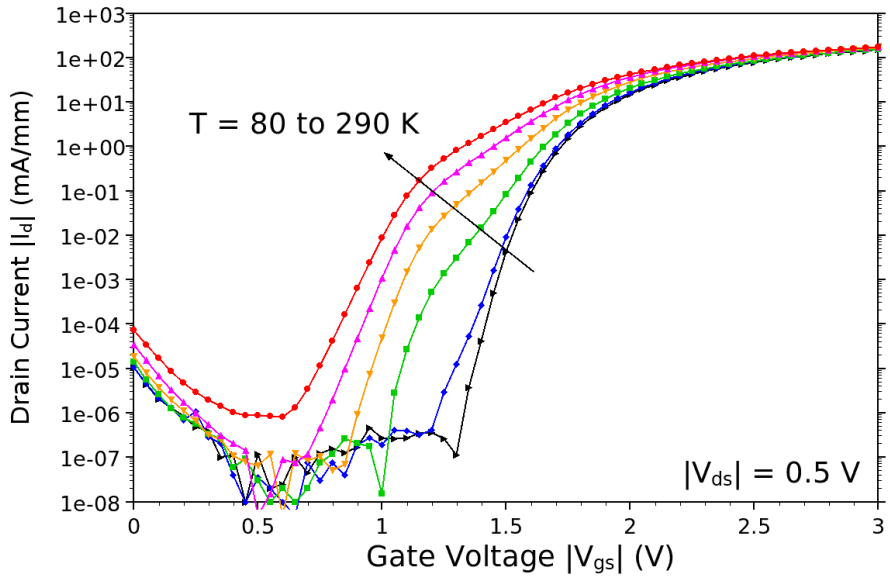

Figure 4.4: Transfer characteristic for $|V_{ds}| = 0.5$ V and temperatures from 290 down to 80 K for a typical device on wafer SBMOS2 #19.

A drain bias of 0.5 V is chosen for the effective Schottky barrier height extraction for the following reasons. Firstly, the drain voltage must be large enough to forward bias the channel-to-drain junction, requiring a drain voltage greater than the zero-bias Schottky barrier height Φ_{b0} of the PtSi-Si system. The generally quoted literature values of 0.22 to 0.28 V for Φ_{b0} suggests at least 0.3 V to be safe.

Secondly, as evident from Fig. 4.4, the parameter analyser is not capable of resolving currents below 10^{-7} mA/mm. At the lowest drain voltages and temperatures, this limit is reached at gate voltages in excess of the room temperature threshold voltage, recommending as high a drain voltage as possible in order to increase the drain current

magnitudes at low temperatures. The upper limit for the drain bias is the voltage at which the tunneling contribution of the drain current becomes appreciable, since that would invalidate the basic assumption of the Schottky barrier height extraction technique. As a compromise between the two lower and the high drain voltage limitations, a drain bias $|V_{ds}| = 0.5$ V is chosen as a suitable value, since it is deemed high enough to extract barrier heights with reasonable accuracy but low enough to be sure of not inducing a significant tunneling current at subthreshold gate voltages.

Because of the very small change in drain current between 80 and 100 K, the data for 80 K is discarded for the extraction of the Schottky barrier height. At 80 K, the SB-MOSFET device is assumed to be a pure tunneling device, evident by the absence of the typical tri-slope shape of the transfer characteristic for 80 K in Fig. 4.4.

The values of $ln(\frac{I_d}{T^2})$ of the drain currents shown in Fig. 4.4 for a fixed gate voltage are calculated and then plotted against gate voltage in an Arrhenius plot. Sample Arrhenius plots at a drain bias of 0.5 V and gate biases of 1.1 to 1.5 V in 100 mV steps for one of the measured devices on wafer SBMOS2 #19 are shown in Fig. 4.5. The slopes of these lines directly give the effective Schottky barrier height for holes, $\Phi_{bp,eff}$, in eV, for the corresponding gate voltage $|V_{gs}|$. This extraction is repeated for all measured gate voltages.

For gate voltages of 1.1 V and below, data points at the lower resolution limit of the parameter analyser are discarded and the barrier height extraction is performed using the remaining data for higher temperatures. Doing so omits the data for 100 K at $|V_{gs}| = 1.1$ V, then, with decreasing gate voltage, the data for successively increasing temperatures. This allows barrier height extraction for a wider range of gate voltages.

The average effective Schottky barrier height extracted in this manner on several 85 nm gate length devices on each wafer is compared in Fig. 4.6 as a function of gate

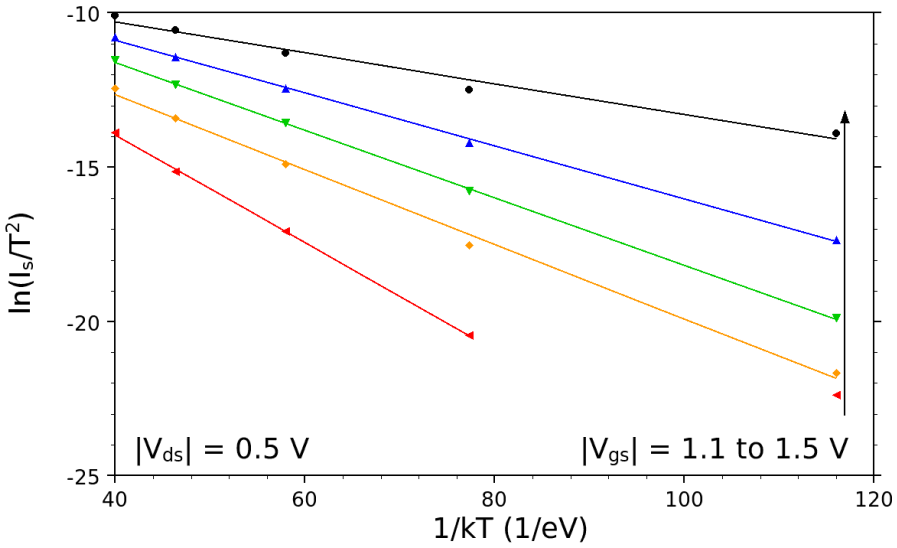

Figure 4.5: Arrhenius plots at $|V_{ds}| = 0.5$ V for $|V_{gs}| = 1.1$ to 1.5 V on the wafer annealed at 500 °C.

voltage for wafers annealed at 500 and 550 °C. As described in section 3.2, the basic assumption of thermionic emission in SB-MOSFET devices is only valid for a very small range of gate voltages in the vicinity of the threshold voltage, typically around 1.1 - 1.2 V.

At very low gate voltages, below $|V_{gs}| = 1.0$ V, drain currents at low temperatures become too small for accurate measurement, resulting in negligibly small measured current variations with temperature [Calvet, 2001].

At higher gate voltage, above $|V_{gs}| = 1.4$ V, the channel begins to invert and thermionic-field and field emission of carriers from the source through the Schottky barrier into the channel contribute to the drain current. The basic assumption of the effective barrier height extraction method, the dominance of thermionic emission current, is no longer applicable and the extracted barrier height is no longer accurate. Since tunneling is considerably less temperature dependent than thermionic emission, the drain current no longer decreases with temperature as predicted by eqn. 3.6 and thus, the

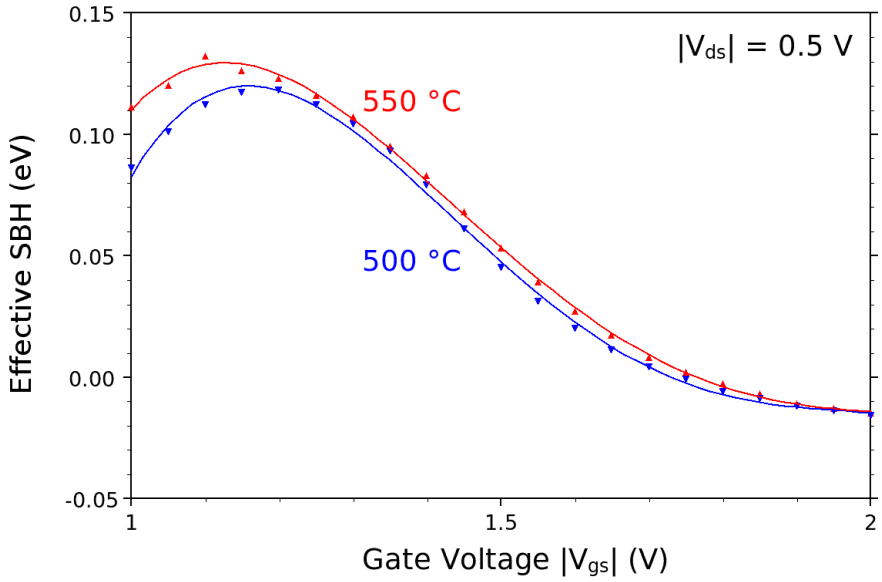

Figure 4.6: Average effective Schottky barrier height versus gate voltage at $|V_{ds}| =$ 0.5 V for devices on wafers annealed at 500 and 550 °C. The latter exhibits a higher effective barrier height.

extracted barrier height decreases, eventually becoming negative.

Taking the effective Schottky barrier height at $|V_{gs}| = 1.15$ V in order to account for the n-type rather than p-type gate material returns barrier heights of 117 $\pm$ 5 meV and 128 $\pm$ 5 meV for wafers annealed at 500 and 550 °C, respectively, an increase of 9%. These values agree reasonably well with results obtained by Dubois and Larrieu [2004] using the same technique on PtSi-Si junctions annealed at 500 °C. Moreover, the barrier height increase with temperature is consistent with barrier height increases observed by Dubois and Larrieu [2004] from 300 to 500 °C.

The extracted Schottky barrier heights of 0.117 and 0.128 eV are considerably smaller than commonly reported zero-bias hole Schottky barrier heights for PtSi-Si of 0.22 to 0.28 eV [Canali et al., 1977, Kikuchi, 1998, Koeneke et al., 1981, Lepselter and Sze, 1968, Murarka, 1983, Sze, 1981, Tanabe et al., 1991]. This may be explained by the

fact that the barrier height extracted in this work is an effective barrier that includes barrier lowering effects. Image force and dipole lowering result from the horizontal electric field at the interface and have been described in section 2.3. Additionally, interface defects have been shown to reduce Schottky barrier heights for PtSi on n-type substrates [Kikuchi, 1998] and this effect may be present in these devices.

Taking the ratio of the thermionic emission currents for the two wafers, $I_{TE,500}$ and $I_{TE,550}$, as a function of the corresponding barrier heights Φ_{500} and Φ_{550}, gives

$$\frac{I_{TE,500}}{I_{TE,550}} = \frac{AA^{**}T^2 e^{\frac{\Phi_{500}}{kT}}}{AA^{**}T^2 e^{\frac{\Phi_{550}}{kT}}} = e^{\frac{\Phi_{500}-\Phi_{550}}{kT}}. \tag{4.1}$$

For the measured average effective Schottky barrier heights of 117 and 128 meV, this predicts an average thermionic emission current ratio of $e^{\frac{0.011}{0.026}} = 1.5$. Taking into account the errors on the extracted barrier heights, this results in expected ratios between 1.1 to 2.2.

The relatively large spread of extracted effective barrier heights and is consistent with observations made during the I-V characterisation of many devices on the two wafers. SB-MOSFETs on wafer SBMOS2 #19, annealed at 500 °C, generally exhibit higher drain currents in the ON state than devices on wafer SBMOS2 #18, annealed at 550 °C. However, the best devices on the latter exhibit comparable performance to the worst devices on the former, while the best on the former substantially outperform the worst on the latter wafer.

The spread of the extracted barrier heights can be attributed to the non-homogeneity of Schottky contacts. The abrupt junction properties can lead to variations in electrical properties, due to interface states or defects, for metal-semiconductor contacts formed in identical fabrication steps. This manifests itself in the large spread of zero-bias Schottky barrier heights of 0.22 to 0.28 eV reported in literature.

4.3 Constant-Current Mobility

The constant current mobility extraction technique, outlined in section 3.3, is applied to devices on wafer SBMOS4 #18. The wafer originated from a different batch, SB-MOS4 instead of SBMOS2, than the ones characterised in the previous sections and underwent an altered fabrication process. Due to the altered processing and the availability of only one wafer of the SBMOS4 series, a full electrical characterisation will be omitted and just the constant current mobility extraction is presented. In general, electrical characteristics of devices on this wafer are very similar to those presented in the previous sections.

The measured drain voltage $|V_{ds}|$ for a forced drain current $|I_{ds}|$ of 10 nA are compared for gate lengths of 55 and 85 nm and 1 μm in Fig. 4.7. The drain voltage exhibits the expected increase with gate length.

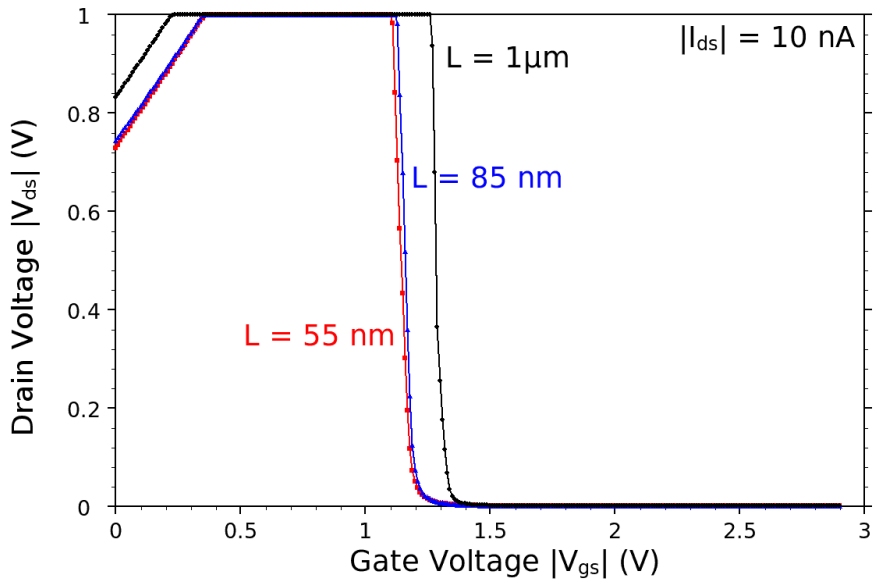

Figure 4.7: Measured drain voltages $|V_{ds}|$ for a forced drain current $|I_{ds}|$ of 10 nA for SB-MOSFETs of gate lengths of 55 and 85 nm and 1 μm on wafer SBMOS4 #18. A drain voltage compliance limit of 1 V is applied during measurements.

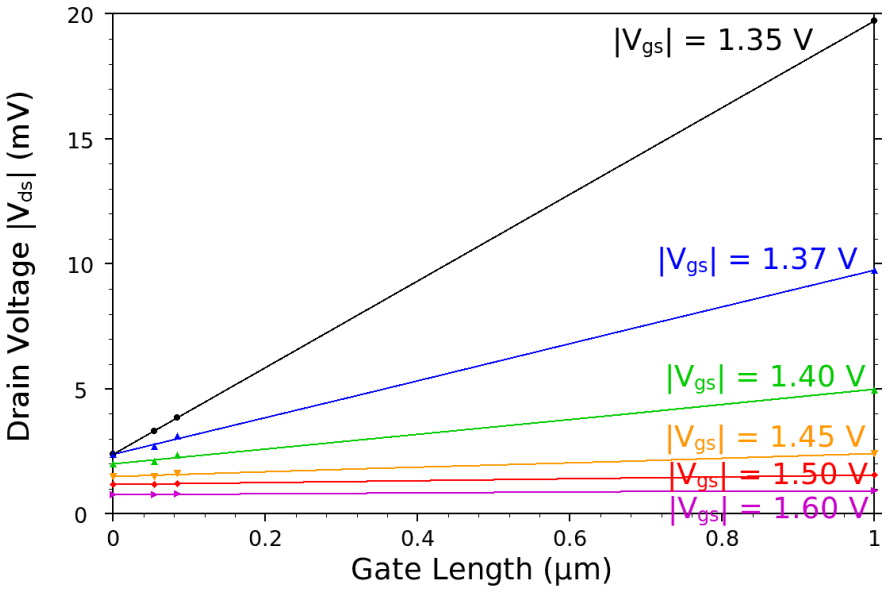

Figure 4.8: Sample drain voltage versus gate length plots at selected gate voltages.

Taking the measured drain voltages for these three gate lengths at a fixed gate voltage and plotting $|V_{ds}|$ versus L generates the straight line plots shown in Fig. 4.8 for selected values of $|V_{gs}|$. The points at $L = 0$ represents the linear extrapolation of the other three points.

Taking the slope $\frac{dV}{dL}$ of the $|V_{ds}|$-L curves for all measurement points allows the effective mobility to be calculated according to eqn. 3.10. Since capacitive measurements are not feasible due to gate leakage issues, the inversion charge Q_i is estimated using $Q_i = C_{ox}(V_{gs} - V_t)$, where the oxide capacitance C_{ox} is calaculated from the device dimensions and the threshold voltage V_t is taken from measured transfer characteristics. The effective mobility μ_{eff} extracted in this manner is depicted versus gate overdrive $|V_{gt}| = |V_{gs} - V_t|$ in Fig. 4.9.

Due to the leaky gate oxide, an extraction of the depletion charge, and hence the vertical effective field, is not possible, so no direct comparison with the universal mobility

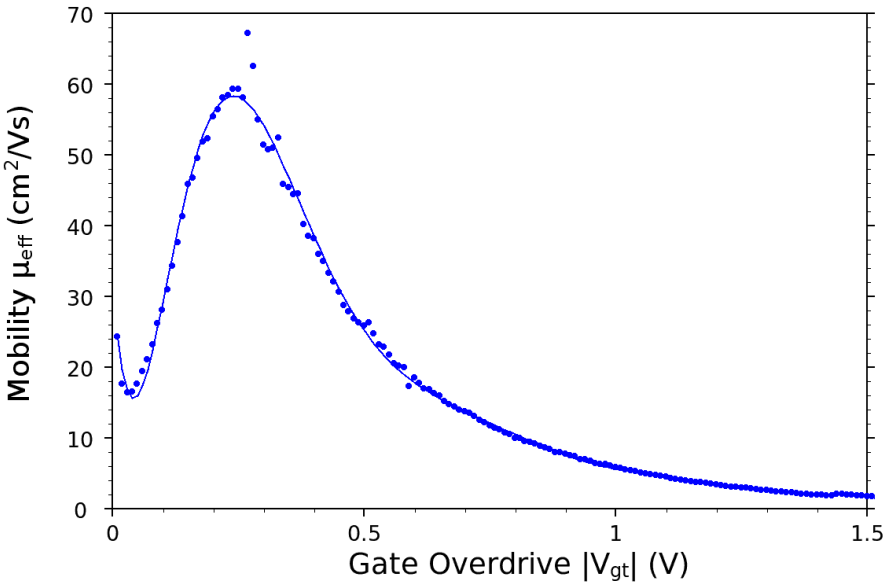

Figure 4.9: Effective mobility extracted using the constant current technique versus gate overdrive.

curve is possible. However, Fig. 3.14 in Taur and Ning [1998] shows a peak mesured effective hole mobility of about 105 cm^2/Vs at 300 K for a substrate doping concentration of $2 \cdot 10^{16}$ cm^{-3}. The peak mobility of 60 cm^2/Vs, though lower, is in reasonable agreement.

However, as evident from Fig. 4.8, the lack of devices of different gate lengths is the achilles heel of the method. The large gap between 85 nm and 1 μm gives too much weight to the 1 μm device. Therefore, this should be viewed as a proof of concept measurement rather than an accurate mobility measurement.

4.4 Current-Voltage Characteristics

4.4.1 Transfer Characteristics

Transfer characteristics of a typical 85 nm gate length SB-MOSFET on wafer SB-MOS2 #19 (half dose channel implant, 500 °C silicide anneal) are shown in Fig. 4.10

for drain biases from 0.2 to 1.4 V in 0.2 V steps. The typical SB-MOSFET current-voltage shape, observable on logarithmic plots, is maintained for all drain voltages and the extent of each of the four regimes outlined in the discussion of carrier transport in SB-MOSFETs in section 2.4.3 is heavily dependent on applied drain voltage.

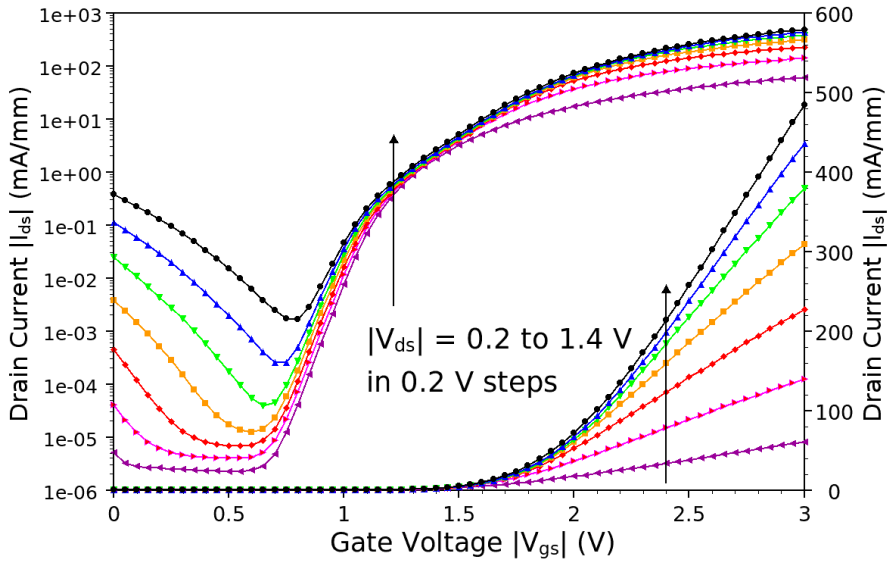

Figure 4.10: Transfer characteristics for drain biases from 0.2 to 1.4 V for a typical 85 nm SB-MOSFET on wafer SBMOS2 #19.

Reverse leakage is highly dependent on drain bias, as evident from the increase of several orders of magnitude of the OFF current below $|V_{gs}| = 0.7$ V in Fig. 4.10. While for $|V_{ds}| = 0.2$ to 0.4 V reverse leakage is negligible, it becomes more and more pronounced as the drain bias is increased. As well as that, the onset of reverse leakage moves to higher gate voltages with increasing drain voltage, indicated by the shifting of the drain current minimum to higher gate voltages. This is due to the higher drain bias raising the quasi-Fermi level in the drain above the channel conduction band and inducing field emission of electrons from drain into the channel at a higher gate voltage. At the highest drain voltages, reverse leakage severely degrades the subthreshold regime and the OFF state, making it hard for the device to fully turn off.

For low drain voltages up to 0.8 V, reverse leakage has negligible impact on the subthreshold regime between $|V_{gs}| = 0.7$ and 1.2 V. However, with increasing drain bias, the lower extent of the subthreshold regime is curtailed by the onset of reverse leakage. With increasing $|V_{ds}|$, reverse leakage of electrons becomes prominent and masks the lower portion of the subthreshold slope. The subthreshold regime is characterised by a steep slope, a consequence of thermionic emission dominating carrier transport. The straight line appearance on a logarithmic scale is evidence of the exponential dependence of thermionic emission on gate voltage, as predicted by eqn. 2.10.

Above $|V_{gs}| = 1.2$ V, a change in slope on the logarithmic plots is observable and indicates the shift from thermionic to thermionic-field emission as the dominant current contribution. Thermionic emission reaches its maximum contribution once the conduction band is raised above the peak of the Schottky barrier and any further increase is a result of Schottky barrier lowering mechanisms decreasing the effective barrier height. The second slope is due to thermionic-field emission dominating the drain current and its increase with gate voltage is seen to be smaller than in the subthreshold regime. Like thermionic emission, thermionic-field emission is exponentially dependent on gate voltage, giving rise to the straight line appearance on a logarithmic scale.

The extent of the thermionic-field emission regime depends on the drain voltage. At the lowest drain bias of 0.2 V, it is very small and the drain current transitions from domination by thermionic emission to saturation without a significant thermionic-field emission regime. The low horizontal electric field keeps thermionic-field emission at the source low, limiting the device to small drain currents.

With increasing drain bias, the horizontal electric field increases, thereby causing carriers to drift to the drain at higher velocities and inducing larger tunneling currents at the source-to-channel interface. Thermionic-field emission then dominates the drain current over a wider range of gate voltages, as evident by the greater extent of the

second straight line portion of the logarithmic transfer characteristic. At the highest drain bias of 1.4 V, the thermionic-field emission regime extends to a gate voltage of about 1.8 V.

At gate voltages in excess of 1.8 V, the drain current deviates from the straight line on the logarithmic scale, indicating that thermionic-field emission is no longer the dominant current contribution. The large gate voltage raises the valence band at the source end of the channel above the Fermi level in the source, causing the thermionic-field emission current contribution to saturate at its maximum contribution and enabling field emission to contribute. Further current increases are due to field emission, with higher drain voltages inducing larger currents by increasing the horizontal electric field.

Bias conditions of $|V_{gs}| = 2.8$ V and $|V_{ds}| = 1.4$ V are considered the ON state of the device to account for the n-poly gate and the oxide thickness. Doing so gives an ON current I_{ON} of 394 mA/mm for the device shown in Fig. 4.10 and an average I_{ON} of 413 mA/mm $\pm$ 16% for 85 nm gate length devices on SBMOS2 # 19, with a maximum drive current of 524 mA/mm. Taking $|V_{gs}| = 0.9$ V as the OFF state gives an OFF current of $6.9 \cdot 10^{-3}$ mA/mm for the device of Fig. 4.10 and an average I_{OFF} of $7.5 \cdot 10^{-3}$ mA/mm $\pm$ 30% on SBMOS2 #19. This gives an I_{ON}/I_{OFF} ratio of $5.7 \cdot 10^4$ with an average of $3.4 \cdot 10^4$ across SBMOS2 #19.

These performance indicators satisfy recommendations by the International Technology Roadmap for Semiconductors [2000 Update] for high performance logic applications of 85 nm printed gate length devices. The requirements are an ON current of 350 mA/mm, OFF current of $10 \cdot 10^{-3}$ mA/mm and an I_{ON}/I_{OFF} ratio of $3.5 \cdot 10^4$.

The performance of these p-channel SB-MOSFET devices compares well to high-performance literature p-channel DSD MOSFETs of gate lengths between 40 and 100 nm, which exhibit ON currents between 303 and 490 mA/mm [Barlage et al., 2001,

Chatterjee et al., 2004, Huang et al., 1999, Lee et al., 1992, Mistry et al., 2000, Taur et al., 1993, Yu et al., 1999] and exceeds drive currents of 176 to 425 mA/mm reported on 20 to 50 nm gate length p-channel SB-MOSFETs in literature [Ikeda et al., 2002, Kudzierski et al., 2000a, Larrieu and Dubois, 2005, Saitoh et al., 1999].

4.4.2 Threshold Voltage and DIBL

Using the constant-current threshold voltage technique with a threshold current I_{th} of 20 nA, as discussed in section 3.1.3, returns a threshold voltage of 1.22 V and a DIBL of 76 mV/V for the SB-MOSFET shown in Fig. 4.10.

An average theshold voltage V_t of 1.19 V $\pm$ 1.6% and an average DIBL of 75 mV/V $\pm$ 24% are observed for all measured devices across wafer SBMOS2 #19. The latter represents a reasonable value for MOSFET operation, albeit with a large spread. Taking into consideration the n-type gate and corresponding 1.1 V shift of all gate voltages, the measured threshold voltage effectively constitutes an average threshold of 0.09 V.

The low threshold may be an indication of trapped charges in the oxide and/or at the oxide interface. The gate oxide is very leaky, which would support this idea, but at the same time prevents any form of direct capacitive measurement on these devices that would allow the properties of the oxide to be established. In order to fit the threshold during simulations of SB-MOSFETs, described in chapter 6, it was necessary to introduce a large interface trap density at the channel-oxide interface in order to obtain a good simulation fit. This can be seen as a loose confirmation of the presence of oxide and interface charge.

4.4.3 Subthreshold Slope

SB-MOSFETs on wafer SBMOS2 #19 exhibit an average low drain voltage (0.1 V) subthreshold slope of 87 $\pm$ 8% mV/dec. This represents an acceptable value for

MOSFET operation. A typical behaviour of SB-MOSFET subthreshold slope with drain bias is shown in Fig. 4.11.

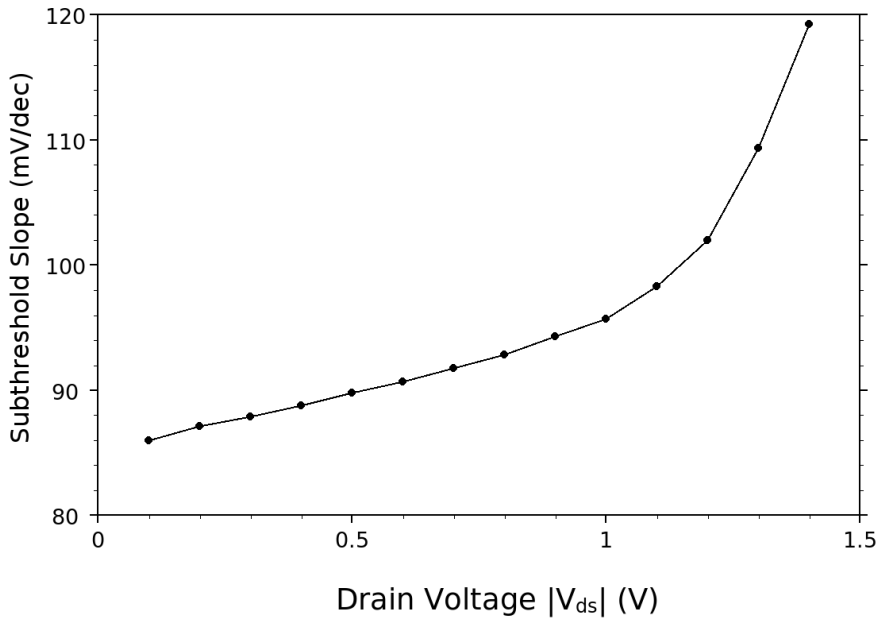

Figure 4.11: Measured inverse subthreshold slopes as a funcion of drain voltage $|V_{ds}|$ for a typical device on wafer SBMOS2 #19.

A linear increase in subthreshold slope from 86 mV/dec at $|V_{ds}| = 0.1$ V to 96 mV/dec at $|V_{ds}| = 1.0$ V is observed. Above $|V_{ds}| = 1.0$ V, a large, exponential-like increase in subthreshold slope occurs, which is attributable to the onset of reverse leakage severely degrading the subthreshold characteristics, as evident by inspection of the subthreshold regime at high drain voltage in Fig. 4.10.

4.4.4 Transconductance

The transconductance curves corresponding to transfer characteristics of Fig. 4.10 are depicted in Fig. 4.12. The peak saturation transconductance for this device is 471 mS/mm with the SBMOS2 #19 wafer average being 473 mS/mm $\pm$ 15%, which is comparable to conventional DSD devices of similar gate lengths [Barlage et al., 2001,

Burghartz et al., 2000, Lee et al., 1992, Taur et al., 1992, 1993].

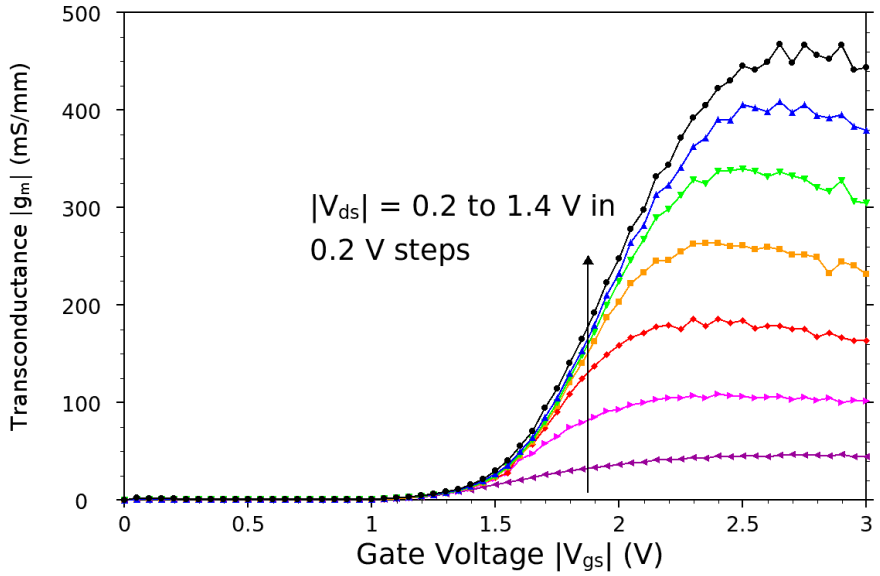

Figure 4.12: Transconductance curves for drain biases from 0.2 to 1.4 V for a typical 85 nm SB-MOSFET on SBMOS2 #19. No clear transconductance peak is observed.

The most important difference in shape to conventional doped source/drain devices is the absence of a clear peak in the transconductance-gate voltage relationship. Mobility degradation due to surface roughness scattering at the oxide-channel interface under high vertical effective fields causes the transconductance of DSD MOSFETs to exhibit a fall-off about 0.5 V above threshold [Taur and Ning, 1998]. By inspection of Fig. 4.12, it is evident that this fall-off does not occur in these SB-MOSFET devices. Instead, the transconductance continually increases up to $|V_{gs}| = 2.5$ V and shows very little decrease beyond 2.5 V. The transconductance peak, if present at all, is very broad and resides at a very high gate overdrive.

The absence of transconductance fall-off may be explained by the carrier injection mechanisms at the source-to-channel interface dominating the drain current rather than drift and diffusion in the channel. The gate voltage modifies the channel potential, which

in turn controls the amount of carriers injected into the channel from the source and lowers the effective Schottky barrier height of the contact. Thus, for gate voltages at which a DSD MOSFET experiences mobility degradation in the channel and associated current saturation, the increasing gate voltage in a SB-MOSFET leads to a continual increase of injected carriers and, consequently, the total drain current. The carrier injection begins to saturate at a higher gate voltage, as can be inferred by the leveling off of the transconductance above $|V_{gs}| = 2.5$ V. This behaviour is unique to SB-MOSFETs at short channel lengths in which the drain current is dominated by the current injection at the source-to-channel Schottky barrier.

4.4.5 Output Characteristics

A set of output characteristics of a typical device on wafer SBMOS2 #19 is shown in Fig. 4.13. Non-saturation of drain current at high drain voltages is observed, which can be attributed to the emission of hot carriers from the source into the channel and the short channel length. The processes of emitting carriers from the metal source over or through the Schottky barrier via thermionic or field emission are both very energetic. Carriers entering the channel can therefore loosely be described as *hot holes* [Rhoderick and Williams, 1988], since the energy that they acquire is well above that of holes present in the channel at equilibrium. Injected holes lose this energy via collisions in the channel until they come to rest at thermal equilibrium. At high gate voltages, the horizontal electric field will accelerate injected carriers towards the drain and they may therefore not lose all their additional energy before exiting the channel via the drain electrode, resulting in the non-saturation of the drain current with drain voltage.

A second notable feature of these curves is the sublinear increase in drain current with drain voltage for small drain voltages up to 0.2 V. This so-called *sublinear effect* is typical for SB-MOSFET devices and results from the presence of the second Schottky barrier between channel and drain [Winstead and Ravaioli, 2000].

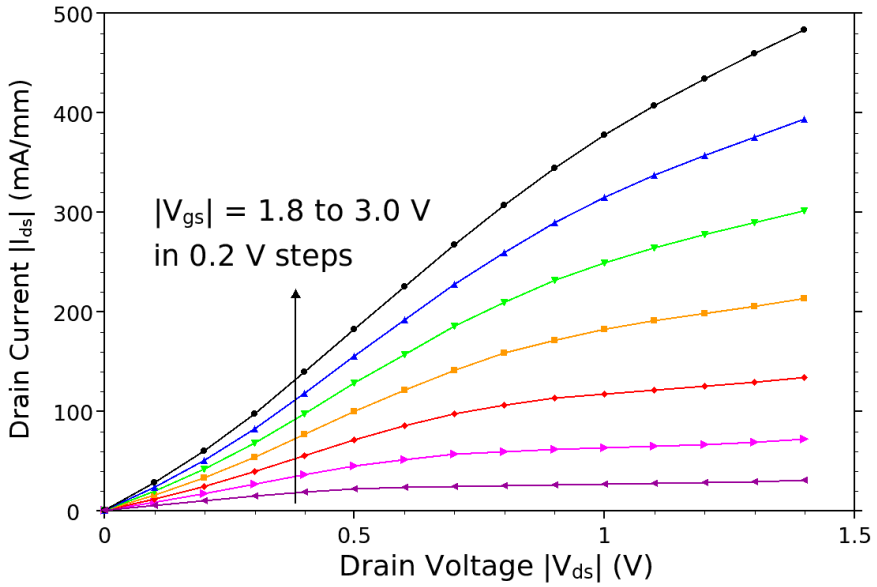

Figure 4.13: Output characteristics of a typical 85 nm gate length device on wafer SBMOS2 #19 for gate voltages from 1.8 to 3.0 V. A sublinear drain current increase with drain voltage is observed at small drain biases.

The band diagram of a SB-MOSFET for very small $|V_{ds}|$ is depicted in Fig. 4.14 to illustrate the cause of this effect. Under these conditions, the channel-to-drain Schottky barrier is slightly reverse biased. Holes travelling from source to drain must first traverse the source-to-channel Schottky barrier, then drift along the channel before having to surmount the second Schottky barrier between channel and drain. This second reverse biased barrier manifests itself as an additional resistance, reducing the drain current and causing a *sublinear* drain current increase with drain voltage [Winstead and Ravaioli, 2000].

As the drain bias is increased, the quasi-Fermi level in the metal drain is raised and the drain-to-channel barrier is continually reduced. Once the drain voltage is of the order of the zero-bias Schottky barrier height (0.2 to 0.3 V), the barrier completely diappears and the channel-to-drain junction becomes forward biased, allowing carriers in the channel to exit via the drain unhindered. The drain current is then source junction limited and

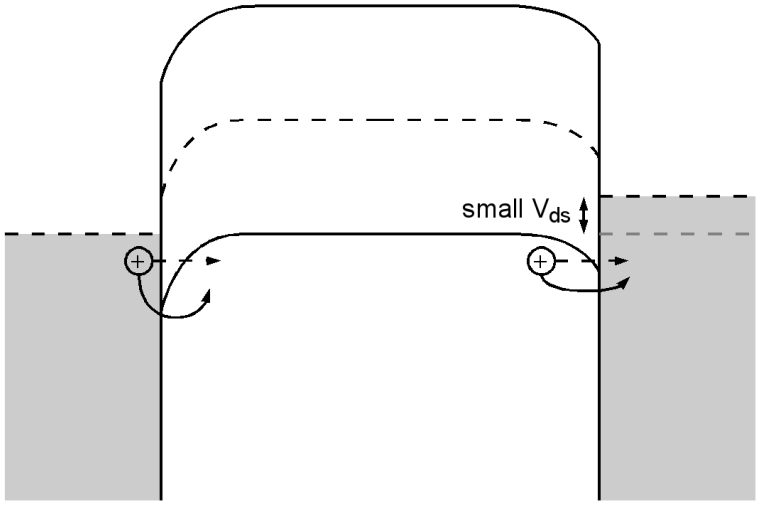

Figure 4.14: Band diagram illustrating the origin of the sublinear effect in SB-MOSFET output characteristics. The second Schottky barrier between channel and drain at low drain voltages hinders carriers exiting the channel.

increases linearly with drain bias, as for a conventional MOSFET.

4.5 Source/Drain Silicide Anneal Temperature

The average transfer characteristics for SB-MOSFET devices on wafers SBMOS2 #18 and #19, undergoing source/drain silicide anneals of 550 and 500 °C, respectively, are compared in Fig. 4.15 for low and in Fig. 4.16 for high drain voltage. All other processing parameters, specifically the channel implant dose, are identical for the two wafers (both are half dose). The lower silicide anneal temperature consistently produces higher drain currents, explainable by the lower effective Schottky barrier height extracted in section 4.2 for the lower silicide anneal temperature.

The increase in effective barrier height from 117 to 128 meV for silicide anneals of 500 and 550 °C measured in section 4.2 corresponds to a predicted 1.53-fold increase in thermionic emission current from source to channel. At $|V_{gs}| = 1.2$ V, where thermionic emission is expected to be the dominant current contribution, the drain currents in

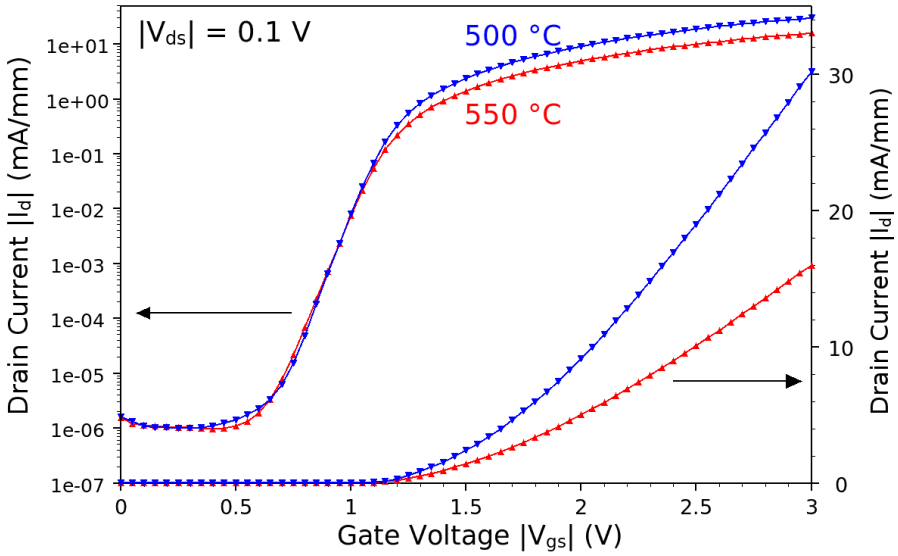

Figure 4.15: Low drain bias transfer characteristics for SB-MOSFET devices with source/drain silicide anneal temperatures of 500 and 550 °C. Lower temperature anneals result in higher drive currents.

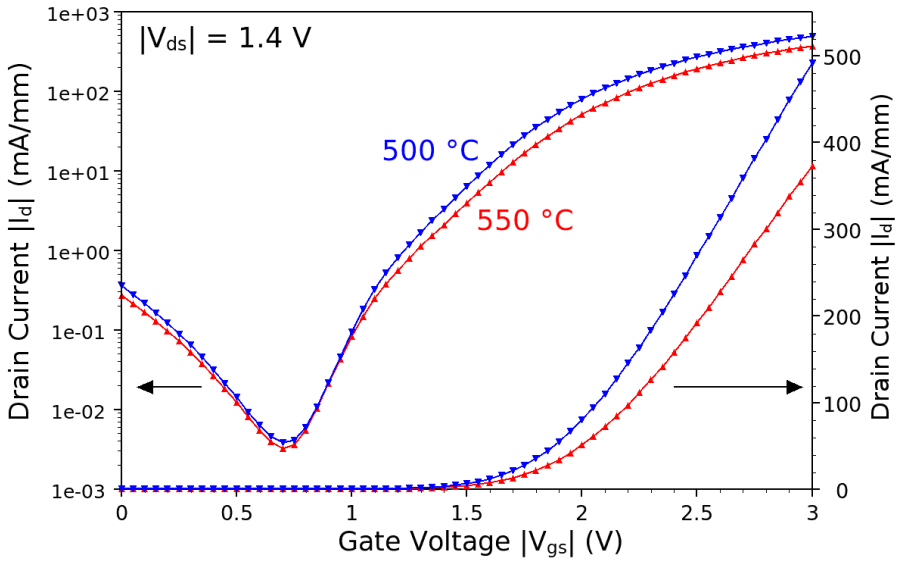

Figure 4.16: Saturation transfer characteristics for SB-MOSFET devices with source/drain silicide anneal temperatures of 500 or 550 °C.

Fig. 4.15 and Fig. 4.16 exhibit ratios of 1.50 and 1.43, respectively, which is in good agreement with the prediction made by the extracted barrier heights of section 4.2.

In saturation, where field emission dominates carrier transport, the two wafers SBMOS2 #18 and #19 exhibit average ON currents of 305 mA/mm $\pm$ 15% and 413 mA/mm $\pm$ 16%, average OFF currents of 4.1 $\cdot$ 10^{-3} mA/mm $\pm$ 29% and 7.5 $\cdot$ 10^{-3} mA/mm $\pm$ 30%, respectively. Average I_{ON}/I_{OFF} ratios are 2.4 $\cdot$ 10^4 and 3.4 $\cdot$ 10^4, respectively. The change in Schottky barrier height between the two wafers has a minor impact on the threshold voltage - 1.21 V $\pm$ 1.7% on SBMOS2 #18 versus 1.19 V $\pm$ 1.6% on #19 and DIBL is similar as well - 79 mV/V $\pm$ 21% and 75 mV/V $\pm$ 24%, respectively.

The transconductances for wafers annealed at 500 and 550 °C are compared in Fig. 4.17 and 4.18 for low and high drain bias, respectively. The large difference in transconductance - 375 mS/mm $\pm$ 11% and 473 mS/mm $\pm$ 15% - is attributable to differences in source-to-channel Schottky barrier height, corresponding with observations made previously on the transfer characteristics.

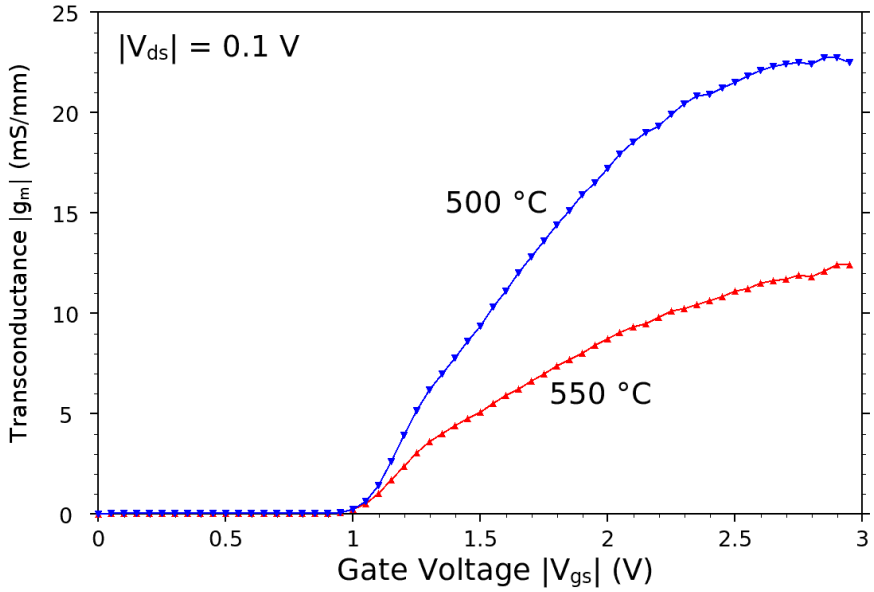

Figure 4.17: Transconductance curves for wafers annealed at 500 and 550 °C at a $|V_{ds}|$ of 0.1 V. The former exhibits substantially higher transconductance, explained by lower Schottky barrier height. No transconductance fall-off with gate voltage is observed.

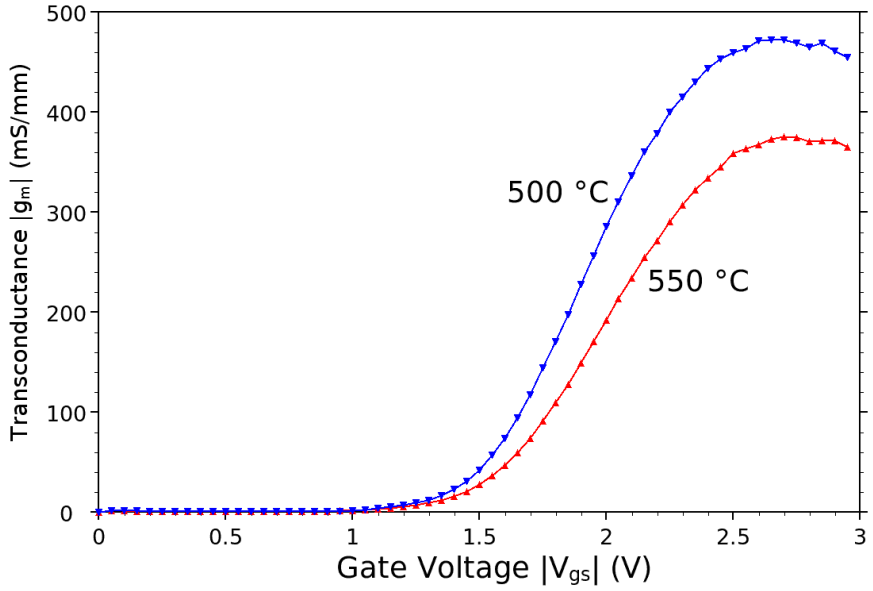

Figure 4.18: Saturation transconductance curves for wafers annealed at 500 and 550 °C at $|V_{ds}| = 1.4$ V. The former exhibits substantially higher transconductance, explained by lower Schottky barrier height. No significant transconductance fall-off with gate voltage is observed.

4.6 Channel Doping

Average transfer characteristics for wafers SBMOS2 # 17 and #19 are compared for low and high drain bias in Fig. 4.19 and Fig. 4.20, respectively. The sole difference in fabrication between the two wafers is the channel implant dose. SBMOS2 #17 received a *full dose* channel ion implantation of As at a dose of $1 \cdot 10^{13}$ cm^{-2}, while SBMOS2 #19 received a *half dose* implant at $5 \cdot 10^{12}$ cm^{-2}. Both wafers underwent source/drain silicide anneals at 500 °C, while all other processing parameters are identical.

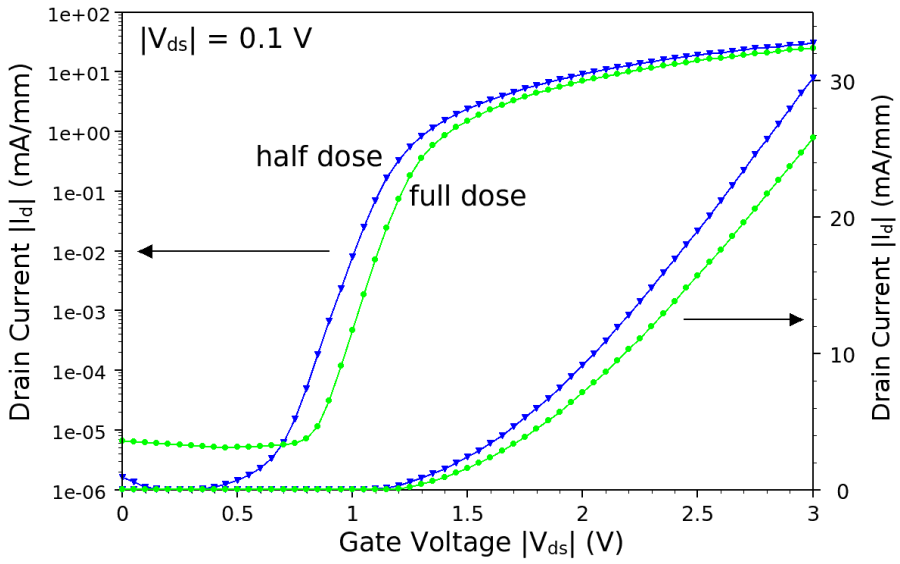

Figure 4.19: Transfer characteristics of devices with half- and full-dose channel implants under low drain bias of 0.1 V. The former exhibits consistently higher drive currents.

Average ON currents are 338 mA/mm ± 1.5% and 413 mA/mm ± 16% with peak transconductances of 423 mS/mm ± 1.4% and 473 mS/mm ± 15% for devices with full- and half-dose channel implants, respectively. While the lower channel doping concentration provides improved performance in terms of both drain current and transconductance, devices with higher channel doping density exhibit better uniformity, evident by the very small spread in saturation drive currents and transconductances.

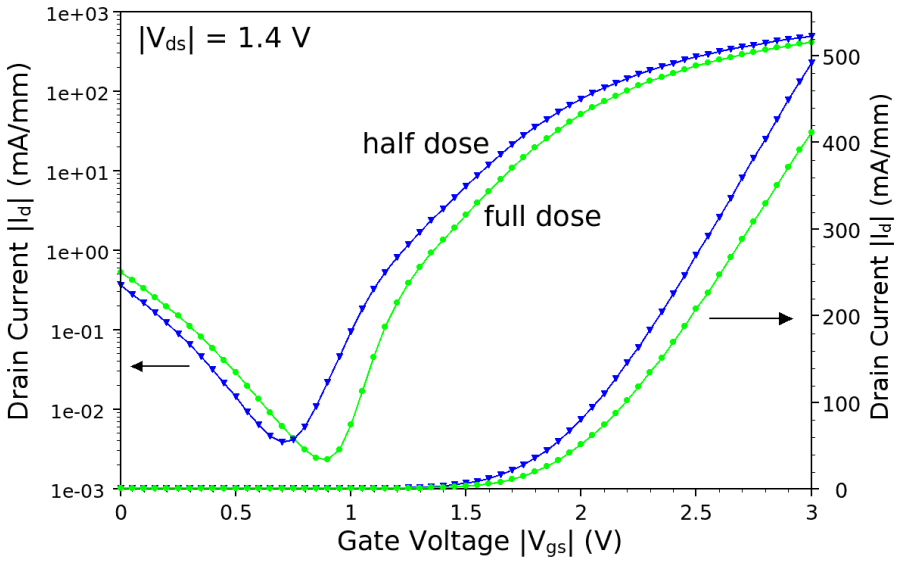

Figure 4.20: Transfer characteristics of SB-MOSFETs with half- and full-dose channel implants under high drain bias of 1.4 V.

Taking $|V_{gs}| = 1.0$ V as the OFF state for devices on SBMOS2 #17 to account for the threshold voltage shift as a result of the increased channel doping gives an average OFF current of $6.3 \cdot 10^{-3}$ mA/mm $\pm$ 11%, which is slightly lower than the value obtained on SBMOS2 #19. The average I_{ON}/I_{OFF} ratio on SBMOS2 #17 is $4.8 \cdot 10^4$.

The average threshold voltage of 1.26 $\pm$ 0.7% V for 85 nm devices on SBMOS2 #17 is 70 mV higher than for SBMOS2 #19. This shift is attributable to the higher channel implant which, according to implant simulations, should result in twice the surface doping concentration.

The average DIBL of 48 $\pm$ 16% mV/dec for the characterised wafers on SBMOS2 #17 is substantially lower than for devices on wafer SBMOS2 #19 of 75 mV/V $\pm$ 24%.

4.7 Temperature

Analysis of SB-MOSFET drain currents at low temperatures gives an insight into the relative contributions of the individual carrier transport mechanisms - thermionic, thermionic-field and field emission - to the total drain current. While the former two are heavily dependent on temperature, the latter is virtually independent of temperature and will increasingly dominate the total current as the ambient temperature is decreased.

Transfer characteristics at temperatures of 80, 100, 150, 200, 250 and 290 K for a SB-MOSFET on wafer SBMOS2 #19 (source/drain anneal temperature of 500 °C and half dose channel implant) at drain voltages $|V_{ds}|$ of 0.1 and 1.4 V are shown in Fig. 4.21 and 4.22, respectively. As expected, in both cases, there is significant variation in drain currents with ambient temperature, yet the extent to which this occurs is highly dependent on gate and drain voltages.

4.7.1 Low Drain Bias

The low drain voltage case of Fig. 4.21 is analysed first. Below $|V_{gs}| = 0.6$ V. measurement equipment limitations prevent accurate acquisition of currents (measured current magnitudes of ∼100 fA), indicating that the drain voltage is too small to induce a significant reverse leakage current, i.e. no tunneling of electrons from the drain into the channel is possible since the quasi-Fermi level in the drain remains below the conduction band in the channel.

Between $|V_{gs}| = 0.6$ and 1.7 V, thermionic emission dominates carrier transport and this is evident by a significant shift of the subthreshold regime towards higher gate voltages as thermionic emission is reduced with decreasing temperature.

Interestingly, the drain current for high gate voltages is still dependent on temperature, with drain currents at $|V_{gs}| = 3.0$ V exhibiting a 2.8-fold reduction from 290 to 80 K.

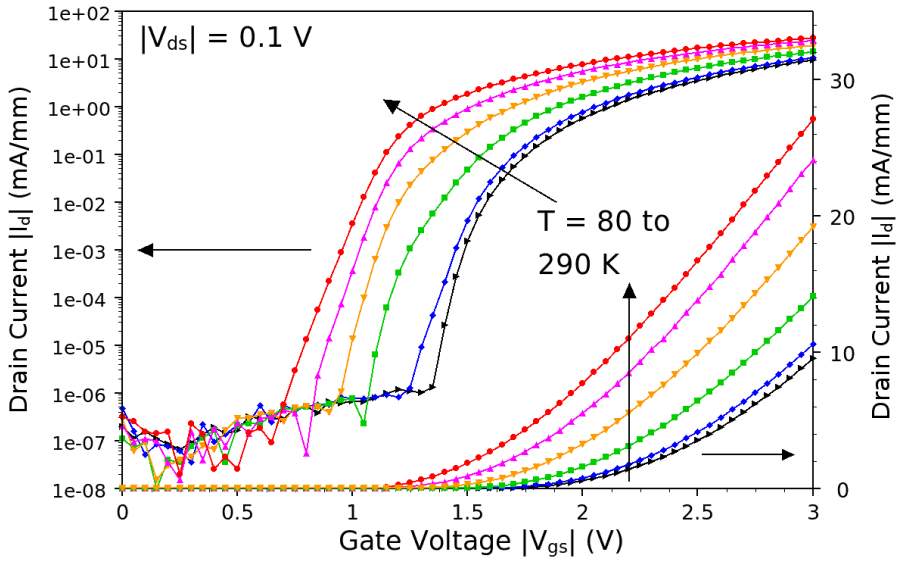

Figure 4.21: Transfer characteristics for temperatures from 80 to 290 K at $|V_{ds}| = 0.1$ V of a device on SBMOS2 #19.

Since it is generally assumed that tunneling dominates the drain current at high gate voltages, this inidicates that thermionic and thermionic-field emission provide significant contributions to carrier transport in the ON state at this very low drain bias.

This may be due to the fact that at $|V_{ds}| = 0.1$ V, the channel-to-drain Schottky barrier is reverse biased and the holes travelling from source to drain must surmount two reverse biased Schottky barriers en route, first the source-to-channel, then the channel-to-drain junctions, as described in section 4.4.5 for the sublinear effect of output characteristics. The current under these conditions is then dominated by thermionic and thermionic-field emission over both of the barriers and would explain the temperature dependence of the drain current.

For $|V_{ds}|$ of 0.3 V and higher, the channel-to-drain junction becomes forward biased and the dependence of ON current on ambient temperature diminishes. The measured ON currents are then largely independent of temperature with drain current ratios at

$|V_{gs}|$ = 3.0 V of 1.3 or less with increasing drain voltage.

4.7.2 High Drain Bias

The situation for high drain bias, depicted in Fig. 4.22, is somewhat different. Most noticably, the reverse leakage currents present below $|V_{gs}|$ = 1.0 V are large at all temperatures. Their small dependence on ambient temperature indicates these currents to be dominated by field-emission with a relatively small contribution from thermionic-field emission processes. This is evidence for the description of reverse leakage currents presented in section 2.4.3.

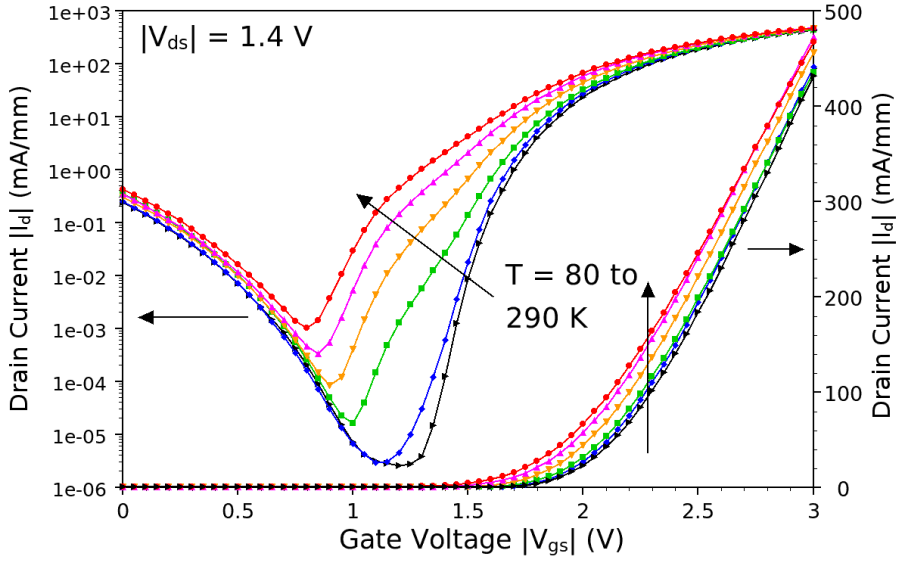

Figure 4.22: Transfer characteristics for temperatures from 80 to 290 K at $|V_{ds}|$ = 1.4 V of a device on wafer SBMOS2 #19.

At all but the lowest two temperatures, the drain current between $|V_{gs}|$ = 0.8 and 1.2 V is dominated by thermionic emission, indicated by reduction in subthreshold current with temperature of almost 5 orders or magnitude. The shape of the transfer characteristics for T = 80 and 100 K, devoid of the typical tri-slope SB-MOSFET characteristic, indicate that operation at these temperature based purely field emission processes over

the whole range of gate voltages. The very low temperature *freezes out* any thermionic or thermionic-field emission processes.

Above $|V_{gs}| = 1.2$ V, the drain current is dominated by a combination of thermionic-field and field emission processes. The exact composition of the two is hard, if not impossible, to determine quantitavely. However, qualitatively, thermionic-field emission begins to dominate the drain current once thermionic emission has reached its maximum contribution, which occurs around the threshold voltage of about 1.2 V for these devices.

From then on, with increasing gate voltage, thermionic-field and then field emission processes at the source-to-channel Schottky barrier represent the dominant current contributions, with the transition between the two being gradual. This is evident by the gradual convergence of the transfer characteristics for different temperatures with gate voltage in Fig. 4.22. Whereas the tranfer characteristic for 290 K contains large thermionic-field emission contributions, the curve for 80 K can be assumed to be a pure field emission characteristic, since the typical tri-slope shape of the curve is no longer present. This observation is consistent with work by Lepselter and Sze [1968], in which SB-MOSFET operation at 77 K is shown to be dominated by tunneling.

At $|V_{gs}| = 3.0$ V, the saturation current ratio of 290 over 80 K is less than 1.1, indicating that the ON current is virtually independent of temperature and therefore due to pure field emission. In fact, the saturation current ratio of less than 1.1 remains down to drain voltages of 0.6 V.

The decrease of saturation drain current with decreasing ambient temperature is indication of it being limited by the source-to-channel Schottky barrier rather than transport in the channel, as presented by Snyder et al. [1995] and Wang et al. [1999]. Carrier mobility in silicon increases with decreasing temperature because of reduced phonon scattering [Taur and Ning, 1998], so a MOSFET with channel-limited current

experiences an increase in drain current with decreasing temperature. However, the decrease in $|I_d|$ of up to 10% from 290 to 80 K observed on these SB-MOSFETs shows that the drain current in saturation is dominated by field emission at the source-to-channel barrier with minor contributions by thermionic and thermionic-field emission.

Chapter 5

RF Characterisation of SB-MOSFETs

5.1 Introduction

Previous RF characterisation, published by Fritze et al. [2004] on very similar SB-MOSFET devices to the ones presented in this work, had determined their RF performance to be 2 - 3 times that of comparable doped source/drain devices, with unity-gain cutoff frequency (f_T) values of up to 280 GHz for 25 nm channel length devices. However, a high drain bias of -2.5 V had been applied during the measurements presented by Fritze et al. [2004], which is twice the ITRS recommendation for high performance logic applications of such gate lengths [International Technology Roadmap for Semiconductors, 2003 Edition] and no in-depth discussion of possible reasons for this performance enhancement were given.

To address this, a more extensive investigation into the RF performance of SB-MOSFET devices at ITRS-based bias conditions was performed in collaboration with the Microwave Laboratory at the Université Catholique de Louvain (UCL), Belgium. Microwave measurements from 45 MHz to 110 GHz were performed on devices on two

wafers, SBMOS2 #18 and #19, both having half dose channel implants and receiving silicide anneals at temperatures of 550 and 500 °C, respectively. The experimental results and conclusions obtained during the collaborative work are presented in this chapter.

5.2 Sample Description

The structural dimensions, such as gate length, oxide thickness and channel doping, of the devices investigated at microwave frequencies are identical to those of the devices presented in section 4.1 of the previous chapter for DC characterisation. SB-MOSFETs consisting of two such 2 μm wide, parallel gate fingers are embedded in coplanar waveguide (CPW) transmission lines for on-wafer microwave measurements, as shown in Fig. 5.1 and 5.2. The resulting total device width is 4 μm and the theoretical oxide capacitance C_{OX} is 6.4 fF.

RF measurements from 45 MHz to 110 GHz are performed using an Agilent 8510XF network analyzer in conjunction with a Cascade probe station with ground-signal-ground (GSG) RF probe tips. Bias conditions are selected based on recommendations for high performance logic applications in the International Technology Roadmap for Semiconductors [2000 Update] and adjusted for the n-poly gate and 1.8 nm thick gate oxide present in the devices. A $|V_{gs}|$ of 2.8 V is considered the ON state to achieve the same oxide field as present in a device with a T_{ox} of 1.5 nm at a gate bias of 1.4 V and a drain voltage of 1.4 V is applied to complete the saturation bias condition. All active device measurements are performed under these saturation biases.

Dedicated on-wafer OPEN, SHORT and THRU deembedding structures are present on both wafers to provide for various deembedding techniques, of which OPEN and OPEN-SHORT were used. Standard RF calibration procedures on alumina substrates were used.

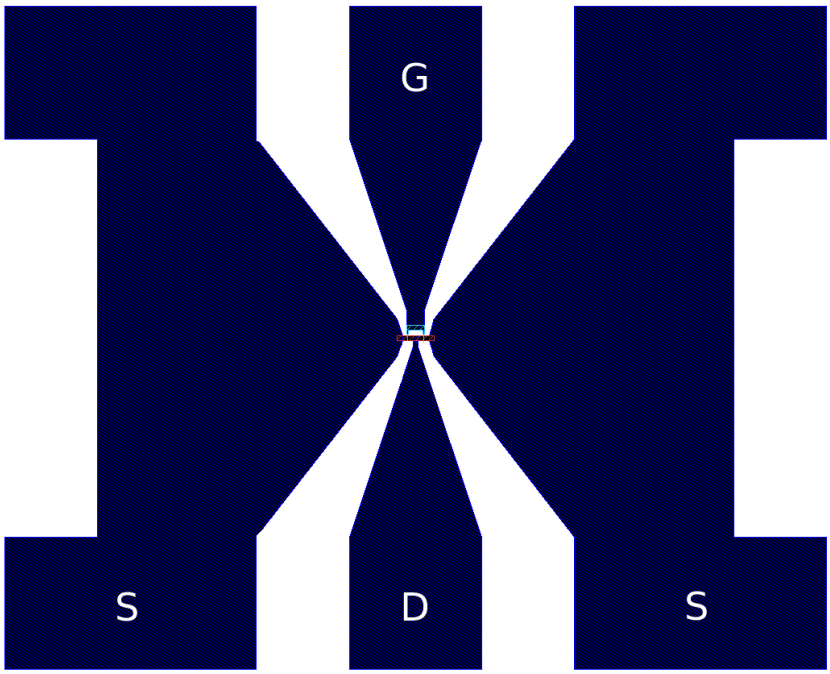

Figure 5.1: Contact geometry of the coplanar waveguide structure used for taking RF measurements. D: Drain; G: Gate; S: Source.

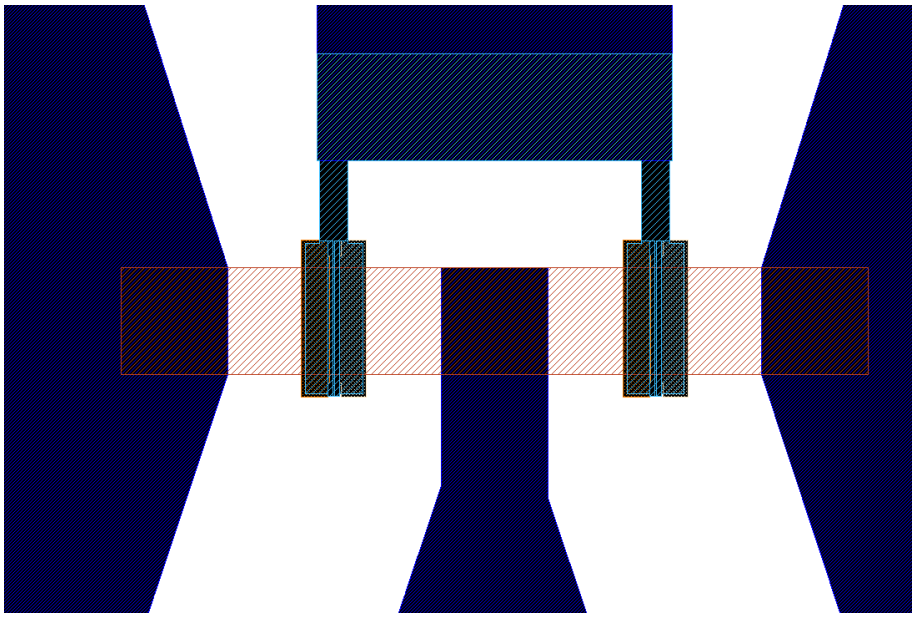

Figure 5.2: SB-MOSFET device structure consisting of two parallel gate fingers embedded at the centre of the CPW in Fig. 5.1.

Two wafers, SBMOS2 #18 and #19, are characterized, both having received half-dose ($5 \cdot 10^{12} cm^2$) As channel implants. The sole difference between the two wafers during fabrication are the metal source/drain silicide anneal temperatures of 550 and 500°C, respectively. DC characterisation has established a significant difference in peak transconductance between devices on these two wafers, attributed to differences in extracted Schottky barrier heights between source and channel, as presented in section 4.2. This information is vital to the analysis performed in this chapter.

Though both shorter and longer gate length devices are present on the wafers, their low yield prompted the measurement of 85 nm gate length devices only.

5.3 S-Parameter Deembedding

Initially, the classical S-parameter deembedding techniques using OPEN and OPEN-SHORT corrections were applied to extract intrinsic device characteristics from the measurement data. This involves taking radio-frequency measurements on the separate, dedicated OPEN and SHORT deembedding structures as well as the active device under test itself. Both OPEN and OPEN-SHORT deembedding techniques are applied to measured S-parameters, but very little difference between their application is observed.

5.3.1 Measurement Variability

During RF characterisation, measurement variability due to contacting was detected and investigated. The first investigation is into the variability of repeat measurements without recontacting. Five repeat measurements were taken on one OPEN structure on wafer SBMOS2 #19 and the input capacitance of the OPEN structure, $C_{in,open}$, calculated from the Y-parameters, converted from measured S-parameters. The extracted input capacitances for the five repeats are shown in Fig. 5.3. Variations of less than 0.25% are observed between measurements, indicating that once contact is established, repeat measurements are very consistent.

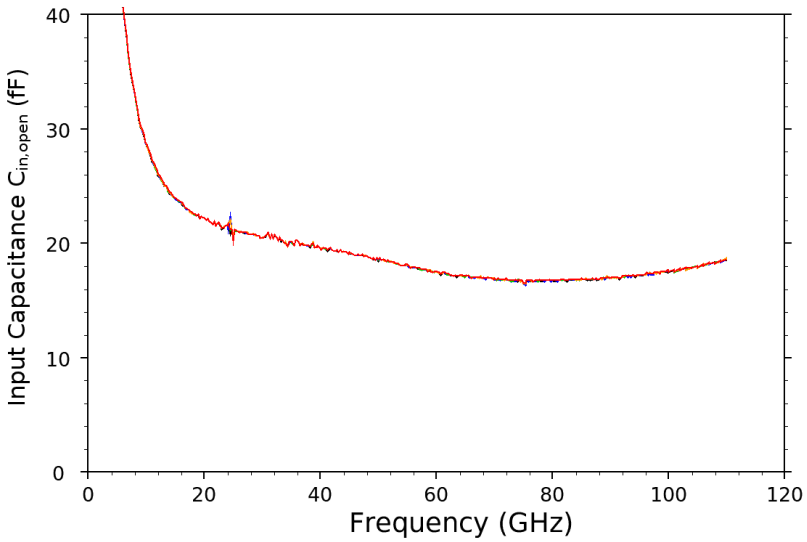

Figure 5.3: Input capacitance $C_{in,open}$ of one OPEN structure on wafer SBMOS2 #19 for five repeats without recontacting between measurements, illustrating the excellent consistency between repeat measurements.

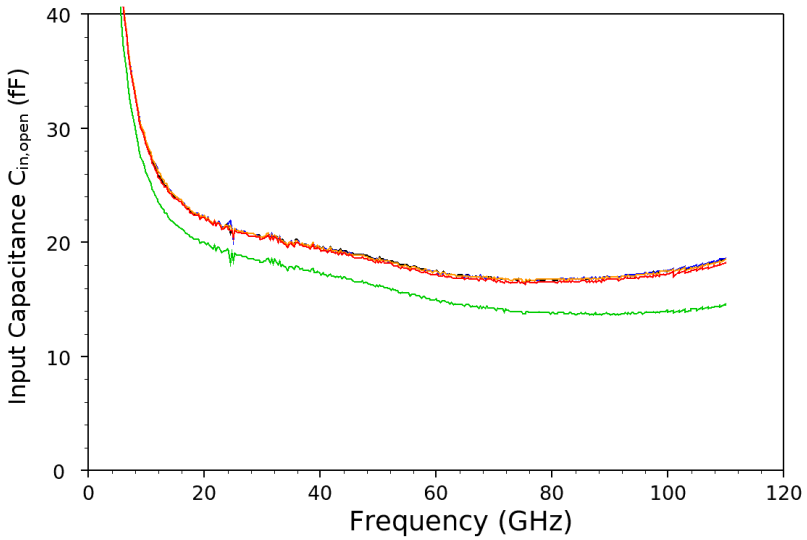

Figure 5.4: Input capacitance C_{open} of one OPEN structure on wafer SBMOS2 #19 for five repeats with recontacting between measurements, illustrating the variability observed between recontacting attempts.

Performing five repeat measurements and applying the same extraction procedure, but recontacting to the same OPEN structure between measurements, results in the input capacitances shown in Fig. 5.4. In this case, while four of the five measurements agree to within 2% and correspond well with the previous repeat measurements, one measurement - the third of the five repeats - differs by up to 25%. Since the only change between measurements is the contacting, this variation is attributed to the properties of the probe-to-pad contact.

The contact pads consist of unsintered aluminium and variations are attributable to changes in contact resistance. However, as evident in Fig. 5.4, this effect seems to be non-systematic, since only the third of five repeats exhibits significant difference.

The measurement dispersion across the entire wafer is investigated by taking single S-parameter measurements on 27 OPEN structures at various locations on wafer. The resulting input capacitances are depicted in Fig. 5.5 along with the corresponding wafer map of Fig. 5.6. A variation of up to 6 fF, or 43% of the smallest measured input capacitance, is observed. No clearly discernable trend of input capacitance variation with die location on-wafer is evident, either. This is very significant, since the expected gate capacitance of the SB-MOSFET itself is 6.4 fF, and the variations in contact properties may therefore lead to substantial inaccuracies in the extracted RF device performance.

The variations of the input capacitance across may be attributed to field oxide thickness non-uniformity across the wafer as well as the contact variability described previously.

The impact of the observed variations is enhanced by the small size of the devices. Usually, RF devices are fabricated with 50 - 100 gate fingers to increase the magnitude intrinsic device properties with respect to the access structure parasitics. Nevertheless,

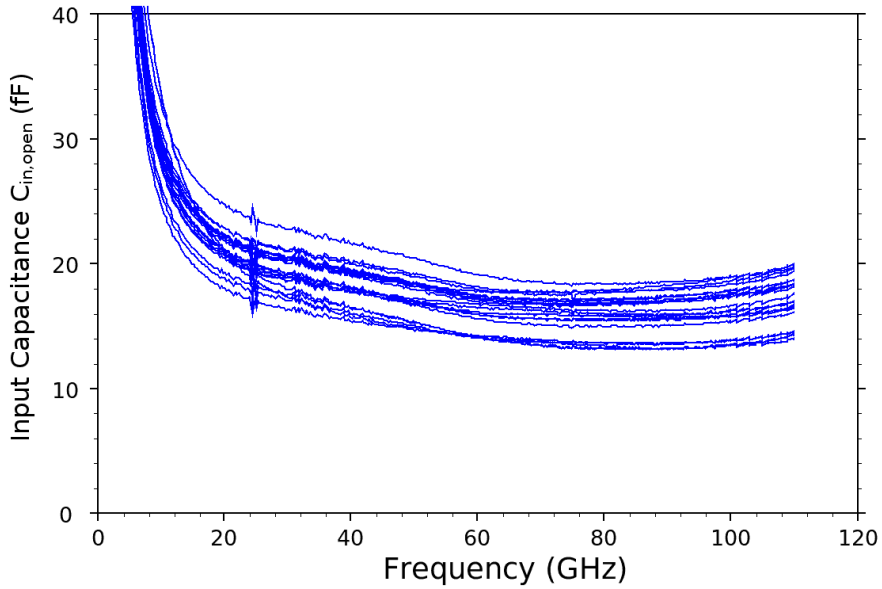

Figure 5.5: Input capacitance of 27 OPEN structures across wafer SBMOS2 #19, illustrating the large variation observed between measurements.

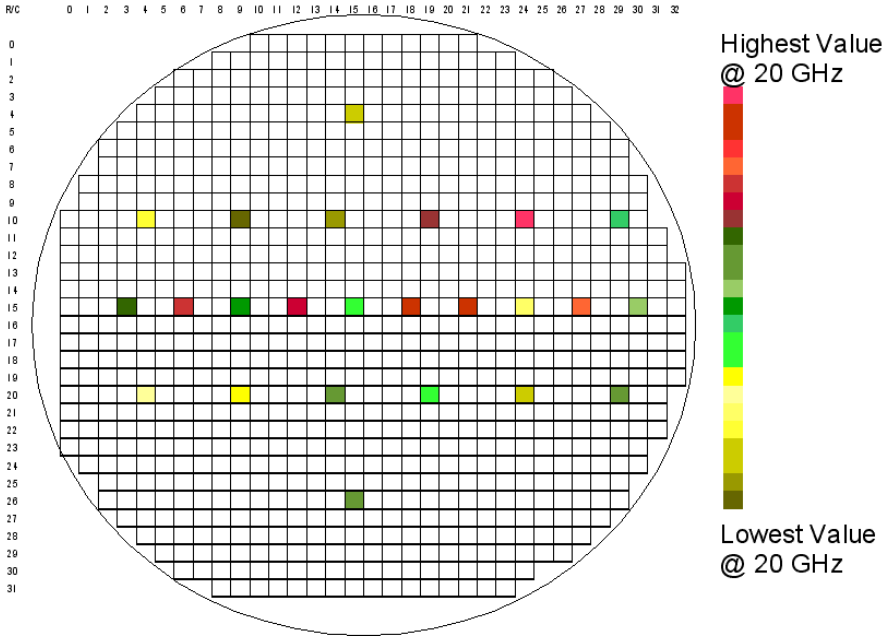

Figure 5.6: Wafer map of measured OPEN structures corresponding to Fig. 5.5. No discernable trend of input capacitance with wafer location is observable.

some of the OPEN deembedded H_{21} data may be deemed valid, when a sufficient slope of -20 dB/dec is observed, but it is just a matter of coincidence.

5.3.2 ColdFET Deembedding

Such uncertainties due to contact property variations can be avoided when using a new de-embedding technique proposed by Paillоncy and Raskin [2006], which withdraws the access pads and lines without the measurement of any dedicated RF test structure. This technique is based on the behaviour of the field effect transistors under ColdFET bias conditions, i.e. performing a frequency sweep with no applied drain bias. The technique was developed during the course of this investigation and the results presented here represent the first application thereof.

The ColdFET de-embedding technique performs active and deembedding measurements on the active device without recontacting, ensuring that parasitics related to the contact pads, in particular those of the contact between pad and probe needle, remain constant between the two measurements. This approach enables accurate S-parameter deembedding even in the presence of contact repeatability problems and access structure or oxide thickness variations. More details about this de-embedding technique can be found in section 3.4.4 and in Paillоncy and Raskin [2006].

The current-gain characteristics extracted using OPEN and ColdFET deembedding are compared for one typical device each from wafers SBMOS2 #18 and #19 in Fig. 5.7 and 5.8, respectively. In both cases, the current-gain characteristics obtained using OPEN deembedding exhibit slopes greater than -20 dB/dec, indicating that the deembedding is not removing all the access structure parasitics. Applying ColdFET deembedding produces current-gain slopes very close to -20 dB/dec in the frequency range between 20 and 60 GHz.

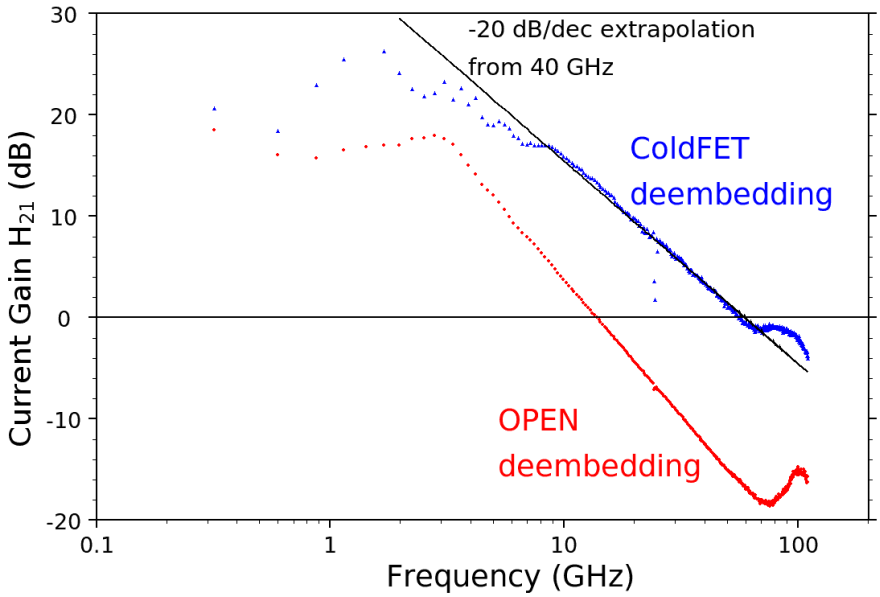

Figure 5.7: Comparison of current-gain plots obtained using OPEN and ColdFET deembedding techniques on wafer SBMOS2 #18.

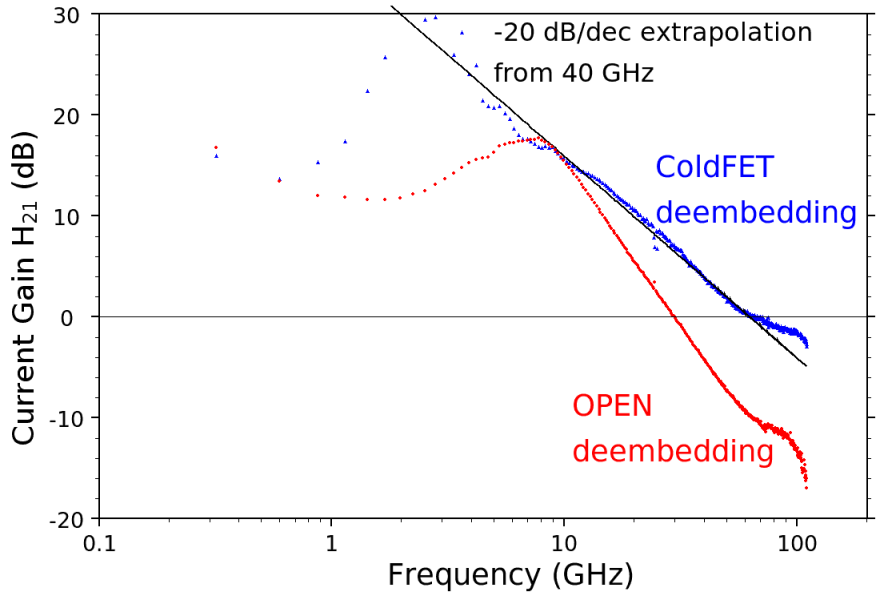

Figure 5.8: Comparison of current-gain plots obtained using OPEN and ColdFET deembedding techniques on wafer SBMOS2 #19.

The anomalous decrease in current-gain below 10 GHz is attributed to residual parasitic conductance due to the access structure that is not fully removed during the deembedding process. While the decrease is very significant for OPEN deembedding, the ColdFET technique is better at correctly removing the parasitics, evident by the better adherence to the -20 dB/dec slope.

The anomalous increase in current-gain above 60 GHz on all plots, loosely describable as a *hump*, is attributable to residual capacitance that is not fully removed by the deembedding processes. Both OPEN and ColdFET deembedding techniques do not fully remove these, and data above 60 GHz is discarded for the extraction of the unity-gain cutoff frequency f_T. The presence of both these anomalies is attributable to the relatively small device geometry compared to the access structure.

The unity-gain cutoff frequency is defined as the point at which the current gain H_{21} becomes unity and the transistor no longer functions as an amplifier [Agilent, Raskin, 1997]. A commonly used method for determining f_T is to extrapolate the measured current gain at 40 GHz at a slope of -20 dB/dec. This convention is adopted in this work and results in extrapolations that agree very well with the measured current gain in the frequency range of 10 to 60 GHz for all measurements, as illustrated by the extrapolations in Fig. 5.7 and 5.8.

Applying this method for determining f_T results in cutoff frequencies of 59 and 62 GHz for the devices depicted in Fig. 5.7 and 5.8, respectively. The average f_T for measured devices on SBMOS2 #18 is 64.4 GHz $\pm$ 6% and 64.5 GHz $\pm$ 8% on SBMOS2 #19.

5.4 Silicide Anneal Temperature

Figure 5.9 compares the current gain characteristics of the two best performing devices on wafers SBMOS2 #18 and #19, extracted using the ColdFET S-parameter

deembedding technique, and shows the extrapolations at -20 dB/dec from 40 GHz used to determine the unity-gain cutoff frequency f_T. The extrapolations are in good agreement with measured data over a wide frequency range between 20 and 60 GHz. Data above 60 GHz is discarded in this analysis, since it is deemed inaccurate, as explained previously. This approach returns cutoff frequencies of 71 and 68 GHz for these two devices.

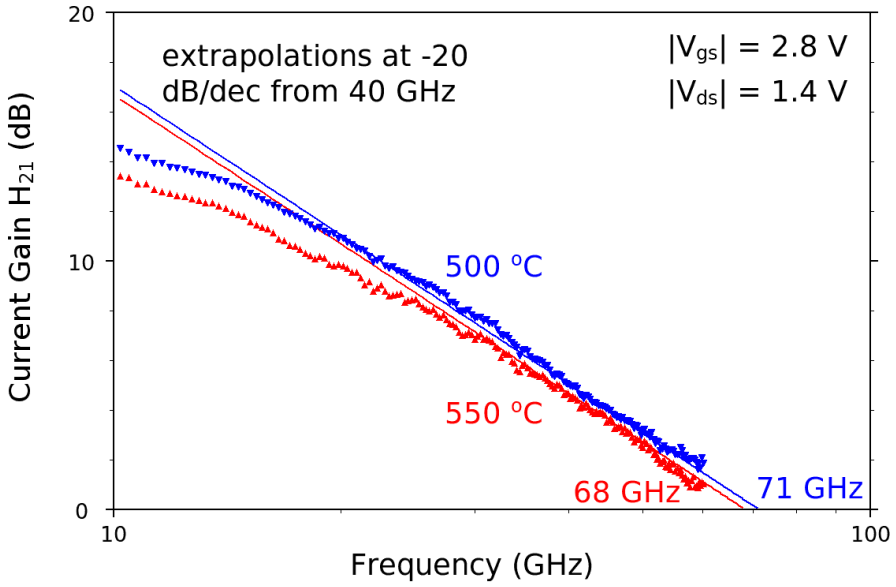

Figure 5.9: Current Gain comparison of wafers annealed at 500 and 550 °C.

Despite substantially differing saturation transconductance values of 469 and 640 mS/mm on SBMOS2 #18 and #19, respectively, obtained during DC characterisation for the particular devices, the extracted cutoff frequencies are surprisingly very similar. In saturation, unity-gain cutoff frequency (f_T), saturation transconductance ($g_{m,sat}$) and total gate capacitance (C_{gg}) are related according to [Tsividis, 1999]

$$f_T = \frac{g_{m,sat}}{2\pi C_{gg}}, \tag{5.1}$$

Wafer ID	Anneal T	$g_{m,sat}$ (mS/mm)	f_T (GHz)	C_{gg,f_T} (fF)
SBMOS2 #19	500 °C	640	71	5.72
SBMOS2 #18	550 °C	469	68	4.40

Table 5.1: Summary of RF performance parameters.

where C_{gg} includes intrinsic gate-to-source and gate-to-drain capacitances and all extrinsic capacitances, such as overlap and fringing-field capacitances between the gate and the source and drain terminals.

Introducing the measured values of $g_{m,sat}$ and the extracted f_T values from Figure 5.9, the equivalent input capacitances for devices from both wafers, denoted as $C_{gg,fT}$, is calculated. The results for both devices are summarized in Table 5.1 and are representative of a number of devices from both wafers.

The electrical properties listed in Table 5.1 show a 30% difference in C_{gg,f_T} between the two wafers. Apart from the source/drain silicide anneal temperatures, both wafers were processed following the same technological parameters and at the same time, thus ruling out variations in physical device dimensions as a cause for this large capacitance variation.

The difference in gate capacitance can be explained by the presence of a higher Schottky barrier for the wafer receiving the 550 °C silicide anneal compared to the wafer receiving the 500 °C silicide anneal, consistent with observations made during DC characterization.

The dominant component of the total gate capacitance C_{gg} is the intrinsic gate-to-source capacitance, C_{gsi}, which is defined as

$$C_{gsi} = \frac{dQ_g}{dV_{gs}}, \tag{5.2}$$

where dQ_g is the charge placed on the gate as a result of an incremental gate-to-source voltage change dV_{gs}. The gate charge in turn is a function of the inversion capacitance. To illustrate this point, let us use a semiquantitative argument and assume that the inversion capacitance is comparable to or smaller than the oxide capacitance. Then eqn. 5.2 may be expressed as [Koomen, 1973]

$$C_{gsi} \sim \frac{1}{\omega} \frac{dI_s}{dV_{gs}}, \tag{5.3}$$

where ω is frequency, I_s is source current and V_{gs} is gate-source voltage. In a SB-MOSFET, the source current is controlled by the Schottky barrier between source and channel and the electric field at the source end of the channel. The latter in turn is modified by the gate-to-source potential. The current shows exponential dependency on barrier height in all models used to describe carrier transport across a Schottky barrier, whether based on thermionic emission [Rhoderick and Williams, 1988] or assuming tunneling as the dominant transport mechanism, using either the WKB approximation [Rhoderick and Williams, 1988, Padovani and Stratton, 1966] or an Airy function approach [Winstead and Ravaioli, 2000, Vega, 2006a]. Common to all these models is an inverse proportionality and an exponential relationship between barrier height and current. This is illustrated by Fig. 5.10, in which tunneling current density has been calculated for various Schottky barrier heights and electric fields using a full Airy function approach. The data in Fig. 5.10 is adapted from Fig. 9 by Winstead and Ravaioli [2000].

Similarly, the gate-to-source capacitance, being proportional to source current according to eqn. 5.3, must also be inversely proportional to and exponentially dependent on the source-to-channel Schottky barrier height.

To put it more concisely, a higher Schottky barrier restricts carrier injection from the source into the channel, resulting in lower drive current and transconductance, as

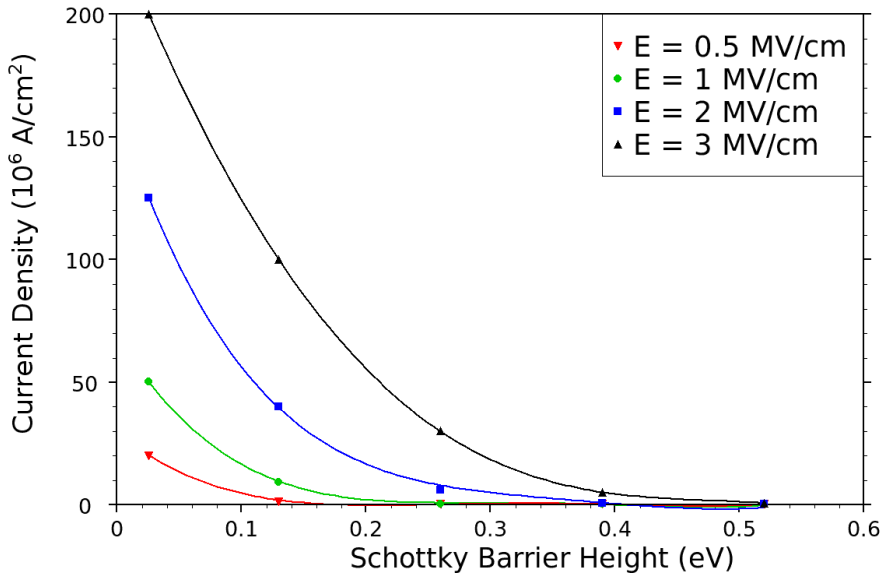

Figure 5.10: Tunneling current density as a function of Schottky barrier height for various horizontal electric field intensities at the Schottky junction; symbols: data points from Winstead and Ravaioli [2000]; lines: exponential fits.

observed during DC characterization. The restriction of carriers entering the channel necessitates a reduced inversion charge density and consequently, a smaller gate capacitance. Therefore, despite exhibiting substantially inferior DC performance, the corresponding reduction in gate capacitance means that the wafer receiving a 550 °C silicide anneal exhibits comparable high-frequency performance to the wafer receiving a 500 °C silicide anneal. This observation is unique to Schottky barrier metal source/drain MOSFETs, due to the transport mechanisms governing carrier transport at the source-channel interface.

5.5 Literature Comparison

A comparison of unity gain cutoff frequencies obtained in this work to literature results for doped source/drain p-MOSFETs [Barlage et al., 2001, Burghartz et al., 2000, Chatterjee et al., 2004, Hashimoto et al., 2004, Holloway et al., 1997, Lee et al., 1992,

Saito et al., 1995, 1998, Taur et al., 1993, Yamamoto et al., 1996] is shown in Figure 5.11 along with a trend line for the literature data. Only publications reporting bulk Si pMOS devices with equivalent oxide thicknesses and supply voltages within a reasonable range with respect to ITRS recommendations are considered to provide a meaningful comparison. The unity gain cut-off frequencies obtained on the two wafers characterized in this work show improvements of 61% and 55% over the literature trend line at 85 nm gate length and even surpass the performance of devices of less than 40 nm gate lengths [Chatterjee et al., 2004].

Figure 5.12 displays a comparison of transconductance values obtained on the two wafers characterized in this work to literature values for publications reporting both cutoff frequency and transconductance [Barlage et al., 2001, Burghartz et al., 2000, Lee et al., 1992, Ohguro et al., 1996, Taur et al., 1993]. Together with Fig. 5.11 this paints an interesting picture.

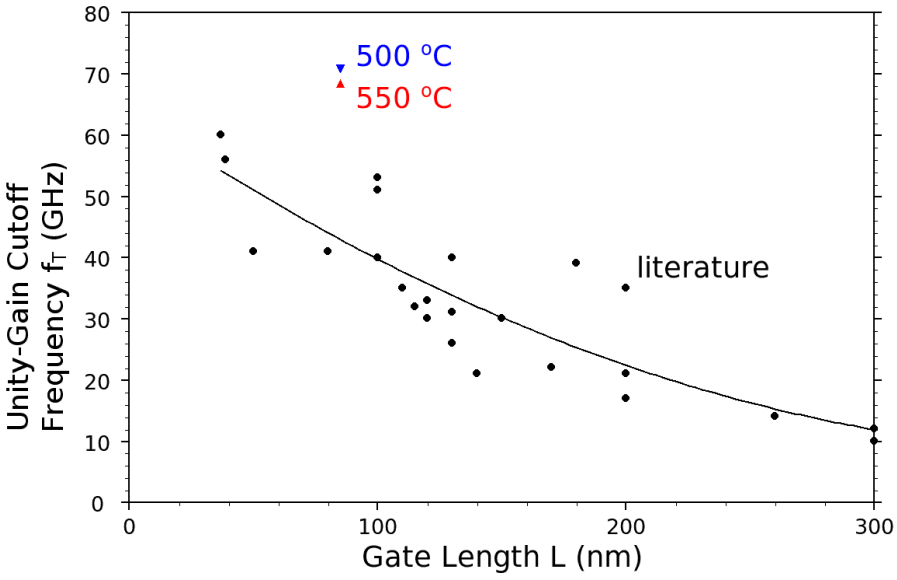

Figure 5.11: Cutoff frequencies of SB-MOSFETs compared to DSD devices reported in literature, illustrating higher cutoff frequencies for SB-MOSFETs; squares: literature doped source/drain devices; triangle down: 500 °C; triangle up: 550 °C SB-MOSFETs.

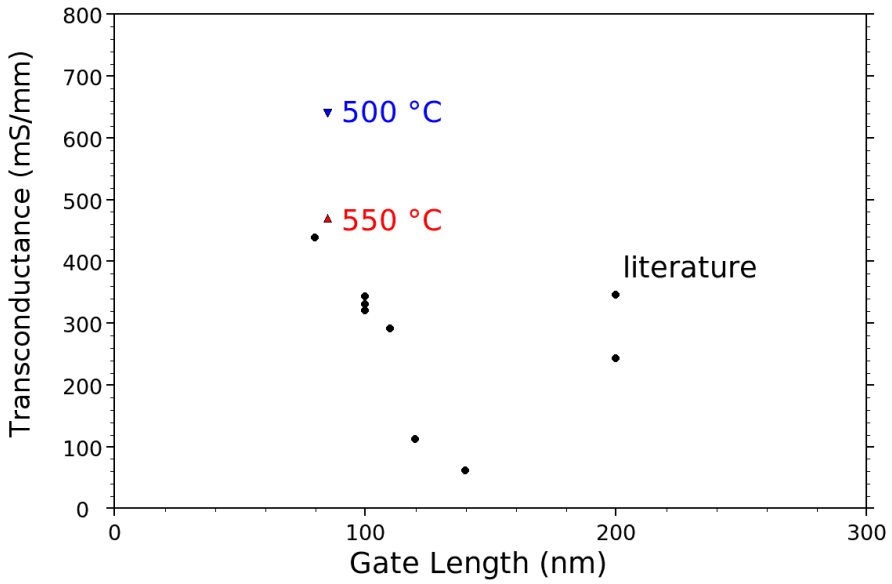

Figure 5.12: Transcondutance comparison of SB-MOSFETs to literature DSD devices reporting both f_T and g_m.

The cutoff frequency improvement on the wafer receiving the 500 °C silicide anneal can be almost entirely attributed to transconductance enhancement - 640 mS/mm for the 85nm SB-MOSFET versus 290 to 438 mS/mm for literature device of gate lengths of 80 - 100nm. The relatively high transconductance can be accredited to reduced mobility degradation at high gate bias voltages, a result of reduced carrier scattering in the channel due to reduced vertical effective fields, consistent with explanations for the absence of a transconductance fall-off presented in section 4.4.4. Additional cut-off frequency improvements can be put down to capacitive factors applicable to both characterized wafers and will be described subsequently.

In contrast, the transconductance of 469 mS/mm obtained on the wafer receiving the 550 °C silicide anneal is comparable to literature devices of similar gate lengths - only 7% higher than the best performing literature device. As postulated in the previous section, the cutoff frequency improvement on this wafer can be explained by a reduction in gate-to-source capacitance due to the restriction of carrier injection from the source

by a higher Schottky barrier.

There are additional factors applicable to both characterized wafers that may contribute to RF performance improvements of SB-MOSFETs over DSD devices. Doped source/drain devices require gate-to-source/drain overlaps in order to confine carriers close to the surface in regions of the source/drain extensions close to the channel, preventing them from entering low-doped, higher resistivity regions and degrading drive current [Thompson et al., 1998]. SB-MOSFETs do not require these overlaps to preserve drive current, thus removing capacitances related to these overlaps and resulting in a lower total gate capacitance.

In addition, quantization effects in the inversion layer of modern thin oxide devices have been shown to play a significant role in lowering the gate capacitance [Takagi et al., 1999]. This effect is more pronounced in the devices reported in this study since the low vertical effective field allows the inversion charge to spread away from the surface, moving the peak of the inversion charge concentration away from the channel surface [Winstead and Ravaioli, 2000]. This effectively increases EOT and leads to a reduction in gate capacitance.

These inversion layer quantization effects and the absence of overlap capacitance serve to reduce active gate capacitance. RF performance is inversely dependent on gate capacitance, so these effects will improve performance compared to conventional doped source/drain devices.

Chapter 6

Modelling of SB-MOSFETs using MEDICI

6.1 Introduction

The optimisation of MOSFET designs using iterative fabrication and characterisation steps is very time-consuming and expensive. Complex simulation packages have been developed that allow the electrical characteristics of a MOSFET to be simulated and enable device designs to be validated prior to fabrication, thereby saving time and money. However, device simulations can only complement, not replace, device fabrication and characterisation and must thus be verified by experimental data.

A number of simulations of SB-MOSFETs have been published. The simplest employ one-dimensional numerical solutions to approximate the source-to-channel carrier injection [Appenzeller et al., 2004, Jang et al., 2003a,b, Knoch and Appenzeller, 2002]. More complex, two-dimensional approaches using numerical [Hattori and Shirafuji, 1994, Huang et al., 1998] and TCAD [Saha et al., 2005] solutions have been used. The most complex simulations involve the use of Monte Carlo methods together with Greens function formalism [Guo and Lundstrom, 2002] or Airy function transfer matrices [Vega,

2006a,b, Winstead and Ravaioli, 2000].

Of aformentioned publications, only three [Jang et al., 2003b, Vega, 2006a, Winstead and Ravaioli, 2000] compare simulated with experimental data. Both Jang et al. [2003b] and Vega [2006a] employed one-dimensional models, whereas Winstead and Ravaioli [2000] performed a full two-dimensional Monte Carlo simulation. However, none of these attempted to create a simulation based on the actual structure of device that the simulation was attempting to replicate.

For this work, the 2-D drift-diffusion simulator *MEDICI*, the device simulator component of the Taurus Medici simulation package [Synopsys Inc., 2005], is used to simulate the behaviour of SBMOSFETs. The cross-section of a SB-MOSFET is used as the basis for the 2-D model structure together with known parameters, such as the channel doping profile. The full range of device parameters, such as device dimensions, doping concentrations and layer thicknesses and electrical properties as well as parameters governing the physical models used for calculating device characteristics can be adjusted and models for simulating Schottky barriers are included. The goal of this work is to develop a 2-D model of a SB-MOSFET that fits to experimental I-V data presented previously in this work.

Whilst electrical measurements capture the total currents entering and exiting a device and all analysis is derived from these, simulations can take a more detailed look at the physical properties of a device. It is possible to plot the (simulated) conduction and valence band profiles, charge distribution, electric field and electrostatic potential, thereby allowing much greater insight into what's actually happening within a device. In particular for SB-MOSFETs, where the drive current in short channel devices is largely determined by carrier transport across the source-channel barrier, it is very beneficial to be able to study these properties individually. Specifically, it is possible to observe the impact of individual components of carrier transport across a Schottky barrier in

isolation, i.e. thermionic emission and tunneling, something unthinkable in experiments, and it is possible to observe barrier lowering effects.

This chapter outlines the procedure applied to set up a successful simulation of devices characterised in the previous two chapters. The focus of the simulation is on generating a simulation fit to 85 nm gate length devices with the purpose of studying the properties of the Schottky barrier in terms of barrier height and barrier lowering as well as the relative importance of thermionic and field emission current contributions as a function of bias conditions.

6.2 Model Description

6.2.1 MEDICI Device Simulator

Overview

MEDICI employs a Finite Element Method (FEM) to simulate devices. This involves the creation of a simulation grid and declaring a set of material properties at each grid point, or *node*, by assigning each region a set of physical and electrical parameters. In addition, boundary conditions at the interfaces between different material types can be defined, such as the interface trap density at Si/SiO_2 interface or rectifying properties of a metal-semiconductor junction. Contact regions may be specified along with bias voltages that allow the current to be calculated as a function of bias conditions.

Based on these entered parameters, MEDICI self-consistently solves three partial differential equations, Poisson's equation and two continuity equations for holes and electrons, for the electrostatic potential Ψ and the electron and hole concentrations n and p [Synopsys Inc., 2005] at each node and according to user specified bias conditions. Using these, it calculates and can plot the electrical characteristics of the device structure that has been entered, such as current density, electrostatic potential, electric field

and charge distribution.

Various different models and region properties, such as semiconductor doping levels, material workfunctions, carrier mobility, Schottky contacts and more can be specified. These may or may not have significant impact on the final results. Of particular interest for SB-MOSFETs is the modelling of carrier transport at its metal-semiconductor junction.

The multitude of possible adjustable parameters makes it imperative to fix as many of the variables as possible, either from known material properties or through measurement. For example, the vertical channel doping profile iss derived from known channel ion implantation doses applied during device fabrication and the device structure and dimensions are extracted from process listings and cross-sectional TEM images.

Models used in this work

Mobility The universal mobility model together with parallel field mobility calculations are used throughout these simulations. The former is suitable for modelling MOSFET inversion layers while the latter accounts for high-field effects, such as carrier heating and velocity saturation, which are expected to occur due to the high horizontal electric fields present between source and channel.

Schottky Contact The MEDICI Schottky contact model can be enabled for specific device regions and in this work is applied to the source and drain regions of the SB-MOSFET. The Schottky barrier height for electrons in MEDICI is defined as the difference between the metal workfunction and the semiconductor electron affinity. The corresponding hole barrier is simply the semiconductor bandbap minus the electron barrier height. Thus, for the simulations, the hole barrier height is modified by changing the metal workfunction of the source and drain.

The barrier height in this case represents the *zero-bias* barrier height excluding barrier lowering mechanisms and should be close to literature values of 0.22 - 0.28 eV. Barrier lowering mechanisms are applied to this zero-bias barrier to give the final *effective* Schottky barrier height, which is expected to be in the region of 0.12 - 0.13 eV, as measured in section 4.2.

Barrier Lowering Barrier lowering consists of two components: image force and dipole lowering, which have been described in Chapter 2. MEDICI's built-in barrier lowering model includes both using the equation [Synopsys Inc., 2005]

$$\Delta\phi_B = \beta \left[\frac{q}{4\pi\varepsilon_{semi}}\right]^{\frac{1}{2}} E^{\frac{1}{2}} + \alpha\, E^{\gamma}, \tag{6.1}$$

where the first term on the right hand side represents image force, the second term dipole lowering and E the electric field at the interface, q the charge of an electron and ε_{semi} the semiconductor permettivity. The factors α, β and γ are fitting parameters without any real physical meaning. Dipole lowering is considered to be linear with electric field [Andrews and Lepselter, 1970], thus γ is fixed to 1 throughout.

Barrier lowering at Schottky contacts is included by adjusting the surface potential Ψ_S using

$$\Psi_{S_{eff}} = \Psi_S \pm \Delta\phi_B \tag{6.2}$$

and calculating hole and electron carrier densities using $\Psi_{S_{eff}}$ rather than Ψ_S. Physically, this means Poisson's equation is solved consistently with charge, but carriers see a combined Poisson and image force potential [Synopsys Inc., 2005].

In the course of this simulation work, it was discovered that the barrier lowering model in MEDICI is only applied to thermionic emission at a Schottky contact but not to field emission. However, the drive current above threshold in a SB-MOSFET is dominated by

tunneling, so the non-application of barrier lowering to field emission results in inaccurate simulation results and barrier lowering must be included by manual calculations in order to apply to tunneling as well.

Tunneling MEDICI includes tunneling at Schottky contacts by the addition of a self-consistent, distributed carrier generation rate, G_{SBT}, to the thermionic emission current, following the approach of Ieong et al. [1998] and Matsuzawa et al. [2000]. The generation rate at each node, shown for holes, is calculated according to

$$G_{SBT}(x) = -\frac{A^{**}\,T}{q}\,|E|\,\Gamma(x)\,ln\frac{1+\frac{p}{\gamma_p N_V}}{1+exp\left[\frac{E_{Fm}-E_V(x)}{kT}\right]}, \tag{6.3}$$

where x is the distance of the node from the interface, A^{**} the Richardson's constant for holes, T the ambient or lattice temperature, q the hole charge, E the electric field, p the hole concentration at x, γ_p the Fermi-Dirac factor at x, N_V the valence band density of states at x, E_{Fm} the Fermi level in the contact, $E_V(x)$ the valence band edge at x and k Boltzmann's constant. The tunneling coefficient $\Gamma(x)$ is given by the Wentzel-Kramers-Broullin (WKB) approximation

$$\Gamma(x) = exp\left(-\frac{2\sqrt{2m_0 m_h}}{\hbar}\int_0^x [E_V(x') - E_V(x)]dx'\right), \tag{6.4}$$

where m_0 is the free electron mass, m_h the effective hole tunneling mass and $\hbar$ Planck's constant. This carrier generation rate is simply added to the thermionic emission current at a Schottky contact.

6.2.2 Device Structure

Since the focus of the experimental work has been on the characterisation of 85 nm SB-MOSFETs and ample measurement data is available, this gate length is chosen for the simulation device. Furthermore, since devices on wafer SBMOS2 #19 exhibited the best DC and RF performance, the SB-MOSFET model is developed to fit to data from

this wafer. This means the use of a half-dose channel implant. A cross-section of the simulation device structure along with its major dimensions is shown in Fig. 6.1.

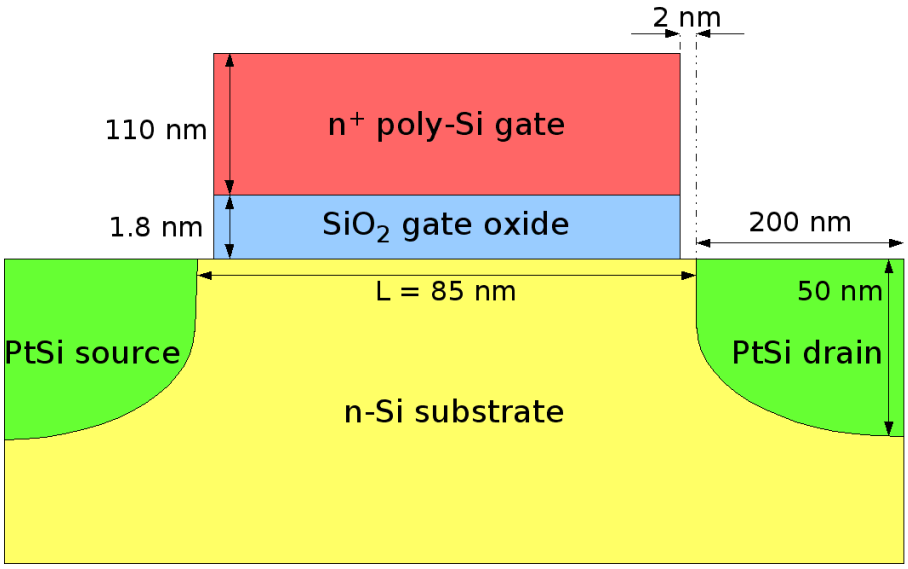

Figure 6.1: Cross-section of simulation device including dimensional parameters.

These dimensions are chosen based on the design variables used during fabrication and cross-sectional TEM images taken of actual devices. One important dimension to emphasise is the presence of a 2 nm gap or *underlap* between n-poly gate and PtSi source and drain. This parameter is of great importance to the performance of SB-MOSFETs [Calvet, 2001, Calvet et al., 2000, 2002].

6.2.3 Methodology

Due to the more complex nature of SB-MOSFETs compared to conventional DSD devices and the multitude of variable parameters that the presence of Schottky barriers adds, the approach to obtaining a good fit of simulation to measurement data is broken down into a number of smaller steps. In addition, prior to fitting, as many parameters as possible are fixed by either measurement, additional simulations or the use of default parameters.

The first step is to define a suitable grid lattice for SB-MOSFETs, since a typical grid employed for the simulation of DSD devices is unsuitable. The second step involves the creation of a fit to the subthreshold regime, in which thermionic emission is the dominant current contribution. The major factors here are the channel doping concentration and the interface trap density.

All further steps focus on generating a fit above threshold, where thermionic-field and field emission dominate the drain current. The most important parameters for this regime are Schottky barrier height, barrier lowering, electron and hole masses and the effective carrier mobility in the channel. To simplify matters, the default values for electron and hole masses are used and the universal mobility model with parallel field calculations is employed throughout. Hence the focus is on generating a fit by varying Schottky barrier height and barrier lowering. Since MEDICI does not apply its barrier lowering model to the tunneling current, barrier lowering has to be included by performing iterative simulations and manually calculating the amount of image force lowering at each bias point.

6.3 Results and Discussion

6.3.1 Grid

The structure of the grid has a major impact on the SB-MOSFET simulation results. The initially employed grid spacing adopted from previous work on conventional DSD devices is depicted in Fig. 6.2, illustrating the constant horizontal grid spacing along the channel. This type of grid is well suited for modelling doped source/drain devices due to the continuous nature of the electrostatic potential between source, channel and drain.

However, due to the abrupt change in electrostatic potential between metal and semiconductor in Schottky contacts, adopting such a grid for the simulation of SB-

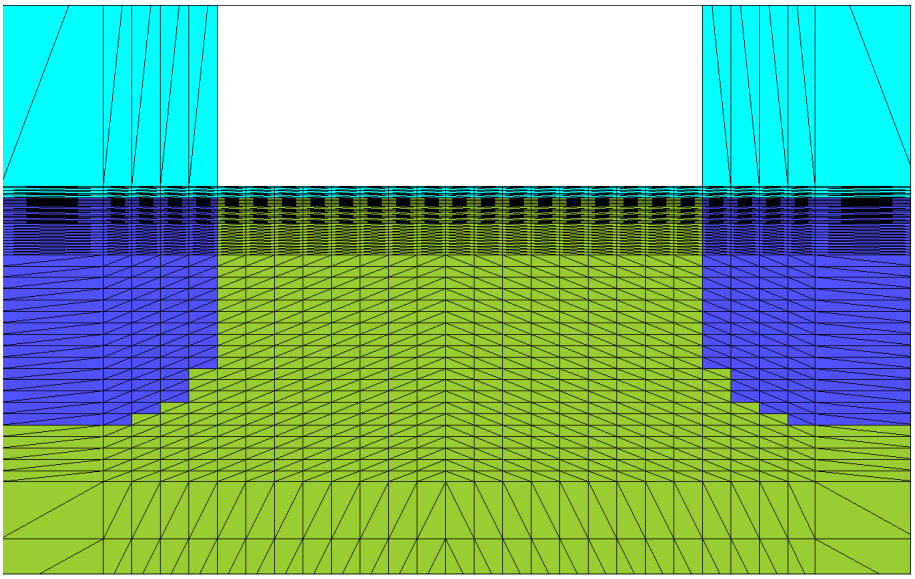

Figure 6.2: Initial, constantly spaced grid resulting in quick simulations but inaccurate results. Green: n-silicon substrate; Dark blue: PtSi source and drain; white: n-polysilicon gate; Light blue: SiO_2

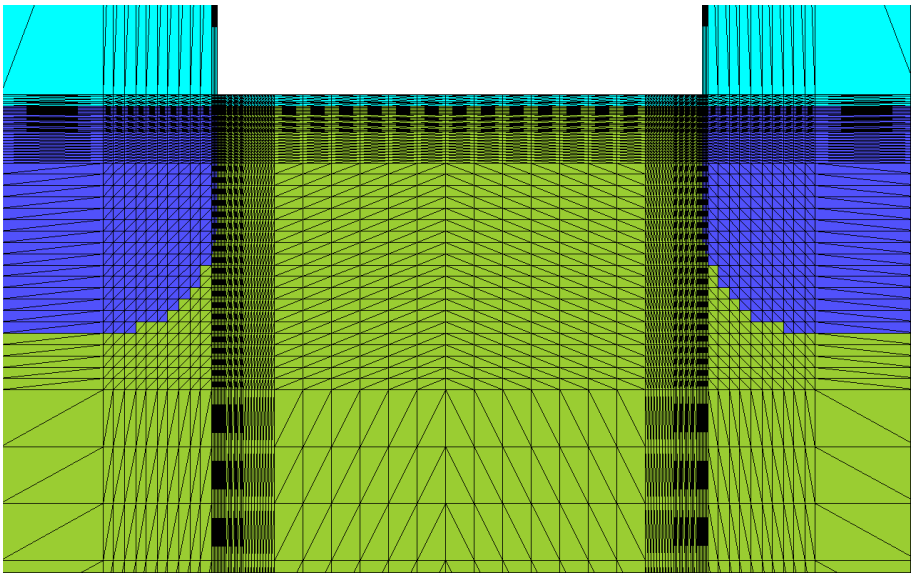

Figure 6.3: Refined grid used for SB-MOSFET simulations, resulting in improved simulation accuracy at the expense of increased simulation times.

MOSFETs produces inaccurate simulation results. The horizontal spacing of grid points means that the simulator cannot accurately account for the rapid changes in electrostatic potential between metallic source/drain and semiconducting channel and is thus unable to accurately calculate the current contribution caused by field emission.

By refining the grid at the source-to-channel and drain-to-channel interfaces, as depicted in Fig. 6.3, more accurate results can be achieved, though at the expense of an enourmous increase in simulation time. The grid of Fig. 6.3 represents the final grid obtained after several iterations of continual grid spacing refinements. Further decreases in grid node spacing at the metal-semiconductor interface resulted in minor differences in simulated drive currents ($\leq 1\%$) while substantially increasing simulation times, whereas coarser grids resulted in appreciable differences in simulation results. Thus, this grid represents a reasonable compromise between simulation accuracy and time.

The simulated drive currents for low drain voltage obtained for the two grids are compared on a semilog scale in Fig. 6.4 and illustrate the large differences in ON currents observed between the two. Standard physical parameters and a barrier height of 0.25 eV without barrier lowering are used in this simulation and no fitting to experimental data has been performed at this stage. In the subthreshold regime, the drive currents for both grids coincide, indicating that both grids accurately model the thermionic emission process.

However, above threshold, no current increase with gate voltage is observed for the coarse grid, leading to a drive current deviation of nearly two decades in the ON state, and indicates that the coarse, constantly spaced grid cannot accurately account for the field emission processes occuring in this regime. A similar discrepancy is observed under high drain bias conditions.

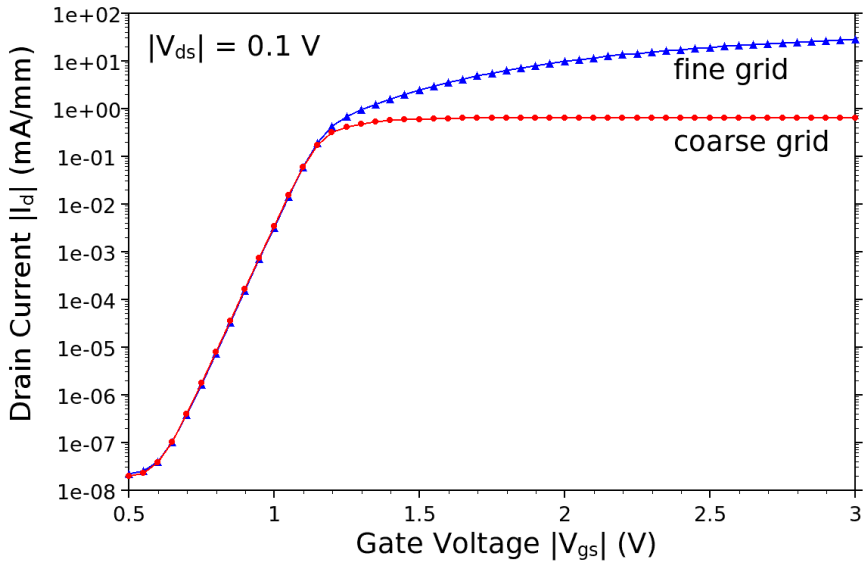

Figure 6.4: Simulated low drain bias transfer characteristic of 85nm gate length SB-MOSFET modelled using coarse and fine grids.

The electrostatic potential profile along the channel surface from source to drain under gate and drain voltages of 2.8 and 0.1 V, respectively, are shown in Fig. 6.5 for the coarse and in Fig. 6.6 for the fine grid. In both plots, the locations of the grid nodes are highlighted by the respective symbols and these can be used to explain why the coarse grid is not suitable for accounting for field emission.

As described previously, MEDICI models field emission by the addition of a carrier generation rate to the thermionic emission current for nodes on the semiconductor side in the vicinity of a Schottky contact, based on equations 6.3 and 6.4 [Synopsys Inc., 2005]. In the case of the coarse grid of Fig. 6.5, the barrier between source and channel is defined by 4 nodes, only one of which resides above the Fermi level. Therefore, the current contribution due to field emission is only be calculated for these few nodes, leading to a massive underestimation thereof.

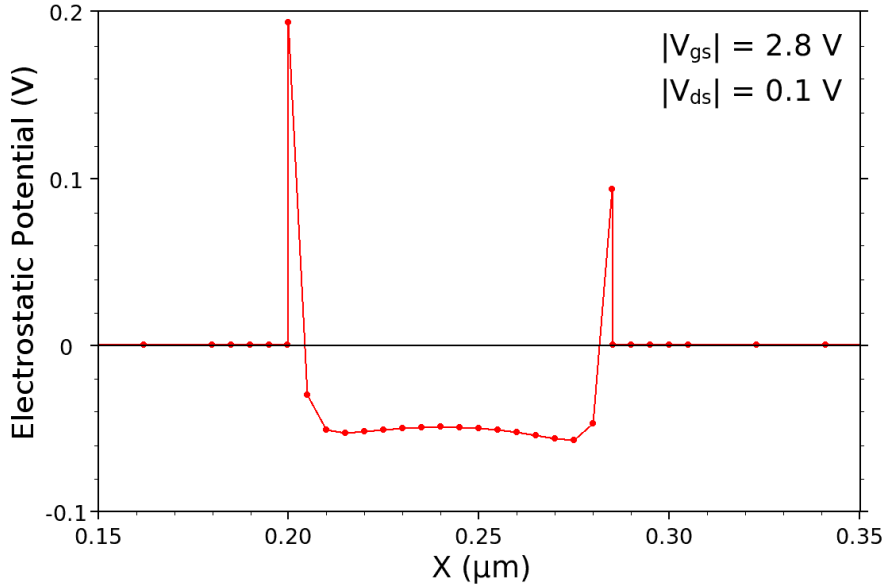

Figure 6.5: Valence band at the channel surface from source to drain under high bias conditions for the coarse grid. The location of the grid nodes are highlighted by circles.

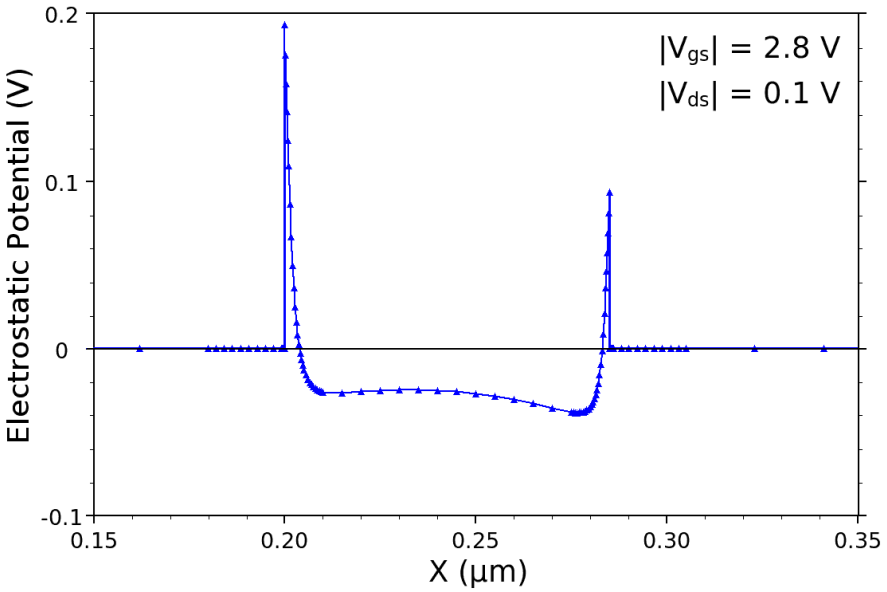

Figure 6.6: Valence band at the channel surface from source to drain under high bias conditions for the fine grid. Grid node locations are highlighted by triangles.

On the other hand, for the fine grid that results in the smooth potential profile of Fig. 6.6, the same barrier is defined by 30 grid nodes and the field emission contribution is calculated for each of these nodes. This leads to a more accurate inclusion of field emission, as evident from the current comparison of Fig. 6.4.

6.3.2 Subthreshold

Having defined a suitable grid, the next step involves the generation of a simulation fit to the subthreshold regime, in which thermionic emission of carriers from the source over the source-to-channel Schottky barrier is the dominant current contribution. The two simulation variables with the greatest impact in this regime are the channel doping concentration and the interface trap density. The Schottky barrier height is found to have a negligible impact on the subthreshold regime. Due to the dominance of thermionic emission for subthreshold bias conditions and in order to reduce simulation times, field emission is not included the subthreshold fitting simulations.

The vertical channel doping concentration profile is generated using the process simulator TSUPREM4, part of the MEDICI modelling package. The process parameters are taken from the device fabrication specifications for the Spinnaker SB-MOSFET wafers. The retrograde channel doping profile of these devices was created by ion implantation of Arsenic through a 8 nm oxide into a lightly phosphorous-doped ($N_D = 10^{15}$) silicon substrate. The implant was followed by a series of anneals, an implant activation anneal, RTP1, at 1050 ^{o}C for 10 seconds, a sidewall spacer anneal, RTP2, at 1100 ^{o}C for 5 seconds and the source/drain silicidation anneal at 500 ^{o}C for 1 hour.

These process parameters are entered into TSUPREM4 to generate a vertical doping profile. The total active doping concentration in the vertical direction obtained in this simulation is compared to measured SIMS data in Fig. 6.7. The dopant concentration at the surface is $1.5 \cdot 10^{16}$ cm^{-3} and the peak concentration of $5.3 \cdot 10^{17}$ cm^{-3} is at a depth of 50 nm.

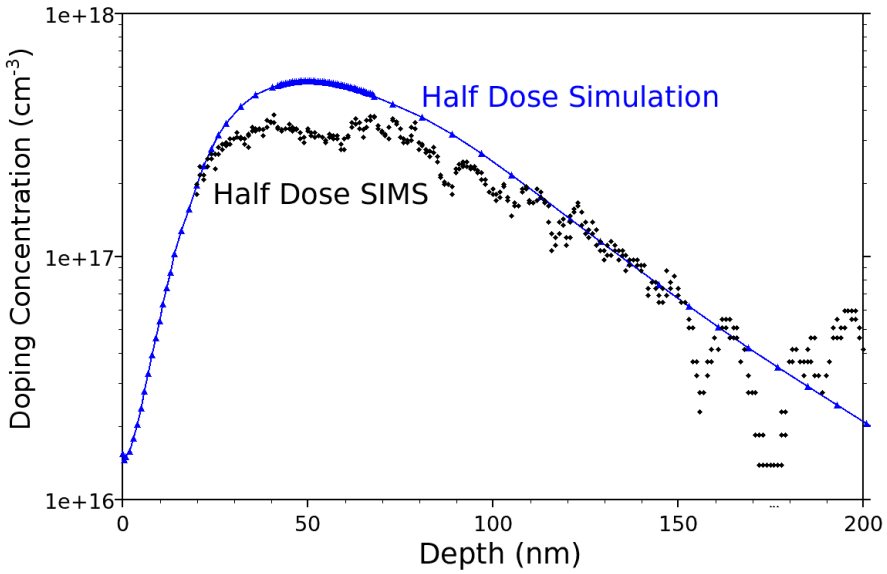

Figure 6.7: Vertical active channel doping profile simulated using MEDICI TSUPREM4 for half-dose As implantation, two RTAs and source/drain silicide anneal. Blue triangles: simulated; Black diamonds: Measured SIMS.

A doping profile for the full dose implant is also generated, as shown in section 4.1, but is not repeated here since it is not used in these simulations.

The second parameter with a great impact on the subthreshold regime is the interface trap density. It is set so $1 \cdot 10^{11}$ cm^{-2} to achieve a good simulation fit to subthreshold. This high value is consistent with the observation that the gate oxide on these devices is poor and very leaky.

The simulated low drain voltage output characteristic generated using this approach is compared to measured data in Fig. 6.8. A reasonable fit to the measured subthreshold regime over three decades of current between $|I_d| = 10^{-2}$ and 10^{-5} mA/mm is achieved. The discrepancy in the ON state is due to the exclusion of field emission for this simulation and illustrates the strong dependence of the drain current on field emission for high gate voltages. Similarly, the differences in the OFF state current are

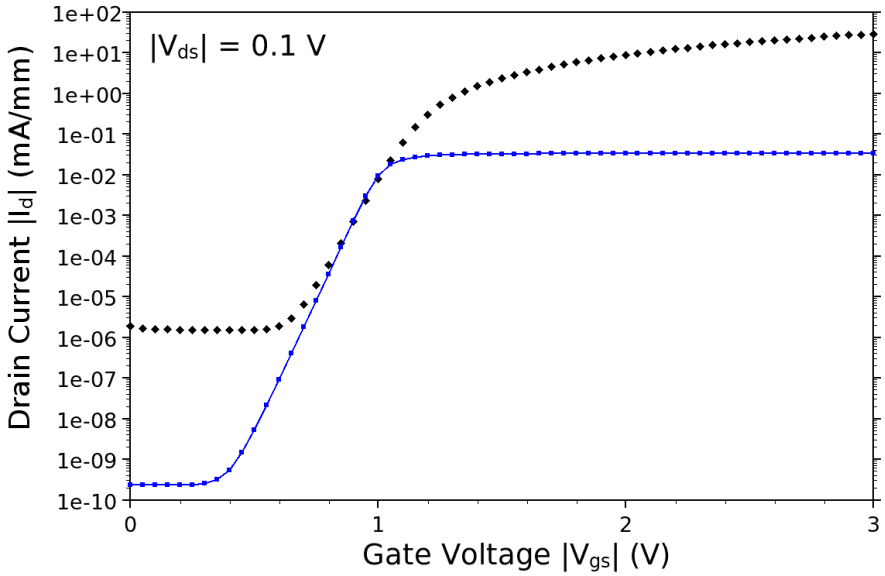

Figure 6.8: Fit to subthreshold regime obtained for a simulation excluding field emission and barrier lowering. A reasonable fit over 3 current decades is obtained. Blue line: simulation. Black diamonds: measurement data.

attributable to reverse leakage currents due to field emission processes, which are not yet considered in the simulation.

6.3.3 Barrier Height

The third step focuses on the Schottky barrier height of the PtSi-Si contacts between source and drain and the channel. In MEDICI, the zero-bias Schottky barrier height for holes is defined as the difference between metal workfunction and semiconductor valence band and can varied by modifying the value of metal workfunction in source and drain regions.

Literature values for zero-bias barrier heights for the PtSi-Si system range from 0.22 to 0.28 eV [Kikuchi, 1998, Koeneke et al., 1981, Kudzierski et al., 2000a, Lepselter and Sze, 1968, Murarka, 1983, Snyder et al., 1995, Sze, 1981, Wang et al., 1999] and recent work on the extraction of effective Schottky barrier height in back-to-back diodes

returned values in the range of 0.12 to 0.15 [Dubois and Larrieu, 2002]. The Schottky barrier height extracted previously on the devices under investigation in the present work returned similar values of 0.11 to 0.13 eV (see section 4.2). However, these latter values represent an effective barrier height that includes barrier lowering effects, whereas the barrier height entered in MEDICI must be the zero-bias value and is expected to be close to the former values.

In order to cover a wide range of possible values, simulations for zero-bias Schottky barrier heights from 0.10 to 0.35 eV in 0.05 eV steps are performed. Field emission is enabled but barrier lowering is disabled for these simulations.

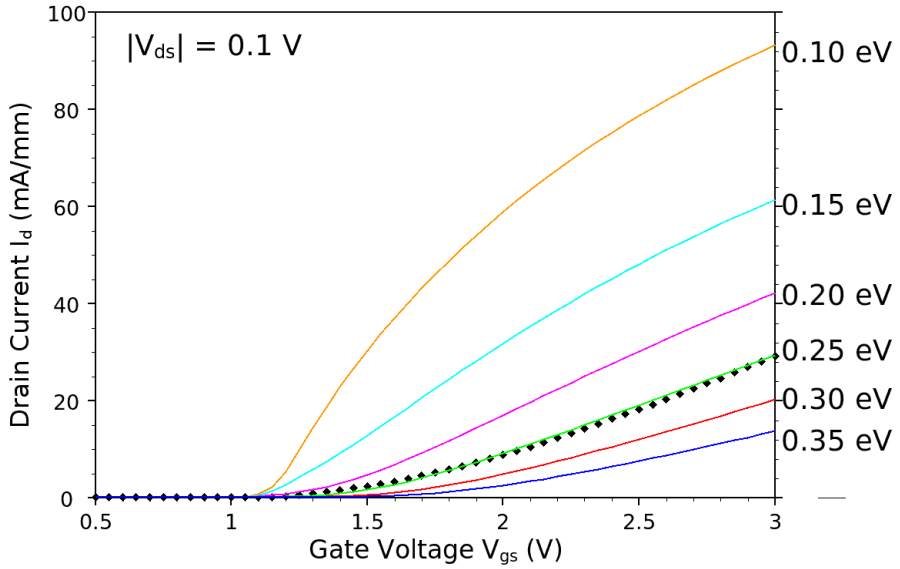

Figure 6.9: Simulated drain currents for V_{ds} = 0.1 V for Schottky barrier heights from 0.10 to 0.35 eV compared to measured data. Large differences up to nearly a decade are observed in the simulated drive current.

The simulated drain currents for barrier heights from 0.10 to 0.35 eV under a low drain bias V_{ds} of 0.1 V are compared to measurement data in Fig. 6.9 on a linear and in Fig. 6.10 on a logarithmic scale. The former highlights the significant impact that barrier height variations have on the ON state of a SB-MOSFET. Nearly a decade variation

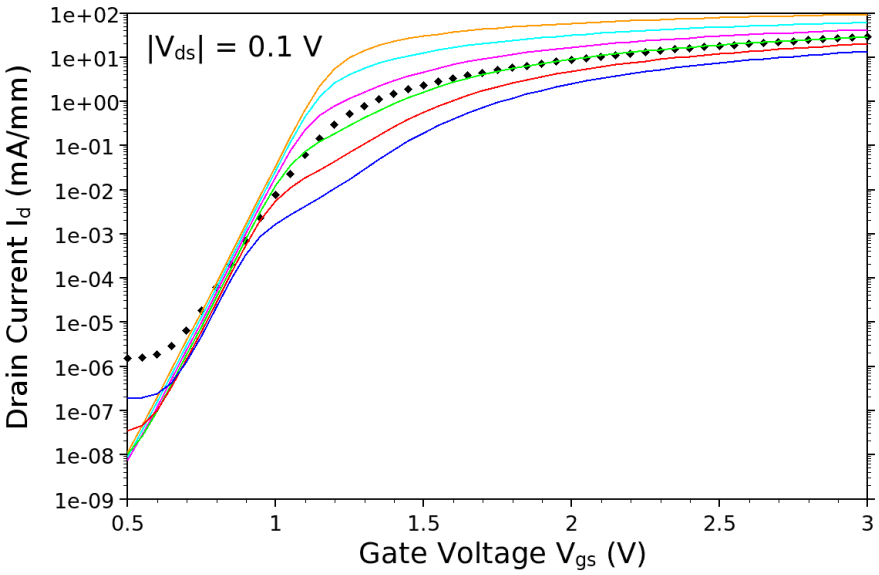

Figure 6.10: Simulated drain currents for $V_{ds} = 0.1$ V for Schottky barrier heights from 0.10 to 0.35 eV compared to measured data on a logarithmic scale. The subthreshold slope remains largely unaffected by barrier height variations.

in drain current is evident at $V_{gs} = 3$ V between the cases of 0.10 and 0.35 eV. The latter figure demonstrates the very small impact of barrier height on the subhthreshold current. The subthreshold slope is unaltered for all barrier heights. Again, significant deviations in the magnitude and shape of the ON current are observed.

Overall, a Schottky barrier height of 0.25 eV is seen to provide the best fit over the whole gate voltage range and is chosen as the zero-bias barrier height for subsequent simulations with the application of barrier lowering. The low drain bias fit is used to select the barrier height value since the measurement data is thought to be less influenced by barrier lowering and thus provide a better approximation. The choice of 0.25 eV coincides very well with aforementioned literature range for zero-bias Schottky barrier heights for PtSi-Si junctions.

The corresponding high drain voltage transfer characteristics are shown in Fig. 6.11 and 6.12 on linear and logarithmic scales respectively. While none of the simulation

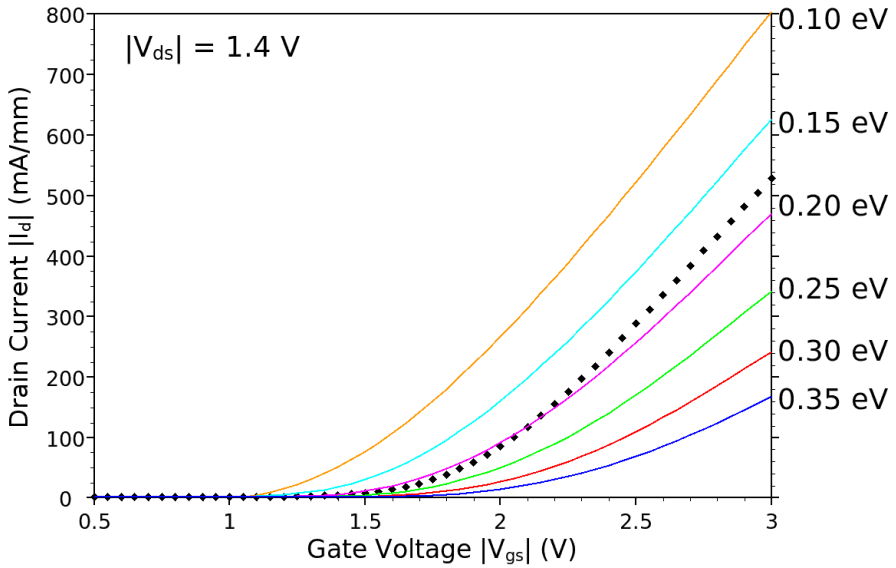

Figure 6.11: Simulated drain currents for $V_{ds} = 1.4$ V for Schottky barrier heights from 0.10 to 0.35 eV compared to measured data.

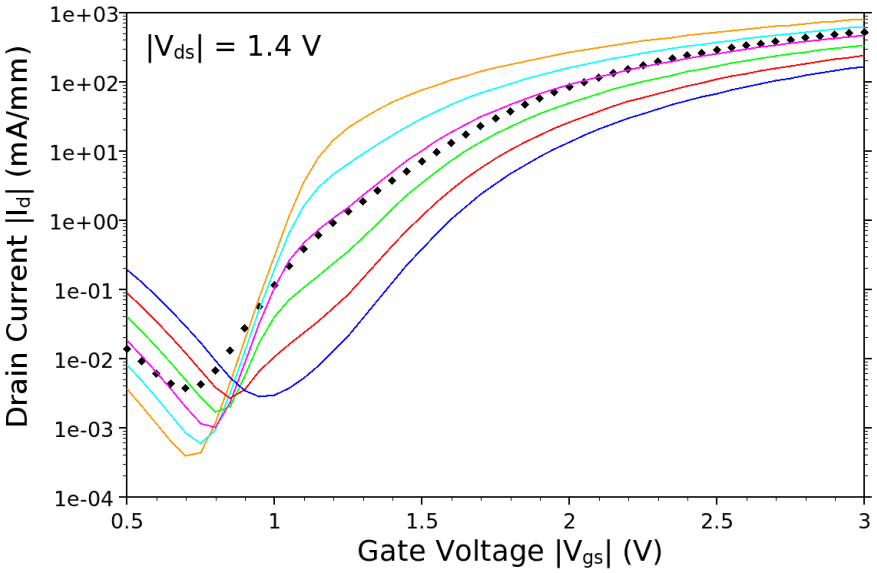

Figure 6.12: Simulated drain currents for $V_{ds} = 1.4$ V for Schottky barrier heights from 0.10 to 0.35 eV compared to measured data.

curves exhibit a reasonable fit to measurement data over the whole range of gate voltages, the characteristic for $\Phi_{Bp} = 0.20$ eV comes closest. This can be seen as an indication of barrier lowering effects becoming prominent under high drain bias.

The dependence of drive current on Schottky barrier height under both low and high drain bias indicates that the source-to-channel junction retains a controlling influence over the total drain current. The drain current does not appear to be channel limited, as postulated by Snyder et al. [1995] and Wang et al. [1999].

6.3.4 Barrier Lowering

The final step is to include barrier lowering mechanisms and fine tune the variables to achieve a good simulation fit. However, during the course of the simulations, it was established that the barrier lowering model built into MEDICI is only applied to thermionic emission, not to field emission calculations. This means that simply enabling MEDICI's built-in barrier lowering model has negligible impact on the drain current in the ON state of a SB-MOSFET, where field emission represents the dominant current injection mechanism.

That does not accurately represent the physical processes at work in a SB-MOSFET, because barrier lowering has an appreciable impact on the effective Schottky barrier height. Therefore, barrier lowering is expected to have an appreciable impact on the drive current, especially at high gate and drain voltages.

In order to circumvent this limitation, barrier lowering is included manually using an iterative simulation approach. In addition to the current, for every simulated bias point, the horizontal electric field E_{hor} at the surface at 1 nm distance from the source-to-channel interface is extracted and used to calculate a barrier lowering coefficient BL_{if} for that bias point to be used in the next iteration. Barrier lowering is calculated using the image force lowering equation [Rhoderick and Williams, 1988]

$$BL_{if} = \sqrt{\frac{qE_{hor}}{4\pi\epsilon_{Si}}}, \tag{6.5}$$

where q is the electron charge and ϵ_{Si} is the dielectric constant of silicon. For the next simulation iteration, these values of BL_{if} are subtracted from the zero-bias barrier height at their corresponding bias point to give the effective barrier height. The simulation is then repeated with the effective barrier heights. Then both current characteristics and horizontal electric field are extracted from simulation, and a new set of barrier lowering coefficients are calculated from the simulated electric field. This prociess is repeated until the variations in barrier lowering become negligible between simulation iterations. Dipole barrier lowering is not included due to the additional complexity it incurs. The intrinsic barrier lowering model of MEDICI was disabled for these simulations to avoid conflicts.

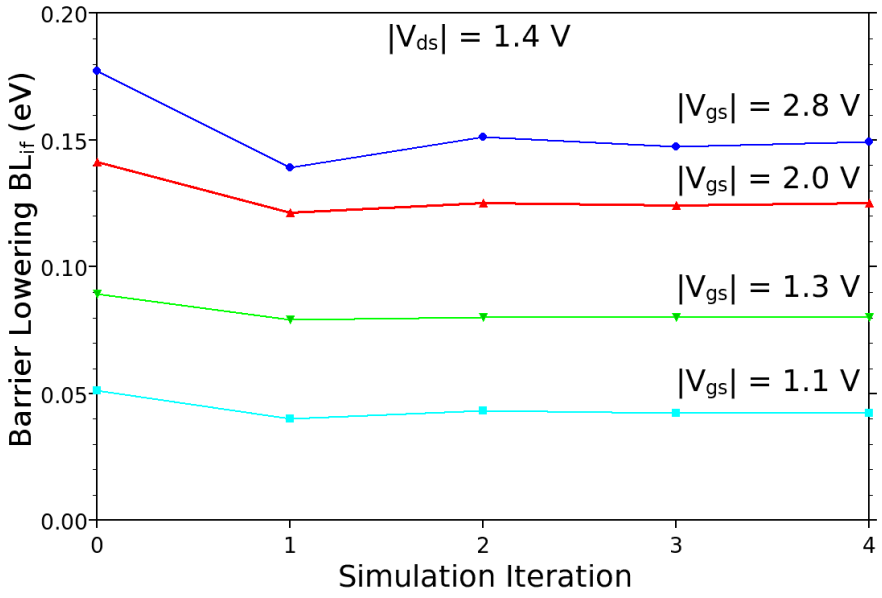

Figure 6.13: Manually calculated barrier lowering coefficient for several simulation iterations and a number of gate voltages under high drain bias, illustrating the convergence of the barrier lowering coefficient with simulation iteration.

The manually calculated image force barrier lowering coefficient BL_{if} is shown as a function of simulation iteration for four gate voltages under high drain bias in Fig. 6.13. Iteration 0 represents the initial situation without any barrier lowering and serves to calculate the initial barrier lowering values.

The initial barrier lowering coefficients calculated in iteration 0 are very large compared to the values for the last iteration. In this iteration, barrier lowering has not yet been accounted for, and the higher barrier leads to larger horizontal electric fields, which in turn result higher barrier lowering coefficients according to eqn. 6.5

In the subsequent iteration, these initial, very large barrier lowering coefficients over-compensate for image force lowering, resulting in an effective barrier that is too small. The following simulation iteration then results in smaller horizontal electric fields at the source-to-channel interface, and consequently barrier lowering coefficients that are smaller than the initial ones. This process of over-, then under-compensating for barrier lowering serves to intrinsically force the barrier lowering coefficients to converge on a value between the two extremes of iterations 0 and 1, as can be seen in Fig. 6.13, with fluctations between successive simulation iterations decreasing with the number of iterations. Furthermore, the fluctuations are exaggerated for higher gate and drain voltages.

Barrier lowering coefficients obtained in this manner are shown in Fig. 6.14 versus gate voltage and in Fig. 6.15 versus drain voltage . Both figures display converged values obtained after five iterations with otherwise unchanged parameters.

The negative barrier lowering below $|V_{gs}| = 0.9$ V in Fig. 6.14 represents an increase in hole barrier and a corresponding decrease in electron barrier height. At these gate voltages, the channel is in accumulation and the horizontal electric field at the source-to-channel interface reverses its direction. The electron barrier decrease is significant

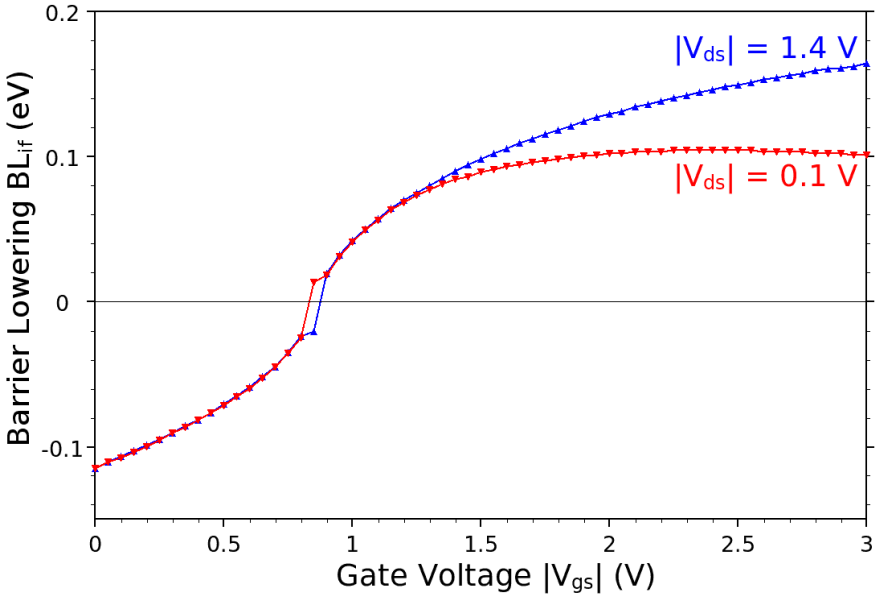

Figure 6.14: Final BL_{if} coefficients versus gate voltage.

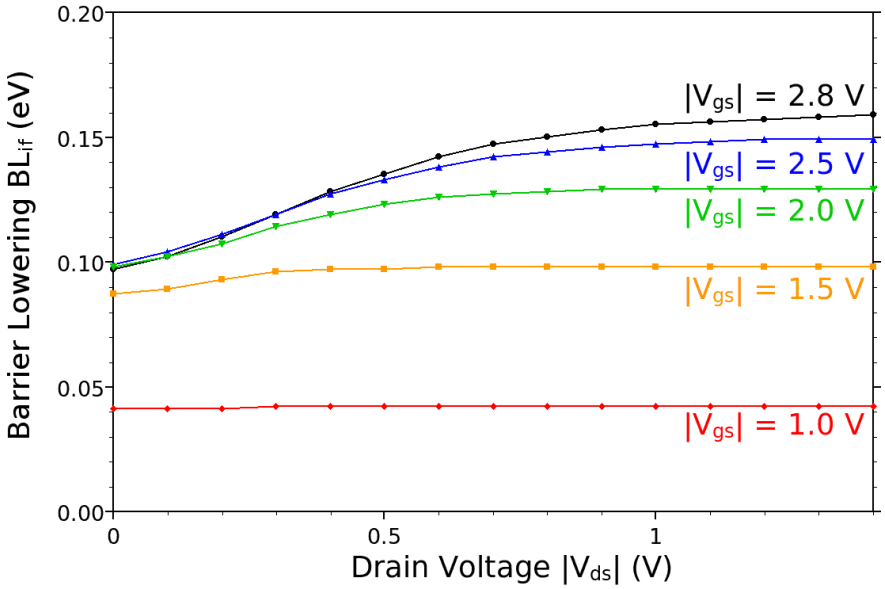

Figure 6.15: Final BL_{if} coefficients versus drain voltage.

for reverse leakage in the OFF state, since that is dependent on electron flow. The kink at $|V_{gs}| = 0.85$ V is an artefact of the manual barrier lowering calculations, but does not noticably affect the current calculations.

Subtracting the peak barrier lowering value of 0.16 eV from the zero-bias value of 0.25 gives a minimum effective barrier height of 0.09 eV for $|V_{gs}| = 3.0$ and $|V_{ds}| = 1.4$ V. This value is in reasonable agreement with effective values of 0.11 to 0.13 eV extracted in section 4.2 and values by Dubois and Larrieu [2004]. Therefore, this simulation work confirms that the Schottky barrier height extracted using the back-to-back diode technique used in the DC section of this work and by Dubois and Larrieu [2004] is in fact an effective value and that image force barrier lowering due to horizontal electric fields is responsible for the difference to literature values based on other measurement techniques that return values in the range of 0.22 to 0.28 eV.

The simulated transfer characteristics for the final simulation iteration are compared to measured data in Fig. 6.16 for a low drain voltage of 0.1 V and in Fig. 6.17 for a high drain voltage of 1.4 V. The output characteristic for a high gate voltage of 2.8 V is compared in Fig. 6.18.

For the low drain bias case of Fig. 6.16, the simulated drain current is in reasonable agreement with the measured data for all gate voltages above 0.7 V. The deviation of simulation and measurement below 0.7 V may be explained by defect-assisted leakage or drain-to-substrate leakage in the measurement data, neither of which are considered in the simulation. The subthreshold slope of the measured data is higher than the simulated one, indicating the presence of some form of degrading effect in the device.

In the case of high drain bias, shown in Fig. 6.17, the simulation is in reasonable agreement with measurement over most of the voltage range. The typical features of SB-MOSFET transfer characteristics, namely the reverse leakage and the tri-slope ON

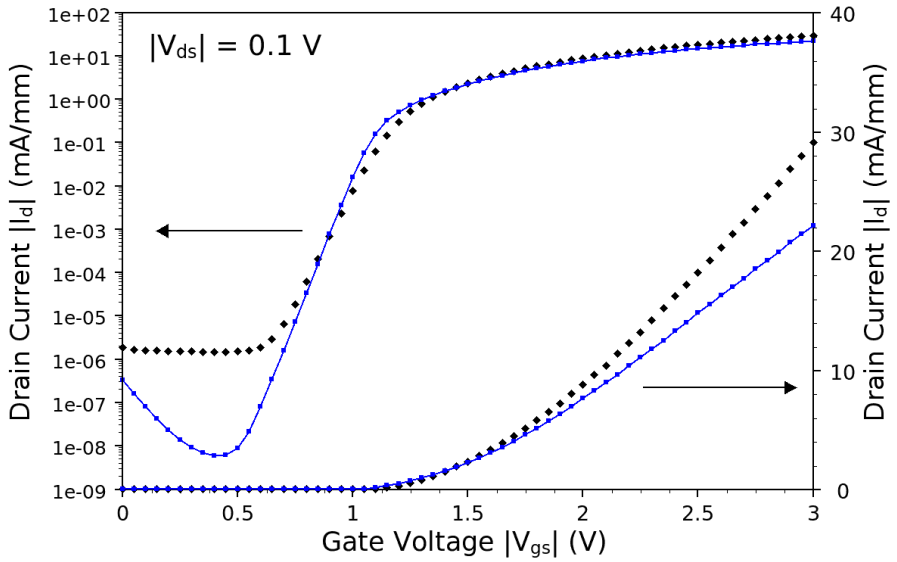

Figure 6.16: Drain current fit for low drain bias. Blue line: simulated. Black diamonds: measured.

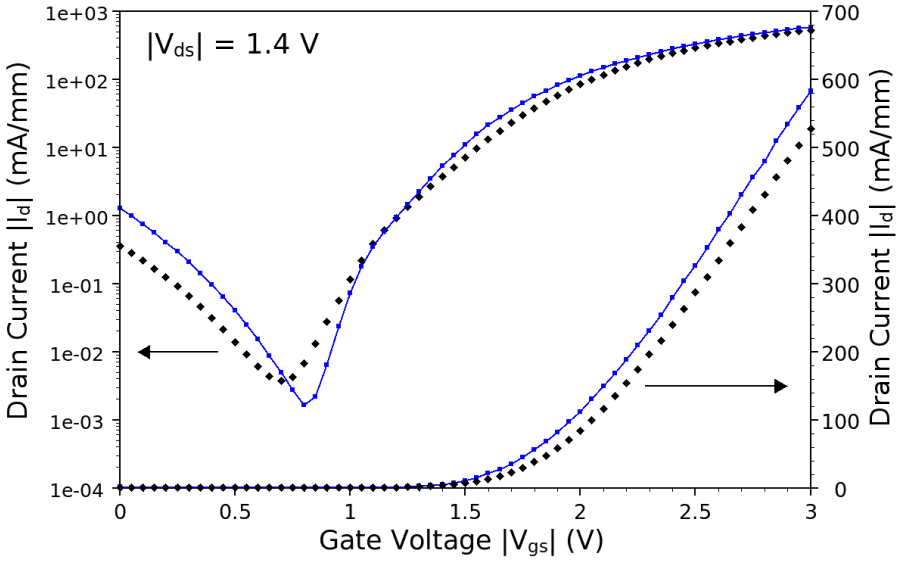

Figure 6.17: Drain current fit for high drain bias. Blue line: simulated. Black diamonds: measured.

characteristic, are replicated in the simulated drain current. The simulated OFF state leakage below $|V_{gs}| = 0.7$ V is higher than the measured value and the current minimum occurs 0.1 V aboves the measured, 0.8 V instead of 0.7 V. As for the low drain bias case, the simulated subthreshold slope is better than the measured, indicating the presence of degradation effects, as mentioned previously.

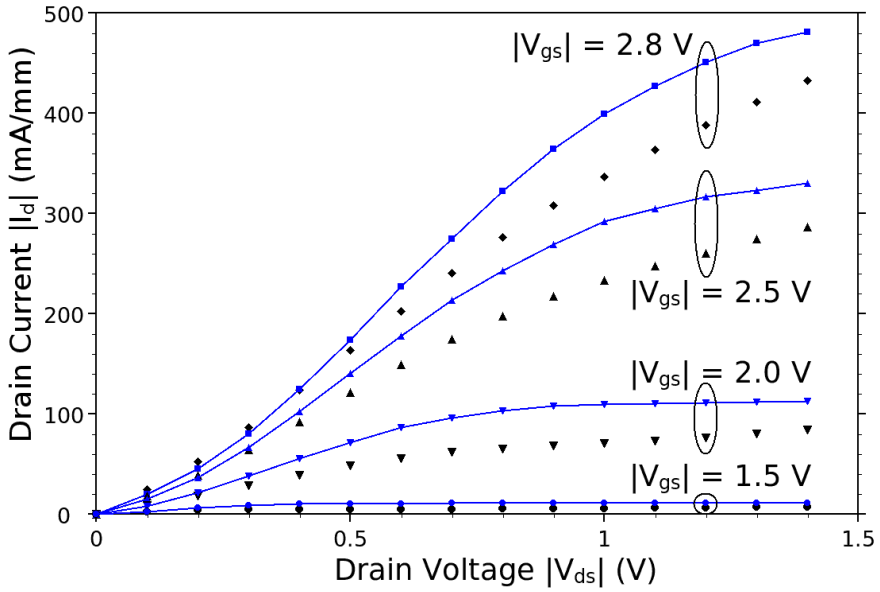

Figure 6.18: Output characteristic fit for high gate bias. Blue line: simulated. Black diamonds: measured.

The simulated output characteristics shown in Fig. 6.18 replicate the *sublinear effect* of SB-MOSFETs at low drain voltages, though this effect is more pronounced than in the measurement data. As well as that, the simulated drain current is consistently higher than the measured data, indicating an over-estimation of the tunneling current.

All in all, a reasonable fit of simulation to measurement is achieved using default values for most parameters, such as carrier mass and mobility. At low drain voltage, an under-estimation of the drain current is observed, whereas for high drain biases the simulated current exceeds measured data, suggesting that the manually incorporated

barrier lowering is too large and exaggerating the tunneling current contribution under high gate and drain voltages. This may be alleviated by either reducing the calculated barrier lowering coefficients at high bias voltages or altering the effective hole mass.

Chapter 7

Discussion and Conclusion

7.1 Summary

The electrical performance of SB-MOSFET devices, mostly of a written gate length of 85 nm, has been investigated under static and radio frequency conditions as well as at low temperatures. Each characterisation method extracts different performance properties and gives insight into the various unique capabilities of SB-MOSFETs compared to DSD counterparts. A two-dimensional simulation model has been created and fitted to experimental current-voltage data.

7.1.1 Electrical DC Characterisation

A series of variable temperature current-voltage measurements are used to extract the effective Schottky barrier height to holes at the source-to-channel interface. A slight increase in effective Schottky barrier height from 0.117 to 0.128 eV is observed for wafers receiving silicide anneals at temperatures of 500 and 550 °C, respectively.

Room temperature DC characterisation established p-channel SB-MOSFET device performance to be very competitive compared to conventional DSD MOSFETs and compatible with ITRS recommendations for high performance logic applications. High

ON currents up to 545 mA/mm and transconductances up to 640 mS/mm are measured.

The increasing effective Schottky barrier height for wafers with higher silicide anneal temperatures has a profound impact on static device performance. Devices annealed at 550 °C exhibit inferior drive currents and transconductances to devices annealed at 500 °C. A doubling of the retrograde channel implant dose from $5 \cdot 10^{12}$ to $1 \cdot 10^{13}$ cm^{-3} results in a threshold voltage increase of 70 mV and decreases in performance but improved device uniformity across the wafer.

Low temperature measurements to investigate the relative contributions of thermionic, thermionic-field and field emission establish reverse leakage to be due to field emission, the subthreshold regime to be dominated by thermionic emission and the ON state by thermionic-field and field emission, with field emission becoming increasingly dominant with increasing drain and gate voltages. At the relatively short gate length of 85 nm, the drain current is not found to be limited by the channel.

A constant drain current mobility extraction technique has been proposed and is applied to the measurement of the effective mobility in SB-MOSFETs. Resulting effective mobilities seem reasonable, but the lack of devices of different gate lengths makes its accuracy doubtful. The results represent a proof of concept for the technique.

7.1.2 Electrical RF Characterisation

Variations in contact properties between contacting attempts to probe to devices presents a major obstacle to the application of conventional deembedding techniques relying on measurement of dedicated on-wafer deembedding structures. This leads to variations in extracted electrical properties, as illustrated by the input capacitance C_{in}, of similar magnitude to the intrinsic SB-MOSFET device properties. Thus, possible variations in measuring deembedding structures may cause significant inaccuracies in extracted RF performance factors. By performing active and deembedding measurement

on the same structure without recontacting and applying the ColdFET deembedding technique, it is possible to extract RF performance factors with reasonable accuracy.

Unity-gain cut-off frequencies of up to 71 GHz have been extracted using a new *ColdFET deembedding* technique, representing an improvement of up to 61% over comparable bulk Si doped source/drain devices reported in the literature. The performance enhancement is attributed to high transconductance on wafers with low Schottky barriers and capacitance reduction due to carrier injection limitation at the source on wafers with high barriers. Absence of overlap capacitances and quantisation effects in the inversion layer are thought provide further reductions in gate-to-source capacitance and contribute to high-frequency performance enhancements.

The carrier transport properties of Schottky barriers lead to the observation that devices exhibiting inferior DC properties due to high source-channel barriers are capable of comparable high-frequency performance. This intriguing observation is attributed to reduced equivalent input capacitance, a result of restriction of charge entering the channel from the source for higher Schottky barrier devices, and is unique to SB-MOSFET devices. For RF applications, the properties of the source-to-channel Schottky barrier, specifically the barrier height, has very little impact on RF performance. This means that the Schottky barrier needn't be optimised for the barrier height, as is the case for DC performance.

7.1.3 2-D Modelling

The 2-D drift-diffusion simulation package MEDICI is employed to generate a two-dimensional model of SB-MOSFETs characterised previously to investigate their unique electrical characteristics. The approach taken is one of creating a simulation device structure based on known structural parameters and subsequently adjusting electrical parameters, specifically the channel doping profile, interface trap density, Schottky barrier

height and barrier lowering contributions, to generate a reasonable fit to measurement data.

The complex nature of SB-MOSFETs, in particular the electrical properties of the abrupt metal-semiconductor junctions, require a methodical approach to generate a fit. First, a mesh grid capable of capturing the rapid changes in electrostatic potential at such an interface is created. Then, the subthreshold regime is adjusted using a simulated retrograde channel doping profile and introducing interface traps to fit the threshold voltage.

Finally, the metal-semiconductor Schottky barrier height is modified to provide the final fit. However, the MEDICI simulation package is found to not apply Schottky barrier lowering to the tunneling model and therefore has to be calculated manually from the simulated horizontal electric field at the interface. This approach generates reasonable simulation fits to measured data and replicated typical SB-MOSFET features, such as the tri-slope transfer characteristics and the sublinear effect on output characteristics. The manually calculated barrier lowering resulted in effective barrier heights close to values obtained experimentally during DC characterisation.

7.2 Suggestions for Further Work

The first suggestion is to apply the constant-current mobility extraction technique using a constant drain current to devices of more gate lengths and a better gate oxide to enable direct split-CV measurement of inversion and depletion charge. This requires the fabrication of SB-MOSFETs with a considerably larger number and range of gate lengths than available in this work. The aim would be to confirm the accuracy of the constant-current mobility technique.

Additionally, there are still a number of simulations that can be performed. The final fit obtained with the MEDICI model developed in this work, shown in Fig. 6.16, 6.17 and 6.18, can surely be optimised. For example, performing simulations with reduced barrier lowering at high drain and gate voltages could result in an improved fit to measured data and may lead to a higher effective barrier height that is closer to the experimentally extracted values.

Moreover, the generality of the SB-MOSFET MEDICI model should be assessed by generating fits to results on the other characterised wafers against the known variables for them. Increasing the zero-bias barrier heights and fitting to results obtained on SBMOS2 #18, experimentally determined to have a slightly higher effective Schottky barrier height, would assess the model validity with respect to variations in metal-semiconductor Schottky barrier height. By performing simulations using a full-dose rather than a half-dose channel implant and comparing simulation results to experimental data from SBMOS2 #17 would determine the validity of the model with respect to channel doping.

Finally, by performing simulations at low ambient temperatures and comparing to measured low temperature I-V data could assess the model accuracy with respect to temperature as well as the relative current contributions made by thermionic, thermionic-field and field emission over the whole range of bias conditions.

Once the generality of this MEDICI model has been assessed, the simulator can then be used for making predictions for improving SB-MOSFET device performance and assist in future device fabrication. For example, the impact of the source-to-channel Schottky barrier height on drive current could be established and possible performance gains due to reductions in the barrier height may be possible as a result. In addition, the influence of the channel doping profile, e.g. by increasing/decreasing it beyond the two concentrations used in this work, can be investigated.

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