Electrical Characterisation of Novel Silicon MOSFETs and finFETs.

By

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Thesis

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This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. Except where specifically stated, all of the work described in this thesis was carried out by the author or under his direction.

Publications

Thomas, S. M., Whall, T.E., Parker, E.H.C., Leadley, D.R., Lander, R.J.P., Vellianitis, G., Watling, J.R. "Accurate effective mobility extraction in SOI MOS transistors." ULIS 2009: 10th International Conference on Ultimate Integration of Silicon

Thomas, S. M., Whall, T.E., Parker, E.H.C., Leadley, D.R., Lander, R.J.P., Vellianitis, G., Watling, J.R. "Improved effective mobility extraction in MOSFETs." Solid-State Electronics, 53(12): 1252-1256, 2009.

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Thomas, S.M., Prest, M.J., Whall, T.E., Beer, C.S., Leadley, D.R., Parker, E.H.C., Watling, J.R., Lander, R.J.P., Vellianitis, G. "Low temperature effective mobility measurements and modelling of high-κ gated Si n-MOS and p-MOS devices" ULIS 2010: 11th International Conference on Ultimate Integration of Silicon

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Donetti, L., Gamiz, F., **Thomas, S.M.**, Whall, T.E., Leadley, D.R., Hellstrom, P.-E., Malm, G., Ostling, M. "On the effective mass of holes in inversion layers" ULIS 2011: 12th International Conference on Ultimate Integration of Silicon

Further publications arising from this thesis are in preparation.

Abstract

To enable the advancement of Si based technology, necessary to increase computing power and the manufacture of more compact circuits, significant changes to the current planar transistor are a necessity. Novel transistor architectures and materials are currently being researched vigorously. This thesis, on the electrical characterisation of non-standard orientated MOSFETs and multi-gate transistors displays detailed insight into the carrier transport and resulting performance limiting mechanisms. The results are composed of three parts.

Firstly, the standard method of extracting carrier effective mobility from electrical measurements on MOSFETs is reviewed and the assumptions implicit in this method are discussed. A novel technique is suggested that corrects the difference in drain bias during current-voltage and capacitance-voltage measurements. It is further shown that the lateral field and diffusion corrections, which are commonly neglected, in fact cancel each other. The efficacy of the proposed technique is demonstrated by application to data measured on a quasi-planar SOI finFET at 300 K and 4 K.

The second part is based on the electrical characterisation of n+poly-Si/SiO_2/Si n- and p- MOSFETs fabricated on (100) and (110) substrate orientations with the full range of channel directions. In depth analysis of the electron and hole mobility was performed at 300 K and 4 K. The 4 K mobilities were modelled in terms of ionised dopant impurity, local SiO_2/Si interface charge and roughness scattering mechanisms. RMS (root mean squared) roughness values in the range $0.34-0.38$ nm and correlation lengths of $2.0-2.3$ nm were extracted revealing comparable interface quality between the (100) and (110) surfaces.

The third part examines the electrical characterisation of TiN/$HfSiO_2$/Si n- and p-finFETs. Fin top surface and sidewalls are in the (100) and (110) planes respectively. Fins have a height of 65 nm with widths in the range of 1872 nm (quasi-planar) to 12 nm. Detailed analysis revealed vertical compressive strain induced by the gate into the fin sidewalls, which enhanced the electron mobility by 60% above the (110) reference, whilst leaving the hole mobility unaffected. Qualitative analysis of the 4 K mobilities suggests that roughness is higher on the sidewalls than on the top surface. This was attributed to the damage caused by the dry etch, used to pattern the fins. A model for remote charge scattering at the $HfSiO_2$/SiO_2 interface was developed. 4 K mobilities from the quasi-planar n- and p-finFETs were then modelled in terms of remote charge, ionised dopant impurity, local SiO_2/Si interface charge and roughness scattering mechanisms. Remote charge densities of $8\text{x}10^{12}$ cm^{-2} were subsequently extracted. Scattering from these charges was shown to be the dominant scattering mechanism in the quasi-planar n-finFET mobility at 300 K.

List of Symbols

All symbols, abbreviations and acronyms have been defined in the text and are listed here for convenience. Note areal means "per area".

α	coefficient of proportionality/Maclaurin series expansion term of an exponential function
C	capacitance
C_0	offset capacitance
C_{acc}	areal accumulation capacitance
C_{BOX}	areal capacitance of buried oxide (BOX)
C_{dep}	areal depletion capacitance
C_{gb}	areal gate-body capacitance
C_{gc}	areal gate-channel capacitance
C_{gc}^{meas}	gate-channel capacitance
C_{gc0}	quasistatic or low frequency gate-channel capacitance
C_{hf}	areal high frequency capacitance
$C_{High\text{-}\kappa}$	areal capacitance of high-κ dielectric
C_{inv}	areal inversion charge capacitance
C_{it}	areal interface trap capacitance at the dielectric/Si interface
C_{it2}	areal interface trap capacitance at the Si/BOX interface
C_{lf}	areal low frequency capacitance
C_{ox}	areal gate oxide capacitance
C_{Si}	areal capacitance of silicon film
C_{SiO2}	areal capacitance of SiO_2 interfacial oxide
C_{tot}	total MOSFET capacitance
D	diffusion coefficient
D_{it}	density of interface traps
δ_z	remote charge delta distribution
Δ	rms fluctuation of interface roughness
ΔL	difference between the masked channel length and real channel length
e	electron charge
E	band edge energy
E_0	ground eigen-energy level
E_c	conduction band edge
E_{conf}	set of discrete energy levels (eigen-energies) associated with confinement
E_{eff}	effective field produced by V_{gs}
E_F	Fermi level (or Fermi energy)
E_{HH}	energy of the heavy hole sub-band
E_i	Intrinsic Fermi level
E_T	total energy of carrier

E_{tran}	energy of a free carrier parallel to the interface
E_v	valence band edge
E_x	electric field along the channel
ε_0	permittivity of free space
$\varepsilon(q)$	dielectric screening function
ε_d	diffusion energy
$\varepsilon_{High\text{-}\kappa}$	permittivity of a high-κ gate dielectric
ε_{ox}	permittivity of a gate dielectric/oxide
ε_{ox}^0	static (low frequency) permittivity of a gate dielectric (used in place of ε_{ox} when comparing to the optical permittivity)
ε_{ox}^∞	optical (high frequency) permittivity of a gate dielectric
ε_{Si}	(static) permittivity of Si
ε_{si}^∞	optical permittivity of silicon
ε_{SiO2}	permittivity of SiO_2
f	measurement frequency of AC voltage
$f(E,T)$	Fermi-Dirac distribution
$F(V_{gs})$	F-function
$F_z(\mathrm{V_{gs}})$	F-function
g_d	drain conductance
g_m	transconductance
$\mathrm{g_v}$	degeneracy
G	conductance
$G(q)$	local field correction in Hubbard's approximation
G_{it}	conductance associated with the loss of an interface trap
G_p	equivalent parallel conductance of interface traps
H_{fin}	fin height
$\hbar$	reduced Planck's constant
i	eigen-energy index
I	total current
I_0	sub-threshold current pre-factor
I_1	current through source and drain
I_2	current through substrate
I_c	quadrature current
I_c'	quadrature current after phase separator
I_d	on current/drain current in linear regime
$I_{diffusion}$	diffusion current component of drain current
I_{dm}	measured drain current in presence of significant gate leakage current
I_{drift}	drift current component of drain current
I_{dsat}	drain current in saturation
I_g	gate leakage current
I_p	in phase current
I_p'	in phase current after phase separator
k	Boltzmann constant
$\boldsymbol{k}$	carrier wavevector
$\boldsymbol{k'}$	carrier wavevector after scattering event

$\boldsymbol{k_F}$	Fermi wavevector
$\boldsymbol{k_x}$	wavevector along the channel (x direction)
$\boldsymbol{k_y}$	wavevector in y direction
$k_{\|\|}$	wavevector in transport plane
κ	MOSFET scaling factor/ dielectric constant/ ratio of diffusion to drift current
L	gate/channel length
L_D	Debye length
Λ	correlation length of interface roughness
m	effective mass
m_0	free electron mass
m_{conf}	effective mass in confinement direction
m_l	longitudinal electron effective mass
m_{scat}	average effective mass in channel plane
m_t	transverse electron effective mass
m_{tran}	effective mass in transport direction
$m_{tran,HH}$	effective mass in transport direction for HH sub-band
n	capacitor divider ratio/ number of fins
n_i	intrinsic carrier concentration
n_{imp}	impurity charge sheet density at dielectric/Si interface
n_r	remote charge sheet density
N_a	acceptor doping concentration
N_d	donor doping concentration
N_{dep}	total depletion charge density
N_{inv}	total inversion charge density
$N_{inv}(0)$	inversion charge density at the source
N_{poly}	doping concentration of a polysilicon gate
η	empirical factor referring to the averaging of the electric field over the carrier distribution in the inversion layer
P	power dissipation per MOSFET
ρ_{2D}	density of states in a sub-band
$\psi(z)$	band perturbation potential /electron wavefunction
ψ_b	potential in the bulk
ψ_c	potential in centre of fin
ψ_s	potential at semiconductor surface
$\boldsymbol{q}$	difference between wavevectors **k** and **k'**
q_s	Thomas-Fermi screening wave number
Q_{dep}	total areal depletion charge
Q_g	total areal gate charge
Q_{inv}	total areal inversion charge
$Q_{inv}(x)$	areal inversion charge at point x
Q_s	total areal charge in semiconductor
R	total MOSFET resistance
R_{ch}	channel resistance
R_d	drain resistance
R_{it}	resistance associated with interface trap loss

R_p	parallel resistance in equivalent circuit
R_s	series resistance in equivalent circuit/ source resistance
R_{sd}	total source and drain resistance
R_{sub}	substrate resistance
$S(q)$	power spectral density
S.S.	sub-threshold slope
$t_{high\text{-}\kappa}$	thickness of high-κ gate dielectric
t_{ox}	thickness of gate oxide
t_r	carrier transit time from source to drain
t_{Si}	thickness of silicon film
t_{SiO2}	thickness of SiO_2 interfacial oxide
T	Temperature
T_{fH}	stress component in fin height
T_{fL}	stress component along channel
T_{fW}	stress component in fin width
τ_{ch}	channel time constant
τ_{it}	interface trap time constant
τ_{sub}	substrate time constant
$\langle\tau\rangle$	mean free time
$\langle\tau_k\rangle$	momentum relaxation time
θ	scattering angle / phase angle (loss tangent)
$\langle\lvert U(q)\rvert^2\rangle$	average random potential of scattering mechanism
μ	carrier mobility
μ_{eff}	effective carrier mobility
μ_{IIS}	ionised impurity scattering limited mobility
μ_{LCS}	local Coulomb scattering limited mobility
μ_{LRS}	local roughness scattering limited mobility
μ_{RCS}	remote Coulomb scattering limited mobility
μ_{Tot}	total modelled mobility
v	carrier velocity along the channel
V	supply voltage
V(z)	potential well
V_{cs}	channel potential with respect to source
V_{ds}	drain bias
V_{fb}	flat-band voltage
V_{gs}	gate bias with respect to substrate
V_{gs0}	gate bias corresponding to C_0
V_{gt}	gate overdrive voltage (V_{gs}-V_t)
V_{ox}	Voltage across gate oxide/dielectric
V_t	threshold voltage
W	channel width
W_{dep}	depletion region width
W_{depm}	maximum depletion width
W_{fin}	fin width

ω	angular frequency
ω_{SO}	angular frequency of the interface longitudinal-optical phonon
x	distance along the channel x=0 at source x = L at drain
x_j	source/drain junction depth
X_c	reactance of capacitor in equivalent circuit
y	distance perpendicular to channel
Y	admittance
z	distance parallel to oxide interface
z_{av}	average distance of the inversion charge from the gate dielectric
ξ	chemical potential

Abbreviations and Acronyms

AFM	Atomic Force Microscopy
BOX	Buried OXide
CET	Capacitive Equivalent Thickness
CFM	Cubic Feet per Minute
CMOS	Complimentary Metal Oxide Semiconductor
CV	Capacitance-Voltage
EOT	Equivalent Oxide Thickness
FDSOI	Fully Depleted Silicon On Insulator
GV	Conductance-Voltage
HH	Heavy Hole
IIS	Ionised Impurity Scattering
LCS	Local Coulomb Scattering
LH	Light Hole
LO	Longitudinal Optical
LRS	Local Roughness Scattering
MOCVD	Metal Organic Chemical Vapour Deposition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OA	Orientated Angle
PDSOI	Partially Depleted Silicon On Insulator
PS	Phonon Scattering
RCS	Remote Coulomb Scattering
RF	Radio Frequency
RPS	Remote Phonon Scattering
RRS	Remote Roughness Scattering
RTA	Rapid Thermal Anneal
SIMOX	Separation by IMplantation of OXygen
SO	Split-Off/Surface Optical phonon mode
SOI	Silicon On Insulator
TEM	Transmission Electron Microscopy
TO	Transverse Optical
VLSI	Very Large Scale Integration

Chapter 1 : Introduction

1.1 Semiconductor industry

Invented 60 years ago, the metal-oxide-semiconductor-field-effect-transistor (MOSFET) is a key building block of today's digital world. Perhaps the most important invention of the 20th century, this electronic switch is the fundamental component in integrated circuits (also known as chips) which are found in nearly all electronic devices. CMOS (complimentary metal-oxide-semiconductor) technology, used in microprocessors, is comprised of pairs of n and p-type MOSFETs to carry out logic functions.

In 1975, Gordon Moore, co-founder of industry leader Intel, predicted that the number of transistors on a chip would double about every two years.[1] This is known as Moore's law. Moore's law has fuelled a technology revolution as the number of transistors integrated into microprocessor chips has exponentially increased for greater computing power. In 1971, the groundbreaking Intel 4004 processor contained 2300 transistors. At the end of 2009, Intel launched their Westmere processor containing over 1.9 billion transistors. Over the next decade, processors will contain 50-100 billion transistors.

1.1.1 Silicon

Silicon has formed the basis of the semiconductor industry, almost since its birth and has remained the material of choice since it superseded germanium, which was used to make the first transistors. Silicon has the advantages of being easily obtainable (comprising a quarter of the Earth's crust), therefore inexpensive. Secondly it has good physical properties that allow easy definition of complex device structures. Lastly its oxide is a very good electrical insulator and, unlike that of germanium, is insoluble in water which reduces processing complexity. These factors combine to provide a cheap platform on which to fabricate reliable MOSFETs.

1.2 CMOS scaling

1.2.1 Constant field/Dennard scaling

Historically, the increase in the number of transistors on a chip was achieved by scaling down the transistor's dimensions by a constant factor 1/κ. In accordance with Moore's law, $\kappa = \sqrt{2}$ was applied every two years when a new generation of chips was manufactured for the first time. This results in a chip with a greater functionality in the same area (or equivalently a chip with the same functionality in a smaller area). Since fabrication costs for a wafer are relatively fixed, the cost per transistor is reduced. Table 1.1 lists the MOSFET parameters and the effects of their scaling on the MOSFET and chip performance.

	MOSFET device and chip parameters	Scaling factor
Scaling parameters	Device dimensions (t_{ox}, L, W, x_j)	$1/\kappa$
	Substrate doping concentration (N_a/N_d)	κ
	Supply voltage (V)	$1/\kappa$
Derived device parameters	Electric fields	1
	Depletion-layer width ($W_{dep} \propto 1/\sqrt{N_a}$)	$1/\kappa$
	Gate oxide capacitance ($C_{ox} = WL\varepsilon_{ox}/t_{ox}$)	$1/\kappa$
	On current (I_d)	$1/\kappa$
	Intrinsic delay time ($C_{tot}V/I_d$)	$1/\kappa$
	Power dissipation ($P = VI_d$)	$1/\kappa^2$
Derived chip parameters	Transistor density ($\propto 1/WL$)	κ^2
	Power density or areal power consumption (P/WL)	1
	Clock/operating frequency ($I_d/C_{tot}V$)	κ

Table 1.1 MOSFET scaling parameters. The scaling factors are derived from constant field scaling. The key metric for MOSFET performance is the intrinsic delay time. C_{tot} is the total capacitance of the device which is composed of the gate oxide capacitance and source/drain junction and parasitic capacitances (adapted from [2])

The scaling factors are derived from constant field scaling whereby the vertical and horizontal electric fields in the MOSFET are kept constant. This is achieved by scaling down the supply voltage in proportion with the dimensions and scaling up the substrate doping concentration.[3] Note that in addition to the increased transistor density on a chip, the MOSFET intrinsic delay time is reduced, enabling the chip to operate faster (at a higher clock frequency) whilst the power density remains constant (i.e. lower power consumption per MOSFET).

1.2.2 Departure from constant field scaling

Scaling has become more challenging with each successive MOSFET generation, as fundamental technological and physical limits of existing processes and materials

are being reached. In particular the oxide thickness (or equivalently the areal oxide capacitance) and source/drain junction depths have ceased to be scaled in proportion with the channel length, resulting in the loss of electrostatic control of the channel by the gate. This has led to a new set of scaling rules and subsequently trade offs between on current (or drive current) and scalability. For example substrate doping concentration has to be scaled up further to reduce so called "short channel length effects", which prevent the gate abruptly switching the MOSFET off, and to reduce leakage current in the "off state". However high doping reduces carrier mobility thereby degrading the on current (increase in intrinsic delay time), reducing the operating speed of chips. Since it is desirable for chips to operate faster than the previous generation, scaling down of the supply voltage has been reduced to compensate and increase the on current. However, this increases the power density, resulting in chips running at increasingly higher temperatures. This has motivated research into increasing the conductivity of the MOSFET to increase the on current, at a lower supply voltage.

Constant field scaling ended in 2003 and since then numerous innovations have enabled the continuation of Moore's law. In 2003, Intel announced the integration of strained silicon to improve the on current of transistors in the 90 nm technology node.[4] In 2005 (65 nm node) the silicon dioxide gate dielectric had been scaled to a thickness of 1.1 nm.[5] Leakage current through it due to quantum mechanical tunnelling of electrons from the channel was now a serious issue. This led to it being replaced by a thicker high-κ (hafnium-based $\kappa \sim 20$) dielectric in conjunction with a

metal gate, partly due for compatibility, in 2008 (45 nm node)[6]. High-κ gate dielectrics, allow for an increase in the physical thickness of the gate dielectric, where the benefits of exponentially lowered leakage current density are achieved while the necessary gate oxide capacitance is attained. The change in process was no minor feat and has been hailed as the biggest advancement in transistor technology since the late 1960s, the result of years of research and development. Currently (32 nm node), state of the art chips use 4th generation strained silicon and 2nd generation high-κ /metal gate technology with transistor channel lengths of around 35 nm (same length used in the 45 nm node).[7] At the end of 2011, Intel's first 22 nm node processors will be in production, the details of which have not yet been released.

1.2.3 SOI

Silicon based scaling is predicted to continue beyond the 11 nm node (2017-18) with channel lengths of 12-18 nm expected. However, below channel lengths of 15-20 nm, the classic bulk MOSFET is expected to run out of steam.[8] Short channel effects and off state leakage current are expected to be severe, the latter causing unacceptably high idle power consumption.

The implementation of silicon-on-insulator (SOI) technology, already employed by IBM and AMD, is one of several strategies employed to follow Moore's law [9]. Fabricating MOSFETs on a layered thin silicon film-insulator-silicon substrate in place of a conventional silicon substrate helps the gate to retain electrostatic control

of the channel and provides numerous other advantages. Thus the film thickness is an additional parameter to the gate oxide for suppressing short channel effects and off state leakage current. This allows SOI MOSFETs to be scaled more aggressively than the classic bulk silicon MOSFET without requiring high substrate doping concentrations. To achieve good switch off characteristics, a silicon film thickness of about a quarter of the channel length is required. At the 22 nm node (late 2011-2012) channel lengths are expected to reach 25 nm, requiring a film thickness of ~6-7 nm.[8]

From a fabrication perspective, SOI substrates are compatible with most conventional processes. i.e. an SOI-based process may be implemented without modification of equipment or significant retooling of an existing fabrication plant. However, SOI substrates are far more expensive than conventional silicon substrates and as yet, Intel have managed to avoid using them though eventually the advantages they present may soon justify the cost.[10-11]

1.2.4 Multi-gate transistors – the finFET

By modifying the MOSFET architecture and using multiple gates, short channel effects and off state leakage current can be suppressed much more effectively than by using an SOI substrate. Multi-gate transistors, for example the tri-gate or finFET (figure 1.1) thus allow for further channel length scaling and may even supersede the SOI MOSFET. The distinguishing characteristic of the finFET is that the gate

straddles a thin, fin shaped body, forming three self-aligned channels along the top and vertical sidewall surfaces of the fin.

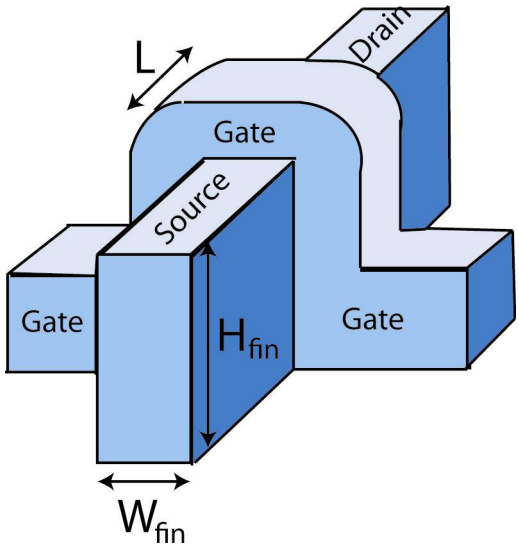

Figure 1.1 Schematic of a finFET. This novel 3D transistor is usually fabricated on an SOI substrate.

The use of three gates surrounding the fin ensures excellent electrostatic control. As the channel length is scaled down, short channel effects and off-state leakage current are suppressed by scaling down the width of the fin. Thus akin to the film thickness of an SOI MOSFET, the fin width is an additional scaling parameter to the gate oxide. The fin width should be roughly half the channel length, i.e. for the 22 nm node, a fin width of ~15 nm is required. Thus the width of the fin, which is defined by lithography, is the minimum dimension in a finFET. The vertical nature of a finFET provides a greater device width per wafer area, enabling finFETs to be packed more densely than planar MOSFETs.

However, fabrication of uniform narrow fins is one of the primary challenges in fabricating finFETs. Regarding the device performance, narrow fins create a high access resistance, reducing the on current. Another challenge is the implementation of high levels of strain into the fins to boost the on current. These issues will become increasingly important for successive finFET generations.

1.3 Current investigation

This thesis is an investigation into the electrical properties of silicon MOSFETs and finFETs. Emphasis is placed on extraction of carrier mobility, its physical interpretation and modelling. Such study is relevant to continue the advancement of silicon based technology.

Whilst there has already been substantial investment by industry giants in finFET technology, there are still a number of aspects that require further research. In particular a single strain configuration that benefits both n- and p-channel devices is highly sought after. Also a physical understanding of hole mobility on the different surfaces and in different channel directions is currently lacking. Mobility is usually extracted on long channel devices. However accurate extraction is becoming increasingly difficult due to high gate leakage in large area devices, high series resistance and absence of substrate contact in some SOI technology.

In chapters 2 and 3 the relevant background material to this investigation is covered, the latter chapter dealing with the necessary characterisation techniques.

Chapter 4 analyses the common assumptions that are so often blindly applied when extracting mobility. A novel extraction technique is proposed and applied to a quasi-planar SOI finFET.

In chapter 5, planar bulk MOSFETs fabricated on (100) and (110) substrate orientations are electrically characterised. New insights into the dependence of mobility on channel direction and surface orientation are obtained.

Chapter 6 presents original work on the electrical characterisation of state of the art strained silicon finFETs with high-κ dielectrics and metal gates.

In chapters 5 and 6 particular attention is on low temperature measurements (down to 4.2 K) from which the various mobility limiting scattering mechanisms are analysed.

Chapter 2 : Theoretical Considerations

2.1 The MOS capacitor

A MOS capacitor consists of a conducting metal layer (metal or heavily doped polysilicon) on top of a dielectric grown or deposited on a semiconductor substrate, the bulk of which can be doped n-type (p-MOS capacitor) or p-type (n-MOS capacitor). The operation of an n-MOS capacitor under gate bias, V_{gs} is now considered. All potentials are with respect to the substrate/bulk which is grounded. At zero applied bias, the bending of the energy bands, necessary to align the Fermi levels, E_F, of the gate and semiconductor, is ideally determined by the difference in the work functions of the metal and the semiconductor. (Band bending signifies a change in electric potential and therefore the existence of an electric field.) Oxide and interface trapped charges can also contribute to an appreciable amount of band bending. For simplicity of discussion, this is ignored here. Band bending changes with the applied bias and the bands become flat when we apply the so-called flat-band voltage to compensate for the difference in work functions. The Fermi level remains constant inside the semiconductor, independent of biasing conditions as there is no net current flow in the direction perpendicular to the interface owing to the very high resistance of the dielectric layer. Very little band bending occurs in the metal due to the abundance of free carriers. An n-MOS capacitor will enter the

accumulation regime of operation when the voltage applied between the metal and the semiconductor is more negative than the flat-band voltage ($V_{fb} < 0$). The negative bias raises the metal Fermi level (i.e. the electron potential energy) with respect to the semiconductor Fermi level and creates an electric field from the substrate, through the oxide (just like an ordinary parallel plate capacitor) into the gate. Electrons in the gate are displaced towards the semiconductor and holes in the semiconductor displaced towards the gate. Figure 2.1a) shows the energy bands in accumulation. The field in the semiconductor causes the bands to bend upward. The Fermi level at the surface is now much closer to the valence band than the Fermi level in the bulk, corresponding to a much higher hole concentration at the surface than the equilibrium hole concentration in the bulk.

When $V_{gs} > V_{fb}$, the capacitor will enter the depletion regime of operation. The positive bias lowers the metal Fermi level with respect to the semiconductor Fermi level. The electric field is now in the direction from the gate to the substrate. Holes in the semiconductor move away (depleted) from the interface, leaving a net negative charge from the acceptor ions. This is known as depletion charge. The bands in the semiconductor bend downwards. The valence band at the surface is now farther away from the Fermi level than the valance band in the bulk expressing the lower hole concentration at the surface than the equilibrium hole concentration in the bulk.

As V_{gs} increases, holes continue to be depleted from the interface leaving behind more acceptor ions resulting in more depletion charge and a wider depletion region. This continues until it becomes energetically favourable for electrons to populate the

conduction band at the surface. The process of electrons populating the conduction band at the surface in a p-type semiconductor is known as surface inversion and the surface behaves like an n-type material. The resulting sheet of electrons at the surface is referred to as the inversion layer. At this point all holes are depleted from the surface and the depletion charge ceases to increase. Figure 2.1b) shows the energy band diagram when the MOS capacitor is in the inversion regime. On the energy band diagram, the bands bend downward so much so, that the conduction band approaches the Fermi level expressing the much higher electron concentration. In the figure, the Fermi level at the surface is as far above the intrinsic level, E_i, as the Fermi level is below the intrinsic level in the bulk semiconductor. Thus the electron concentration at the surface is the same as the hole concentration in the semiconductor. This condition is known as the threshold inversion point and the corresponding gate voltage known as the threshold voltage, V_t. The additional field lines from the gate now terminate on the inversion charge rather than the depletion charge, thereby screening the semiconductor from any further band bending. When $V_{gs}>V_t$, we enter into strong inversion where more inversion charge will be generated whilst the band bending remains essentially constant.

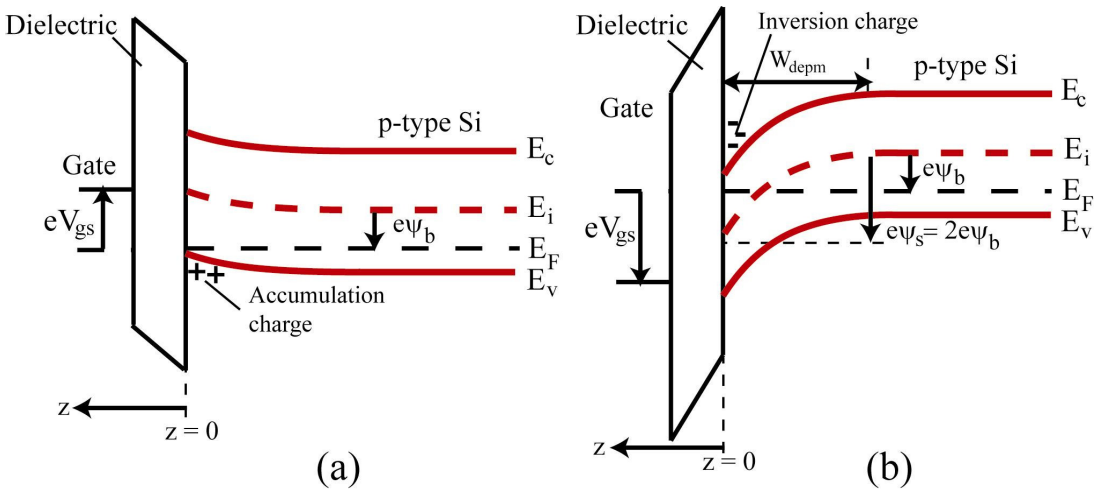

Figure 2.1a) n-MOS capacitor in accumulation and b) inversion

The gate voltage at inversion is related to the flat-band voltage, V_{fb}, voltage across the oxide, V_{ox} and the semiconductor ψ_s

$$V_{gs} = V_{fb} + V_{ox} + \psi_s = V_{fb} + \frac{Q_s}{C_{ox}} + \psi_s \qquad (2.1)$$

where C_{ox} is the areal oxide capacitance and Q_s is the areal total surface charge at the semiconductor-oxide interface, composed of the areal inversion and depletion charges, Q_{inv} and Q_{dep} respectively. It is common to express Q_{inv} and Q_{dep}, as inversion charge density N_{inv} and depletion charge density N_{dep} (normalised with respect to electron charge). We explicitly define ψ_s, the "surface potential", as the difference between the intrinsic Fermi-level (in V) at the surface and its bulk level. Note that the perturbations of the conduction band, valence band and intrinsic Fermi-level band are equal. The band perturbation potential as a function of distance perpendicular to the interface, $\psi(z)$ is a parabolic function. At the edge of the depletion region, $\psi(z = W_{dep}) = 0$. At the surface (z = 0) the band perturbation

potential is equal to the surface potential ψ (z = 0) = ψ_s. W_{dep} is the width of the depletion region. Integrating Poisson's equation from the bulk to the interface gives an expression for $d\psi(z)/dz$. Depending on the regime of device operation, certain terms will dominate allowing the expression to be simplified. From which;

$$W_{dep} = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0\psi_s}{eN_a}} \tag{2.2}$$

Where ε_{Si} is the semiconductor relative permittivity, e the electron charge, and N_a is the ionised acceptor concentration, which is normally approximately equal to the substrate doping concentration. The depletion charge per unit area is approximately:

$$Q_{dep} = eN_aW_{dep} \tag{2.3}$$

The surface potential at the onset of strong inversion:

$$\psi_s = 2\psi_b = 2\frac{kT}{e}\ln\left(\frac{N_a}{n_i}\right) \tag{2.4}$$

where the bulk potential $\psi_b = \frac{E_F - E_i}{e}$ as shown in Figure 2.1. n_i is the intrinsic carrier concentration, k the Boltzmann constant, T the temperature

When in inversion, the depletion region reaches its maximum width W_{depm};

$$W_{depm} = \sqrt{\frac{4\varepsilon_{Si}\varepsilon_0 kT\ln(N_a/n_i)}{e^2N_a}} \tag{2.5}$$

obtained by substituting eqn. (2.4) into eqn. (2.2)

At threshold, $Q_s = Q_{dep}$. Combining the equations above, V_t can be expressed in the following form;

$$V_t = V_{fb} + 2\psi_b + \frac{\sqrt{2\varepsilon_0\varepsilon_{Si}eN_a(2\psi_b)}}{C_{ox}} \tag{2.6}$$

2.2 The metal-oxide-semiconductor-field-effect-transistor

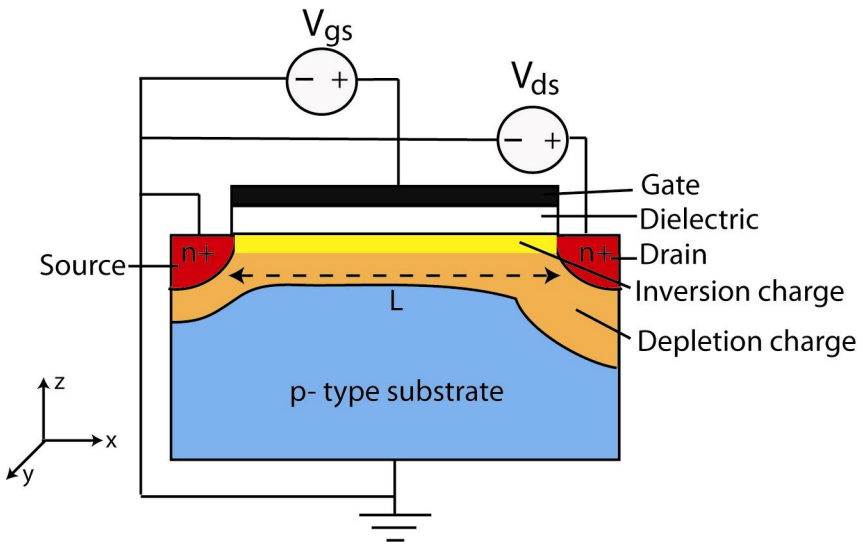

Figure 2.2 n-MOSFET schematic showing the electrical connections

A standard semiconductor MOSFET consists of a MOS capacitor with a highly doped source and drain region either side, each with a respective metal contact. An n-channel "enhancement mode" MOSFET has a p-type semiconductor and n+ source and drain regions and a p-channel MOSFET has a n-type semiconductor and p+ source and drain regions. Figure 2.2 is a schematic of an n-channel MOSFET including the electrical connections. Note the source and substrate are grounded. When $V_{gs} < V_t$, the p-type substrate is either in accumulation or depletion and no current can flow between the source and drain even when in the presence of the bias V_{ds}. The MOSFET acts like two back-to-back p-n junction diodes. When $V_{gs}>V_t$, the semiconductor surface is inverted to n-type, forming a conducting channel between the n+ source and drain. When V_{ds} is applied an electron current will flow from the source to the drain. Increasing the gate bias increases the concentration of electrons at the semiconductor surface, and allows more current to flow. The gate can

therefore be used to modulate the current flow between source and drain, giving rise to the switching operation in integrated circuits.

2.2.1 On state

As can be seen from Figure 2.2 the geometry of the MOSFET is different in the *x*,*y* and *z* directions. Therefore a proper analysis requires the study of charge flow in the three dimensions requiring complex numerical techniques. To simplify the description of effects within a MOSFET, the gradual channel approximation is commonly made. This assumes that the electric field along the channel, E_x of the MOSFET is much smaller than the vertical electric field and enables the use of the one-dimensional form of Poisson's equation. Thus W_{dep} at a point x along the channel is given by the potential at that point using the simple one-dimensional results in section 2.1. This approximation is good if the gate/channel length L is larger than the W_{dep}.

Under the charge-sheet approximation, it is further assumed that all the inversion charges are located at the semiconductor surface in a sheet, and there is no potential drop or band bending across the inversion layer. Thus it can be written:

$$Q_{inv}(x) = C_{ox}\left(V_{gs} - V_t - V_{cs}(x)\right) \tag{2.7}$$

where $V_{cs}(x)$ is the channel potential with respect to the source. $V_{cs} = 0$ at the source and $V_{cs} = V_{ds}$ at the drain. $x = 0$ at the source end and equal to L, at the drain end.

The electron flow in the channel, or drain current, I_d is a drift current caused by E_x;

$$I_d = \frac{Q_{inv} WL}{t_r} \tag{2.8}$$

where W is the channel width and t_r the carrier transit time. If the velocity of the carriers is constant between the source and drain;

$$t_r = \frac{L}{v} \tag{2.9}$$

where the carrier velocity along the channel, v, is related to E_x by the carrier mobility, μ, which for now is assumed to be constant and independent of E_x:

$$v = \mu E_x = \mu \frac{dV_{cs}(x)}{dx} \tag{2.10}$$

By combining equations (2.7)-(2.10):

$$I_d = C_{ox} \mu W \frac{dV_c}{dx} \left(V_{gs} - V_t - V_{cs}(x) \right) \tag{2.11}$$

By integrating from source ($x = 0$, $V_{cs}(0) = 0$) to drain ($x = L$, $V_{cs}(L) = V_{ds}$)

$$\int_0^L I_d \, dx = C_{ox} \mu W \int_0^{V_{ds}} \left(V_{gs} - V_t - V_{cs}(x) \right) dV_{cs} \tag{2.12}$$

The drain current is constant along the channel and for $V_{ds} << V_{gs} - V_t$, the final expression for I_d is obtained:

$$I_d = \mu \frac{W}{L} C_{ox} \left[\left(V_{gs} - V_t \right) V_{ds} - V_{ds}^2 / 2 \right] \tag{2.13}$$

This equation captures the basic on-state behaviour of a MOSFET, which starts at $V_{gs} \geq V_t$ and provided $0 < V_{ds} < V_{gs} - V_t$ the drain current increases linearly with V_{gs} since the quadratic term can be ignored.

This is called the linear region and is often simplified to:

$$I_d = \mu \frac{W}{L} C_{ox} \left[\left(V_{gs} - V_t \right) V_{ds} \right] \tag{2.14}$$

As V_{ds} is increased, I_d increases but Q_{inv} at the drain decreases (equation (2.7)) creating a non uniform distribution of Q_{inv} along the channel. Once $V_{ds} = V_{gs}$-V_t, Q_{inv} at the drain end of the channel reaches zero, creating a region of high resistance, and the channel is said to be pinched off. Further increase in V_{ds} results in an extension of the pinch-off point towards the source and the extra potential is dropped across this increasing resistance. The drain current remains essentially constant and the MOSFET is said to be in the saturation region.

The saturation current, I_{dsat}, is given by:

$$I_{dsat} = \mu \frac{W}{2L} C_{ox} \left(V_{gs} - V_t \right)^2 \text{ for } V_{ds} > V_{gs} - V_t \tag{2.15}$$

In equation (2.10), the carrier mobility μ was introduced as the proportionality coefficient in the dependence of drift velocity on the applied field. This was assumed to be constant to convey the basic physics of MOSFET operation. μ is dependent on the effective mass of the carriers which is calculated from the band structure of the semiconductor. In bulk silicon, μ = 1500 $cm^2V^{-1}s^{-1}$ for electrons and 450 $cm^2V^{-1}s^{-1}$ for holes at 300 K.[12] In a MOSFET channel however, μ is usually much smaller as carriers suffer collisions from various scattering sources (detailed in section 2.9). The average time between these collisions is known as the mean free time $\langle \tau \rangle$. Depending on the scattering source, a carrier may still have a net momentum in its direction prior to being scattered. The momentum relaxation time is the mean time

for a carrier to lose all its momentum via scattering. μ is related to the momentum relaxation time $\langle \tau_k \rangle$ and the effective mass in the transport direction, m_{tran};

$$\mu = \frac{e\langle \tau_k \rangle}{m_{tran}} \tag{2.16}$$

Since I_d is proportional to μ, higher μ corresponds to faster switching circuits instigating research into ways to decrease m_{tran} and increase $\langle \tau_k \rangle$.

2.2.2 Off state

Experimentally, Q_{inv} does not abruptly equal zero when $V_{gs} \leq V_t$. The transition from full depletion to strong inversion is in fact more gradual as there are mobile carriers in the channel even for sub-threshold V_{gs}. Their concentration is very small and rapidly decays as V_{gs} is reduced below V_t. Nonetheless they account for the gradual decay of I_d from above threshold toward zero. The current I_d, which exists for $V_{gs} \leq V_t$ is known as the sub-threshold current and occurs when the channel is weakly inverted corresponding to $\psi_b < \psi_s < 2\psi_b$. The electrons have to overcome the potential barrier formed by the n+ source and p-substrate. Consequently a diode-like exponential current-voltage equation is used to model the sub-threshold current;

$$I_d = \mu C_{ox} \frac{W}{L}(n-1)\left(\frac{kT}{e}\right)^2 e^{e(V_g - V_t)/nkT}\left(1 - e^{-eV_{ds}/kT}\right) \tag{2.17}$$

where $n = 1 + C_{dep}/C_{ox}$

A plot of $ln(I_d)$ as a function V_{gs} gives a linear behaviour in the sub-threshold regime. The reciprocal slope of this line is known as the sub-threshold slope, *S.S.*

which is a measure of the efficacy of V_{gs} in modulating I_d. A small sub-threshold slope (steep transition from off state to on state) is desirable for the ease of switching the transistor current off. Sub-threshold slope and its extraction is discussed in detail in section 3.4.1.

For a very small V_{gs}, the sub-threshold current is reduced to the leakage current of the source/drain junctions. This determines the off-state leakage current and therefore the standby power dissipation in CMOS circuits. High quality source and drain junctions are therefore an important requirement.

For further analysis of the MOS capacitor and MOSFET, the reader is referred to the texts by Taur and Ning[2], Dimitrijev[13] and Nicollian and Brews[14].

2.3 Si band structure

2.3.1 Conduction band

The effective mass of a carrier, m is calculated from the energy band structure E-**k** relationship using:

$$\frac{1}{m} = \frac{1}{\hbar^2}\frac{\partial^2 E}{\partial k^2} \tag{2.18}$$

where $\hbar$ is the reduced Planck's constant, **k** is the direction dependent wave vector and m is expressed in units of the free electron mass, m_0. For an analysis of carrier transport in the Si MOSFET inversion layer, accurate description of the E-**k** relationship near the conduction – or valence band minima (band-edges) is sufficient

providing E_x is low. The conduction band edge is composed of 6 degenerate minima located along the <100> directions (referred to as Δ minima). The constant energy surfaces of these minima are ellipsoids as shown in Figure 2.3.

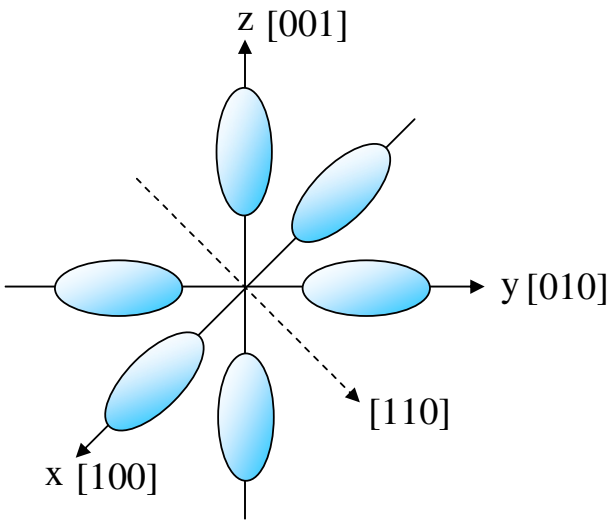

Figure 2.3 Constant energy surfaces of the conduction band minima

For a given direction, the minima can be approximated as parabolas enabling a constant effective mass to be assigned.[15] The mass along the symmetry axis of the ellipsoids (<100> directions) is called the longitudinal mass, m_l = 0.916m_0. The mass within the plane normal to the symmetry axis is the transverse mass, m_t = 0.190m_0. With regards to a MOSFET, typically the mass in the z direction, m_{conf}, the average mass in the *xy* plane, m_{scat} and the transport direction, m_{tran} are important when considering carrier transport. Note if the constant energy surface is a circle in the *xy* plane, the mass is independent of direction (isotropic) in this plane i.e. $m_{tran} = m_{scat}$.

2.3.2 Valence band

The valence band consists of three strongly interacting sub-bands: the heavy-hole band (HH); the light-hole band (LH); and the spin-orbit/split-off band (SO). The HH and LH bands are degenerate at the Brillouin zone centre (Γ point), 1.1 eV below the conduction band minima. The SO band is higher in hole energy, separated from the HH and LH by 44 meV. The LH and HH bands are anisotropic meaning the effective mass depends on crystallographic direction. The close proximity of the bands produces significant non-parabolicity of the variation of E with $\mathbf{k}$, especially in the HH case. The constant energy surface of the HH band can be visualized as a cube with dented in faces. With increasing energy, the dents become more pronounced. A detailed description of Si band structure is given by Kittel[16].

2.4 Carriers in the MOSFET inversion layer

In sections 2.1 and 2.2, the inversion layer was approximated as a 2D-sheet at the dielectric/channel interface. However, in order to study the physics of carriers within the inversion layer, we cannot make this approximation. In reality carriers are confined in a potential well formed by the dielectric barrier and the semiconductor minority carrier band edge, which bends down severely towards the interface due to the gate field. This gives rise to energy quantization and carriers are confined some distance away from the interface. Therefore for a precise description, a quantum mechanical approach has to be used. A good description is given in Dobrovolsky

and Litovchenko[17], with the pioneering work carried out by Stern and Howard[18], Stern[19] and Ando *et al.*[20]

2.4.1 Confinement

Quantum confinement splits the degeneracy of the energy bands. Carrier motion perpendicular (z direction) and parallel (xy plane) to the interface must now be considered separately and the respective energies calculated and summed to give the total allowed energy, E_T of a carrier;

$$E_T = E + E_{conf} + E_{tran} \tag{2.19}$$

where E is the classical energy of the band edge in a bulk 3D semiconductor, E_{conf} is a set of discrete energy levels associated with confinement and E_{tran} is the energy associated with free carrier motion parallel to the interface. For example:

$$E_{tran} = \frac{\hbar^2\left(k_x^2 + k_y^2\right)}{2m_{tran}} \tag{2.20}$$

where m_{tran} is isotropic in the xy plane.

Thus the total available energies of a carrier consist of parabolas/valleys with their minima coinciding with discrete energy levels, E_{conf}. These are known as sub-bands.

The values of the minima determine the occupation of the sub-bands. So before we can understand carrier transport along the channel, we must first understand the dependence of the energy levels on V_{gs}, more explicitly the electric field, and on the Si band structure in the confinement direction.

For an electron confined within the well, its wave function and allowable energies can be found by solving the 1D Schrödinger equation:

$$\left(-\frac{\hbar^2}{2m_{conf}}\frac{d^2}{dz^2}+V(z)\right)\psi(z)=E_{conf}\psi(z) \tag{2.21}$$

Here $\psi(z)$ is the electron wavefunction. The potential well can be modelled as an infinitely deep triangular well (the well known triangular well approximation).[19, 21] We assume that the potential barrier at the dielectric/semiconductor interface is infinite and the potential decreases linearly from the interface:

$$V(z)=-zE_{eff} \tag{2.22}$$

where E_{eff} is the effective field a carrier experiences. (calculation of E_{eff} is given in section 3.4.3)

Thus equation (2.21) can be solved to give the eigen-energies;[19]

$$E_{conf}=\left(\frac{\hbar^2}{2m_{conf}}\right)^{\frac{1}{3}}\left(\frac{3}{2}\pi eE_{eff}\left(i+\frac{3}{4}\right)\right)^{\frac{2}{3}} \tag{2.23}$$

where i = 0,1,2… This gives rise to a series of discrete energy levels, the separation of which increases with increasing E_{eff} and decreasing m_{conf}. We shall use equation (2.23) to gain a semi-quantitative understanding of the confinement effects in silicon starting with the conduction band, for an n-MOSFET, and then the valence band, for a p-MOSFET.

Conduction band

Figure 2.4 shows the orientation of the constant energy ellipsoids in the <100> direction. The two ellipsoids along the z direction have their longitudinal effective

mass perpendicular to the surface. So they respond to E_{eff} with their longitudinal mass, $0.916m_0$. The other four respond with the transverse effective mass, $0.190m_0$ because their transverse effective mass is perpendicular to the surface. Thus to calculate the eigen-energies, equation (2.23) has to be evaluated twice, once for $m_{conf} = m_l$ and again for $m_{conf} = m_t$. For both values, a series of eigen-energies will be obtained (i = 0,1,2..). Each set of eigen-energies, can be visualised as a ladder. In general sub-bands corresponding to the larger m_{conf} are called unprimed sub-bands and sub-bands from the other ladder are called primed sub-bands. Unprimed sub-bands are labelled E_0, E_1, E_2 etc. and primed sub-bands are labelled E_0', E_1', E_2' etc. E_0 is commonly referred to as the ground state and is the reference for the other sub-band energies. In this case unprimed sub bands have a degeneracy, g_v, of two as there are two ellipsoids in this group, (also commonly referred to as Δ_2 sub-bands) and the sub-bands of the primed ladder have a degeneracy of 4 (Δ_4 sub-bands). Most carriers will occupy the ground sub-band as it is lowest in energy. Therefore its corresponding value of m_{tran} is largely responsible in determining μ.

The density of states is constant for each sub-band and is given by

$$\rho_{2D} = \frac{g_v m_{scat}}{\pi \hbar^2} \tag{2.24}$$

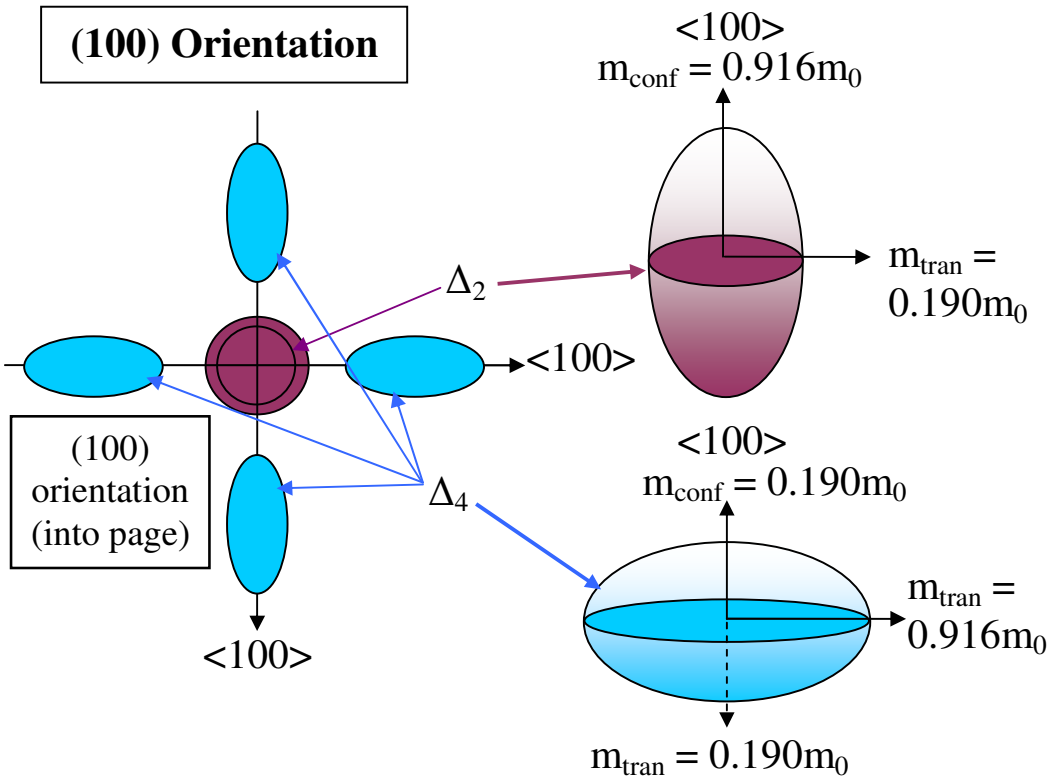

Figure 2.4 Constant energy surfaces of the Si conduction minima in the (100) plane.

Figure 2.5 shows the orientation of the constant energy ellipsoids in the <110> direction. Table 2.1 lists the various masses and degeneracy factors for the (100) and (110) wafer orientations. Note on the (110) orientation the unprimed sub-bands have a degeneracy of 4 and the primed sub-bands have a degeneracy of 2. Electron mobility is highest on the (100) wafer orientation. The reader is referred to chapter 5 for detailed analysis of the dependence of electron mobility as a function of direction on the (100) and (110) orientations.

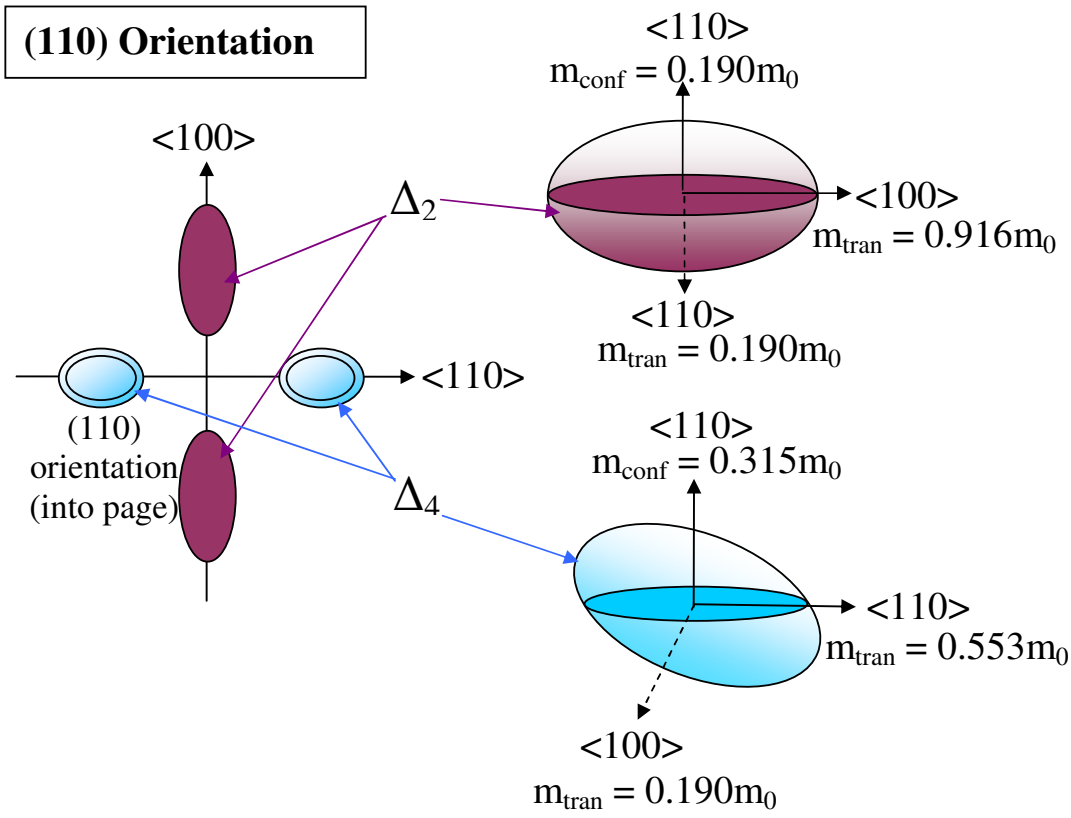

Figure 2.5 Constant energy surfaces of the Si conduction minima in the (110) plane.

Surface Orientation	<100> m_{tran}/m_0	<110> m_{tran}/m_0	m_{conf}/m_0	m_{scat}/m_0	g_v
(100)	0.190 0.190/0.916	0.190 0.315/0.553	0.916 0.190	0.190 0.417	Δ_2 Δ_4
(110)	0.190 0.916	0.553 0.190	0.315 0.190 (Modulated by confinement)	0.324 0.417	Δ_4 Δ_2

Table 2.1 Electron effective masses[22-23]

Uchida *et al.*[24] shows that the conduction band in the <110> direction, i.e. the quantization direction for a (110) wafer, is non-parabolic, especially for energies larger than 0.1 eV above the conduction band minima. This is shown in Figure 2.6.

Under confinement, the Δ_2 ground sub-band exceeds this energy and only becomes occupied when $N_{inv} > 2x10^{12}$ cm^{-2}. (Here Uchida *et al*. analyse with respect to N_{inv} rather than E_{eff}) Thus, m_{conf} of the Δ_2 sub-bands is heavier because of the "non-parabolicity". Figure 2.7 shows the resulting decrease in energy splitting between the Δ_2 and Δ_4 sub-bands as a function of N_{inv}.[22, 24-25]

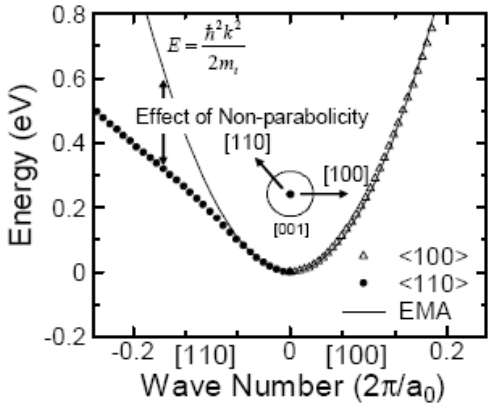

Figure 2.6 Conduction band E-k relation showing the non-parabolicity in the [110] direction. EMA: constant Effective Mass Approximation (sourced from [24])

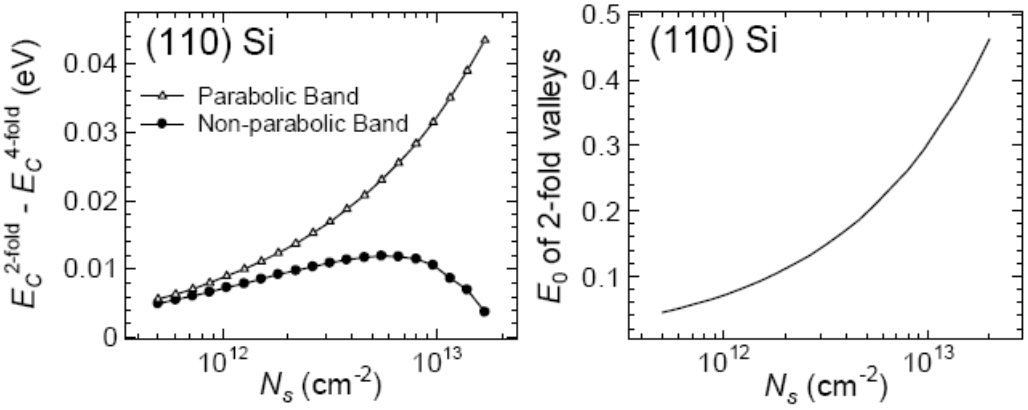

Figure 2.7a) Energy splitting of the Δ_2 and Δ_4 sub-bands b) Ground Δ_2 sub-band energy as a function of inversion charge density (N_s in this figure). (sourced from [24])

Valence band

Figure 2.8 shows 2D schematics of the constant energy surfaces for the lowest lying HH, LH and SO sub-bands. With increasing N_{inv}/E_{eff}, carriers occupy higher energies and the energy surfaces change shape. Due to the complex nature of the valence band, accurate calculations of the various effective masses as a function N_{inv}/E_{eff} require repeated solutions of the **k•p** equation and Poisson's equation. This is computationally very expensive requiring large computer resources.[26-28] As a result, substantial simplifications have to be made. Techniques to compute the valence band structure with greater accuracy, for use in Monte Carlo simulations of hole transport, are continuously being developed.[29-31] For experimental interpretation of mobility and other device measurements, single values of m_{tran}, m_{scat} and m_{conf}, calculated at $\mathbf{k} = 0$ (i.e. at a very low N_{inv}/E_{eff}) are widely used. Values reported for the (100) and (110) substrate orientations in the literature are shown in Table 2.2. Under confinement the split-off sub-band is increased further in energy beyond the HH and LH sub-bands and can be ignored as it is scarcely populated. To the author's knowledge, no values for m_{scat} or m_{tran} have been published for the (110) orientation. For the (100) orientation, the HH and LH sub-bands respond to E_{eff} with effective masses $0.29m_0$ and $0.20m_0$ respectively. In comparison to the conduction band in this orientation, a relatively small splitting occurs due to the small difference in m_{conf}.

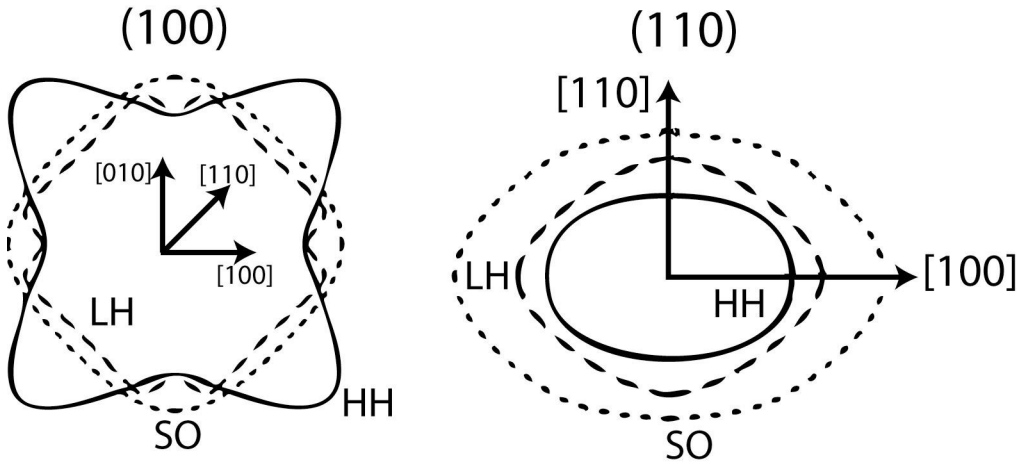

Figure 2.8 Constant energy surfaces of the lowest lying HH, LH and SO sub-bands in the (100) and (110) surface orientations. (adapted from [29])

Surface Orientation	m_{tran}/m_0 <100>	m_{tran}/m_0 <110>	m_{scat}/m_0	m_{conf}/m_0	Sub-band
(100)	0.28 (Saito *et al.*[32])	0.58 (Saito *et al.*)	0.43 (Takagi *et al.*[33])	0.29 (Takagi *et al.*)	HH
	0.20 (Saito *et al.*)	0.15 (Saito *et al.*)	0.17 (Takagi *et al.*)	0.20 (Takagi *et al.*)	LH
(110)				0.50, 0.59 (Mizuno *et al.*[34], Saitoh *et al.*[35])	HH
				0.15 (Saitoh *et al.*)	LH

Table 2.2 HH and LH effective masses of Si. No values for (110)/<100> and <110> have been reported

Hole mobility is highest along the <110> direction on the (110) wafer orientation. The reader is referred to chapter 5 for detailed analysis of the dependence of hole mobility as a function of direction on (100) and (110) orientations.

2.5 Carrier scattering in the inversion layer

We now consider some of the scattering mechanisms that degrade the carrier mobility along the channel, namely Coulomb scattering from charge at the dielectric/Si channel interface, Coulomb scattering from ionised dopants in the substrate and scattering from a non-uniform dielectric/Si interface. In each case, the most simplistic analysis is presented where all carriers are confined to the ground sub-band (the electrical quantum limit), where T = 0 K. This greatly simplifies scattering analysis as all carriers are represented by the same wavefunction. At T = 0 K, the Fermi distribution is a step function where states below E_F are completely filled and states above E_F are empty. This is known as a degenerate distribution or degenerate gas in the case of an inversion layer. We approximate this condition by cooling to 4.2 K where typically;

$$E_F > kT \tag{2.25}$$

Due to the finite temperature, states around E_F will be partly filled and therefore only these are important as far as transport is concerned. Therefore only scattering at E_F need be considered.

Not considered in the following sub sections is scattering by lattice vibrations. Such vibrations are caused by thermal agitation of the lattice which disrupts the periodicity of the crystal, creating disorder. Lattice vibrations are much like the vibrations of a harmonic oscillator such the energy of each normal mode must be quantised. The quantum of energy is viewed as a particle called a phonon. Phonons can be thought of as particles which propagate through the crystal with well defined energy and momentum. It is possible for carriers to emit or absorb phonons. The degree of phonon scattering depends on the number of phonons present which is a strong function of temperature. Therefore at very low temperatures phonon scattering can be neglected.

In the electrical quantum limit, we are able to relate the measurable, N_{inv} to the Fermi wavevector, $\mathbf{k_F}$ and Fermi energy, E_F. Using equation (2.24);

$$N_{inv} = \int_0^{E_F} \rho_{2D} dE = \int_0^{E_F} \frac{g_v m_{scat}}{\pi\hbar^2} dE \tag{2.26}$$

$$E_F = \frac{\pi\hbar^2}{g_v m_{scat}} N_{inv} \tag{2.27}$$

For an isotropic mass in the *xy* plane, equation (2.20) can be written;

$$E_F = \frac{\hbar^2 k_F^2}{2m_{scat}} \tag{2.28}$$

Equating equations (2.27) and (2.28) gives;

$$k_F = \left(\frac{2\pi N_{inv}}{g_v} \right)^{\frac{1}{2}} \tag{2.29}$$

Computations show the electrical quantum limit is valid for electrons and holes on a (100) orientation at T = 77 K.[36] However, it is common to make this approximation at 300 K.[37-38]

2.5.1 Scattering theory

In the following theory, equations are given in SI units. The Stern-Howard[18] wavefunction for carriers in the ground sub-band of a triangular well given is by;

$$\psi(z) = \left[\frac{b^3}{2}\right]^{\frac{1}{2}} z \exp\left(-\frac{bz}{2}\right) \tag{2.30}$$

where

$$b = \left(\frac{12e^2 m_{conf}}{\hbar^2 \varepsilon_0 \varepsilon_{Si}}\left(\frac{11}{32}N_{inv} + N_{dep}\right)\right)^{\frac{1}{3}} \tag{2.31}$$

The average distance of the inversion charge from the dielectric can be estimated using;

$$z_{av} = \frac{3}{b} \tag{2.32}$$

Note the larger m_{conf}, the smaller z_{av} i.e. the nearer the carriers are, on average, to the dielectric.

Lets consider the case where a electron with wave vector **k** is elastically scattered by some disorder to **k'** as shown in Figure 2.9. Conservation of energy requires that the wave vectors before and after the collision have the same magnitude, so the vectors lie on a circle in **k**-space.

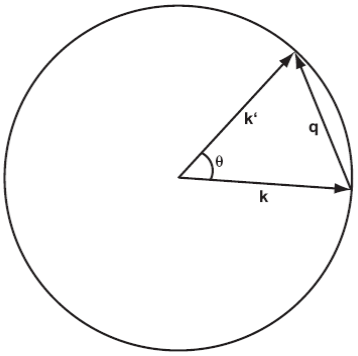

Figure 2.9 Elastic scattering event where k = k' (sourced from [39])

From simple trigonometry;

$$q^2 = k^2 + k'^2 - 2kk'\cos(\theta) \tag{2.33}$$

Provided momentum is conserved i.e. **k = k'** and considering scattering takes place at E_F with wave vector $\boldsymbol{k_F}$ we can write;

$$q = 2k_F \sin\left(\frac{\theta}{2}\right) \tag{2.34}$$

Ando *et al.*[20] give the scattering rate as;

$$\frac{1}{\tau_k} = \frac{m_{scat}}{2\pi\hbar^3}\int_0^{2\pi}\frac{\left\langle |U(q)|^2 \right\rangle}{\varepsilon(q)^2}(1-\cos(\theta))d\theta \tag{2.35}$$

$\left\langle |U(q)|^2 \right\rangle$ is the average random potential and contains the relevant information pertaining each scattering mechanism. $\varepsilon(q)$ the dielectric screening function defined later. $(1-\cos\theta)$ is a weighting factor to account for change in momentum in the x direction.

2.5.2 Local Coulomb scattering (LCS)

Within the gate dielectric, a variety of fabrication induced charged impurities are present. Depending on their proximity to the interface, they can scatter carriers in the inversion layer via the Coulomb force. At the Si/dielectric interface, the termination of the Si lattice creates states with energies distributed throughout the Si band-gap. Such states are called interface states or interface traps. These states can capture electrons from the conduction and valence bands and thus become charged depending on V_{gs} and the nature of the state. States in the top half of the band-gap are acceptor-like (neutral when unoccupied by an electron) and states in the bottom half donor-like (neutral when occupied by an electron). The probability of occupation of a state by an electron is determined by its energy relative to E_F, states below which are occupied. Since the energy of a state is fixed relative to the Si band edges, its occupancy can change depending on band bending. In the case of a n-MOSFET in strong inversion, the charged interface states are negatively charged acceptors. In the case of a p-MOSFET in strong inversion, the charged interface states are positively charged donors. These two cases are shown in Figure 2.10.

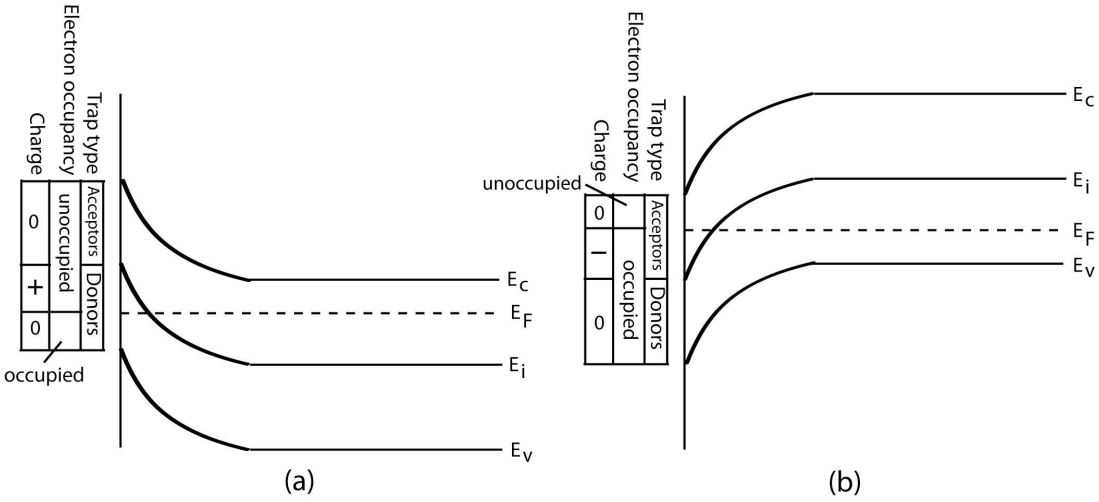

Figure 2.10 Charged interface states in strong inversion for a (a) p-MOSFET and an (b) n-MOSFET

A detailed description of the types of charges in a SiO_2 gate dielectric is given in Taur and Ning[2].

A quantitative treatment of scattering from charged impurities has been given by Gold and Dolgopolov[40]. The random potential representing the interaction of a 2D gas with a sheet of impurities is

$$\left\langle \left|U(q)\right|^2 \right\rangle = n_{imp}\left(\frac{e^2}{2\varepsilon_{Si}\varepsilon_0}\frac{1}{q}\right)^2 \left[F_i(q)\right]^2 \tag{2.36}$$

where n_{imp} is the impurity charge sheet density at the dielectric/Si interface and $F_i(q)$ is a form factor

$$F_i(q) = \left(1+\frac{q}{b}\right)^{-3} \tag{2.37}$$

This scattering mechanism is referred to as local Coulomb scattering (LCS) due to its proximity to the channel to distinguish it from remote Coulomb scattering (RCS) which is considered in section 2.6.5.

2.5.3 Local roughness scattering (LRS)

Any deviation from an abrupt dielectric/Si interface causes a change in the width of the quantum well, which in turn, gives rise to variation in the eigenenergies. If such roughness is located at random sites across the interface, then the perturbation of the energy levels constitutes an effective scattering mechanism for carriers confined along the interface. Interface roughness scattering is most effective at high N_{inv}/E_{eff} where carriers are confined close to the rough interface. We will refer to roughness scattering at the dielectric/Si interface as local roughness scattering (LRS). Roughness is characterized by two parameters; Δ the rms fluctuation in z from the mean position of the interface (z = 0) and Λ, the correlation length of the roughness oscillations in the *xy* plane.

Despite 40 years of research, it is fair to say that the morphology of the SiO_2/Si interface is still under debate. The morphology of the roughness is described by the power spectral density $S(q)$ which is related to the random potential by;

$$\left\langle \left|U(q)\right|^2 \right\rangle = q_s^2 E_F^2 \left(1 + 2N_{dep}/N_{inv}\right)^2 S(q) \tag{2.38}$$

A Gaussian morphology, first proposed by Ando *et al.*[20], was adopted as the standard means of characterising roughness, in the absence of actual structural data. The Gaussian random potential is[40]

$$\left\langle \left|U(q)\right|^2 \right\rangle = \pi\Delta^2\Lambda^2 q_s^2 E_F^2 \left(1 + 2N_{dep}/N_{inv}\right)^2 e^{-q^2\Lambda^2/4} \tag{2.39}$$

Later Goodnick *et al.*[41] studied roughness at a (100) SiO_2/Si interface using TEM (transmission electron microscopy) and found that an exponential model was more suitable. The exponential random potential is given by[36];

$$\left\langle \left|U(q)\right|^2 \right\rangle = \pi\Delta^2\Lambda^2 q_s^2 E_F^2 \left(1 + 2N_{dep}/N_{inv}\right)^2 \Bigg/ \left[1 + \left(\frac{\Lambda^2 q^2}{2}\right)\right]^{\frac{3}{2}} \tag{2.40}$$

Both models continue to be used and intermediary models have been proposed by some groups[36, 38, 42]. Pirovano *et al.*[36, 43] put forward the argument that physical characterization techniques are not sensitive enough to measure interface roughness. They argue that the choice between the two spectral shapes cannot be made relying on high resolution TEM and AFM measurements. Even if the roughness was measured accurately, such microscopy techniques are not able to sense the surface potential which enters into scattering calculations. By generating 1D random spatial patterns from Gaussian and exponential models, they show that the Gaussian surface is compatible with the dimensions of lattice steps at the Si<100> surface. On the contrary, the surface described by the exponential model shows spikes on distances shorter than the lattice steps. They argue that it is unlikely that the potential perturbing the carrier motion at the interface can feature such high-

frequency components, thereby concluding a Gaussian model is more accurate. Following the argument of Pirovano *et al*., a Gaussian model is used in this work.

2.5.4 Ionised impurity scattering (IIS)

The ionised donors or acceptors that make up the depletion region in a MOSFET scatter carriers in the inversion layer via the Coulomb force. We adopt the model used by Ando *et al*.[20] and Karavolas[44], originally formulated by Stern and Howard[18]. Similar to LCS, the random potential for IIS is;

$$\left\langle \left|U(q)\right|^2 \right\rangle = N_a \left(\frac{e^2}{2\varepsilon_{Si}\varepsilon_0} \frac{1}{q} \right)^2 \left[F_i(q, z_i)\right]^2 \tag{2.41}$$

this time we assume a uniform ionised doping concentration, N_a (or N_d for a p-MOSFET) and use the form factor;

$$F(q, z_i) = \frac{1}{2}\left(1 + \frac{\varepsilon_{SiO2}}{\varepsilon_{Si}}\right) P(z_i) + \frac{1}{2}\left(1 - \frac{\varepsilon_{SiO2}}{\varepsilon_{Si}}\right) P_0 e^{-qz_i} \tag{2.42}$$

where

$$P(z_i) = \frac{b^3}{(b-q)^3}\left[e^{-qz} - \left(a_0 + a_1 z + a_2 z^2\right)e^{-bz}\right] \tag{2.43}$$

$$a_0 = \frac{2q\left(3b^2 + q^2\right)}{(b+q)^3} \tag{2.44}$$

$$a_1 = \frac{4bq(b-q)}{(b+q)^2} \tag{2.45}$$

$$a_1 = \frac{q(b-q)^2}{(b+q)} \tag{2.46}$$

$$P_0 = \frac{b^3}{(b+q)^3} \tag{2.47}$$

We now not only integrate over θ but over W_{depm};

$$\frac{1}{\tau_k} = \frac{m_{scat}}{\pi\hbar^3} \int_0^{W_{depm}} dz \int_0^{2\pi} d\theta \frac{\left\langle |U(q)|^2 \right\rangle}{\varepsilon(q)^2} (1-\cos(\theta)) \tag{2.48}$$

2.5.5 Screening

In this section we define the screening parameters used in the previous sections. Although perturbations in the potential lead to scattering events, carriers can rearrange themselves, lowering their overall energy and so screen these fluctuations. The dielectric function is given as

$$\varepsilon(q) = 1 + \frac{q_s}{q} F(q)[1 - G(q)] \tag{2.49}$$

where q_s is the Thomas-Fermi screening wave number

$$q_s = \frac{g_v m_{scat} e^2}{2\pi\varepsilon_0 \varepsilon_{Si} \hbar^2} \tag{2.50}$$

F(q) is the form factor to take account of the finite extension of the electron wave function from the interface;

$$F(q) = \frac{\frac{1}{2}\left(1 + \frac{\varepsilon_{SiO2}}{\varepsilon_{Si}}\right)\left(1 + \frac{9}{8}\frac{q}{b} + \frac{3}{8}\frac{q^2}{b^2}\right)}{\left(1 + \frac{q}{b}\right)^3} + \frac{\frac{1}{2}\left(1 - \frac{\varepsilon_{SiO2}}{\varepsilon_{Si}}\right)}{\left(1 + \frac{q}{b}\right)^6} \tag{2.51}$$

G(q) is the local field correction in Hubbard's approximation;

$$G(q) = \frac{1}{2g_v} \frac{q}{\left(q^2 + k_F^2\right)^{\frac{1}{2}}} \tag{2.52}$$

2.6 MOS dielectrics

Presented in this section is a brief review of gate dielectrics/oxides pertinent to the results in chapter 6. For a detailed discussion on nearly every aspect of SiO_2 and high-κ gate dielectrics, the reader is referred to the excellent books by Huff and Gilmer[45] and Houssa[46]. The review papers by Robertson[47-48] also provide a good comprehensive overview. In this thesis ε_{ox} is used to denote the permittivity/dielectric constant of a dielectric in general (be it SiO_2 or a high-κ dielectric). The 'κ' or 'K' in high-κ dielectric are just alternative notations of permittivity.

2.6.1 Origin of permittivity

A dielectric is an electrical insulator that may be polarised by the action of an applied electric field. When a dielectric is placed in an electric field, electric charges do not flow through the material, as in a conductor, but only slightly shift from their average equilibrium positions causing polarisation- positive charges are displaced in the direction of the field and negative charges displaced in the opposite direction. This creates an internal electric field which opposes the applied field inside the dielectric. The dielectric constant, or permittivity, of an insulator is a relative measure of its polarisability which depends upon its composition and crystal

structure. The total polarisability may usually be separated into three parts: electronic, ionic and dipolar. The electronic contribution arises from the displacement of the electron shell relative to a nucleus. The ionic contribution comes from the displacement of a charged ion with respect to other ions. The dipolar polarisability arises from molecules with a permanent electric dipole moment that can change orientation in an applied electric field.[16] Each of these contributions takes a finite amount of time to respond to the applied field. Thus if the field is oscillating, the contribution of each of these polarisabilities depends on frequency therefore so does the permittivity. Typically a static (low frequency) dielectric constant, ε_{ox}^{0} and an optical (high frequency) dielectric constant, $\varepsilon_{ox}^{\infty}$ are quoted for a dielectric. Metal-oxides have a much higher static dielectric constant compared to SiO_2 which was historically used for the gate dielectric. The static dielectric constant of a metal oxide results from the contribution of ionic and electronic polarisation. Electronic polarisation is roughly inversely proportional to the square of the band gap. Insulators, by definition, have large band gaps so the large dielectric constant stems from a larger ionic polarisation, due to highly polarisable (soft) metal-oxygen bonds. The optical dielectric response is mainly electronic since heavier and slower ions cannot respond fully at high frequencies. As a result it is usually much less than the static response and not too different from that of SiO_2. This yields a large difference between ε_{ox}^{0} and $\varepsilon_{ox}^{\infty}$. In contrast, SiO_2 has weakly polarisable (hard) covalent silicon-oxygen bonds resulting in its small static dielectric constant of 3.9 and optical dielectric constant of 2.5.[49]

2.6.2 Dielectric requirements

SiO_2 is an excellent gate insulator as it has a band gap of 9 eV that is well centered around silicon's bandgap of 1.1 eV thereby providing a high barrier for electrons and holes. Unfortunately, the band gaps of many of the high-κ oxides of interest are considerably less than the 9 eV of SiO_2 as shown in Figure 2.11. The barrier heights (band offsets) at both the valence and conduction band must be over about 1 eV to prevent significant gate leakage current.[47]

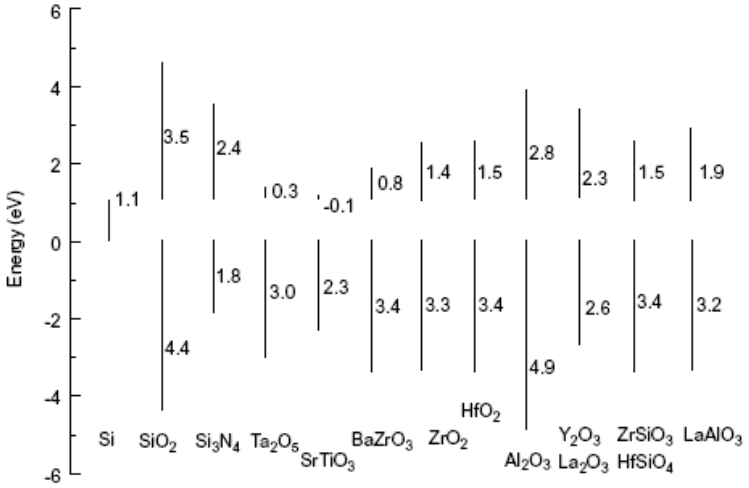

Figure 2.11 Conduction and valence band offsets of various dielectrics with respect to Si band-gap. (sourced from [50])

Unfortunately band gap tends to vary inversely with κ as shown in Figure 2.12.

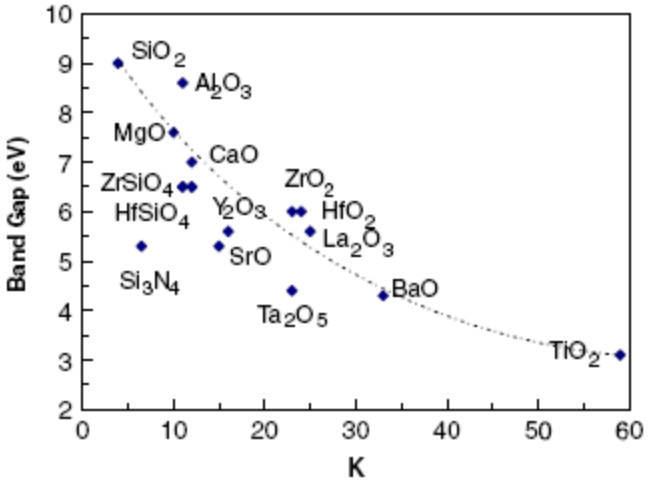

Figure 2.12 Band-gap energy as a function permittivity for a range of dielectrics [48].

In addition to having a high enough permittivity and sufficiently large band offsets to act as barriers for electrons and holes, there are a number of other requirements for the dielectric to act as a satisfactory gate insulator. It must be thermodynamically stable in contact with the substrate and have a low defect density not only within the material but also ideally at its interface with the substrate and gate, to prevent the degradation of MOSFET electrical properties (i.e. μ, *S.S.*, V_t instability). Depending on the process flow, it may also have to withstand high annealing temperatures necessary for dopant activation.[45] In the standard CMOS process flow, after the gate dielectric is grown or deposited there are various ion implantation steps in which dopants are implanted into the silicon substrate. These dopant ions do not participate in conduction of carriers until they are activated (made to occupy substitutional lattice sites). Activation is done via a process known as rapid thermal annealing (RTA). The wafers are placed in a furnace that reaches temperatures of 1000 °C-1050 °C in seconds. The wafers are held at that temperature for ~5 seconds and then cooled rapidly.

2.6.3 Capacitance of high-κ dielectrics

C_{ox} is related to its thickness, t_{ox} and permittivity by

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox}} \tag{2.53}$$

i.e. an oxide with a higher dielectric constant allows the use of a physically thicker layer but with the same capacitance per unit area as that required by SiO_2. This is called the equivalent oxide thickness (EOT). When dealing with high-κ dielectrics it is more instructive to interpret EOT as the thickness of SiO_2 that would be required to achieve the same areal capacitance as the high- κ material in consideration.

$$EOT = \varepsilon_{SiO2}\frac{t_{High-\kappa}}{\varepsilon_{High-\kappa}} \tag{2.54}$$

where $t_{high-\kappa}$ and $\varepsilon_{High-\kappa}$ are the thickness and relative dielectric constant of the high-κ material, respectively. Accounting for the inversion layer not being confined exactly at the interface, we get the capacitive equivalent thickness (CET). The CET of a dielectric is often quoted as it is calculated from a capacitance measurement of a MOS capacitor or MOSFET in strong inversion.[45]

An interfacial layer of SiO_2 often exists between the Si channel and the high-κ layer. This can be intentional or unintentional. Many high-κ dielectrics have thermally unstable interfaces with Si which results in the thin interfacial layer growing between the high-κ layer and the silicon. This is caused by the diffusion of oxygen from the high-κ oxidising with the silicon substrate during the activation anneal rather than during the high-κ deposition. Oxygen diffusion can be reduced by alloying the high-κ with SiO_2 as the silicon atoms are covalently bonded to oxygen.

Addition of nitrogen can also be used to lower diffusion rates further. From a scaling point of view, interfacial layers are undesirable as they lower the achievable oxide capacitance i.e. the overall oxide capacitance consists of the two dielectrics in series;

$$\frac{1}{C_{ox}} = \frac{1}{C_{SiO2}} + \frac{1}{C_{High-\kappa}} \tag{2.55}$$

From this we can derive an expression for the EOT of this composite gate stack;

$$EOT = \varepsilon_{SiO2}\left(\frac{t_{SiO2}}{\varepsilon_{SiO2}} + \frac{t_{High-\kappa}}{\varepsilon_{High-\kappa}}\right) \tag{2.56}$$

Despite the fact that it increases the EOT, an interfacial layer does have some beneficial qualities with regard to carrier mobility in the device channel. For that reason a SiO_2 interfacial layer can intentionally be thermally grown prior to the high-κ deposition. The thermal growth of SiO_2/Si is well understood; its thickness can be well controlled and ensures a good quality (low roughness and interface charge) channel interface. A SiO_2 layer separates the channel from the high-κ dielectric which reduces the influence of the various scattering sources in the latter [51-53] (detailed in section 2.6.5).

2.6.4 Hafnium based dielectrics

There has been a world wide consolidation towards hafnium based dielectrics.[54] Like SiO_2, hafnium based dielectrics are amorphous. In hafnium oxide, it is interesting to observe from Figure 2.11 that the barrier for holes is over double that for electrons, indicating that it will insulate holes better than electrons. However, hafnium oxide becomes crystalline or poly-crystalline at low temperatures (the exact

temperature is dependent on the annealing ambient and other processing conditions). Poly-crystalline dielectrics are undesirable as they are composed of grains whose boundaries serve as high leakage current paths. In addition, grain size and orientation vary randomly throughout the film which can lead to significant variations in κ.[53] The crystallisation problem can be overcome by alloying hafnium oxide with SiO_2, to form hafnium silicate ($HfSiO_2$) which retains the stability against crystallisation close to 1000°c. By doing this the material becomes more SiO_2 like, in that it's band-gap increases, but its dielectric constant decreases.[47, 55] The static and high frequency dielectric constant of hafnium silicate as a function of silicon composition is shown in Figure 2.13.

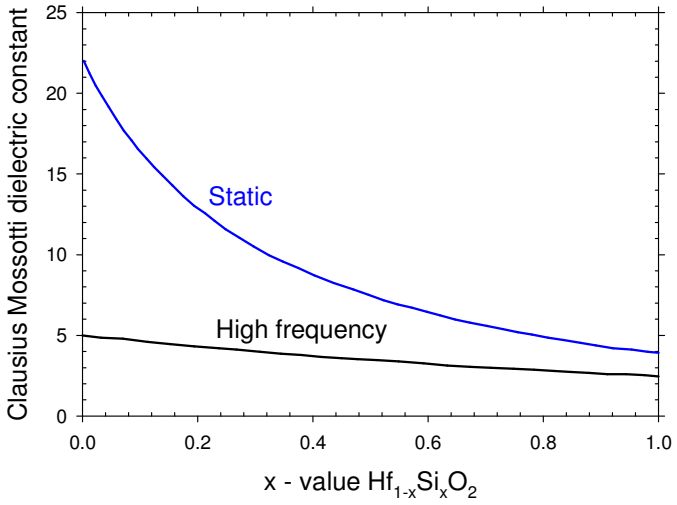

Figure 2.13 Static and high frequency dielectric constant of $Hf_{1-x}Si_xO_2$ as a function of x, extracted from the Clausius-Mossotti relation (adapted from [53])

The addition of nitrogen to hafnium silicate (HfSiON) increases both the dielectric constant and its crystallisation temperature.[47, 56] However nitrogen incorporated into the gate, high-κ dielectric or interfacial layer can diffuse down to the channel

interface during dopant activation, generating a large number of interface states, degrading device characteristics (e.g. mobility, 1/f noise).[57-61]

2.6.5 High-κ mobility degradation

From equations (2.14) and (2.15), an increase in C_{ox} due to a high-κ dielectric should result in an increase in on current. i.e. for a given supply voltage a greater inversion charge, thus a more conductive channel is achieved. However, electron mobility in devices with hafnium based dielectrics and interfacial layer thicknesses of less than 2 nm, are presently lower than those with just a SiO_2 dielectric, particularly at low to mid E_{eff}. This is the case even with intentional thermal SiO_2 interfacial layers, which provide excellent channel interface quality.[57] A major objective of current research is to understand how this can be rectified. Three scattering mechanisms are thought to play a role; remote phonon scattering, remote Coulomb scattering and remote roughness scattering. These sources of scattering are termed remote as they are separated from the channel by the interfacial layer. The relative contribution of each is currently under debate. Various studies, detailed below, have shown each mechanism to be significant 2 nm from the channel. Thus device engineers are faced with a trade-off between high on current and scalability.

Remote phonon scattering (RPS)

Fischetti *et al.*[49] studied the role of phonon scattering from high-κ dielectrics on electron mobility in detail. The basic concepts are briefly reviewed here. As mentioned previously, the static dielectric constant of high-κ dielectrics results

primarily from ionic polarization, due to highly polarisable (soft) metal-oxygen bonds. Associated with these bonds are low-energy lattice oscillations (and associated phonons), which are "optical" in nature due to the ionic character of the atomic bonds. This triggers frequent emissions and absorption processes by thermal electrons. Electrons in the inversion layer can couple with surface optical (SO) modes arising at the dielectric/silicon interface from the longitudinal-optical (LO) modes of the dielectric. The coupling strength is proportional to

$$\hbar\omega_{SO}\left(\frac{1}{\varepsilon_{Si}^{\infty}+\varepsilon_{ox}^{\infty}}-\frac{1}{\varepsilon_{Si}^{\infty}+\varepsilon_{ox}^{0}}\right) \tag{2.57}$$

where $\varepsilon_{si}^{\infty}$ is the optical permittivity of silicon and ω_{SO} is the angular frequency of the interface longitudinal-optical phonon. ω_{SO} is calculated from the dominant transverse-optical (TO) phonon modes in the dielectric and can be approximated by;

$$\omega_{SO}=\omega_{TO}\left(\frac{\varepsilon_{ox}^{0}+\varepsilon_{Si}^{\infty}}{\varepsilon_{ox}^{\infty}+\varepsilon_{Si}^{\infty}}\right)^{\frac{1}{2}} \tag{2.58}$$

It is important to note in equation (2.57), the large difference between ε_{ox}^{0} and $\varepsilon_{ox}^{\infty}$ in high-κ dielectrics, results in a large coupling strength therefore large degradation of mobility.

Although the hard bonds of SiO_2 result in an undesired small static dielectric constant, this also results in a small difference between ε_{ox}^{0} and $\varepsilon_{ox}^{\infty}$ and so in a small electron/phonon coupling strength. Secondly the hard bonds results in large LO and SO phonon energies. Thermal electrons cannot emit excitations of such large energy

and at room temperature there are too few thermally excited phonons to be absorbed. Thus in MOSFETs with a SiO_2 gate dielectric, this type of phonon scattering is negligible. Watling *et al*.[53] observe less than a 5% reduction in drive current when including this in the simulation of such devices.

For $HfSiO_2$ the difference between ε_{ox}^{0} and $\varepsilon_{ox}^{\infty}$ decreases with decreasing Hf composition as shown in Figure 2.13. The reduction in coupling strength is accompanied by increasing phonon energies which together serve to reduce the mobility degradation.[53, 62-63] Remote phonon scattering is reduced further with increasing SiO_2 interfacial layer thickness for two reasons 1)The scattering potential decreases with increasing distance from the high-κ dielectric by a factor $e^{-qt_{SiO2}}$ 2)The turning on of SiO_2 SO modes thereby decoupling the phonons in the high-κ and electrons in the channel.[49, 53]

Remote Coulomb scattering (RCS)

Charge densities ranging from $6x10^{12}$ cm^{-2}[64] to $7x10^{13}$ cm^{-2}[51] at the high-κ/interfacial SiO_2 layer have been reported in hafnium based gate stacks. These have been attributed to induced dipoles (remote dipole scattering).[51, 65-67] In the model proposed by Kita *et al.*[68], dipoles at the HfO_2/SiO_2 interface are formed by diffusion of oxygen atoms from HfO_2 to SiO_2, driven by the areal density difference in oxygen atoms. This leaves oxygen vacancies in the HfO_2 (positive charge) and excess oxygen in the SiO_2 (negative charge). Diffusion of any nitrogen in the gate stack also creates fixed charge.[57, 69] Electrostatic interaction with these charges

modifies the electrostatic potential seen by carriers in the channel. The resulting scattering has been shown to degrade electron mobility particularly at low to mid E_{eff}. With increasing E_{eff}, screening by inversion charges reduces the scattering potential. Akasaka *et al*.[69] also report significant charges at the gate/high-κ interface.

Remote roughness scattering (RRS)

Li *et al*.[70] first developed an analytical model of remote roughness scattering from the metal/oxide in Al/SiO_2/Si n-MOSFETs. Gamiz *et al.*[71] devlop a model for remote roughness scattering in poly-Si/SiO_2/Si n-MOSFETs. Since the advent of high-κ gate stacks, some groups have developed models of roughness from the high-κ/interfacial oxide interface[72] and the gate/high-κ interface[73] suggesting it may degrade mobility. However currently there is no publication that has convincingly shown that this is important by means of analysis of experimental data.

2.7 Gate electrode

As device dimensions and supply voltages continue are scaled down, V_t should be scaled down accordingly to ensure the on current is not reduced. The work function of the gate electrode is largely responsible in setting V_t. For an n-MOSFET, a gate electrode of low work function, equal to the conduction band edge of Si (~4.05 eV), is desired. This depletes the substrate, bending the conduction band at the surface towards the Fermi level, thus only a small V_{gs} is needed for inversion. For a p-MOSFET, a gate electrode of large work function, equal to the valence band edge of

Si (~5.17 eV), is desired. Such "band edge" gates are necessary for a low V_t and S.S. in bulk MOSFETs.[48, 74]

In the past, gate electrodes were made from polycrystalline Si (poly-Si). This is Si degenerately doped n-type or p-type, for n- and p-MOSFETs respectively, to set the work functions as required. Poly-Si has the advantage that it is refractory, easily deposited, and compatible with SiO_2 and the process flow. However, although degenerately doped, poly-Si has limited carrier concentration (10^{19} – 10^{20} cm^{-3}). In inversion, poly-Si gates become depleted, effectively adding another capacitance in series with the oxide. The net result is an increase in EOT reducing MOSFET scalability. Hobbs *et al.*[75-77] showed that poly-Si gates are incompatible with high-κ dielectrics. A metal gate has a much higher carrier concentration (~10^{22} cm^{-3}) and so gate depletion is reduced. Furthermore, metal gates are also effective for screening the soft optical phonons in high-κ dielectrics, thereby reducing remote phonon scattering.[78-81].

There are many metal candidates but no world wide consensus as to which metal should be used as the parameters that influence the work function are complex. A metal's work function depends on its alloy composition, how it's deposited and the underlying high-κ composition. Work function stability after the RTA has been a major issue leading to intensive research into compounds with high thermal stabilities such as nitrides, carbides and silicides of transition metals. TiN, TaN, HfN are all stable enough but have mid-gap work functions. Most metals react with the

underlying oxide causing the effective work function of the gate stack to migrate towards the mid-gap of silicon during the RTA.[54] One approach to tune the work function is to deposit capping layers (e.g. Al_2O_3 or La_2O_3 for p-MOSFETs and n-MOSFETs respectively), onto the high-κ dielectric. During the RTA, these caps are doped into the high-κ dielectrics forming dipoles at the interface which modulate the effective work function of the gate stack.[68, 82-83] Another approach (now being used by Intel) is to employ a "gate last" process where a "dummy gate" is deposited on the high-κ dielectric, the RTA then applied, the dummy gate removed and then the band edge metal gate deposited.[7, 84-85] Obviously with this approach, the metal does not experience the high temperature anneal but the process is more complicated and costly. A final solution is to use a mid-gap metal gate for both n- and p-MOSFETs, thereby relaxing the band edge constraint, and control V_t using silicon on insulator (SOI) and/or multiple gate technology (sections 2.9 and 2.10).

2.8 The short channel effect

The short channel effect is the decrease of the MOSFET V_t as the channel length is reduced.[2] This is important as it is hard to control channel lengths precisely due to process tolerances. Statistical variations in channel lengths then lead to problems with V_t control.

When deriving V_t for an ideal MOSFET in section 2.1 it was assumed that the depletion charge was balanced by equal but opposite charges in the gate. However in a real MOSFET, the depletion regions at the source and drain extend into the channel region. Providing the channel is sufficiently long, the source and drain

depletion regions only occupy a small fraction of the entire channel and V_{gs} controls essentially all of the depletion charge. Thus the MOSFET can be abruptly switched off. As the channel length decreases, the fraction of charge controlled by the gate decreases. Less gate charge is now required to invert the channel, resulting in a lower V_t. With increasing V_{ds}, the reverse-biased depletion region at the drain extends further into the channel area and the gate controls even less depletion charge, further lowering V_t. When V_{ds} is sufficiently high or channel length sufficiently short, the drain depletion region merges with the source depletion region. Thus the source-channel potential barrier is lowered below the built in potential resulting in significant drain leakage current with the gate unable to shut it off. Control of the channel by the gate can be retained by not only increasing C_{ox} but by proper scaling down of the source and drain junction depths and scaling up of the substrate doping concentration. Increasing the doping concentration reduces the depletion region widths, however carrier mobility is degraded due to increased number of ionised impurities and increased vertical electric field. In addition, V_t is increased.

If the source and drain junction depths were equal to the inversion layer thickness, the gate would retain complete control of the channel. However achieving such ultra-shallow junctions is limited by diffusion of the source and drain dopants.

2.9 Silicon on insulator (SOI) technology

The short channel effect can be reduced by fabricating MOSFETs on a silicon film atop a ~100 nm to 400 nm thick buried insulating substrate, known as a buried oxide or BOX (typically SiO_2). The silicon film forms the substrate of the MOSFETs. The BOX restricts the depth of the source and drain depletion regions thus reducing their influence on the channel. This not only allows a low substrate doping concentration, promoting a high carrier mobility, but also relaxes the need to scale C_{ox} so aggressively. The BOX also has the benefit of reducing the source to substrate and drain to substrate junction capacitances which translates to faster MOSFET switching. For VLSI applications, the most suitable techniques to manufacture SOI substrates are oxygen-ion implantation (SIMOX) into a Si wafer and wafer bonding techniques (e.g. smart cut®, NanoCleave®, AcuThin®, ELTRAN®).

The characteristics of an SOI MOSFET is dependent on the thickness, t_{Si} and the doping concentration of the silicon film above the BOX. Two types of MOSFET can be distinguished: MOSFETs in which the silicon is never completely depleted i.e. $t_{Si} > W_{depm}$ (a partially depleted SOI MOSFET (PDSOI)) and MOSFETs where the silicon can be completely depleted $t_{Si} < W_{depm}$ (fully depleted SOI MOSFET (FDSOI)).

If the neutral region in a PDSOI MOSFET is connected to ground by a substrate contact, the characteristics of the device will be exactly the same as a bulk MOSFET. If the neutral region is left floating, it can become charged causing the properties of the device, such as V_t, to be dependent on the history of its

operation.[86] In addition the device will present a host of "floating body effects" such as the kink effect and the presence of a parasitic open-base bipolar transistor between the source and drain.[87] These effects complicate design and require greater design margins. FDSOI minimises floating body effects therefore is considered more viable.[88] The physics of FDSOI MOSFETs is considered from now on.

The areal depletion charge in a FDSOI MOSFET is given by;

$$Q_{dep} = eN_a t_{Si} \tag{2.59}$$

Thus either a low substrate doping and/or a thin Si film is necessary to ensure the MOSFET is fully depleted. Providing $C_{ox} >> C_{BOX}$, and neglecting interface charge at the Si/BOX interface, the expression for V_t is very similar to the bulk MOSFET;[89]

$$V_t = V_{fb} + 2\psi_b + \frac{eN_a t_{Si}}{C_{ox}} \tag{2.60}$$

Typically the substrate receives no intentional doping which minimises ψ_b (equation (2.4)). The use of a mid-gap gate sets V_{fb} to 0 V assuming no charges in the dielectric. Reducing t_{Si} reduces Q_{dep}. i.e. theoretically a very low V_t can be achieved using FDSOI technology. [90]

The increased control of the channel by the gate can be understood by comparing the distribution of depletion charges in long channel and short channel bulk and FDSOI MOSFETs as shown in Figure 2.14.

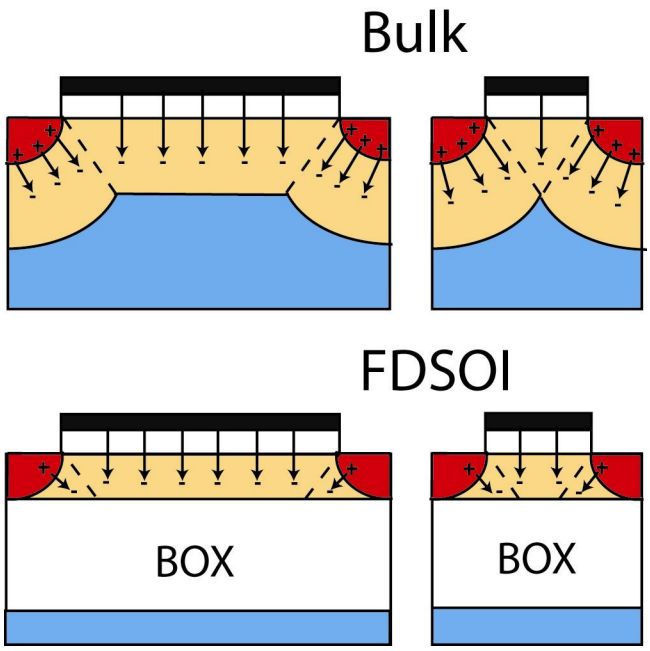

Figure 2.14 Charge distribution in long and short channel bulk and FDSOI MOSFETs.

In the long channel bulk MOSFET, the depletion region controlled by the gate can be represented by the area of a trapezoid, where the lengths of the upper and lower base are almost equal to the channel length. In a short channel bulk MOSFET the area is now a triangle. However in a short channel FDSOI MOSFET, gate depletion charge retains its trapezoid shape due to the restriction of the source and drain depletion regions by the BOX. It is obvious that reducing t_{Si}, ensures the gate will control a greater fraction of the channel.[91-93] A simple scaling rule for FDSOI MOSFETs demands $t_{Si}/4 < L$ to achieve good turn-off characteristics.[94] This has led to extensive research into ultrathin SOI MOSFETs.[93, 95-97]

However fabricating uniform ultrathin films is a challenge. In addition, carriers in ultrathin SOI are prone to self heating due to the low thermal conductivity of the

BOX.[98-99] This degrades carrier mobility and the reliability of the device. Furthermore there is a limit on the scalability of FDSOI MOSFETs. Eventually ultra-thin films will no longer adequately suppress short channel effects as channel lengths decrease. Under high $V_{ds,}$ the drain electric field component through the BOX will cause appreciable barrier lowering near the source, increasing the sub-threshold slope and off current.[100-102] This field can be reduced by decreasing the thickness of the BOX and using a highly doped substrate or an underlying ground plane to terminate the field lines.[92, 103] However reducing the thickness of the BOX increases the source and drain junction capacitance therefore the capacitive load of the device. Simulations by Koh *et al*.[101] and Wong *et al.*[97] show that using a thick BOX with a very low dielectric constant, reduces the drain electric field through it, allowing further scaling. For further information on nearly every aspect of SOI technology and its applications, the reader is referred to the books by Colinge[104], Cristoloveanu and Li[105] and Marshall and Natarajan[106].

2.10 Multiple gate technology

2.10.1 Channel control

By using additional gates, the electrostatics of the channel can be controlled much more effectively than in the FDSOI MOSFET allowing for further scaling. The basic principle is shown in Figure 2.15 which shows how the addition of a second gate further suppresses the source and drain depletion regions.

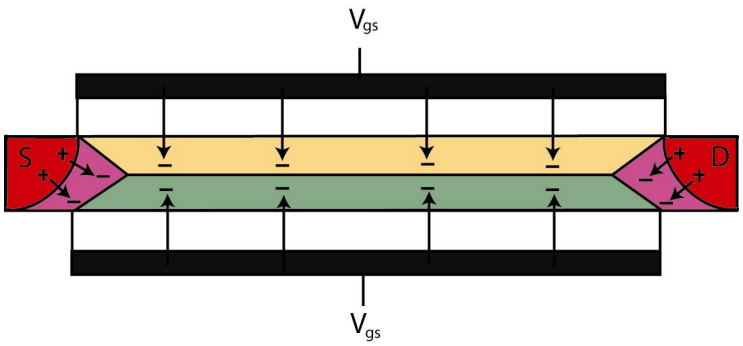

Figure 2.15 Cross section of a fully depleted double-gate MOSFET. The electric fields (arrows) and corresponding depletion charges from both gates and the source and drain are shown.

This notion has given birth to a host of three-dimensional multi-gate MOSFETs which include a range of double-gate, triple-gate and surrounding-gate MOSFETs, with the latter theoretically providing the best possible control of the channel region.[103]

2.10.2 The finFET

From the range of multi-gate MOSFETs, the finFET has emerged as the most promising candidate to replace the planar MOSFET due to processing simplicity. It follows conventional MOSFET processing and can be fabricated in any Si pilot line. The basic fabrication process is described in section 6.2. A finFET can have multiple fins in parallel, all straddled by a single gate line, thus its effective width is given by;

$$W_{eff} = n\left(2H_{fin} + W_{fin}\right) \tag{2.61}$$

where n is the number of fins, H_{fin} and W_{fin} is the fin height and width respectively. Adequate suppression of the short channel effect and off state leakage current requires that $W_{fin} \sim L/2$. It is desirable for H_{fin} to be as large as possible to maximise

W_{eff}, therefore I_d. Thus for the 22 nm node and beyond, the finFET can essentially be treated as a fully depleted double gate device where I_d flows predominantly along its sidewall surfaces. Due to their vertical nature, a finFET's sidewalls and top surface lie in the (110) and (100) planes respectively when the device is oriented parallel or perpendicular to the wafer flat of a standard (100) wafer. I_d therefore flows along the <110> direction. In this orientation, the hole mobility is maximised but the electron mobility is minimised. The electron mobility could be maximised by rotating the fins 45° as then the sidewalls would be in a (100) plane. However this incurs an area penalty on the wafer and increases complexity in circuit design, making it an unlikely option in VLSI circuits.

2.10.3 FinFETs in inversion

The proximity of a second gate can modify the electrostatics significantly and therefore the inversion charge distribution compared to a bulk MOSFET. The basic principles are most easily illustrated by considering a double gate finFET. Consider the effect of decreasing W_{fin} whilst keeping V_{gs} constant. The corresponding change in the energy band diagram is shown in Figure 2.16.

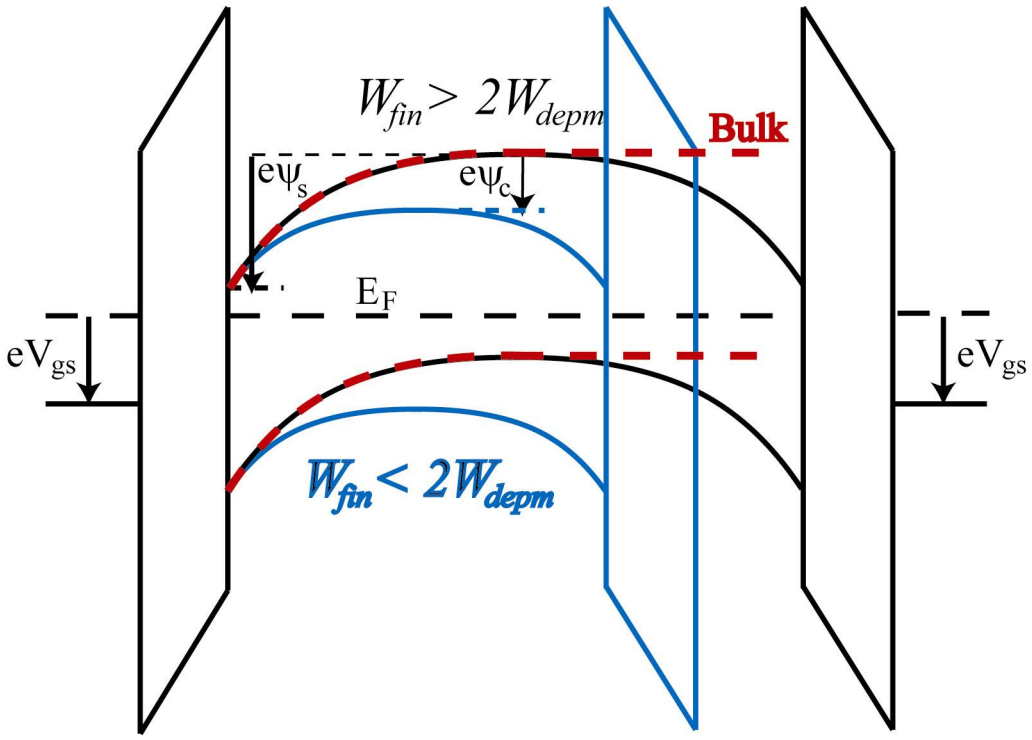

Figure 2.16 Energy-band diagram of two double-gate n-finFETs of different W_{fin} in inversion (V_{gs} > 0 V applied to both gates). ψ_c , the potential at the middle of the fin, increases with decreasing W_{fin}, increasing the electron concentration throughout the fin. The band diagram of a bulk n-MOSFET is shown for comparison.

Providing $W_{fin} > 2W_{depm}$ a neutral region exists between both the depletion regions separating the channels. When $W_{fin} < 2W_{depm}$, the fin becomes fully depleted and Q_{dep} decreases linearly with W_{fin}. As the charge on the gate, Q_g is fixed, electrostatics requires that Q_{inv} increases by the same amount to restore the total charge. (The electric field lines from Q_g now uncompensated by Q_{dep} are paired with extra inversion charges.) As V_{gs} is fixed, V_{ox} and therefore ψ_s remain constant. The voltage drop inside the silicon, ψ_s-ψ_c which is mainly across Q_{dep} will reduce with

decreasing W_{fin}. The relationship of this voltage drop with W_{fin} and N_a is given by; [107]

$$\psi_s - \psi_c = \frac{eN_a W_{fin}^2}{8\varepsilon_0 \varepsilon_{Si}} = \frac{Q_{dep} W_{fin}}{8\varepsilon_0 \varepsilon_{Si}} \tag{2.62}$$

Therefore, the potential in the centre of the fin, ψ_c will increase. As the Fermi level is constant for all W_{fin}, increased ψ_c means increased electron concentration (Q_{inv}) throughout the fin i.e. Q_{inv} is no longer confined at the interfaces. This is known as volume inversion.

The onset of volume inversion in a finFET depends not only on N_a and W_{fin}, but also V_{gs}. A quantum mechanical description is necessary in this case. Consider a finFET such that the electron wave functions are confined by the dielectric band offsets of the two sidewall interfaces. For small V_{gs}, the band bending ψ_s- ψ_c , is small enough that the two sidewall interfaces and conduction band edge create a square quantum well whose eigenenergies are well separated from one another (in contrast to the triangular well of a bulk MOSFET), as shown in Figure 2.17. The position of these energy levels above the conduction band edge is given by;

$$E_{conf} = \frac{\hbar^2}{2m_{conf}} \left(\frac{\pi . i}{W_{fin}} \right)^2 \tag{2.63}$$

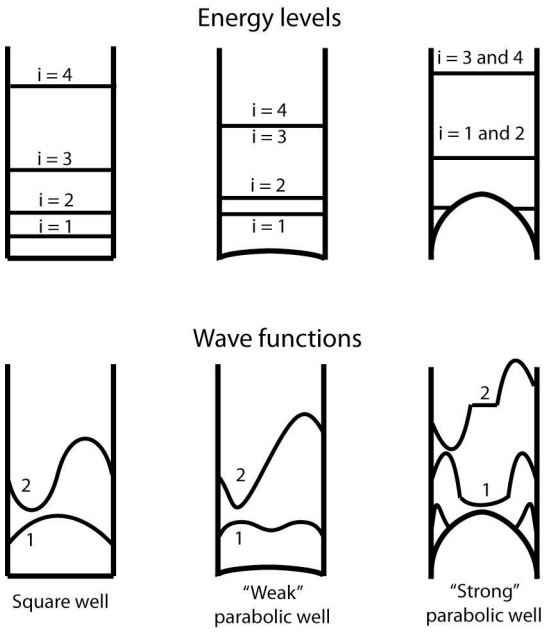

Figure 2.17 Four first energy levels and two first wave functions, ψ(z) in square, weak parabolic and strong parabolic potential wells formed by the two dielectric interfaces and conduction band edge in a double gate finFET. Note sub-wells are created at both interfaces in the strong parabolic case, confining the lowest energy states. The electron concentration is proportional to $\psi(z)^2$. (adapted from [104])

In this instance, the lowest sub-band is predominantly occupied, whose wave function peaks at the middle of the well, and thus volume inversion occurs. As V_{gs} (therefore ψ_s-ψ_c) increases, the conduction band edge becomes more parabolic (shown in Figure 2.17). This change in shape of the well causes the energy levels to superimpose and shift up and pair (E_1 with E_2, E_3 with E_4, etc), resulting in the wave functions peaking closer to the interfaces. Further increase of V_{gs} (ψ_s- ψ_c) causes the conduction band edge to become strongly parabolic and the energy levels to become degenerate through pairing. The wave functions now peak close to the interfaces, i.e. surface inversion now occurs.[104] Volume inversion is maintained for higher V_{gs}

by decreasing W_{fin}. (As ψ_s- ψ_c is reduced with decreasing W_{fin} (equation 2.62) the well retains its square shape.)

2.10.4 Confinement effects on V_t

When W_{fin} or (t_{Si} in a SOI MOSFET) is thinner than a critical value, typically 10 nm, V_t starts to increase instead of decreasing.[108] This is due to the strong energy quantisation between the two dielectric interfaces which effectively increases the Si band-gap. Thus the classical analysis of V_t is no longer valid. The smaller W_{fin}, the wider the separation between eigenenergies and the higher the value of the lowest sub-band energy. As the sub-band energies, importantly the lowest sub-band energy, is further from the Fermi level, a higher V_{gs} is necessary for inversion.

2.10.5 Carrier mobility in finFETs

Volume inversion

Carrier mobility in SOI MOSFETs and double gate MOSFETs/finFETs has been intensively investigated. In an SOI n-MOSFET, bulk phonon[109-110] and interface roughness[111-112] scattering rates increase for t_{Si} less than 20 nm and 10 nm respectively. Depending on the interface charge density, Coulomb scattering from the BOX interface may also be significant when $t_{Si} < 10$ nm.[113] For a finFET or double gate MOSFET operating in the volume inversion regime, carrier scattering is reduced. Simulations by Gamiz *et al.*[114] show the reduction in confinement due to volume inversion reduces bulk phonon scattering. Since the interface roughness

perturbation potential and Coulomb potential are larger near the interfaces and decrease towards the center of the channel, interface roughness and Coulomb scattering are also reduced.[115-118]

Strain technologies

Straining silicon is an effective way to engineer its band structure and enhance the carrier mobility.

The most effective strain configuration for electrons is uniaxial tensile along the <110> direction on the (110) orientation. This not only lowers the Δ_2 sub-bands which exhibit m_{tran} = 0.190m_0, but warps the Δ_2 sub-band energies reducing m_{tran} and increasing m_{conf}. This results in comparable mobility to that on the (100) unstrained orientation.[24] Thus the worst current flow direction can be converted into the best direction.

For hole mobility, uniaxial compressive strain along the <110> direction on the (110) orientation is the best configuration, increasing the already high mobility as compared to the (100) orientation. This increases the energy split between the LH and HH sub-bands reducing scattering between them.[35, 119]

Implementing these strains into the finFETs sidewalls to boost the poor (110)/<110> electron mobility and provide further enhancement to the hole mobility have been hot topics in recent years. Current methods utilize strained substrates (global strain),

or individual stressors for each finFET (local strain). Since the required stress directions are opposite for n- and p-finFETs, these techniques differ. For n-finFETs;

- a biaxial (2D) tensile strained SOI substrate is used as the starting wafer. The strain perpendicular to the fins is relaxed during fin patterning resulting in uniaxial tensile strain (the lateral strain relaxation technique)[120-124]
- local strain techniques consist of tensile stress liners, e.g. SiN, deposited over the gate[120, 125-129] and SiC source drains.[125-126]

For p-finFETs;

- a biaxial compressive strained SiGe OI substrate is used as the starting wafer. Lateral strain relaxation is performed during patterning resulting in uniaxial compressive strain[121, 130]
- local strain techniques consist of compressive stress liners[120, 128-129, 131] and SiGe source and drains[127, 132-133].

It is known that a thin metal layer intrinsically induces a certain amount of stress depending on its thickness, deposition method and temperature.[134] A stressed metal gate electrode, recently employed by Intel[7], has the advantage of applying stress, without requiring any additional processing steps. Thus its implementation into finFET technology is of great interest.[135-140]. However, due to the 3D nature of a fin, understanding the stress transfer is non-trivial. Furthermore, the effect of different stress distributions on electron mobility has only recently been understood.[141]

2.10.6 Fin access resistance

With decreasing W_{fin} access resistance increases due to the reduction in cross sectional area. This reduces the effective V_{gs} therefore I_d and has long been recognized as a performance limiting bottleneck in finFETs. As a result, source drain engineering is being researched vigorously.[132, 142-146]

Chapter 3 : Electrical Characterisation Techniques

This chapter describes the experimental apparatus and interpretation of the electrical measurements that were employed to characterise the FETs in this work. From measurements of current and capacitance as a function voltage, a vast amount of information regarding the device operation can be extracted. Further information can be obtained by measuring over a range of temperatures. The description of the measurement apparatus is a condensed version of that written by Beer.[147] The extraction techniques are abridged versions from Schroder[148] and Nicollian and Brews[14]. For additional information, the reader should consult these texts.

3.1 Measurement apparatus

All measurements were performed using a Desert Cryogenics probe station capable of being cooled to 4.2 K. Electrical connections to a wafer are made via a substrate chuck on which the wafer sits and four tungsten probe needles (of radius 10 μm). The probe needles are operated with three micrometers each, allowing movement on all axes. The range of motion in each direction is large enough to allow any point on the substrate chuck (3 cm x 4 cm) to be reached by any of the four probe needles. A good electrical contact between wafer and chuck is achieved by sticking the back of the wafer to a thin piece of copper using silver conductive paint, and then taping the

edge of the copper piece onto the substrate chuck. The region around the wafer is kept free of electrical noise by a shield, which the probe arms enter through metal-braided holes that maintain a closed conducting surface around the wafer area. High quality connections and coaxial cable throughout the measurement system ensure that the signal is protected from interference right to the probe needles.

The shield in turn is housed in a completely closed chamber as it needs to be under vacuum when cooling for thermal insulation and removal of moisture from the chamber environment. A vacuum of ~10^{-6} mbar is achieved with a two-stage pumping system consisting of a rotary roughing pump and a small turbo pump. Probe arms are able to move while maintaining vacuum with bellows, which expand and contract thus keeping the chamber sealed. Probe needles are thermally connected to both the shield and the substrate chuck with thick copper braids to ensure that the probes cool somewhat before having contact with the wafer. A glass window is present above the wafer, in the shield and the vacuum chamber, to allow the probe needles to be aligned with a microscope situated above. The shield window is lead plated so not to compromise the electrical shielding. Temperature sensors are present both at the shield and substrate chuck, which are monitored electronically by a Lakeshore 330 temperature controller. This also controls two heaters, one under the substrate chuck and one under the shield, automatically using a negative feedback algorithm to achieve the user-specified temperature. Cryogenic liquid (nitrogen or helium) is contained in a closed dewar. The internal pressure of the dewar (0.5 bar) pushes liquid up a transfer tube, where it evaporates and flows through into the low temperature probe station. It travels under the substrate chuck

and back out to vent. To ensure the temperature remains stable at 4.2 K, a high flow rate is required and achieved using an Edwards 9 CFM rotary pump.

Connections to a device are made by manipulating the micrometers, whilst monitoring the probe tips through a microscope. Once contact to a device is made, the viewport of the measurement chamber is covered to provide a dark, electrically shielded environment.

3.2 Current-voltage measurements

"The most common measurement to perform on a MOSFET is an I_d-V_{gs} sweep: a gate voltage is applied to achieve the off-state and incremented to the on state (negative to positive bias for n-MOSFETs), a constant bias to the drain is applied and the resulting drain current is measured. The substrate and source are biased at 0 V. The currents in the source, gate and substrate are measured in addition to the drain to check that the MOSFET is operating normally without excessive leakage. All I_d-V_{gs} measurements were made using an Agilent 4156C parameter analyser. This is an extremely sensitive (minimum detectable current of the order of a fA), piece of equipment which has a programmable interface enabling measurements to be performed and saved efficiently. It also contains in-built integration options to minimise electrical noise."[147]

3.3 Capacitance-voltage measurements

Capacitance-voltage (CV) and small signal conductance-voltage (GV) measurements were made using an Agilent E4980A precision LCR meter. This operates by superimposing a small oscillating AC voltage on a DC voltage, which is applied to the gate. The resulting AC current through the source, drain or substrate is measured from which the capacitance and conductance are calculated (the conductance is discussed below). As for the I_d-V_{gs} sweep, the DC voltage is applied to achieve the off-state and incremented to the on-state. The capacitance i.e. the change in charge in response to the AC voltage is thus calculated for each DC voltage. Using a four terminal pair configuration, the LCR meter models the MOSFET as either a capacitor, C in parallel with a resistor/conductance, G or a capacitor in series with a resistor. The parallel configuration is usually chosen as it most closely resembles a MOSFET. The conductance is thus measured together with the capacitance. Figure 3.1 is a block diagram showing the internal working of the LCR meter when using the parallel configuration.

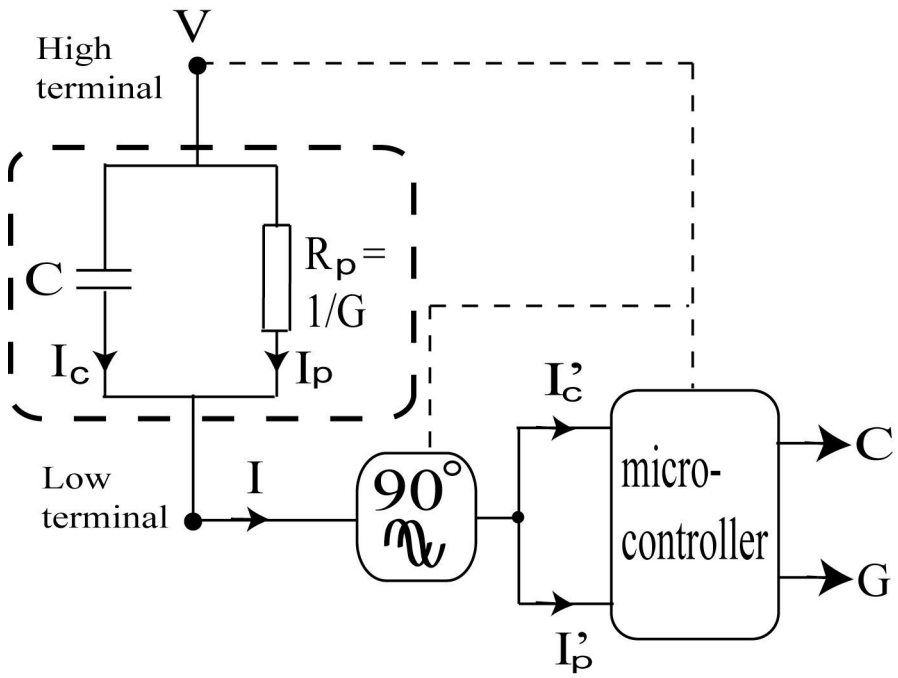

Figure 3.1: Operation of the LCR meter modelling the MOSFET as a capacitor in parallel with a resistor. AC and DC voltages applied by the "high terminal" and resulting current, I, measured by the "low terminal". The 90° phase separator then splits the current I into I_c' and I_p'. The microcontroller calculates C and G from I_c' and I_p' respectively.

Calculation of *C* and *G* requires accurate measurements of the individual currents I_c and I_p. I_c is the displacement current through the capacitor also commonly referred to as the quadrature current component as it is 90° out of phase with AC voltage. I_p is in phase with the AC voltage and represents small signal energy losses due to changes in occupancy of bulk and interface traps, (discussed in section 3.4.1) and also DC leakage current through the gate dielectric. The LCR meter measures the total current *I*, which it passes through a phase separator where *I* is split into I_c' and I_p' which are 90° out of phase and in phase with the AC voltage respectively. A microcontroller, running a feedback algorithm, calculates the capacitance and conductance from I_c', I_p', the magnitude and frequency, *f* of the AC voltage.

Obviously for an accurate calculation of capacitance and conductance we require $I_c = I_c'$ and $I_p = I_p'$ respectively, i.e. the phase separator must be able to accurately separate I_c and I_p. For an accurate measurement of capacitance, the amplitude of I_c must be sufficiently large as not to be masked by I_p to prevent noisy or distorted CV profiles. Furthermore, I_c and I_p in general may not be clean sinusoidal signals but contain various harmonics and noise. Consequently, we require $R_p >> X_c$ where $X_c = 1/j\omega C$ and $\omega = 2\pi f$. Thus large area MOSFETs and/or high measurement frequencies are needed. Measuring large area MOSFETs also minimises the influence of parasitic capacitances inherent in the device. However a trade off is required as large devices exhibit higher gate leakage current which may reduce R_p to an unacceptable level, further necessitating high measurement frequencies. The LCR meter enables measurements with frequencies of 20 Hz – 2 MHz. MOSFETs with ultrathin oxides suffering from very high gate leakage currents may require measurements at radio frequencies (RF CV), typically ≥1 GHz[149]. In this work such measurements were not necessary.

Until now we have not considered the effect of series resistance R_s shown in Figure 3.2. R_s may originate from a high gate, source/drain, substrate or contact resistance.

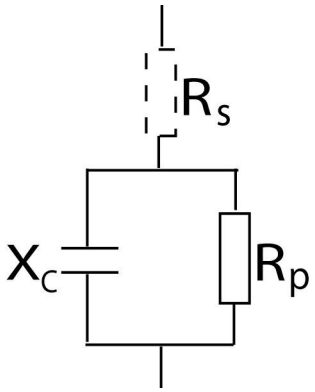

Figure 3.2 Parasitic resistance in series with the parallel equivalent circuit

The LCR meter does not account for R_s in the parallel equivalent circuit so we must ensure $R_s << X_c // R_p$ so that R_s does not significantly reduce I_c and I_p leading to large errors in the calculations of C and G. In the case where $R_p = \infty$ (or G = 0) and R_s is non negligible, the series equivalent circuit is best suited. If the parallel circuit is selected, then a low measurement frequency is necessary to ensure X_c is sufficiently high. If the device exhibits a high series resistance and gate leakage current, no easy solution is forthcoming.

A phasor diagram of the admittance of the parallel equivalent circuit is shown in Figure 3.3.

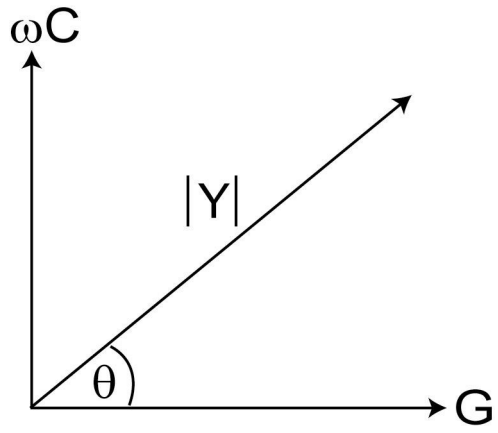

Figure 3.3: Phasor diagram of the admittance of the parallel equivalent circuit. G = 0 for an ideal capacitor and θ = 90°.

The phase angle (or loss tangent) is given by;

$$\tan\theta = \frac{\omega C}{G} \tag{3.1}$$

For an ideal capacitor, $G = 0$ (i.e. only the displacement current exists) therefore $\theta = 90°$. In research, devices are not optimised and high series resistances, interface trap densities and gate leakage currents are not uncommon, reducing θ.

Prior to measurements, various corrections must be performed to take into account the position and length of the cables, which themselves exhibit a capacitance and resistance. There is a built in function which determines correction parameters automatically. A TestPoint program provides a user-friendly interface to the E4980A to specify measurement parameters such as measurement frequency of the AC voltage, DC voltage range, time delays and signal averaging parameters. The

program graphs the capacitance and conductance measured as a function of DC voltage allowing the user to determine whether the measurement was successful.

3.3.1 Capacitance-voltage profile

The equivalent circuit of a MOSFET is shown in Figure 3.4. In a real MOSFET there will also be parasitic capacitances between the gate and source/drain and between the substrate and source/drain but for a large area MOSFET, these are usually negligible.

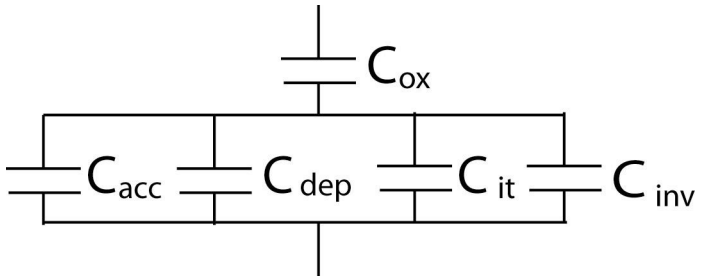

Figure 3.4: Equivalent circuit of a MOSFET C_{ox}, C_{acc}, C_{dep}, C_{it}, C_{inv} are the dielectric (oxide), accumulation, depletion, interface trap and inversion capacitances respectively.

The C-V profile of an n-MOSFET is shown in Figure 3.5. This is measured by connecting the gate to the high terminal and the source, drain and substrate to the low terminal (2 terminal measurement).

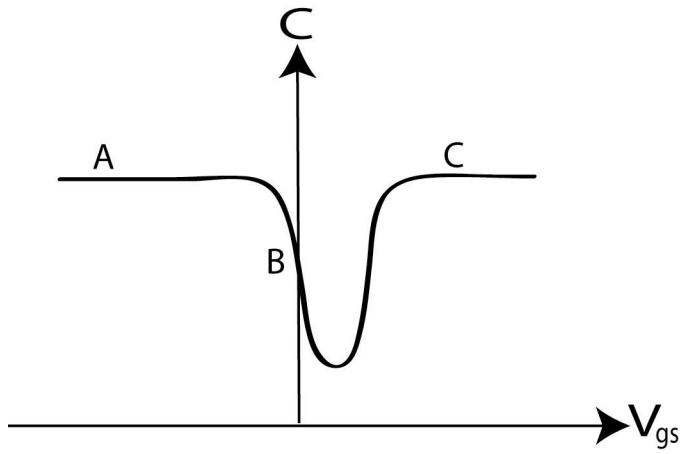

Figure 3.5: CV profile of a n-MOSFET. A: accumulation, B: depletion and C: inversion.

The total capacitance C is given by:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{acc} + C_{inv} + C_{dep} + C_{it}} \tag{3.2}$$

C_{inv} and C_{acc} are the areal inversion and accumulation layer capacitances respectively, C_{dep} is the areal depletion layer capacitance and C_{it} is the areal capacitance of the interface traps. The effect of C_{it} on the measured capacitance is considered in section 3.4.1. It should be noted that not all of these capacitances are present at any one time. At point A in the figure, V_{gs} is negative and the MOSFET is in the accumulation region, i.e. majority carriers (holes) in the p-type substrate strongly attracted to the dielectric-semiconductor interface. The differential change in voltage caused by the AC voltage, causes a differential change in charge on the gate and also the accumulation charge. The large number of majority carriers screens the dielectric interface from the substrate and the measured capacitance is $C_{ox.}$ (In the equivalent circuit, $C_{acc} >> C_{ox}$). As V_{gs} becomes more positive, the majority carriers are repelled from the surface and a depletion region begins to form (B). The AC

voltage causes a differential change in the depletion charge i.e. depletion region width. The measured capacitance is now the result of two capacitors in series; that due to the dielectric and that due to the forming depletion region. Hence:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \tag{3.3}$$

$$C_{dep} = \frac{\varepsilon_0 \varepsilon_{Si}}{W_{dep}} \tag{3.4}$$

where interface traps have been neglected. The measured capacitance now begins to decrease. The width of the depletion region increases as V_{gs} is made more positive until the band bending reaches the threshold inversion point, where minority carriers (electrons) readily supplied from the source and drain, form an inversion layer (C). The inversion layer screens the depletion region. The AC voltage causes a differential change in charge on the gate and the inversion charge, thus the measured capacitance is $C_{ox.}$ (In the equivalent circuit, $C_{inv} >> C_{ox}$).

3.3.2 Split C-V

Since the inversion charge is supplied by the source and drain, and the depletion charge by the substrate, individual measurements of the source and drain, and substrate currents allow the inversion and depletion capacitances to be obtained separately. This is known as the split CV technique and was proposed by Koomen[150] and later used by Sodini *et al.*[151] in the extraction of carrier mobility (chapter 4). Figure 3.6 and Figure 3.7 show the experimental setup and both halves or branches of a split CV measurement.

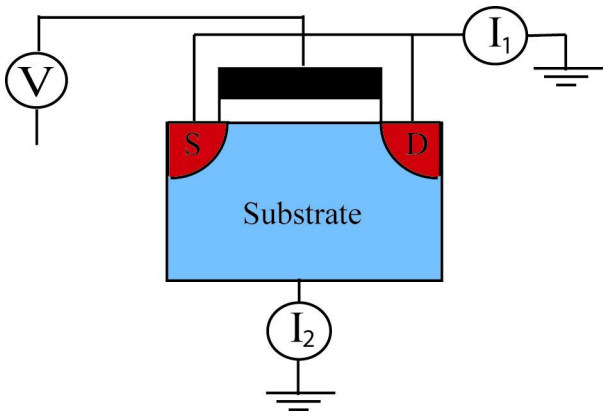

Figure 3.6 Electrical connections to measure the split CV of a MOSFET.

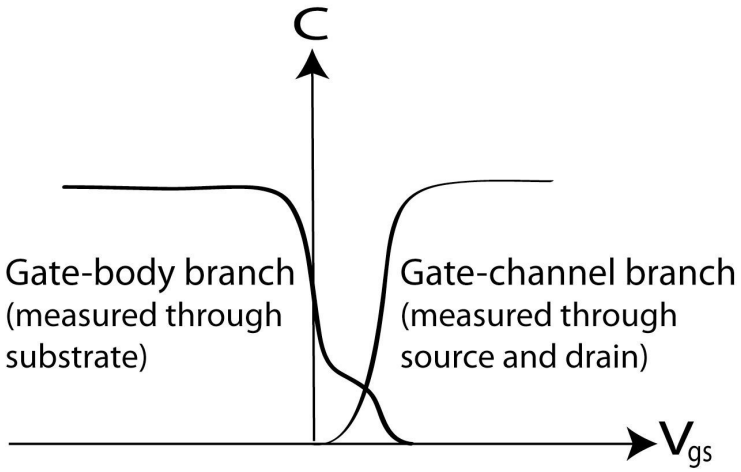

Figure 3.7:Gate-channel and gate-body split CV profiles for an n-MOSFET.

The gate-channel branch of the capacitance, C_{gc}, is obtained by measuring the current through the source and drain, (I_1 in the figure) with the substrate grounded. In accumulation and depletion, the source and drains are electrically disconnected from the channel and only the gate overlap capacitances are measured. In inversion, the potential barriers between the channel and source and drain regions are reduced. Minority carriers from the heavily doped source and drain regions now flow to the channel to form the inversion layer and I_1 registers a current. Although the minority carriers are in abundance in the source/drain regions, they encounter a resistance on

their way to the channel. The channel resistance and the various capacitances limit the frequency response of the minority carriers. Either the frequency of the AC voltage must be sufficiently low or the channel length sufficiently short to ensure the minority carriers have enough time to form the inversion charge. To avoid distortion of the CV curve (seen by a shift of the capacitance particularly in weak inversion where the channel resistance is high), the measurement frequency must satisfy the criterion;[152]

$$f << \frac{1}{2\pi\tau_{ch}} \tag{3.5}$$

where τ_{ch} is the channel time constant. From Haddara *et al.*'s analysis based on a transmission line model [152], we can derive an equation based on measurable quantities;

$$f << \frac{4I_d}{2\pi C_{gc0} V_{ds}} \tag{3.6}$$

where C_{gc0} is the quasistatic or low frequency gate-channel capacitance (in Farads). As a guide, for SiO_2 dielectrics thinner than 2 nm, L should be 10 μm or less when using a measurement frequency of 1 MHz.[153]

The gate-body branch of the capacitance, C_{gb}, is obtained by measuring the current through the substrate, (I_2 in the figure) with the source and drain grounded. In accumulation, majority carriers from the substrate flow to the surface and in depletion, majority carriers are repelled from the interface. Therefore a current I_2 is measured. In inversion, the depletion charge stops increasing as it rapidly becomes screened by the inversion charge. Thus the depletion charge no longer responds to the AC voltage (the inversion charge responds but is not measured in this

configuration), no current I_2 is measured and the capacitance is zero. Accumulation and depletion carrier response is limited by the substrate resistance, R_{sub} (or well resistance) hence the measurement frequency must satisfy the criterion;

$$f << \frac{1}{2\pi\tau_{sub}} = \frac{1}{2\pi R_{sub} C_{gb}} \tag{3.7}$$

where τ_{sub} is the substrate time constant.

Majority carriers have very short response times so this is only becomes an issue for RF CV measurements[149] or when measuring at very low temperatures where substrate dopants are starting to be frozen out.

3.4 Extraction techniques

3.4.1 Interface trap density

We now consider the effects of interface traps/states on C-V and G-V measurements. Traps change occupancy in depletion and weak inversion, as the band bending changes in these regimes and the Fermi level is swept through the band gap. (Band bending essentially fixed in strong inversion.) In depletion, the majority carrier band edge (valence band for an n-MOSFET) is close to the Fermi level and exchanges carriers with traps. In weak inversion the minority carrier band edge (conduction band for an n-MOSFET) is closer to the Fermi level and communicates with traps. The change in trap occupancy in response to the AC voltage, gives rise to an extra capacitance, C_{it} in parallel with C_{dep} as shown in Figure 3.4. This results in a higher measured capacitance than if no traps were

present. C_{it} only contributes if the time period of the AC voltage is greater than the trap response times (see below). Several techniques are now described, which allow the density of interface traps, D_{it} (expressed in units $cm^{-2}eV^{-1}$) to be extracted.

High-Low Frequency C-V Technique

This technique exploits the fact that it takes some finite time for interface traps to change occupancy; therefore if the measurement frequency is high enough, there will be insufficient time for the interface traps to respond and the measured capacitance will exclude C_{it}.

In depletion we have that $C_{acc} = C_{inv} = 0$ therefore:

$$\frac{1}{C_{lf}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep} + C_{it}} \tag{3.8}$$

$$\frac{1}{C_{hf}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \tag{3.9}$$

where C_{lf} and C_{hf} are the capacitances measured under low frequency (typically 100 Hz) and high frequency (typically 1-2 MHz) conditions respectively. Rearranging these equations and eliminating C_{dep} yields an expression for C_{it}:

$$C_{it} = \frac{C_{ox}C_{lf}}{C_{ox} - C_{lf}} - \frac{C_{ox}C_{lf}}{C_{ox} - C_{hf}} \tag{3.10}$$

C_{it} is related to D_{it} by;

$$D_{it} = \frac{C_{it}}{e} \tag{3.11}$$

As C_{lf} and C_{hf} are measured as a function of V_{gs}, D_{it} is obtained as such. It is often more useful to plot D_{it} as a function of energy within the semiconductor band-gap using:

$$\psi_s = \int_{V_{fb}}^{V_{gs}} \left(1 - \frac{C_{lf}}{C_{ox}}\right) dV_{gs} \tag{3.12}$$

To obtain ψ_s over the whole device operating range, the integral should be split into two parts: integration from flat-band to inversion and integration from flat-band to accumulation. ψ_s then corresponds to the valence band edge in accumulation and the conduction band edge in inversion (in eV).

Conductance technique

In depletion, the conductance represents the energy loss resulting from changes in interface trap occupancy, caused by the AC voltage. A loss occurs when an interface trap cannot capture or emit carriers in phase with the AC voltage, i.e. the response of the trap lags behind the AC voltage. No losses are observed at very low frequencies, as traps respond immediately, or at very high frequencies, as traps do not respond at all.

The loss associated with a single trap can be represented by a resistance R_{it} in series with its capacitance with time constant $\tau_{it} = C_{it} R_{it}$ as shown in Figure 3.8a). As the LCR meter measures a conductance, it is more convenient to represent a trap by a G_{it} and C_{it} pair as shown in Figure 3.8b).

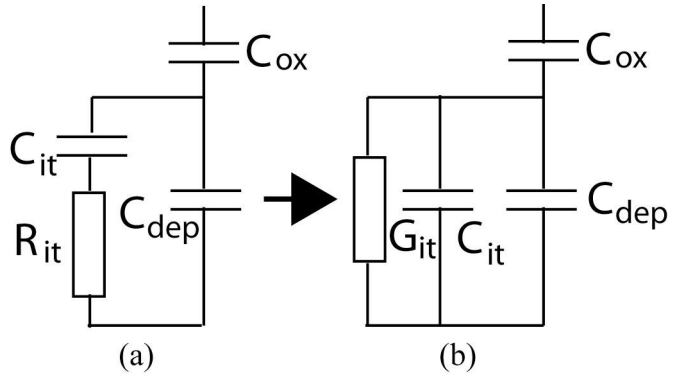

Figure 3.8a) Equivalent circuit of a MOSFET in depletion including an interface trap of time constant $\tau_{it} = R_{it}C_{it}$ b) parallel equivalent circuit

Capture and emission occurs primarily by traps located within a few *kT/e* above and below the Fermi level. Each interface trap level within this interval contributes a different energy loss depending on its energy from the Fermi level, giving rise to a dispersion of time constants. The distribution of interface traps can be modelled by adding corresponding G_{it} and C_{it} elements in parallel for each trap level. Integrating the trap admittances and accounting for the time constant dispersion, Nicollian and Brews[14] show that the resulting equivalent parallel conductance of the traps, G_p can be calculated from the measured conductance, G and capacitance, C using;

$$\frac{G_p}{\omega} = \frac{\omega G C_{ox}^2}{G^2 + \omega^2 \left(C_{ox} - C\right)^2} \tag{3.13}$$

Equation (3.13) is derived based on interface trap interactions with the majority carrier band. By measuring the capacitance and conductance as a function of V_{gs} and ω, D_{it} is calculated in depletion from the maximum of a G_p/ω versus ω plot using;

$$D_{it} = \frac{2.5}{e}\left(\frac{G_p}{\omega}\right)_{\max} \tag{3.14}$$

To ensure that the maximum G_p/ω is observed, the frequency range needs to be large (~100 Hz to ~1 MHz) as does the number of frequencies used. The extraction is repeated at each applied DC voltage thus obtaining D_{it} as a function of V_{gs}. This can be converted to D_{it} as a function of band-gap energy using equation (3.12). The conductance technique is one of the most sensitive methods to determine D_{it} as the conductance is measured directly. However it does require a large number of measurements and their analysis is very time consuming. In weak inversion, occupation of interface traps by minority carriers and also occupation of bulk traps contribute to the conductance introducing error in the above technique.

Sub-threshold Slope Technique

The sub-threshold slope (or sub-threshold swing), is a measure of how quickly a MOSFET switches off, specifically the change in V_{gs} required to reduce I_d by one decade. It follows directly from a plot of $\log_{10}(I_d)$ against V_{gs};

$$S.S = \left(\frac{d(\log_{10} I_d)}{dV_{gs}} \right)^{-1} = \ln(10)\frac{nkT}{e} \tag{3.15}$$

which is measured in mV/decade. n is the capacitor divider ratio which is an indication of the fraction of V_{gs} appearing at the channel interface as ψ_s. A value of n close to 1 is highly desirable as ultimately ψ_s is responsible for modulating the barrier between the source and drain and therefore I_d. For a bulk MOSFET;

$$n = \left(1 + \frac{C_{dep} + C_{it}}{C_{ox}} \right) \tag{3.16}$$

Note the sub-threshold slope is strongly dependant on the interface trap capacitance which increases its value. It is not possible to achieve a value below approximately 60 mV/decade at room temperature.

D_{it} can be extracted in weak inversion from the sub-threshold slope of a MOSFET using $D_{it} = C_{it} / e$;

$$D_{it} = \frac{C_{ox}}{e}\left(\frac{eS.S}{2.3kT} - 1\right) - \frac{C_{dep}}{e} \tag{3.17}$$

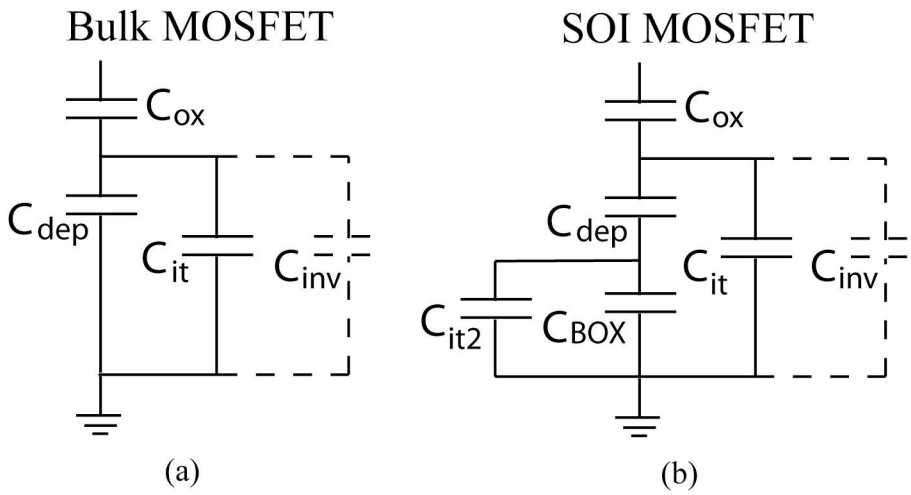

Figure 3.9 Comparison of the equivalent circuits of a a) bulk and b) FDSOI MOSFET. C_{it2} is the interface trap capacitance at the Si/BOX interface and C_{BOX} is the buried oxide capacitance. A thick box (small C_{BOX}) ensures a near ideal sub-threshold slope.

In the case of a FDSOI MOSFET, the equivalent circuit in depletion is more complicated as shown in Figure 3.9 leading to;

$$n = \left(1 + \frac{C_{it}}{C_{ox}} + \frac{C_{dep}}{C_{ox}}\right) - \frac{\frac{C_{dep}}{C_{BOX}}\frac{C_{dep}}{C_{ox}}}{1 + \frac{C_{it2}}{C_{BOX}} + \frac{C_{dep}}{C_{BOX}}} \tag{3.18}$$

where

$$C_{dep} = C_{Si} = \frac{\varepsilon_{Si}\varepsilon_0}{t_{Si}} \tag{3.19}$$

C_{it2} is the areal interface trap capacitance at the Si/BOX interface and C_{Si} is the areal capacitance of the Si film. The presence of C_{BOX} and C_{it2} reduces the sensitivity of the sub-threshold slope technique making it unsuitable for extracting D_{it}.

Excluding C_{it} and C_{it2} from the equivalent circuit we obtain;

$$n = 1 + \frac{C_{dep}C_{BOX}}{C_{ox}\left(C_{dep} + C_{BOX}\right)} \tag{3.20}$$

For a thick BOX, $C_{BOX} << C_{ox}$ and $C_{BOX} << C_{dep}$. As a result n is usually close to unity and a sub-threshold slope close to the ideal 60 mV/decade is obtained.

3.4.2 Flat-band voltage

The flat-band voltage, V_{fb} is an important parameter when analysing capacitance profiles as it marks the boundary between accumulation and depletion. For a uniform substrate doping concentration, a plot of $1/C_{hf}^2$ against V_{gs} in depletion has a linear slope. In accumulation, C_{hf} is constant, therefore the slope is zero. Thus the knee at the boundary between accumulation and depletion corresponds to V_{fb}. For

greater accuracy, evaluating $\frac{d^2\left(1/C_{hf}^2\right)}{dV_{gs}^2}$ produces a peak, the maximum of which coincides with V_{fb}.

3.4.3 Inversion charge, depletion charge and vertical field

The sum of the parasitic gate-drain and gate-source overlap capacitances (measured in accumulation) cause a vertical shift (parasitic offset) in the measured C_{gc} profile. This becomes increasingly significant the smaller the area of the device. The intrinsic C_{gc} profile can be recovered by subtracting the offset from the measured C_{gc} profile. This is not always as straightforward as it sounds and is examined in detail in chapter 4. The inversion charge density can then be obtained by integrating C_{gc} with respect to V_{gs}:

$$Q_{inv}\left(V_{gs}\right) = \int_{-\infty}^{V_{gs}} C_{gc}\left(V_{gs}\right) dV_{gs} \tag{3.21}$$

Similarly, the depletion charge density is obtained by integrating C_{gb} from the flat-band voltage:

$$Q_{dep}\left(V_{gs}\right) = \int_{V_{fb}}^{V_{gs}} C_{gb}\left(V_{gs}\right) dV_{gs} \tag{3.22}$$

Equations (3.21) and (3.22) assume that interface traps do not contribute to the measurements of C_{gc} and C_{gb}. As discussed in section 3.4.1, interface traps can affect CV measurements in depletion and weak inversion. Their contribution is most noticeable in a C_{gc} profile; manifested as a (frequency dependent) shoulder in weak inversion. Thus to accurately calculate Q_{inv} in weak inversion and Q_{dep}, a high

enough measurement frequency should be selected to prevent most of the traps from responding.

The effective vertical field, E_{eff}, usually expressed in $MVcm^{-1}$, is an approximation to the average normal electric field a carrier in the channel experiences, as a result of the applied gate bias. It is given by

$$E_{eff} = \frac{Q_{dep} + \eta Q_{inv}}{\varepsilon_0 \varepsilon_{Si}} \tag{3.23}$$

where η is an empirically determined factor referring to the averaging of the electric field over the carrier distribution in the inversion layer. This factor was given as 11/32 in the scattering theory in section 2.5.1 according to equation (2.31). The effective carrier mobility, μ_{eff}, extraction detailed in chapter 4, has historically been expressed as a function of E_{eff}. On a (100) orientation, Takagi *et al.*[154] show that a universal relationship exists for μ_{eff} over a wide range of E_{eff} and substrate doping concentrations when η = ½ for electron and ⅓ for hole inversion layers.

On a (110) orientation, Takagi *et* a*l.*[155] and Lee *et al.*[23] show using η = ⅓ is necessary to maintain the universality for electron μ_{eff}. However recent detailed studies have shown that the universality of hole μ_{eff} breaks down on the (110) orientation and the conventional definition of η = ⅓ is incorrect.[35, 119, 156] Irie *et al.*[156] show that the value of η is strongly related to the occupation of the lowest sub-band, where the larger the occupation, the larger the value of η. Irie *et al.*[119] demonstrate that η also depends on channel direction, therefore on the scattering mechanisms in the inversion layer. They show that η = ⅓ for holes is particularly

unsuitable for the <110> channel direction. Furthermore, the modified carrier distribution brought about by strain, SOI and multiple gates means the concept of universality fails.[157]

In chapter 5, where (100) and (110) bulk MOSFETs are analysed, hole μ_{eff} is plotted as a function of N_{inv} and E_{eff}. Following convention [34, 158-160], Takagi *et al.*'s values for η are used and their μ_{eff} data included as a reference.

3.4.4 Doping profile

The doping concentration of the substrate can be extracted from the C_{gb} profile in depletion. This technique is based on the width of the depletion region changing in response to the AC voltage. Assuming an abrupt depletion layer edge and complete dopant ionisation, the doping concentration is extracted using:

$$N(V_{gs}) = \pm 2\left(e\varepsilon_0\varepsilon_{Si} \, d\left(1/C_{hf}^2\right)/dV_{gs} \right)^{-1} \tag{3.24}$$

where the positive sign is for an n-type substrate and the negative sign for a p-type substrate.

To obtain the doping concentration as a function of depth, equation (3.24) is calculated for each value of V_{gs} from flat-band throughout depletion. From equations (3.4) and (3.9) the corresponding value of W_{dep} can be calculated from;

$$W_{dep} = \varepsilon_0\varepsilon_{Si}\left(\frac{1}{C_{hf}} - \frac{1}{C_{ox}} \right) \tag{3.25}$$

The onset of inversion limits the maximum depth which can be probed since this is when the depletion depth reaches its maximum value. Since the charges that respond to the AC voltage are mobile majority carriers, equation (3.24) actually measures the majority carrier concentration at the edge of the depletion region, rather than the dopant ion concentration itself. As a result, the resolution of this technique is limited by the Debye length, L_D, which is "a measure of the distance over which a charge imbalance is neutralised by majority carriers."[148] The Debye length is constant for a uniform doping concentration and is given by:

$$L_D = \left(\frac{\varepsilon_0 \varepsilon_{Si} kT}{q^2 N_a} \right)^{1/2} \tag{3.26}$$

The resolution of this technique for a doping concentration of 10^{17} – 10^{18} cm^{-3} is therefore around 10 nm. If the doping profile changes abruptly in a distance comparable to the Debye length or less, the extracted profile will represent an average of the true profile.

3.4.5 Drain current correction in the presence of significant gate leakage current

If the gate dielectric is sufficiently thin and/or the MOSFET area sufficiently large, gate leakage current, I_g reduces the measured drain current, I_{dm}. For low V_{ds}, approximately half the gate current flows from the source and half from the drain as shown in Figure 3.10. Using Kirchoff's current law, the intrinsic drain current I_d can be recovered;[161]

$$I_d = I_{dm} + I_g/2 \tag{3.27}$$

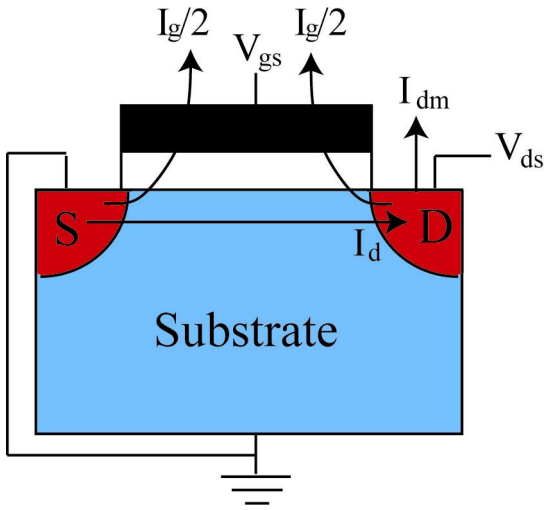

Figure 3.10 MOSFET cross section showing the true drain current I_d, gate current I_g and the measured drain current I_{dm}. For small V_{ds}, approximately half the gate current flows from the source and half from the drain.

3.4.6 Threshold voltage

The threshold voltage, V_t, defined in section 2.1 is often loosely quoted as the value of V_{gs} at which the MOSFET begins to turn on. When looking at experimental data however, the threshold voltage is not obvious and thus many different methods for extracting it have been proposed and in general they do not agree on a single value. A review of 11 different extraction techniques is provided in the paper by Ortiz-Conde *et al.*[162] A common technique is the linear extrapolation method. The I_d-V_{gs} curve of the MOSFET is measured with low V_{ds} to ensure that the MOSFET is operating in the linear regime. In an ideal MOSFET, I_d is expected be linearly

dependent on V_{gs}, as shown by equation (2.13), which is repeated here:

$$I_d = \mu_{eff} \frac{W}{L} C_{ox} \left[(V_{gs} - V_t) V_{ds} - V_{ds}^2 / 2 \right] \tag{3.28}$$

However, a real MOSFET exhibits sub-threshold leakage currents causing I_d to be non-linear in the threshold region. At high V_{gs} the slope of the I_d-V_{gs} curve will decrease due to resistances of the source and drain regions, degraded carrier mobility and possibly high gate leakage current. Between these two regimes there is a point of maximum slope on the I_d-V_{gs} curve which by this method is extrapolated back to the point of zero drain current, with this being defined as V_t. This method can suffer if either the sub-threshold leakage is high extending the non-linearity of I_d to higher V_{gs}.

A more preferred technique is the transconductance method proposed by Tsuno *et al*.[163] The transconductance g_m is given by;

$$g_m = \frac{dI_d}{dV_{gs}} \tag{3.29}$$

This is essentially the same as the linear extrapolation method except that the transconductance is extrapolated to zero from the point of its maximum slope. This technique assumes that the mobility in the threshold region is dominated by Coulomb scattering and is therefore proportional to N_{inv}:

$$\mu_{eff} \approx \alpha N_{inv} \approx \frac{\alpha C_{ox}}{e} (V_{gs} - V_t) \tag{3.30}$$

Substituting equation (3.30) into (3.28) and differentiating with respect to V_{gs} yields an expression for the transconductance:

$$g_m = \frac{dI_d}{dV_{gs}} = \frac{W}{L}\frac{2\alpha}{e}C_{ox}^2\left(V_{gs} - V_t\right)V_{ds}. \qquad (3.31)$$

As expected, g_m exhibits a linear dependence on V_{gs} at threshold and extrapolation to zero gives $V_{gs} = V_t$. The maximum slope of g_m usually lies in the non-linear tail of the I_d-V_{gs} curve. Thus this method tends to obtain a value of V_t closer to the point where I_d becomes negligibly small.

V_t can alternatively be defined as the V_{gs} that induces a given N_{inv}. Thus V_t can be extracted based on the electrostatics rather than current or carrier mobility. Esseni *et al*.[110] apply this technique to ultrathin SOI MOSFETs, where mobility is a complicated function of t_{Si}, defining $V_t = V_{gs}$ corresponding to $N_{inv} = 2\text{x}10^{11}$ cm^{-2}. Obviously this technique relies on accurate extraction of N_{inv}.

3.4.7 Source-drain resistance

The source and drain are not perfect conductors and have a resistance. The total resistance of the source and drain is called the source-drain resistance R_{sd} or access resistance. If this is comparable to the resistance of the channel, I_d is degraded. The most severe I_d degradation occurs in the linear region (low V_{ds}) of MOSFET operation when V_{gs} is high because the channel resistance is low. The various contributions to R_{sd} are described in detail in Taur and Ning[2]. The most common method to extract R_{sd} is to treat the MOSFET as an equivalent circuit comprising the source (R_s), drain (R_d) and channel (R_{ch}) resistances in series, where $R_{sd} = R_s + R_d$. Assuming that R_{sd} is a constant and that R_{ch} for a given gate overdrive ($V_{gt} = V_g - V_t$)

is proportional to channel length (i.e. it's resistivity is constant per unit length), then R_{sd} can be extracted from a range of MOSFETs with different channel lengths. The total MOSFET resistance, $R = V_{ds}/I_d$ is plotted against channel length for several values of V_{gt}. Note that V_t must be known for each MOSFET and that the extraction technique used, must not be systematically affected by channel length. Linear regressions are then performed through each series of points associated with each V_{gt}. These regressions should intersect at a single point. Note the channel lengths used should be small as not to exert excessive leverage on the slope of the regressions (see figure 5.9a) for an example). The point of intersection corresponds to the co-ordinates (ΔL, R_{sd}). ΔL accounts for any discrepancy between the written channel length L (as defined by the mask during fabrication) and the real channel length L'. Thus we can define L' as:

$$L' = L - \Delta L \tag{3.32}$$

As with R_{sd}, this is most significant on MOSFETs with a short channel lengths where R_{ch} and L are comparable to R_{sd} and ΔL respectively. ΔL and R_{sd} may be obtained with greater accuracy by plotting the intercept against the gradient of each regression. This should yield a straight line with gradient $-\Delta L$ and intercept R_{sd} found by a second linear regression (see figure 5.9b) for an example).

Chapter 4 : Improved Mobility Extraction in MOSFETs

4.1 Introduction

This chapter describes the theory and extraction of the low field effective channel mobility, μ_{eff} for the devices in this thesis. The methodology is demonstrated on a long channel SOI quasi-planar finFET at 300 K and 4 K. We begin with briefly describing the conventional extraction for a bulk MOSFET.

4.2 Conventional extraction

From sections 2.2.1 and 2.2.2 the total drain current, I_d in a MOSFET is due to carrier drift and diffusion. We shall express that here as;

$$I_d = I_{Drift} + I_{Diffusion} \tag{4.1}$$

$$\frac{I_d}{W} = Q_{inv}\mu E_x - D\frac{dQ_{inv}}{dx} \tag{4.2}$$

where $D = \varepsilon_d \mu / e$ is the diffusion coefficient and ε_d the diffusion energy (defined later by equation. (4.11)).

The effective mobility μ_{eff}, is extracted using equation (4.2) where typically I_d is measured by applying a voltage of 50 mV to the drain (for n-MOSFETs), and by making a number of approximations. Firstly, I_d is due to drift current only i.e. the

MOSFET operates well above threshold. When $V_{gs}>>V_t$ and V_{ds} is low, Q_{inv} can be approximated as being uniform from the source to drain allowing the diffusion term in (4.2) to be dropped $\left(dQ_{inv}/dx = 0\right)$ and E_x to be given by V_{ds}/L. Thereby (4.2) can be simplified and μ_{eff} calculated using:

$$\mu_{eff} = \frac{I_d L}{V_{ds} W Q_{inv}} \tag{4.3a}$$

This can also be expressed by replacing I_d/V_{ds} with the drain conductance, g_d

$$\mu_{eff} = \frac{g_d L}{W Q_{inv}} \tag{4.3b}$$

where

$$g_d = \frac{dI_d}{dV_{ds}} \tag{4.4}$$

Hence, determining μ_{eff} requires the measurement of Q_{inv} and I_d as a function of V_{gs}. Q_{inv} can be approximated by $Q_{inv} = C_{ox}\left(V_{gs} - V_t\right)$, applicable when the MOSFET is operating in the above-threshold, drift-limited regime. This leads to error in the calculated mobility as not only is it an approximation, but it relies on C_{ox} and V_t which are not necessarily well known. As detailed in section 3.4.3 a more accurate approach based on a direct measure of Q_{inv} as a function of V_{gs} is from the split C-V technique, providing that interface traps do not affect the measurement.

4.3 Improved extraction- bulk MOSFET

Equation (4.3a) is most commonly used to obtain effective mobility due to its simplicity. In this section we address the approximations made in section 4.2.

4.3.1 Diffusion and E_x-field correction

To extract the mobility near threshold, the diffusion current in equation (4.2) should be considered. With a finite applied V_{ds} near threshold, the Q_{inv} is not uniformly distributed over the channel length - Q_{inv} decreases towards the drain, hence is a function of position along the channel x and applied gate voltage V_{gs}. The lateral field E_x will also be dependent on this charge distribution. Sodini *et al.*[151] show that the values of dQ_{inv}/dV_{gs} (C_{gc}), dQ_{inv}/dx and E_x follow the same functional dependence with V_{gs}. Provided the drain bias is low and ignoring interface traps, Sodini *et al*. derive;

$$C_{gc} = C_{ox}F\left(V_{gs}\right) \tag{4.5}$$

where $0 \le F\left(V_{gs}\right) \le 1$ and $F\left(V_{gs}\right)$ explicitly given by;

$$F\left(V_{gs}\right) = \frac{dQ_{inv}/d\psi_s}{C_{ox} + dQ_s/d\psi_s} \tag{4.6}$$

Q_s is the total semiconductor charge (defined in section 2.1)

It is also shown that;

$$E_x = F\left(V_{gs}\right)\frac{V_{ds}}{L} \tag{4.7}$$

$$\frac{dQ_{inv}}{dx} = F\left(V_{gs}\right)\frac{C_{ox}V_{ds}}{L} \tag{4.8}$$

Substituting (4.7) and (4.8) into (4.2);

$$\frac{I_d}{W} = \mu_{eff} \frac{V_{ds}}{L} F\left(V_{gs}\right)\left\{Q_{inv} + \frac{\varepsilon_d}{e} C_{ox}\right\} \tag{4.9}$$

$$\mu_{eff} = \frac{\left(I_d / V_{ds}\right)L}{F\left(V_{gs}\right)W\left\{Q_{inv} + \frac{\varepsilon_d}{e} C_{ox}\right\}} \tag{4.10}$$

which is a more complete expression for mobility over the whole V_{gs} range. Although (4.10) is simple enough, it was not explicitly stated in the original paper by Sodini *et al*. Note that no extra measurements are required than when the mobility is calculated with (4.3a) or (4.3b). One point not considered by Sodini *et al.* is that inversion layers are often degenerate at large V_{gs}. Sodini *et al.* use $\varepsilon_d = kT$ which is only valid in weak inversion when the inversion layer is non degenerate.

Zebrev and Gurbonov[164] show;

$$\varepsilon_d = kT\left(1 + e^{-(E_F - E_0)/kT}\right)\ln\left(1 + e^{(E_F - E_0)/kT}\right) \tag{4.11}$$

This reduces to $\varepsilon_d = kT$ in weak inversion and $\varepsilon_d = E_F - E_0$ in strong inversion.

Sodini *et al*. state that the diffusion and E_x-field corrections have a "cancelling effect" effectively implying only the drift expression (4.3a) is required even near threshold. However, they provide no explicit theoretical proof of this statement.

4.3.2 Finite drain bias correction

Q_{inv} measured by split CV, where V_{ds} = 0 V, can lead to significant error in the extraction of $\mu_{eff,}$ since the finite drain bias during the measurement of I_d reduces Q_{inv} particularly near threshold. Ideally I_d would be measured at very low bias (Sodini *et*

al. suggest $V_{ds} < kT/e$), but then noise is an issue so many I_d measurements use V_{ds} = 50 mV[65, 154, 165-166] and in some cases 100 mV[167] which creates a non-uniform channel. Alternative CV techniques have been devised that measure the gate-to-drain and gate-to-source capacitances separately whilst biasing the substrate and the source to create the same bias conditions as the I_d measurement.[168-169] Modelling the channel as a transmission line network has also been employed with high frequency AC admittance measurements.[170] In each case, the measurement configurations are cumbersome, complicating an already difficult measurement. In addition, they cannot be used for SOI devices without substrate contacts (above the BOX), severely limiting their use in current and future technologies.

To address this problem, we propose a new and simple technique to extract either I_d/V_{ds} or g_d at V_{ds} = 0 V. Rather than trying to modify the CV measurement (possibly introducing additional errors), to obtain the correct Q_{inv}, we measure sets of I_d for different V_{ds} and perform linear regressions to obtain the limiting values of either I_d/V_{ds} or g_d at V_{ds} = 0 V. The approach is somewhat different in the regions of sub-threshold and strong inversion:

From equation (2.17) we can write the drain current in sub-threshold as;

$$I_d = I_0\left(1 - e^{-\frac{eV_{ds}}{kT}}\right) \tag{4.12a}$$

where

$$I_0 = \mu_{eff} C_{ox} \frac{W}{L}(n-1)\left(\frac{kT}{e}\right)^2 e^{e(V_g - V_t)/nkT} \tag{4.12b}$$

$$g_d = \frac{dI_d}{dV_{ds}} = I_0 \frac{e}{kT} e^{-\frac{eV_{ds}}{kT}} \tag{4.13}$$

or

$$\ln(g_d) = -\frac{e}{kT} V_{ds} + \ln\left(\frac{e}{kT} I_0\right) \tag{4.14}$$

Hence a plot of $ln(g_d)$ against V_{ds}, at a particular gate voltage, is a straight line with the intercept yielding $g_d(V_{gs}, V_{ds} = 0) = I_0\, e/kT$. Note that in the limit of small V_{ds} (4.12a) reduces to $I_d = I_0 eV_{ds}/kT$, so I_d/V_{ds} is numerically equal to g_d in the limit of V_{ds} = 0. The predicted slope of $-e/kT$ can be used to check the extraction is valid. Beyond threshold the slope of the semi-log plot will be seen to deviate from $-e/kT$. In the strong inversion region, plots of I_d/V_{ds} against V_{ds} for given V_{gs} yield straight lines with the obvious intercepts of I_d/V_{ds} at V_{ds} = 0 V.

4.4 Mobility extraction in SOI MOSFETs and finFETs

When extracting the mobility of finFETs, the masked W_{fin} value may differ appreciably from the physical value in very narrow finFETs. Mobility in narrow finFETs is considered in chapter 6. This may lead to error in the mobility when using (4.10). The preferred equation which is widely used in the literature[171-173] removes the W dependence by factoring out the area (WL) in C_{gc}:

$$Q_{inv} = \frac{1}{WL} \int_{-\infty}^{V_{gs}} C_{gc}^{meas} dV_{gs} \tag{4.15}$$

Inserting (4.15) into (4.3a) gives the drift only expression;

$$\mu_{eff} = \frac{L^2 I_d}{V_{ds} \int_{-\infty}^{V_{gs}} C_{gc}^{meas} dV_{gs}} \tag{4.16a}$$

or

$$\mu_{eff} = \frac{L^2 g_d}{\int_{-\infty}^{V_{gs}} C_{gc}^{meas} dV_{gs}} \tag{4.16b}$$

Of course equations (4.16a) and (4.16b) can be applied to an ordinary bulk MOSFET. Any error in L is likely to be insignificant in the present work as only long channel devices (≥10 μm) are considered.

4.4.1 E_x-field and diffusion correction

To investigate the effect of the E_x-field and diffusion corrections analytically, we use the theory by Zebrev and Gorbunov[164] who derive the drain current for a FDSOI MOSFET based on the sum of the drift and diffusion currents;

$$I_d = e\frac{W}{L} DN_{inv}(0)\frac{1+\kappa}{\kappa}\left\{1-\exp\left(-\frac{\kappa}{1+\kappa}\frac{eV_{ds}}{\varepsilon_d}\right)\right\} \tag{4.17}$$

which is based only on quantities near the source ($x = 0$)

In their analysis they introduce the control parameter κ, which is the ratio of diffusion to drift current and is dependent on the various capacitances of an SOI device.

$$\kappa = \frac{I_{Diffusion}}{I_{Drift}} = \left|\frac{d\xi}{d\psi_s}\right| = \frac{C_{ox}}{\left|dN_{inv}/d\xi\right|} n \tag{4.18}$$

where ξ is the chemical potential and *n* has been defined by equation (3.20), repeated below;

$$n = \left(1 + \frac{C_{Si} C_{BOX}}{C_{ox}\left(C_{Si} + C_{BOX}\right)}\right) \tag{4.19}$$

Providing $C_{ox} >> C_{BOX}$, as is the case for this work, $n = 1$ corresponding to the bulk non-SOI case. Zebrev and Gurbonov give;

$$\frac{dN_{inv}}{d\xi} = \frac{eN_{inv}}{\varepsilon_d} \tag{4.20}$$

therefore

$$\kappa = \frac{C_{ox}\varepsilon_d}{e^2 N_{inv}} \tag{4.21}$$

The electric field along the channel is given by;

$$E_x = \frac{\varepsilon_d / e}{\kappa L} \frac{1 - \exp\left(-\frac{\kappa}{1+\kappa}\frac{eV_{ds}}{\varepsilon_d}\right)}{1 - \frac{x}{L}\left(1 - \exp\left(-\frac{\kappa}{1+\kappa}\frac{eV_{ds}}{\varepsilon_d}\right)\right)} \tag{4.22}$$

If we let

$$\alpha = -\frac{\kappa}{1+\kappa}\frac{eV_{ds}}{\varepsilon_d}$$

If $V_{ds} \to 0$, $\alpha << 1$ and E_x simplifies to

$$E_x = \frac{\varepsilon_d / e}{\kappa L} \frac{1 - 1 + \alpha}{1 - \frac{x}{L}(1 - 1 + \alpha)}$$

$$= \frac{\varepsilon_d / e}{\kappa L}\alpha$$

$$= \frac{V_{ds}}{L}\frac{1}{1+\kappa} \tag{4.23}$$

$$E_x = \frac{V_{ds}}{L}\frac{1}{1+\frac{C_{ox}\varepsilon_d}{e^2 N_{inv}}} \tag{4.24}$$

Thus using the model by Zebrev and Gurbonov, we have derived a new F function, $F_z(V_{gs})$;

$$F_z\left(V_{gs}\right) = \frac{1}{1+\kappa} = \frac{1}{1+\frac{C_{ox}\varepsilon_d}{e^2 N_{inv}}} \tag{4.25}$$

Zebrev and Gurbonov derive the inversion charge density along the channel as;

$$N_{inv}(x) = N_{inv}(0)\left(1-\frac{x}{L}\left(1-\exp\left(-\frac{\kappa}{1+\kappa}\frac{eV_{ds}}{\varepsilon_d}\right)\right)\right) \tag{4.26}$$

As for (4.23), when the exponent << 1;

$$N_{inv}(x) = N_{inv}(0)\left(1-\frac{x}{L}\frac{\kappa}{1+\kappa}\frac{eV_{ds}}{\varepsilon_d}\right) \tag{4.27}$$

To evaluate the diffusion term we need an expression for dQ_{inv}/dx

$$\frac{dN_{inv}(x)}{dx} = -\frac{N_{inv}(0)}{L}\frac{\kappa}{1+\kappa}\frac{eV_{ds}}{\varepsilon_d} \tag{4.28}$$

$$\frac{dQ_{inv}(x)}{dx} = -\frac{V_{ds}}{L}\frac{\kappa}{1+\kappa}\frac{N_{inv}(0)e^2}{\varepsilon_d} \tag{4.29}$$

As $V_{ds} \to 0$ N_{inv} is uniform across channel and $N_{inv}(0) = N_{inv}$.

$$\frac{dQ_{inv}(x)}{dx} = -\frac{V_{ds}}{L}\frac{\kappa}{1+\kappa}\frac{N_{inv}e^2}{\varepsilon_d} \tag{4.30}$$

Substituting (4.21) into (4.30);

$$\frac{dQ_{inv}(x)}{dx} = -\frac{V_{ds}C_{ox}}{L}\frac{1}{1+\kappa} \tag{4.31}$$

$$\frac{dQ_{inv}(x)}{dx} = -F_z(V_{gs})\frac{C_{ox}V_{ds}}{L} \tag{4.32}$$

By substituting F_z into μ_{eff}, any variation in the lateral field E_x is exactly compensated for by the diffusion term, leaving the original "uncorrected" (4.16a). Thus we have shown theoretically that the E_x-field and diffusion corrections cancel out over the entire V_{gs} range supporting the claim of Sodini *et al*. However, the particular capacitance values must first be assessed to check n = 1 for this to be the case. It is interesting to note that whereas the weak inversion current is diffusion-like at high V_{ds}, it is drift-like at low V_{ds}. This can be seen from (4.17) which reduces to the drift only current when $V_{ds} \to 0$.

4.5 Experimental application to an SOI MOSFET

To test the suggested methodology the various corrections are applied to a quasi-planar (W_{fin} = 1.872 µm and L = 10 µm) FDSOI n-finFET at 300 K and 4 K. The device specification is given in section 6.2. In this work it was possible to measure I_d-V_{gs} from V_{ds} of 100 mV down to 5 mV and C_{gc} at frequencies of 100 kHz-1 MHz. V_{gs} of 0 to 2 V was applied in 25 mV steps. No substrate contact is present therefore C_{gb} measurements were not possible.

4.5.1 I_d - V_{gs}

At large V_{gs} the measured drain current, I_{dm} is reduced due to gate leakage current, I_g. This has been corrected by adding the gate leakage current using equation (3.27). This is shown in Figure 4.1a) for V_{ds} = 50 mV. The leakage corrected I_d is shown in Figure 4.1b) for a range of V_{ds}.

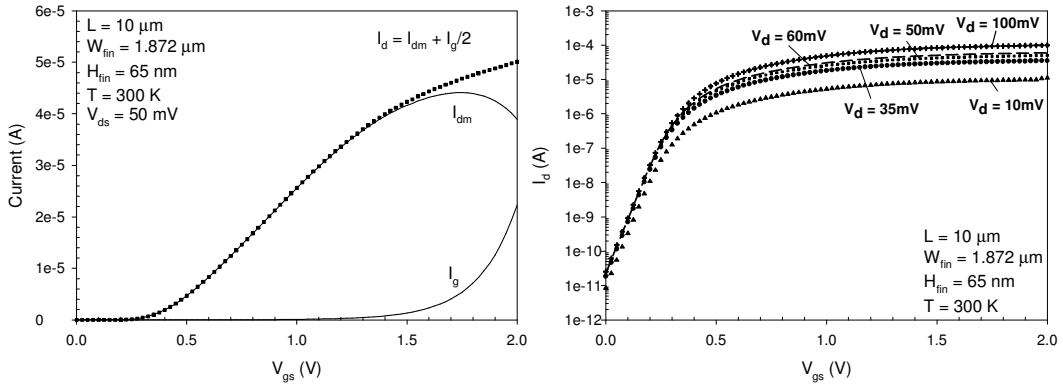

Figure 4.1 a) Gate leakage correction I_{dm} and I_g are the measured drain current and gate leakage currents b) Corrected drain current data for a range of drain biases at 300 K

4.5.2 C_{gc} - V_{gs}

Using equation (3.6), f < 5 MHz is necessary for complete formation of the inversion charge. Figure 4.2a) shows the 300 K C_{gc}- V_{gs} characteristics and phase angles. No frequency dependent shoulder in weak inversion or suppression of capacitance is present, implying that interface traps and access resistance are not corrupting the measurement. The decrease in θ with increasing V_{gs} is due to I_g. Higher measurement frequencies reduce the reactance of C in the equivalent circuit (figure 3.1), increasing I_c yielding higher values of θ. Note despite the difference in θ with

frequency, the measured capacitances are the same over most of the V_{gs} range. (i.e. the LCR meter is still able to measure the quadrature current in the equivalent circuit). This shows that a drop in θ due to I_g does not necessarily mean the measured capacitance is inaccurate. However above 1.5 V, I_g exceeds a critical value and a frequency of 10 kHz is no longer sufficient to measure C_{gc} accurately- as seen by the drop in capacitance.

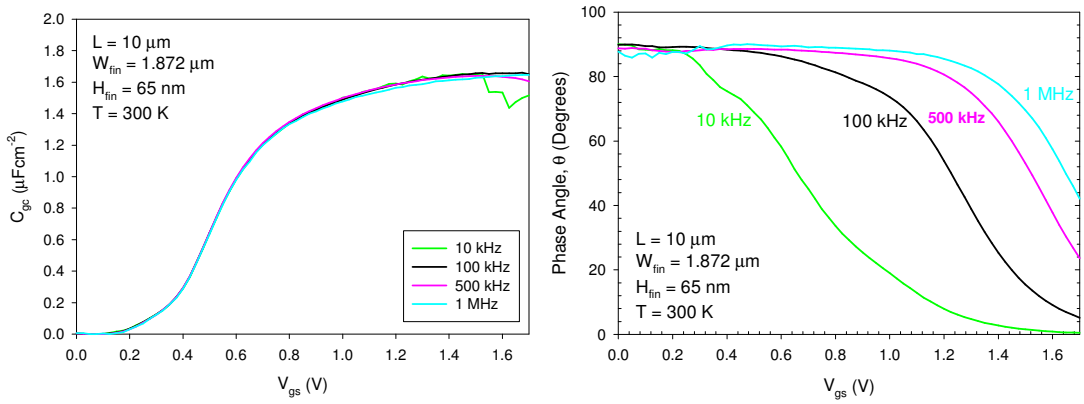

Figure 4.2 a) Gate-channel capacitance for measurement frequencies in the range 10 kHz – 1 MHz. Below 10 kHz measurement noise was unacceptably high. b) Corresponding phase angles

Figure 4.3 shows the calculated N_{inv} from the 100 kHz measurement. It must be pointed out that although $\theta = 90°$ in weak inversion this does not necessarily mean N_{inv} can be calculated accurately in this region. Although parasitic capacitances due to the equipment are accounted for prior to measurement, the gate-drain and gate-source overlap parasitic capacitances are included in the measurement. These are directly measured when the device is off during a C_{gc} measurement producing an offset, C_0, which must be subtracted for accurate calculation of N_{inv} and μ_{eff} in weak

inversion. Neglect leads to an overestimation of N_{inv} which can lead to profound underestimation in the peak mobility. However the parasitics are not always constant and the signal to noise ratio may be poor making the subtraction difficult. In addition, the measurement accuracy of the LCR meter ($\pm 1\%$ when $C \sim 0.3$ pF and f = 100 kHz – 1 MHz) may be an issue when measuring such small capacitances. In Figure 4.3 the offset was subtracted at V_{gs} = 0.075 V (V_{gs0}) corresponding to the minimum capacitance of 0.380 pF. Terada *et al.*[174] state that V_{gs0} should be defined as V_t *-5S.S*. However they assume C_0 is solely due to parasitics. In any case using their equation, with V_t ~0.4 V (Figure 4.6) and the measured *S.S.* = 65 mV/Dec., also yields a value of ~0.075 V.

In Figure 4.4 we demonstrate the effect of subtracting C_0 at different V_{gs} on μ_{eff}. In this example, a 2% variation in C_0, (corresponding to a V_{gs} difference of 50 mV) causes μ_{eff} to vary by a factor of 2.6 at $N_{inv} = 1\text{x}10^9$ cm^{-2}. Due to the sensitivity of C_0 on μ_{eff} and N_{inv} in weak inversion, μ_{eff} can only be reliably extracted from N_{inv} of approximately $1\text{x}10^{11}$ cm^{-2} to within an error of less than 5 %.

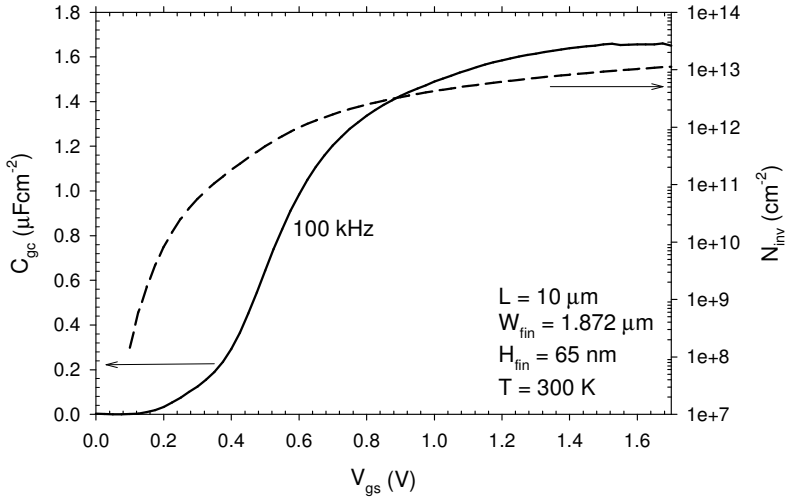

Figure 4.3 Gate-channel capacitance measured at 100 kHz and calculated inversion charge density

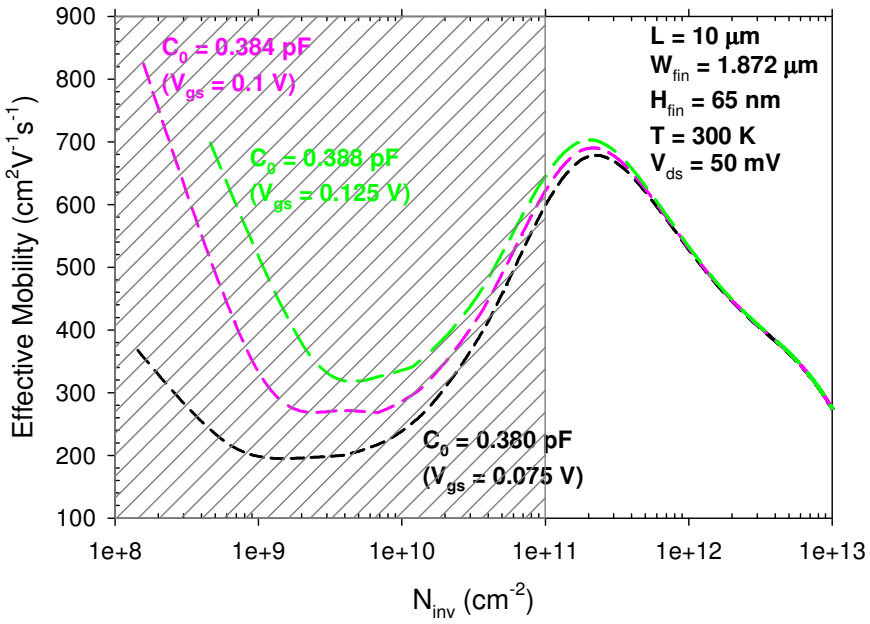

Figure 4.4 Effect of subtracting the offset capacitance on effective mobility extraction

4.5.3 μ_{eff} extraction

To demonstrate the possible application of the V_{ds} correction in weak inversion, μ_{eff} has been calculated down to N_{inv} =1x10^{10} cm^{-2}, based on a C_0 = 0.380 pF. Figure 4.5 shows the "uncorrected" 300 K mobility as a function of N_{inv}, for a range of drain biases. The large suppression of inferred mobility at higher V_{ds} can clearly be seen, especially at low N_{inv}, confirming the necessity of extrapolating to V_{ds} = 0 V.

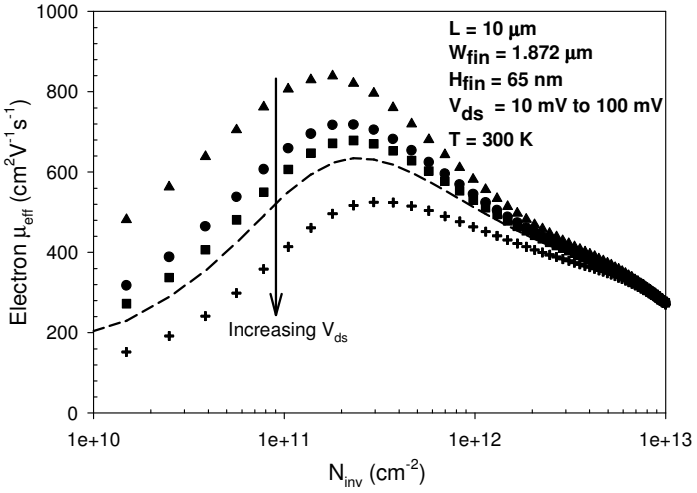

Figure 4.5 Extracted mobility at 300 K showing the effect of increasing drain bias from 10 mV to 100 mV

As V_{ds} is increased, Q_{inv} decreases for a given V_{gs} due to the channel pinch off effect -which becomes increasingly prevalent the smaller $V_{gs} - V_{ds}$. This manifests itself as an increase in V_t – seen by the shift in I_d in Figure 4.1b) and the extracted V_t in Figure 4.6. The extracted mobility decreases as the measured Q_{inv}, is larger than during an I_d measurement.

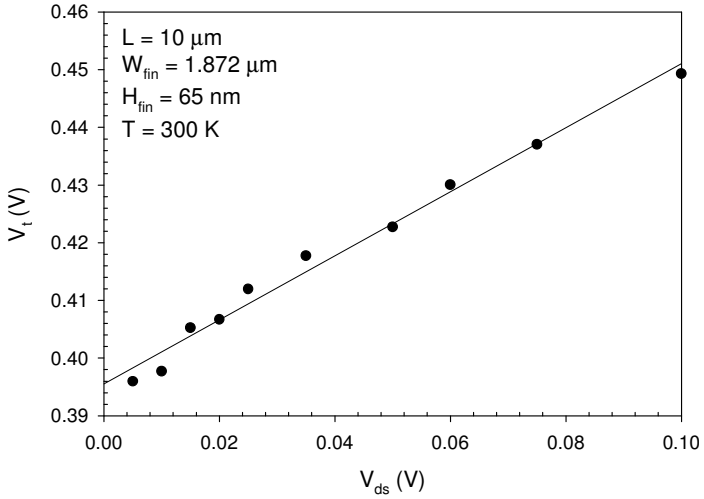

Figure 4.6 Threshold voltage extracted from the max slope of transconductance measured as a function of drain bias

The conductivity (g_d and I_d/V_{ds}) at V_{ds} = 0 V was extracted over the entire V_{gs} range. Figure 4.7 and Figure 4.8 show examples of the regression used in sub-threshold, at V_{gs} = 0.225 V, and in strong inversion at V_{gs} = 0.70 V, respectively. In each case we see the predicted straight line behavior and are able to extract a conductance value for V_{ds} = 0 V. Figure 4.7 has the correct slope of -38 V^{-1} and typical regression coefficients are better than 0.98, indicating high accuracy. Note that the conductance in strong inversion (where carrier mobility is often reported) is already 8% lower at the standard measuring bias of V_{ds} = 50 mV than at V_{ds} = 0 V.

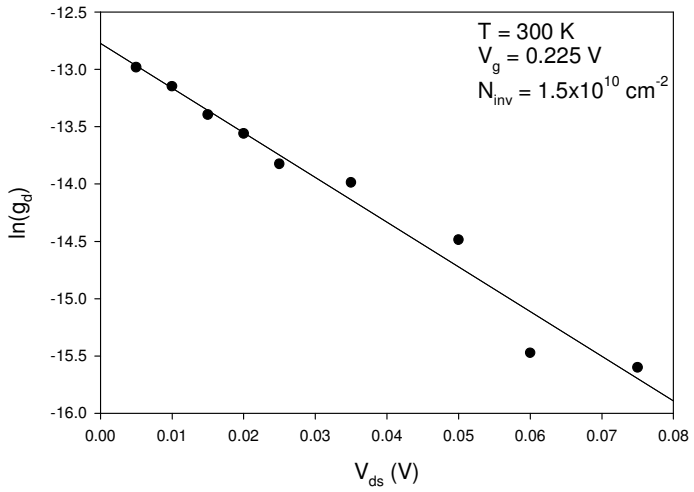

Figure 4.7 Semi-log variation of drain conductance with drain bias in the sub-threshold region enabling the zero bias conductance to be extracted as the intercept

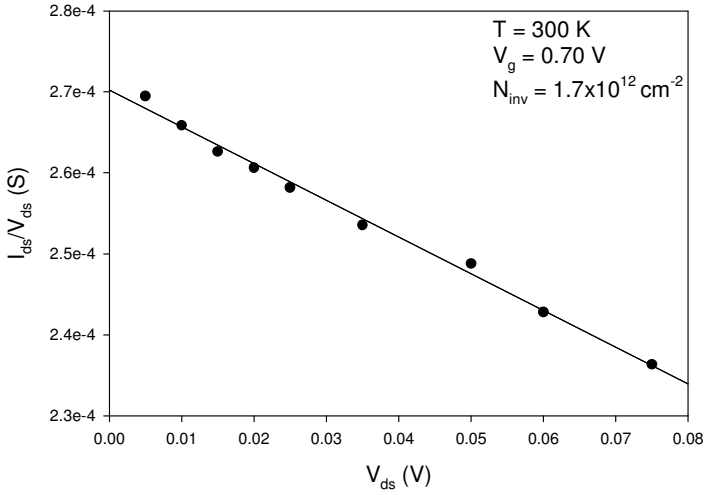

Figure 4.8 Variation of drain current with drain bias in strong inversion from which the zero bias conductance can be extrapolated

Having extracted the zero bias conductance values corresponding to each inversion charge density, and considering that the diffusion and E_x-field corrections cancel, μ_{eff} can be calculated accurately as shown in Figure 4.9.

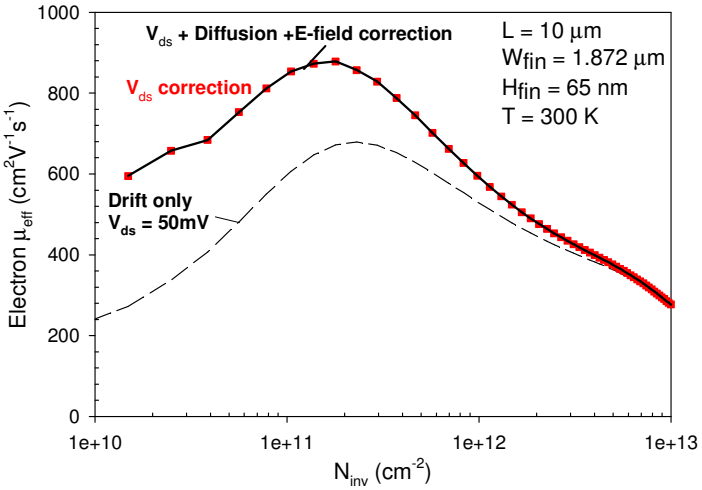

Figure 4.9 300 K mobility showing the effect of the various corrections

Although μ_{eff} may not be accurate for N_{inv} ~10^{10} cm^{-2} some intuitive understanding can still be gained. The fall in μ_{eff} to the left of the peak in Figure 4.9 may be partially due to fast trapping processes that affect the CV measurement.[148, 151] Nevertheless, μ_{eff} at 300 K shows a tendency to be independent of N_{inv}, which is sensible in that it is consistent with the theory of interface charge scattering of non-degenerate carriers[17] and measurements of geometric magnetoresistance[175-176] on SiO_2 gated SOI transistors, which are not subject to trapping effects. Where geometric magnetoresistance methods are not available, it may still be possible to obtain meaningful μ_{eff} data from improved measurements of N_{inv}. Although a measurement frequency is used at which it is expected that most of the traps will be unable to respond, trapping effects may be further suppressed by inversion charge pumping[177] or by RF CV measurements.[149] Other useful approaches combine CV techniques with modelling[150, 178]. Furthermore, there maybe MOSFETs for which fast trapping is not an issue, for example, in state of the art CMOS

technologies. With these provisos, the principles established in this work could have wider applicability.

Chapters 5 and 6 include modelling of μ_{eff} at 4 K. Therefore, it is important to assess the significance of V_{ds} on the extraction of μ_{eff}, as this may lead to incorrect fitting parameters in the modelling. Figure 4.10 shows the "uncorrected" 4 K μ_{eff} as a function of N_{inv}, for a range of V_{ds}. Possible corner inversion in the device at low temperature prevented accurate μ_{eff} extraction below N_{inv} = 7x10^{11} cm^{-2}.[179] Nevertheless μ_{eff} still strongly depends on V_{ds}. At 4 K, we also obtain good linear fits from which to extract zero bias conductivity values as shown in Figure 4.11. The corrected mobility is shown in Figure 4.12.

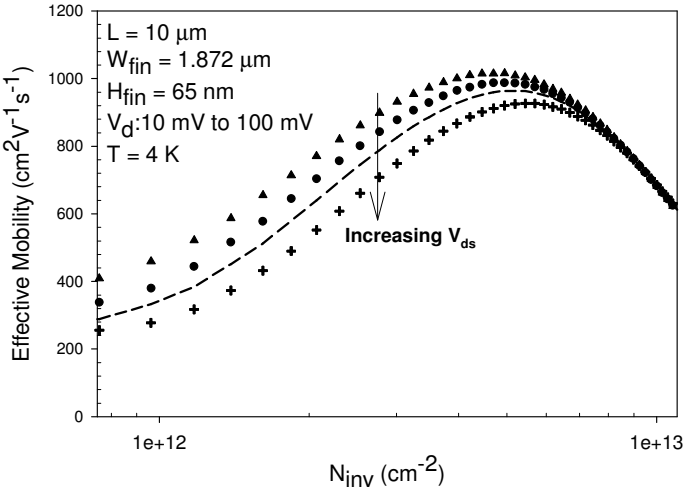

Figure 4.10 4 K extracted mobility showing the effect of increasing drain bias from 10 mV to 100 mV

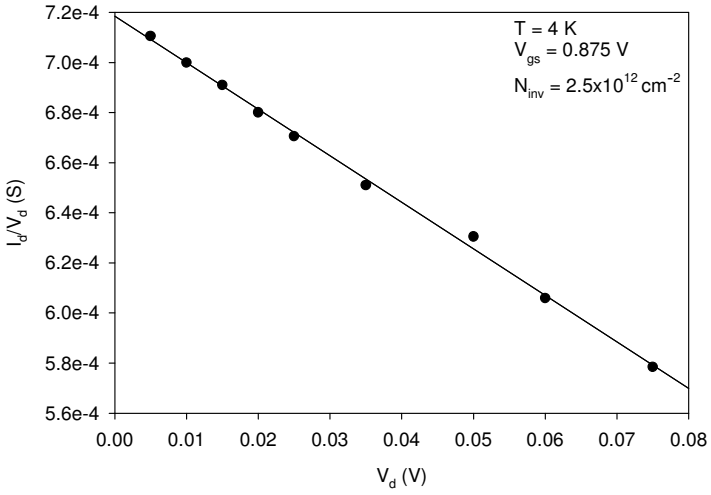

Figure 4.11 I_d/V_{ds} in strong inversion at 4 K

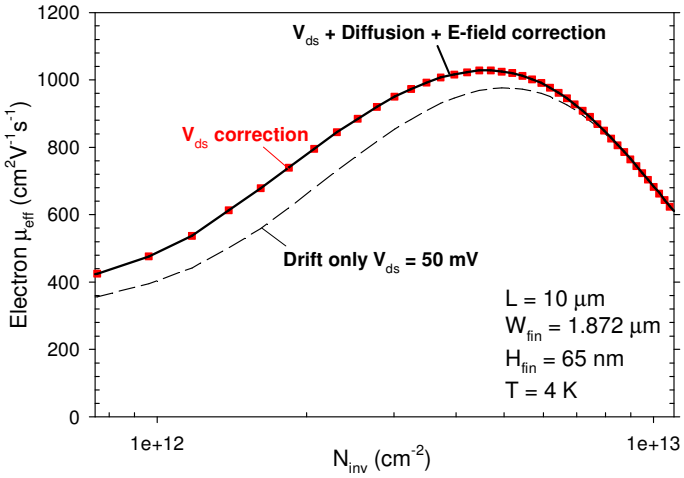

Figure 4.12 4 K effective mobility showing the effect of the various corrections

It must be pointed out that it may be possible to extract the mobility without needing to apply the V_{ds} correction. Providing I_d can be measured using a very low V_{ds} ~5 – 10 mV (i.e. noise is not an issue due to measuring equipment, device contacts etc.) the extraction may be sufficiently accurate. However this should be checked by applying the V_{ds} correction on at least one device for the batch under examination.

4.6 Summary

In this chapter, the theory and extraction of the low field effective channel mobility has been analysed. Typical mobility calculations ignore the variation in the field along the channel, carrier diffusion and the absence of drain bias during C_{gc}-V_{gs} measurements. A novel regression technique was proposed to extrapolate the drain conductance to $V_{ds} \to 0$, without relying on any elaborate measurement technique, to correct for the difference in drain bias between the I_d-V_{gs} and C_{gc}-V_{gs} measurements. Corrections for the variation in the field along the channel and carrier diffusion, included in the analysis, are shown to cancel in the limit $V_{ds} \to 0$. The effective mobility was subsequently extracted on a FDSOI MOSFET at room temperature and at 4 K. Not correcting for the difference in drain bias leads to significant error. Thus, accurate mobility is obtained using the drift only expression with the drain conductance correction, providing the inversion charge is known accurately.

Chapter 5 : Si MOSFETs on (100) and (110) orientated substrates

5.1 Introduction

CMOS technology has conventionally been fabricated on (100) orientated substrates/wafers, as the bandstructure in this orientation maximises the electron mobility. Secondly the interface trap density at the SiO_2/Si interface is generally lowest on this orientation. The conventional channel direction for MOSFETs is along the <110> direction. However, there is growing interest in fabricating MOSFETs on (110) orientated substrates, as the band structure in this orientation maximises hole mobility – over double that of (100) substrates.[29, 180-184] Unfortunately, in this case, electron mobility is reduced by half.[155, 185] To get the best of both worlds, IBM's hybrid orientation technology (HOT)[181-182] utilises both the (100) and (110) orientations for n- and p-MOSFETs respectively. However, despite the extensive number of publications on carrier transport in p-MOSFETs, understanding of hole mobility currently lags behind electron mobility, due to the complicated nature of the valence band.[26-31]

The results on the electrical characterisation of n- and p-MOSFETs fabricated on bulk (100) and (110) wafers over the full range of channel directions are presented in

this chapter. Emphasis is placed on understanding the dependence of mobility on orientation, channel direction and E_{eff}/N_{inv}.

5.2 Device overview.

The MOSFETs were fabricated at KTH, Royal Institute of Technology, Sweden on 100 mm diameter wafers. The main process steps are as follows.

Phosphorus and boron implants formed N and P-wells for the substrates of the p- and n-MOSFETs respectively. The implant doses were $1x10^{13}$ cm^{-2} of phosphorus at 300 keV and $1x10^{13}$ cm^{-2} of boron at 100 keV. In both cases the intentional doping concentration was ~10^{17} cm^{-3}. Dry thermal oxidation for 35 min at T = 700°C was then used to grow the SiO_2 gate dielectric. N+ polysilicon was deposited on the SiO_2 to form the gate itself with a projected thickness of 150 nm. The doping concentration of the n+ poly gate was ~10^{20} cm^{-3}, measured by the author from the resistivity of a van der Pauw structure. Source and drain regions were formed by implanting with $2x10^{15}$ cm^{-2} of arsenic at 50 keV and $1x10^{15}$ cm^{-2} of boron at 4.5 keV for the n- and p-MOSFETs respectively. A 950°C rapid thermal anneal for 30 seconds followed to activate the dopants. Connections to the gate, source, drain and substrate and their contact pads were formed by depositing 12 nm of Ni followed by sputtering TiW and then Al.

5.2.1 Device layout

Each wafer is divided up into chips 5 mm square, each containing a host of process control/test structures and MOSFETs. The MOSFETs are divided into two arrays; the variable size (VS) array and the orientated angle (OA) array. In the variable size array channel lengths, and widths, vary from 0.5 μm to 200 μm, and 10 μm to 100 μm, respectively. In the OA array, MOSFETs have a fixed size (W = 4.7 μm and L = 25 μm) with channel directions varying by 178°. 0° is parallel to the wafer flat, corresponding to the <110> and <112> directions for the (100) and (110) wafers respectively. The test structures consist mainly of diodes, van der Pauw and Kelvin structures. The majority of the I_d-V_{gs} measurements were performed with V_{gs} swept from 0 to -4 V and -0.5 V to 3.5 V for the p- and n-MOSFETs respectively with $V_{ds} = \pm 10mV$. Most of this chapter focuses on the OA MOSFETs. Firstly, I_d-V_{gs} measurements on 10-20 10 μm x 10 μm p-MOSFETs were measured on different chips across each wafer to check device uniformity and locate the region of the best performing devices. A plot of peak g_m vs V_t is shown in Figure 5.1a) This single plot is a very useful way to quickly identify overall device performance as it not only shows any variation in V_t and peak g_m, the latter essentially a measure of mobility, but identifies any correlation between the two. Beer[147] shows that correlation between V_t and peak g_m across a wafer can be caused by a systematic variation in D_{it}.- Regions with high values of D_{it} caused large shifts in V_t and degraded the mobility. Figure 5.1b) lends some support to this theory as higher values of D_{it} also increase the sub-threshold slope which we observe.

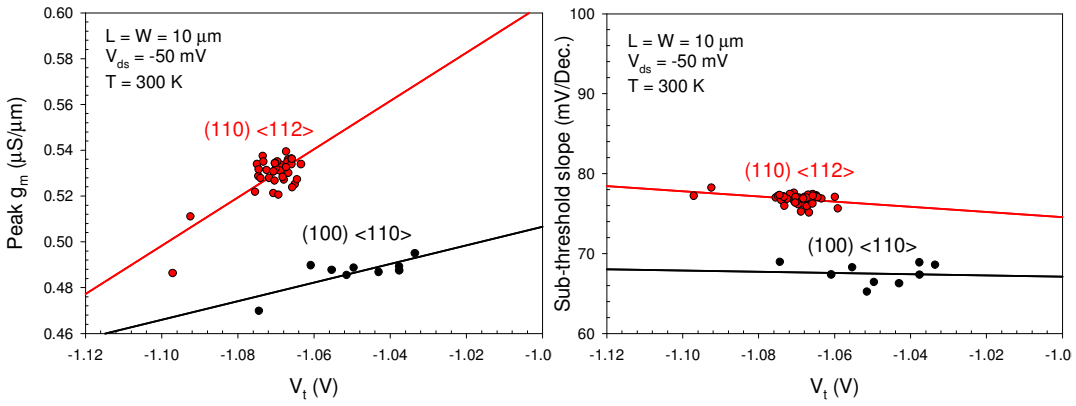

Figure 5.1 a) Peak g_m vs V_t b) S.S. vs V_t measured on 10 µm x 10 µm p-MOSFETs across the (100) and (110) wafers. The variation in peak g_m is 5% and 10% for the (100) and (110) wafers indicating good uniformity. A more negative V_t is correlated to a smaller peak g_m and higher S.S. most probably due to a variation in D_{it}.

Chips containing the best performing MOSFETs (highest peak g_m) were subject to detailed investigation upon which the rest of this chapter is based.

5.3 Capacitance – voltage measurements

5.3.1 Split CV

Split CV measurements were performed on 50 µm x 50 µm, 100 µm x 100 µm, 200 µm x 100 µm and 25 µm x 4.7 µm n- and p-MOSFETs on both wafers. This was necessary to check the capacitance scaled with area between the devices, and also to identify any size related measurement problems (e.g. high gate leakage current, frequency dispersion due to slow minority carrier response). Measurements were performed using frequencies of 100 Hz, 10 kHz, 100 kHz, 500 kHz and 1 MHz. The

size and frequency dependences on capacitance are now shown for the (100) p- and n-MOSFETs.

(100) p-MOSFETs

For frequencies exceeding 10 kHz, clear dispersion is present in inversion for the 100 µm x 100 µm and 200 µm x 100 µm p-MOSFETs due to the large channel time constants associated with the long channel lengths. Figure 5.2 compares C_{gc} between 100 µm x 100 µm and 25 µm x 4.7 µm (100) p-MOSFETs. For the large MOSFET, the measurement frequency should be less than 12 kHz (calculated using equation (3.6)) in weak inversion (V_{gs} = - 1 V) to ensure the minority carriers have sufficient time to respond.

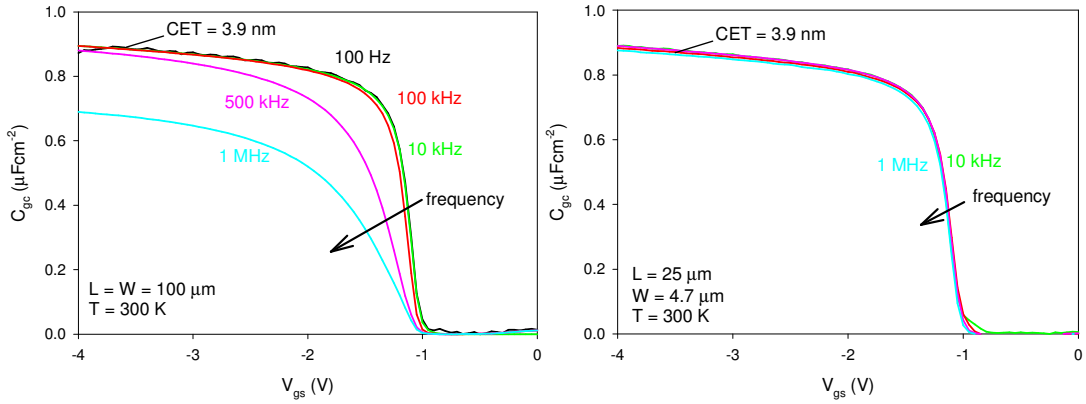

Figure 5.2 C_{gc} as a function of frequency for 100 µm x100 µm and 25 µm x 4.7 µm (100) p-MOSFETs

In the case of the 25 µm x 4.7 µm MOSFET, the measurement frequency should be no greater than 100 kHz. However below 10 kHz, measurement noise was unacceptably high and is not shown. Providing a suitable frequency was chosen, the

capacitance scaled with area between MOSFETs indicating uniform oxide growth, with a CET of 3.9 ± 0.1 nm.

Measurement noise prevented reliable C_{gb} measurements on devices smaller than 50 µm x 50 µm even for frequencies of 1 MHz. This is unusual considering the relatively large area of the device. Since the devices are not isolated from the wafer bulk, perhaps coupling of thermal noise from the wafer/substrate chuck to the substrate well is responsible.[186-187] Thus C_{gb} was measured on the 100 µm x 100 µm MOSFETs. Figure 5.3 shows the split CV of a 100 µm x 100 µm p-MOSFET and the C_{gc} branch of a 25 µm x 4.7 µm p-MOSFET for comparison. The phase angles also shown are close to 90° over most of the data range.

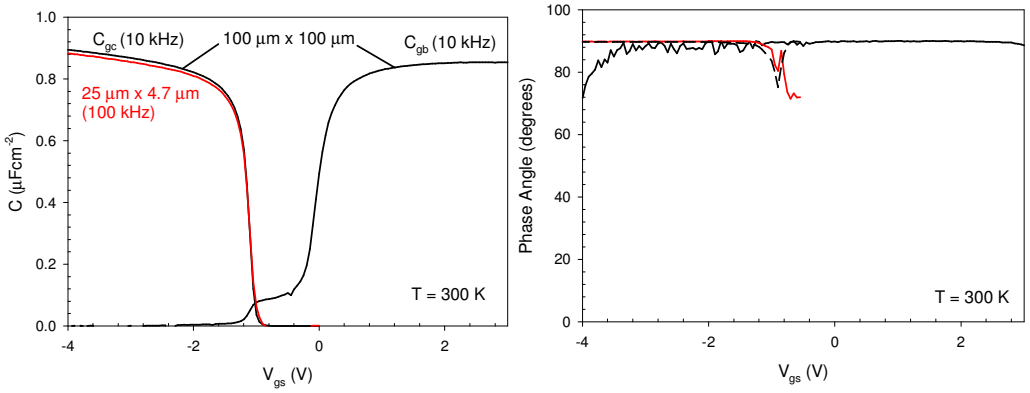

Figure 5.3 Split CV and phase angles for a (100) 100 µm x 100 µm p-MOSFET. C_{gc} branch from 25 µm x 4.7 µm p-MOSFET included for comparison

(100) n-MOSFETs

Figure 5.4 compares C_{gc} between 100 µm x 100 µm and 25 µm x 4.7 µm (100) n-MOSFETs. A CET of 4.1 ± 0.1 nm was measured in strong inversion. Frequency

dispersion was considerably lower than for the p-MOSFETs as electrons respond more quickly than holes, due to their higher mobility. No dispersion was observed for the 25 µm x 4.7 µm n-MOSFET. However, the n-MOSFETs have a higher gate leakage current. This is manifested clearly for the 25 µm x 4.7 µm MOSFET, visible by the noise at high V_{gs} for a frequency of 10 kHz. In this case, a frequency of ~500 kHz was necessary to reduce the capacitive reactance for the LCR meter to accurately measure the quadrature current and calculate the correct capacitance.

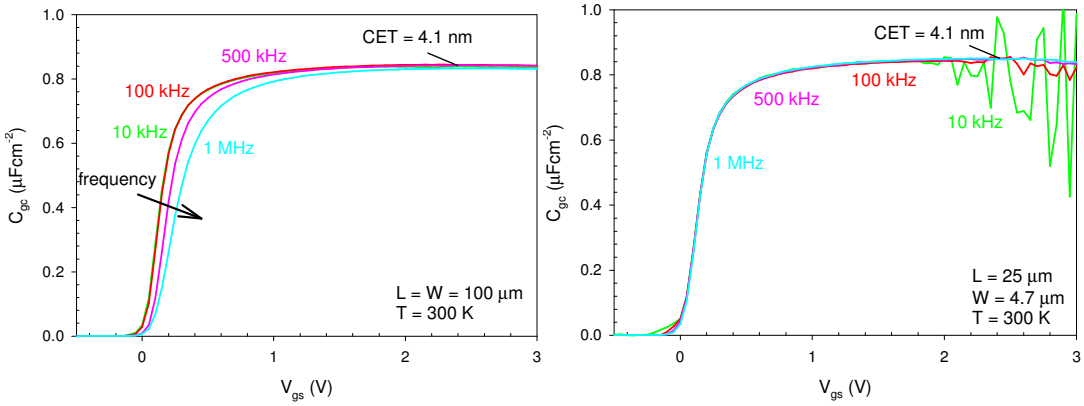

Figure 5.4 C_{gc} measured as a function of frequency for 100 µm x 100 µm and 25 µm x 4.7 µm (100) n-MOSFETs. Measurement noise was unacceptably high for frequencies below 10 kHz. No frequency dispersion was observed in the 25 µm x 4.7 µm n-MOSFET.

The C_{gb} and C_{gc} branches of the 100 µm x 100 µm n-MOSFET are shown together in Figure 5.5. The corresponding phase angles are also shown.

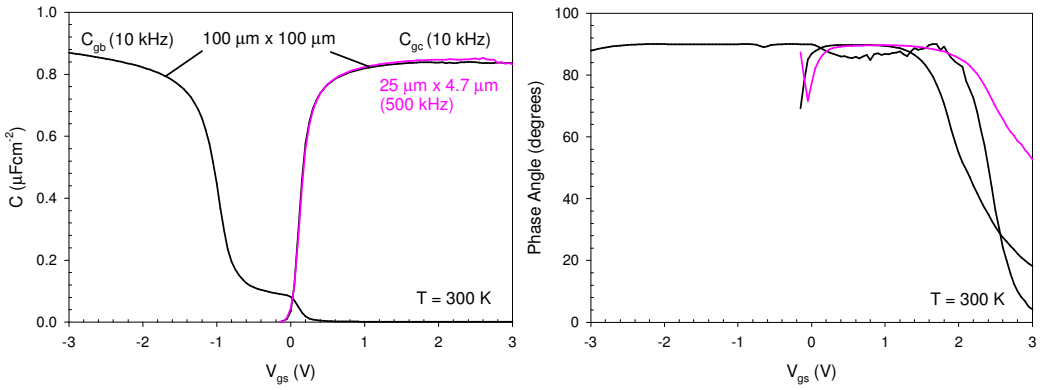

Figure 5.5 a) Split CV for the (100) 100 µm x 100 µm n-MOSFET and the C_{gc} branch for the 25 µm x 4.7 µm n-MOSFET. b) Corresponding phase angles. The drop at high V_{gs} is due to gate leakage current

Now the intricacies of the capacitance measurement have been discussed, we can compare the split CV between the (100) and (110) n- and p-MOSFETs. These are shown in Figure 5.6. CET is higher on the (110) wafer due to the faster oxidation rate of (110) Si.[180, 188] On each wafer, CET between the n- and p-MOSFETs are within error of each other with no obvious difference due to quantum confinement, which is probably insignificant to the relatively thick oxides. On the (100) wafer, quantum confinement would result in a larger CET for the p-MOSFET compared with the n-MOSFET. This can be understood by considering the occupation of the dominant sub-bands. At 300 K ~60% of electrons occupy the Δ_2 valleys (m_{conf} = $0.916m_0$) when N_{inv} ~ 10^{12} cm^{-2} (V_{gs} = 0.4 V)[189] thus are confined closer to the interface than holes (HH m_{conf} ~ $0.29m_0$). On the (110) wafer, a higher CET for the n-MOSFET might be anticipated as electrons in the Δ_4 valleys (m_{conf} = $0.315m_0$), are confined further from the interface than holes (HH $m_{conf} > 1m_0$ see Figure 5.25).

No significant depletion of the n+poly Si gate was evident, due to its high doping. This is usually identified by a steep decrease in the capacitance in inversion and in accumulation for the n- and p-MOSFETs respectively.[2]

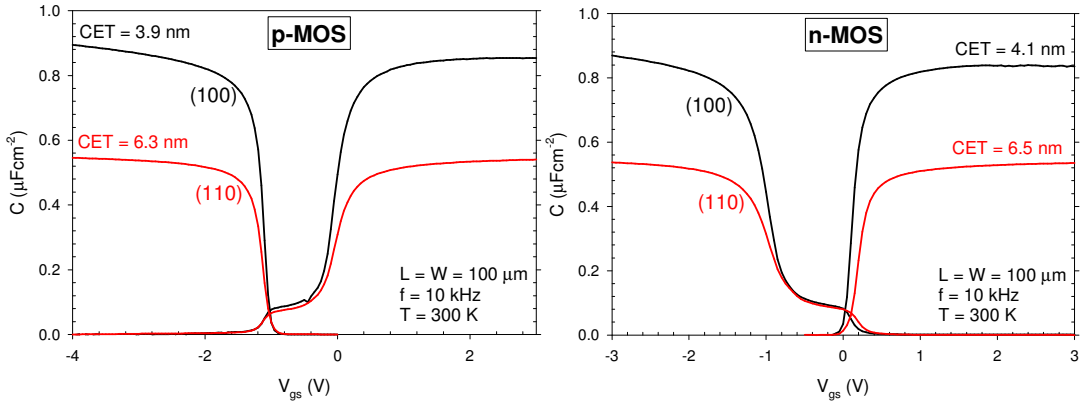

Figure 5.6 Split CV characteristics for the p- and n-MOSFETs on the (100) and (110) orientations

5.3.2 Flat-band voltage and interface trap density

The work function difference between the n+poly Si gate and substrate, and oxide charge near the SiO_2/Si interface create a built in field across the oxide and SiO_2/Si interface (band bending). V_{fb} compensates for this field. The values are shown in Table 5.1.

	(100) V_{fb}	(110) V_{fb}
nMOS	-0.9 V $\pm 0.05V$	-0.9 V $\pm 0.05V$
pMOS	-0.1 V $\pm 0.05V$	-0.1 V $\pm 0.05V$

Table 5.1 Flat-band voltages for n- and p-MOSFETs on (100) and (110) orientations. Since V_{gs} was incremented in 50 mV steps, V_{fb} is accurate to within 50 mV.

Following the approach by Witczak *et al.*[190], D_{it} was extracted using the high-low frequency, conductance and sub-threshold slope techniques (techniques described in section 3.4.1). Figure 5.7 shows the D_{it} as a function of energy in the silicon band gap, for both the n- and p-MOSFETs. The conductance technique, usually applicable from flat-band to weak inversion, could only be applied over a narrow range of the band-gap on these MOSFETs. This might be due to the limitation of the LCR meter in separating the in-phase current, (from which the conductance is calculated), from the quadrature current. The large quadrature current, due to the large MOSFET area, may be masking the in-phase current over most of the energy range.

As expected for a (100) SiO_2/Si interface, D_{it} exhibits a "U" shaped distribution with energy, with mid-gap values within the range low 10^9 to low 10^{10} $cm^{-2}eV^{-1}$. Previous studies have measured such values on (100) SiO_2/Si interfaces using the conductance technique.[14] However it should be pointed out that the mid-gap values extracted using the high-low frequency technique here, are likely to be in error. The resolution limit of the high-low frequency technique depends on C_{it}/C_{dep} i.e. on band bending and doping concentration. For a doping concentration of 10^{17} cm^{-3}, Nicollian and Brews[14] calculate the minimum D_{it}, that can be measured to within an accuracy of 10% at mid-gap, is $9x10^{10}$ $cm^{-2}eV^{-1}$. A further error occurs close to flat-band, marked by the shaded regions, where significant round off error due to the subtraction of the low and high frequency capacitances occurs.

Note the good agreement between techniques towards the minority band edges where the high-low frequency technique is most accurate and where the conductance and sub-threshold slope techniques could be applied. Oxidation of a (110) surface results in a higher D_{it} than on a (100) surface due to a higher density of surface atoms and available bonds.[181, 191] The apparent lower D_{it} near mid-gap, may be due to the low resolution of the high-low frequency technique as already discussed.

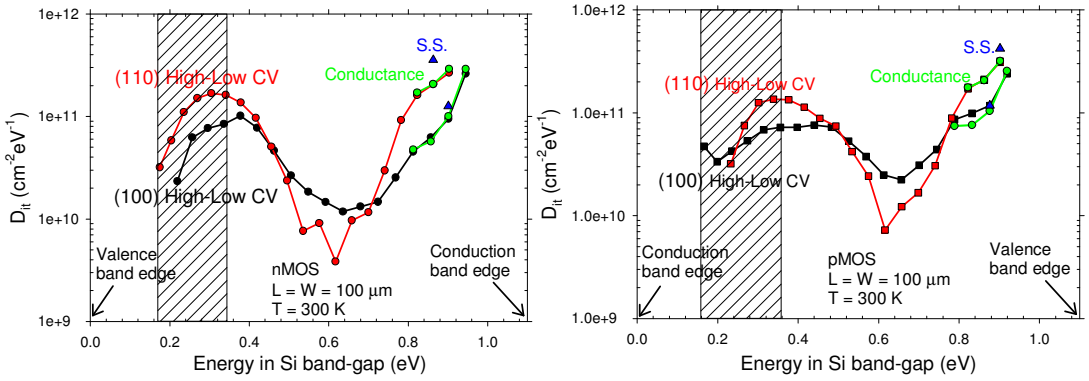

Figure 5.7 D_{it} extracted on 100 µm x 100 µm n- and p-MOSFETs as a function of silicon band gap energy. Shaded areas indicate regions close to flat-band where large round-off errors can occur due to the subtraction of high and low frequency capacitances.

5.3.3 Substrate doping profiles

Figure 5.8 shows the extracted doping profiles for the n-well and p-well substrates, corresponding to the p- and n-MOSFETs respectively. The doping is fairly uniform with an average concentration of $8x10^{16}$ cm^{-3} for both n- and p-wells on both wafers.

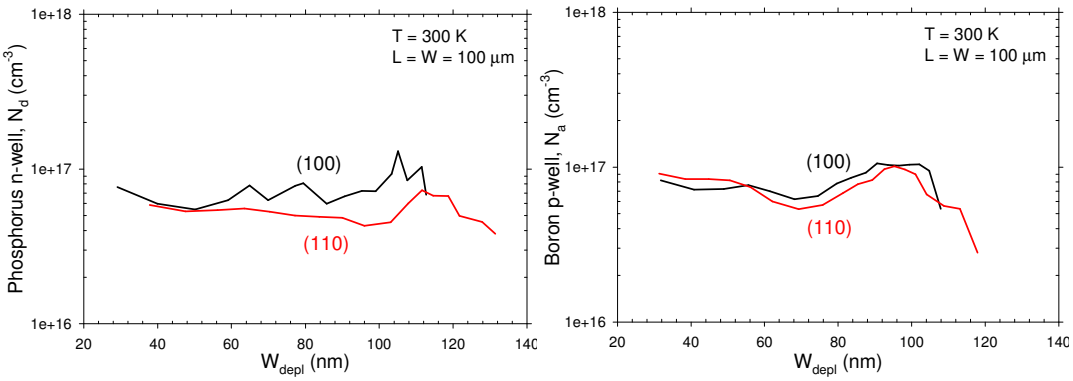

Figure 5.8 Extracted doping profiles for 100 µm x 100 µm n- and p-MOSFETs on (100) and (110) orientations

5.4 Extraction of R_{sd} and ΔL

It was expected that R_{sd} and ΔL would be negligible fraction of the total resistances and channel lengths. Nevertheless, R_{sd} and ΔL extractions were performed to check this was the case. MOSFETs with channel lengths of 0.5 µm, 0.8 µm, 1 µm and 3 µm and width 10 µm were used in the extractions. Excellent linear regressions (coefficients of determination close to 1) enabled R_{sd} and ΔL to be extracted with high accuracy for the n- and p-MOSFETs on both wafers. As an example, Figure 5.9 shows the R_{sd} and ΔL extraction for the (100) p-MOSFETs. The complete set of results is summarised in Table 5.2.

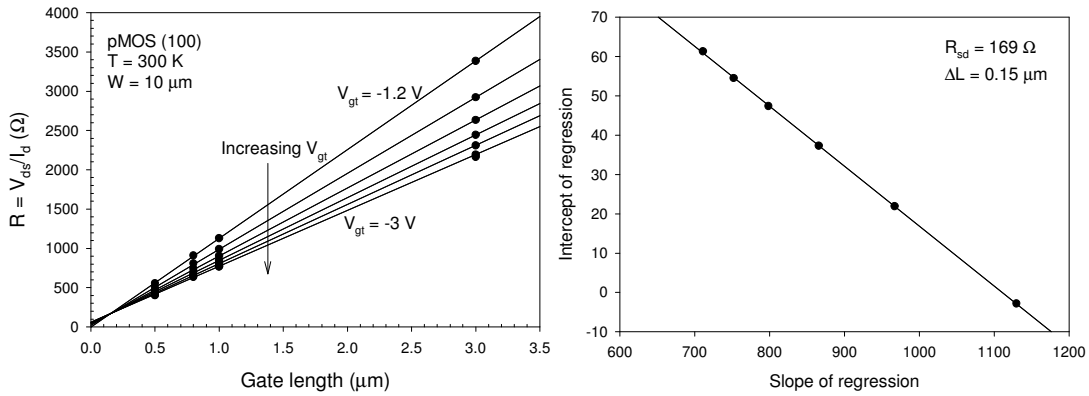

Figure 5.9a) Linear regressions ($V_{gt} = V_{gs} - V_t$) and b) second regression to extract R_{sd} and ΔL for (100) p-MOSFETs.

	(100)			(110)		
	R_{sd} (Ωµm)	ΔL (µm)	$R=V_{ds}/I_d$ (Ωµm)	R_{sd} (Ωµm)	ΔL (µm)	$R=V_{ds}/I_d$ (Ωµm)
nMOS	830	0.05	~10^5	150	0.04	~10^5
pMOS	1690	0.15	~10^6	1080	0.14	~10^5

Table 5.2 Summary of R_{sd} and ΔL for the n- and p-MOSFETs on (100) and (110) wafers. Total resistance, R is for the OA 25 µm x 4.7 µm MOSFETs in strong inversion

Total resistance, *R* has been calculated for 25 µm long devices in strong inversion with $V_{ds} = \pm 10mV$. The results show that R_{sd} and ΔL make up negligible fraction of *R* and *L* and therefore do not need to be accounted for in any further analysis. The p-MOSFETs exhibit higher values of R_{sd} and ΔL than the n-MOSFETs. This can be explained by considering that boron diffuses more easily than arsenic,[192] (due to its smaller mass) during the 30 second 950° RTA. The greater diffusion reduces the abruptness of the junction resulting in a higher R_{sd}[193-194] and ΔL, the latter due to diffusion under the gate. In addition boron diffusion is faster for (100) compared to

(110) Si[195] which might explain the higher R_{sd} and ΔL for the (100) p-MOSFETs. The same mechanism may also explain the same trend in the n-MOSFET data.

5.5 p-MOSFET current – voltage measurements

For the remainder of the chapter, we now focus on the orientated angle (OA) MOSFETs. A large number of I_d-V_{gs} measurements with V_{ds} = -10 mV over the whole range of channel directions were performed to extract g_m, V_t, *S.S.* and μ_{eff}. Typically, I_{on}/I_{off} ratios of 10^8 were measured, (I_{on} corresponding to I_d at $V_{gt} = V_{gs} - V_t$ = -2.5 V), indicating good switching behaviour which comes as no surprise considering the long channel lengths. Gate leakage current was always at least 4 orders of magnitude lower than I_d on the (100) wafer and 7 orders of magnitude lower on the (110) wafer. I_d is highest along the <100> and <110> directions on the (100) and (110) orientations respectively. I_d-V_{gt} for these directions and orientations are shown in Figure 5.10.

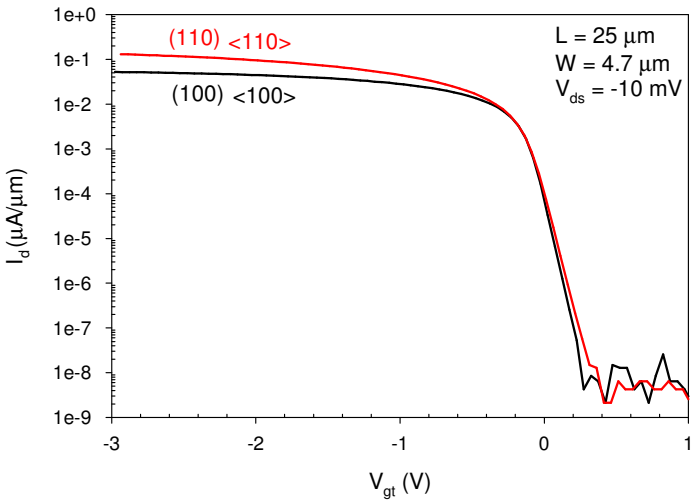

Figure 5.10 Linear I_d vs V_{gt} characteristic for 25 µm x 4.7 µm (100)/<100> and (110)/<110> p-MOSFETs

5.5.1 Transconductance

Figure 5.11 a) shows peak g_m, normalised by channel width, as a function of channel direction and Figure 5.11 b) shows the full g_m characteristics for a select range of channel directions as a function of V_{gt}. Peak g_m is a measure of mobility, which can be seen by differentiating equation (2.13) with respect to V_{gs}. The (110)/<110> MOSFET shows a 54% enhancement over the (100)/<110> MOSFET despite its thicker gate oxide. For the (110) wafer, a 50% variation in peak g_m between the <110> and <100> directions is observed. Whereas for the (100) wafer, a 3% variation between the <100> and <110> directions is observed. The variation on each wafer is due to the anisotropic m_{tran}, therefore hole mobility. (Hole mobility is analysed in section 5.7.3 to 5.7.5). A striking feature is the difference in degradation of g_m between the two wafers above a V_{gt} of -0.3 V.

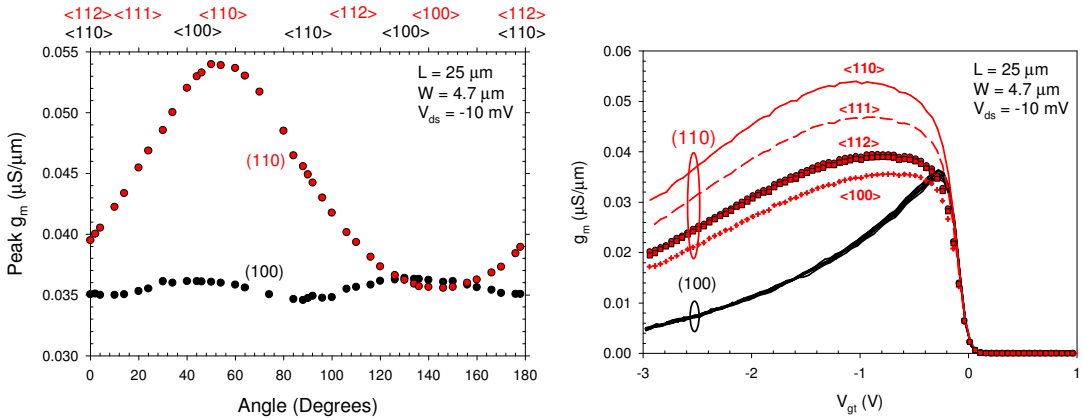

Figure 5.11 a) Peak g_m vs channel direction/angle b) g_m vs V_{gt} for 25 µm x 4.7 µm (100) and (110) p-MOSFETs

5.5.2 Threshold voltage

Figure 5.12 shows V_t, calculated from the maximum slope of g_m, as a function of channel direction. For both wafers, V_t is independent of channel direction with V_t = -1.02 V and -1.06 V extracted for the (100) and (110) wafers respectively. Inserting V_{fb} = 0.1 V, which accounts for the small difference in Fermi-levels between the n+ poly gate and n-type substrate, N_d = 8x10^{16} cm^{-3} and C_{ox} = 0.90 µFcm^{-2} for the (100) wafer and C_{ox} = 0.54 µFcm^{-2} for the (110) wafer, which accounts for difference in oxide thickness and confinement, into equations (2.4) and (2.6), gives V_t = -1.03 V and -1.13 V which are very close to the extracted values.

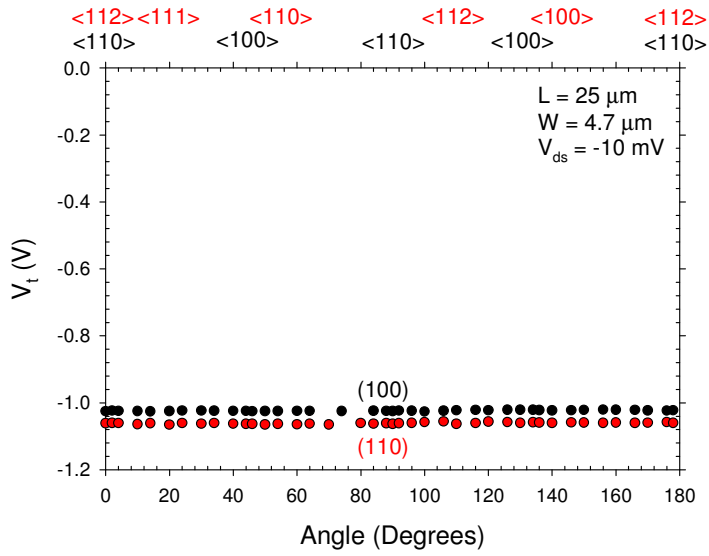

Figure 5.12 V_t vs channel direction/angle for 25 µm x 4.7 µm (100) and (110) p-MOSFETs

5.5.3 Sub-threshold slope

Figure 5.13 shows the sub-threshold slope as a function of channel direction. For both wafers, *S.S.* is independent of channel direction with *S.S.* = 70 mV/Dec. and 78 mV/Dec extracted for the (100) and (110) wafers respectively. The increase above the ideal *S.S.* of ~ 60 mV/Dec is due to D_{it}, slightly higher for the (110) wafer, which degrades the ability for the device to switch from the off state to the on state and vice versa. The slight scatter in the data is due to some of the devices anomalously exhibiting higher off current, the origin of which is unknown and unimportant in this work.

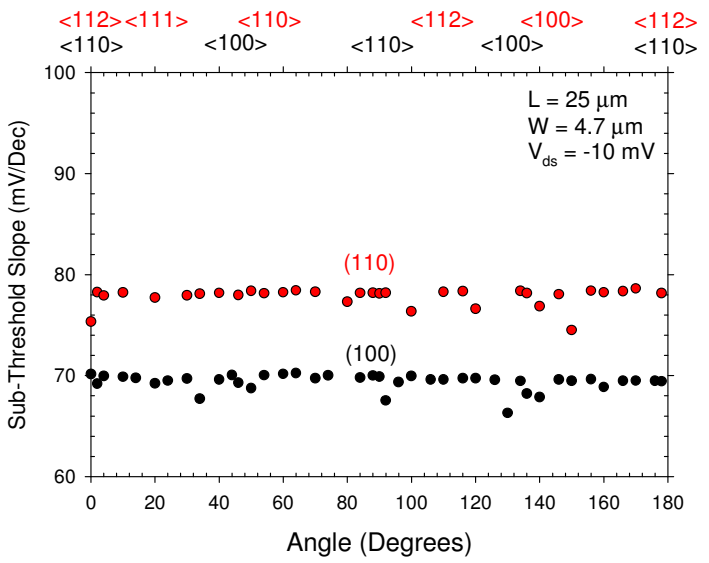

Figure 5.13 Sub-threshold slope vs channel direction/angle for 25 µm x 4.7 µm (100) and (110) p-MOSFETs

5.6 n-MOSFET current-voltage measurements

Following the same procedure on the p-MOSFETs, a large number of I_d-V_{gs} measurements over the whole range of channel directions were performed to extract g_m, V_t, *S.S.* and μ_{eff}. In all measurements $V_{ds} = 10$ mV. I_g was higher in the n-MOSFETs than the p-MOSFETs requiring the gate leakage current correction to be applied to I_d. At $V_{gt} = 2$ V, I_g was typically the same order of magnitude as I_d for the (100) wafer and 4 orders of magnitude lower for the (110) wafer. The higher I_g in this case as compared to the p-MOSFETs is most likely due to the smaller SiO_2 barrier at the minority carrier band edge (3.5 eV for n-MOSFETs compared to 4.4 eV for p-MOSFETs). I_d is highest on the (100) orientation where it is independent of channel direction. On the (110) orientation, I_d varies with channel

direction with its maximum along the <100> direction. Figure 5.14 shows I_d-V_{gt} characteristics for the (100)/<100> and (110)/<100> n-MOSFETs.

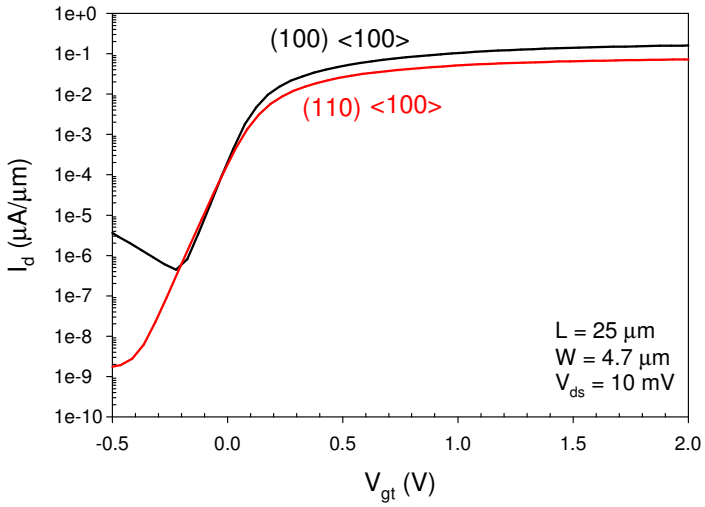

Figure 5.14 Linear I_d vs V_{gt} characteristic for 25 µm x 4.7 µm (100)/<100> and (110)/<100> n-MOSFETs

5.6.1 Transconductance

Figure 5.15a) shows the peak g_m normalized by channel width as a function of channel direction and Figure 5.15b) shows the full g_m characteristics for a select range of directions as a function of V_{gt}. For the (110) wafer, a 24% variation in peak g_m between the <100> and <110> directions is observed. Whereas for the (100) wafer, peak g_m is independent of channel direction. The (110)/<100> n-MOSFET shows a 48% decrease compared to the (100) n-MOSFETs, not accounting for the thicker oxide on the (110) orientation.

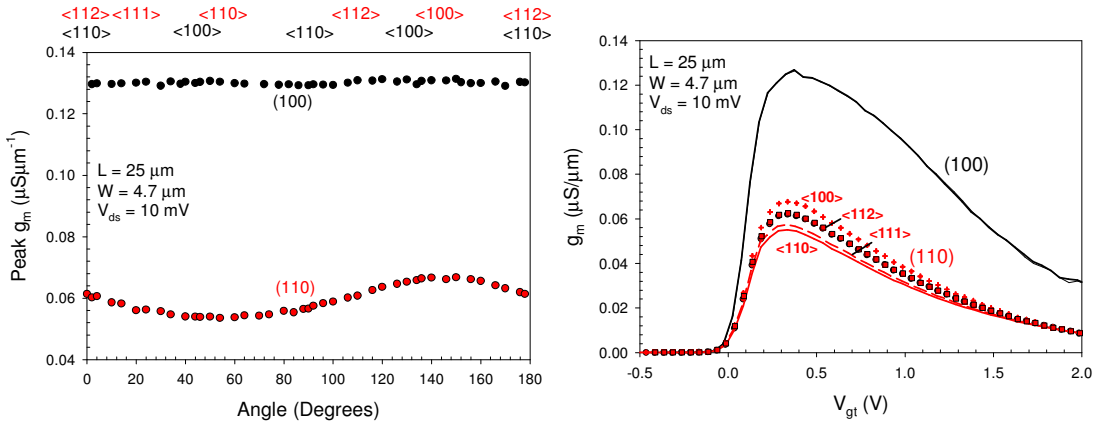

Figure 5.15 a) Peak g_m vs channel direction/angle b) g_m vs V_{gt} for 25 µm x 4.7 µm (100) and (110) n-MOSFETs

5.6.2 Threshold voltage

Figure 5.16 shows V_t for both wafers is independent of channel direction. V_t = 0.11 V and 0.02 V for the (110) and (100) wafers respectively. Unlike the p-MOSFETs, the n+ poly gate serves to deplete the substrate, resulting in very small values of V_t. From equations (2.4) and (2.6) we obtain V_t = 0.13 V for the (110) wafer and 0.03 V for the (100) wafer which are very close to the extracted values.

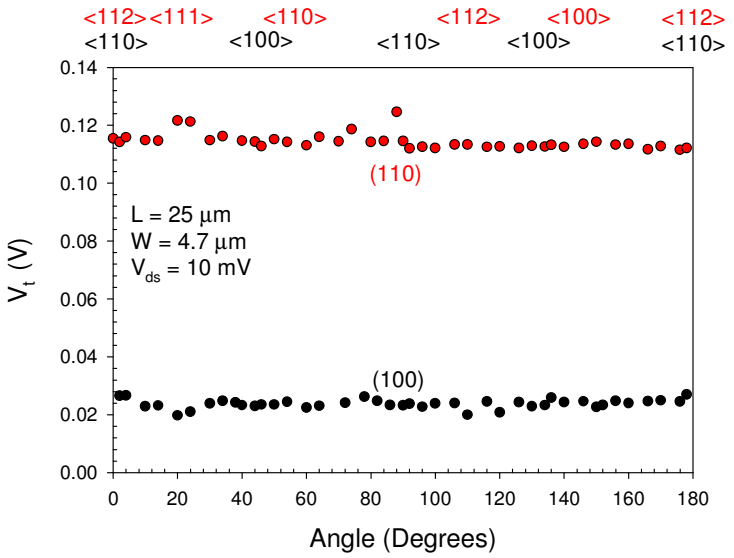

Figure 5.16 V_t vs channel direction/angle for 25 µm x 4.7 µm (100) and (110) n-MOSFETs

5.6.3 Sub-threshold slope

S.S. is shown in Figure 5.17. As for the p-MOSFETs, *S.S.* is independent of channel direction with values of ~71 mV/Dec and ~78 mV/Dec for the (100) and (110) wafers. Again, the scatter in the data is due to some devices exhibiting anomalously high off currents.

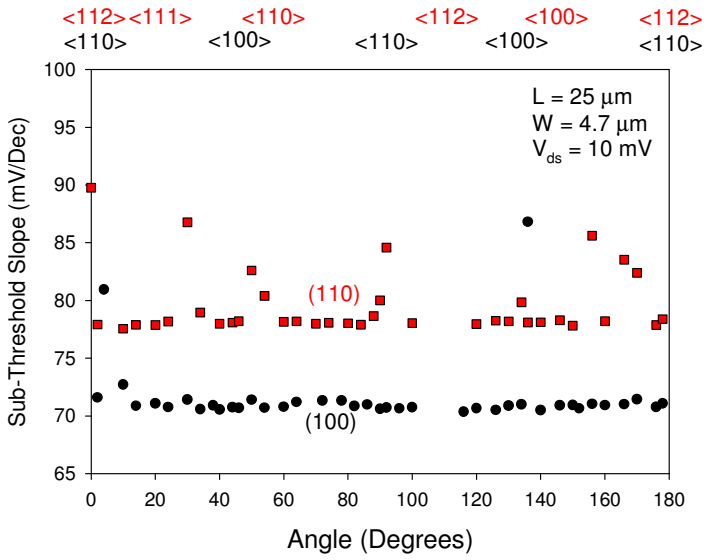

Figure 5.17 Sub-threshold slope vs channel direction/angle for 25 µm x 4.7 µm (100) and (110) n-MOSFETs

5.7 Effective mobility

The variation in I_d and g_m with channel direction and orientation is due to the variation in mobility. We now examine the dependence of effective mobility on surface orientation and channel direction. I_d-V_{gs} measured with $V_{ds} = \pm 10mV$ was sufficiently low that error in peak μ_{eff} due to the finite V_{ds} did not exceed 2%.

Remote charge and remote roughness scattering from the poly-Si/SiO_2[37, 71, 196-198] interface should be negligible for the oxide thicknesses in this work. Thus the mobility limiting scattering mechanisms are due to bulk phonons, ionised impurities in the substrate, interface charge and roughness from the SiO_2/Si interface. At 4 K, phonons are frozen out allowing a more detailed study of interface roughness, the

dominant cause of mobility degradation at high E_{eff}. Modelling of the 4 K mobility to extract the SiO_2/Si roughness parameters, Δ and Λ, for both (100) and (110) orientations, is presented in section 5.8.

5.7.1 n-MOSFETS - Variation of μ_{eff} with channel direction and surface orientation

The electron effective masses are reproduced in Table 5.3 for convenience.

Surface Orientation	<100> m_{tran}/m_0	<110> m_{tran}/m_0	m_{conf}/m_0	m_{scat}/m_0	g_v
(100)	0.190 0.190/0.916	0.190 0.315/0.553	0.916 0.190	0.190 0.417	Δ_2 Δ_4
(110)	0.190 0.916	0.553 0.190	0.315 0.190 (Modulated by confinement)	0.324 0.417	Δ_4 Δ_2

Table 5.3 Electron effective masses for the (100) and (110) orientations

Figure 5.18a) shows the peak mobility as a function of channel direction and Figure 5.18b) shows the mobility at E_{eff} = 0.6 MVcm^{-1}. The mobility on the (100) wafer is independent of channel direction with peak μ_{eff} ~ 455 cm^{2}V^{-1}s^{-1}. This can be explained by considering that quantum confinement between the oxide and conduction band splits the degeneracy of the Δ_2 and Δ_4 conduction band minima. Due to the large difference in m_{conf}, (m_{conf} = 0.916m_0 for Δ_2 and m_{conf} = 0.19m_0 for Δ_4) the majority of electrons populate the lower energy Δ_2 valleys which have circular constant energy contours in the *xy* plane (confinement in the *z* direction). Electrons thereby have m_{tran} = 0.19m_0 independent of channel direction and, for a

given E_{eff}, μ_{eff} is independent of channel direction. At E_{eff} = 0.6 MVcm^{-1}, interface roughness scattering dominates, reducing μ_{eff} to 350 cm^{2}V^{-1}s^{-1}.

The peak mobility on the (110) wafer varies by 26% depending on orientation; μ_{eff} = 336 cm^{2}V^{-1}s^{-1} along the <100> direction and 267 cm^{2}V^{-1}s^{-1} along the <110> direction. The variation can be explained by an anisotropic m_{tran}. Under confinement, the Δ_4 valleys are lower in energy than the Δ_2 valleys. Compared to the (100) orientation, the splitting is a lot smaller due to the small difference in confinement masses (m_{conf} = 0.315m$_0$ for Δ_4 and m_{conf} = 0.190m$_0$ for Δ_2) and at room temperature, a large percentage of electrons have sufficient energy to occupy the Δ_2 valleys. However, the μ_{eff} variation can be explained considering the more heavily populated, Δ_4 valleys.[24] From figure 2.5, m_{tran} is largest (0.553m$_0$) along the <110> direction, corresponding to the lowest μ_{eff} and lowest (0.19m$_0$) along the <100> direction, corresponding to the highest μ_{eff}. In the Δ_2 valleys, m_{tran} varies in the opposite direction (largest along the <100> (0.916m$_0$) and smallest along the <110> (0.190m$_0$) directions). Thus if the population of the Δ_2 valleys increases at the expense of the Δ_4 valleys, the μ_{eff} variation is reduced.

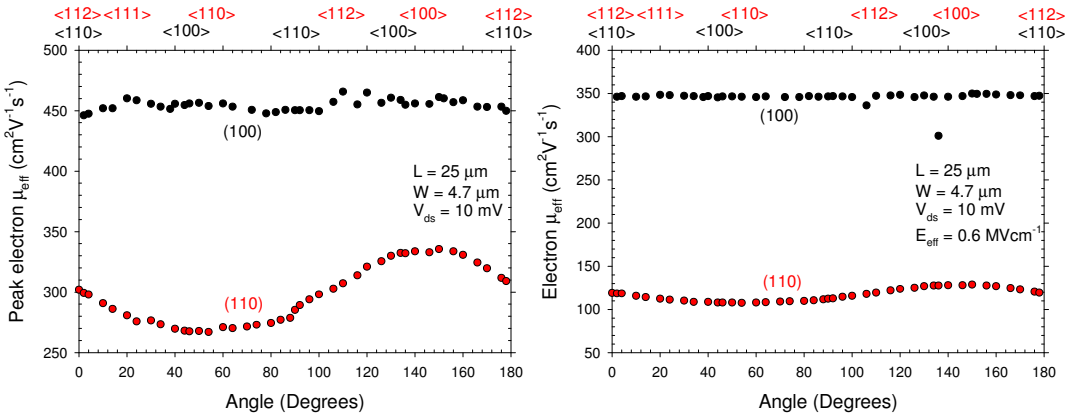

Figure 5.18a) Peak electron μ_{eff} and b) electron μ_{eff} at E_{eff} = 0.6 MVcm^{-1} vs channel direction/angle for 25 µm x 4.7 µm (100) and (110) n-MOSFETs

5.7.2 n-MOSFETs – Variation of μ_{eff} with E_{eff}

μ_{eff} vs E_{eff} for a select range of devices on the (100) and (110) orientations are shown in Figure 5.19 and may be qualitatively interpreted on the basis of models used by previous authors. The lower μ_{eff} on the (110) orientation is largely attributable to the smaller energy split between the Δ_4 and Δ_2 valleys and the larger density of states of the lower energy valleys. The smaller energy split results in increased inter-band optical phonon scattering and population of Δ_2 valleys. The higher density of states results in a higher scattering frequency.[199-200]

The small roll off at low E_{eff} is due to LCS and IIS. An understanding of the processes affecting the lower limit of μ_{eff} in this regime is restricted by accurate calculation of Q_{inv}, making it difficult to analyse these effects. In the work by Nakabayashi *et al.*[201], the individual mobilities limited by LCS and IIS have been extracted and analysed. For a given D_{it}, the mobility limited by LCS is largely

independent of orientation due to a trade-off between m_{conf} and m_{tran}. - A larger m_{conf} results in confinement of carriers nearer to the interface charge, increasing scattering, which serves to reduce the mobility. Since ionised impurities are distributed uniformly in the substrate, differences in confinement between orientations are irrelevant to the mobility limited by IIS.

At E_{eff} = 0.6 MVcm^{-1} the variation in μ_{eff} with channel direction is reduced to 20%, shown more clearly in Figure 5.18b) This reduction between (110)/<100> and (110)/<110> with increasing E_{eff} is attributable to the non-parabolicity of the E-**k** relationship along the <110> direction at the energy minima. This effectively increases m_{conf} of the Δ_2 valleys when their minima exceed 0.1 eV, which then decreases the rate of splitting with increasing E_{eff}. Once E_{eff} increases beyond ~0.4 MVcm^{-1}, the non-parabolicity reduces the energy difference between the Δ_2 and Δ_4 valleys, thereby increasing the occupancy of the Δ_2 valleys at the expense of the Δ_4 valleys. This results in an increase in μ_{eff} along the <110> and a decrease along the <100> directions.[24-25] This also accounts for the steeper decrease in μ_{eff} with increasing E_{eff} on the (110) orientation compared to that on the (100).[199] In addition, Gaubert *et al*.[159] show that LRS begins to limit μ_{eff} at lower E_{eff} on the (110) orientation. This can be understood considering the higher density of states and therefore LRS rate. Figure 5.19b) shows μ_{eff} measured at 4 K and Figure 5.20 shows the ratio $\mu_{eff\ <100>}/\mu_{eff\ <110>}$ at 300 K and 4 K. At 4 K the majority of carriers reside in the Δ_4 valleys[24] and therefore a constant ratio equal to $m_{tran\ <100>}/m_{tran\ <110>}$ (~2.9) might be expected. However the decrease above E_{eff} ~0.4 MVcm^{-1}

demonstrates that the increase in m_{conf} of the Δ_2 valleys due to the non-parabolicity is sufficient that electron repopulation still plays a role.[24]

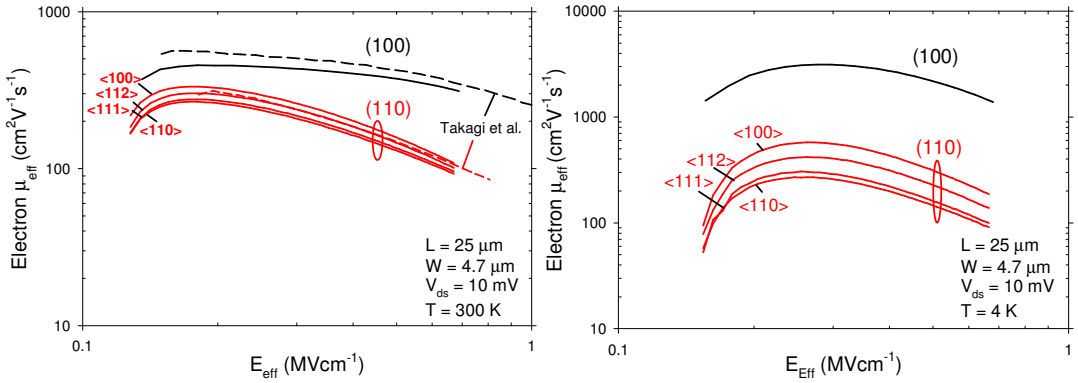

Figure 5.19 Electron μ_{eff} vs E_{eff} extracted at 300 K and 4 K. For the (100) orientation, one plot is shown as μ_{eff} is independent of channel direction. Takagi *et al.*'s data (N_a = 1x10^{17} cm^{-3} for (110)[155] and 7.2x10^{16} cm^{-3} for (100)[154]) is included for comparison.

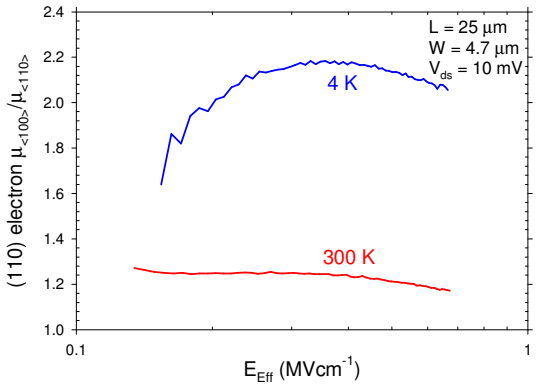

Figure 5.20 Electron $\mu_{eff\ <100>}/\mu_{eff\ <110>}$ vs E_{eff} at 300 K and 4 K on the (110) orientation. These ratios show the same trend as Uchida *et al.*[24]

5.7.3 p-MOSFETs – Variation of hole μ_{eff} with orientation

Hole mobility as a function of surface orientation, channel direction and N_{inv} has been investigated by many authors.[29-30, 34, 184, 202-204] However the role of the effective masses and LH-HH sub-band splitting is under debate. Whilst the variation of mobility with channel direction is explained by an anisotropic m_{tran}, there are no reports of how m_{tran}, m_{scat} and m_{conf} vary with N_{inv}, making a comprehensive understanding of the mobility and scattering mechanisms difficult. The reported hole effective masses (at **k** = 0 i.e. for very low N_{inv}) are reproduced below for convenience.

Surface Orientation	**m_{tran}/m_0 <100>**	**m_{tran}/m_0 <110>**	**m_{scat}/m_0**	**m_{conf}/m_0**	**Sub-band**
(100)	0.28 (Saito *et al.*) 0.20 (Saito *et al.*)	0.58 (Saito *et al.*) 0.15 (Saito *et al.*)	0.43 (Takagi *et al.*) 0.17 (Takagi *et al.*)	0.29 (Takagi *et al.*) 0.2 (Takagi *et al.*)	HH LH
(110)				0.50, 0.59 (Mizuno *et al.*, Saitoh *et al.*) 0.15 (Saitoh *et al.*)	HH LH

Table 5.4 Literature values of hole effective masses calculated at k = 0.

m_{conf}, m_{scat} and m_{tran} for the HH band were calculated using 4 band **k•p** at **k** = 0 by Dr. Jeremy Watling at the Device Modelling Group, University of Glasgow. The masses are shown in Table 5.5

(100)				(110)			
m_{conf}/m_0	m_{scat}/m_0	m_{tran}/m_0		m_{conf}/m_0	m_{scat}/m_0	m_{tran}/m_0	
0.28	0.42	<100>	0.28	0.56	0.54	<100>	0.28
		<110>	0.56			<110>	0.56
						<112>	0.56
						<111>	0.69

Table 5.5 Effective masses calculated by 4 band k•p for the HH sub-band (calculated by Dr Jeremy Watling)

Note the good agreement with the literature values. The values obtained for (110) m_{tran} and m_{scat} are discussed in relation to μ_{eff} further on.

Figure 5.21a) shows the peak μ_{eff} as a function of channel direction and Figure 5.21b) shows μ_{eff} at E_{eff} = 0.6 MVcm^{-1}/N_{inv} = 1x10^{13} cm^{-2}. It is reminded that hole mobility is plotted as a function of N_{inv} as well as E_{eff} due to the ambiguity of η in the calculation of E_{eff} (equation 3.23). Peak μ_{eff} on the (100) wafer varies by ~7% between the <100> (peak μ_{eff} = 139 cm^{2}V^{-1}s^{-1}) and <110> (peak μ_{eff} = 130 cm^{2}V^{-1}s^{-1}) channel directions. In the case of the (110) wafer, peak μ_{eff} varies by ~46% between the <110> (peak μ_{eff} = 242 cm^{2}V^{-1}s^{-1}) and <100> (peak μ_{eff} = 165 cm^{2}V^{-1}s^{-1}) channel directions. Comparing the two orientations, peak μ_{eff} on the (110) orientation is enhanced by 86% along the <110> direction and 19% along the <100> direction. At E_{eff} = 0.6 MVcm^{-1}/N_{inv} = 1x10^{13} cm^{-2} these enhancements increase to 300% and 80%. Recent work [34-35, 199, 204] attributes the higher mobility on the (110) orientation to the suppression of inter-band optical phonon scattering using the following argument. The LH-HH energy split is larger on the (110) orientation than on the (100) due to the larger difference in m_{conf}.[29, 35] Uchida *et al.*[199-200] shows for a doping concentration of ~10^{17} cm^{-3} the LH-HH energy split on the (110)

orientation is larger than the optical phonon energy. Thus inter-band optical phonon scattering is suppressed, particularly with increasing E_{eff}. On the (100) orientation, the LH-HH energy splitting is much smaller than the optical phonon energy, thus optical phonon scattering is not suppressed regardless of E_{eff}. Although this partly explains the weak dependence of μ_{eff} with E_{eff}/N_{inv} on the (110) orientation and the strong degradation of μ_{eff} on the (100) orientation, shown more clearly in Figure 5.22, this argument does not account for the difference in m_{tran} and m_{scat} between the two orientations or the impact of the other scattering mechanisms.

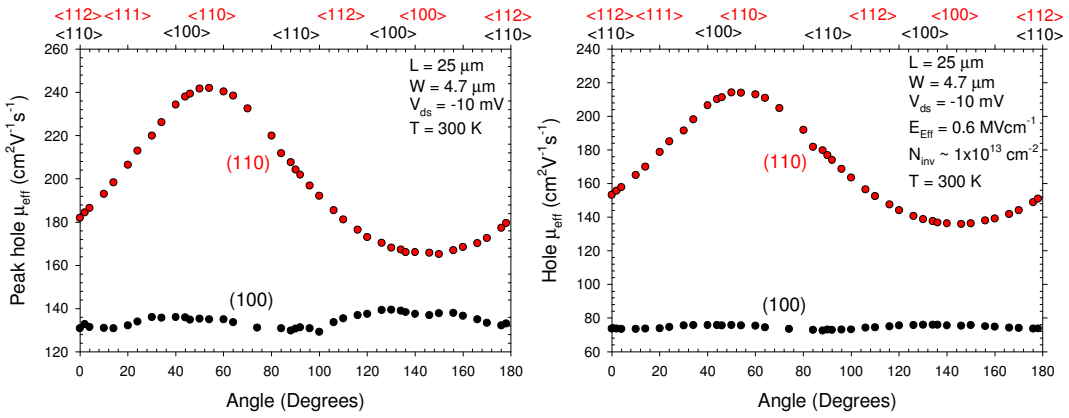

Figure 5.21a) Peak hole μ_{eff} and b) μ_{eff} at N_{inv} = 1x10^{13} cm^{-2}/E_{eff} = 0.6 MVcm^{-1} vs channel direction/angle for 25 μm x 4.7 μm (100) and (110) p-MOSFETs. Note η = ⅓ is used in the calculation of E_{eff}.

The variation with E_{eff} and N_{inv} for a few select channel directions are shown in Figure 5.22a) and Figure 5.22b). For comparison, Irie *et al.*'s[119] (110) hole μ_{eff} is included in Figure 5.22b). It is expected that their larger μ_{eff}, which is significant at low N_{inv}, might be explained by a lower doping concentration, therefore lower IIS and LCS.

5.7.4 p-MOSFETs – Variation of hole μ_{eff} with E_{eff}/N_{inv}

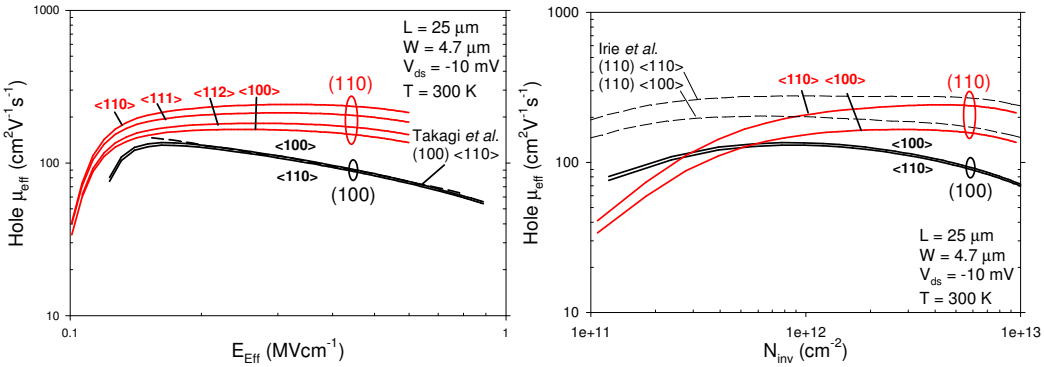

Figure 5.22a) Hole μ_{eff} vs $E_{eff.}$ Takagi *et al.*'s[154] (100)/<110> data ($N_d = 5.1x10^{16}$ cm^{-3}) is included for comparison b) Hole μ_{eff} vs $N_{inv.}$ Irie *et al.*'s[119] (110)/<110> and <100> data (N_d ~ 10^{15} cm^{-3}?) is included for comparison. Note η = ⅓ is used in the calculation of E_{eff}.

We now discuss the behaviour of hole μ_{eff} on the (100) orientation. As already stated, the peak μ_{eff} on the (100)/<100> orientation is 7% higher than on the (100)/<110> orientation. Simulations by Fischetti *et al.*[29] show that μ_{eff} should be higher in the <110> direction than the <100> direction. On the other hand Gaubert *et al.*[159] measure a 10% enhancement in the <100> direction but provides no physical explanation. Sayama *et al.*[205] measure an ~8% enhancement in the <100> direction at low E_{eff} and attribute it to the lighter HH mass in the <100> direction. Saito *et al.*[32] observe a 5% enhancement in the <100> direction, specifying the masses in Table 5.4. As m_{tran} differs by a factor of 2 between the two directions, they state this "might result in a μ_{eff} enhancement of a factor ~2". However this can only be based on occupation of the HH band. The small difference of m_{conf} between the LH and HH sub-bands results in a small HH and LH splitting and subsequently a large occupation of the LH, serving to increase μ_{eff}, particularly along the <110>

direction, possibly explaining the small enhancement. Despite the small difference in m_{conf}, Takagi *et al*. points out that with increasing confinement, more holes occupy the HH band. Therefore we might expect to see the enhancement increase with increasing E_{eff}/N_{inv}. What is actually observed is a small decrease in enhancement, ~4% at $E_{eff} = 0.6$ MVcm^{-1}. At 4 K, where population of the HH sub-band is higher, a much greater enhancement is expected. However, only a 9% enhancement in peak μ_{eff} is observed as shown in Figure 5.26. From the above discussion, μ_{eff} can not be explained in terms of the effective masses in Table 5.4. Furthermore, the calculated values of m_{tran} on the (110) orientation also do not predict the correct trend in mobility - forecasting the highest mobility along the <100> channel direction. It is therefore fair to say that effective masses, calculated at $\mathbf{k} = 0$ have very limited application in explaining μ_{eff}. Thus more detailed calculations of the hole masses are required to correctly interpret the mobility.

5.7.5 Improved effective mass calculation and 300 K hole μ_{eff} analysis

A more appropriate method to calculate the hole masses is to average equation (2.18) over **k** in the transport plane, $\boldsymbol{k}_{\|}$, weighted by the Fermi distribution.[31] Thus to calculate m_{tran} in the HH sub-band;

$$\frac{1}{m_{tran,HH}} = \left\langle \frac{1}{\hbar^2}\frac{\partial^2 E}{\partial k_x^2} \right\rangle_{HH} = \frac{1}{\hbar^2}\int \frac{\partial^2 E_{HH}(k_{\|})}{\partial k_x^2} f\left(E_{HH}(k_{\|}), T\right) d^2 k_{\|} \qquad (5.1)$$

Upon the author's request, the effective masses in the HH sub-band at 300 K and 4 K as a function of N_{inv}/E_{eff} were calculated by Dr. Luca Donetti and Prof. Francisco

Gamiz at the Departamento Electronica, Universidad de Granada, Spain. $E_{HH}(k_{\|})$ was calculated with their 6-band **k•p**-Poisson solver, details of which are given in [30-31]. The simulator calculates m_{tran} as a function of N_{inv}. m_{conf} was evaluated based on known energy levels in triangular wells with different E_{eff}.

To gain a simplistic understanding of μ_{eff}, we follow the approach of Donetti *et al.*[31] and analyse μ_{eff} in terms of the dominantly occupied HH sub-band. This is obviously more accurate for the (110) orientation due the large LH-HH sub-band splitting. Figure 5.23 shows m_{tran}, calculated by this technique at $N_{inv} = 1\text{x}10^{13}$ cm^{-2}, as a function of channel direction on both the (100) and (110) orientations.

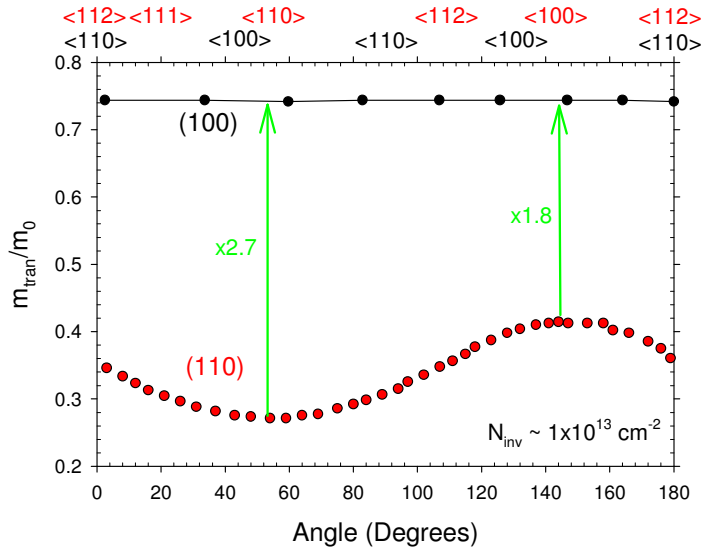

Figure 5.23 m_{tran} in the HH sub-band as a function of channel direction on (100) and (110) orientations. m_{tran} was calculated from an average over the k-plane for $N_{inv} = 1\text{x}10^{13}$ cm^{-2}. The variation on the (110) orientation is comparable to the variation in the experimental μ_{eff}. (Calculations performed by Luca Donetti and Prof. Francisco Gamiz.)

On the (110) orientation, the variation in m_{tran} is comparable to the variation in μ_{eff} with enhancements of 270% and 80% over the (100) orientation. i.e. largely explaining not only the variation of μ_{eff} with channel direction but also the enhancement of μ_{eff} over the (100) orientation. This implies that reduced inter-band optical phonon scattering at high N_{inv} is of secondary importance. On the (100) orientation, m_{tran} is independent of channel direction. A slightly lower m_{tran} in the <100> direction than in the <110> direction was expected to explain the small enhancement of μ_{eff}. However the difference may be small enough to have been averaged out during the calculations.

Figure 5.24a) and b) shows m_{tran} and m_{scat} vs N_{inv} and Figure 5.25 shows m_{conf} vs $E_{eff.}$ m_{tran} has been calculated for just the <100> and <110> directions on the (110) orientation as these directions show the greatest variation in μ_{eff}. It is interesting to observe that m_{tran} and m_{scat} on the (110) orientation decrease with increasing N_{inv} whereas they increase with increasing N_{inv} on the (100) orientation. For the (100) orientation and <110> direction, $m_{tran} = 0.58m_0$ at $N_{inv} = 3x10^{10}$ cm^{-2} agreeing with Saito *et al.*[32] However, this value is not relevant for the full range of device operation. At low N_{inv}, m_{tran} is larger on the (110) orientation. This explains the crossover in μ_{eff} between the (100) and (110) orientations at low N_{inv}, observed in Figure 5.22b). Thus it can be inferred that m_{tran} largely explains the difference between μ_{eff} on the (100) orientation and on the (110) orientation as a function of N_{inv} as well as channel direction. We now propose a hypothesis as to why the scattering mechanisms appear to play a secondary role. Firstly, the scattering mechanisms are

convoluted functions of m_{scat} and m_{conf}. In the case of the (110) orientation, m_{conf} increases with E_{eff}. (Note the value, $0.56m_0$, close to the values in Table 5.4 and Table 5.5, is approached as E_{eff} tends to zero.) It is possible that the increase in m_{conf} and the decrease in m_{scat} with increasing N_{inv} compensate each other. As discussed in section 5.7.3, the increase in m_{conf} increases the LH-HH sub-band splitting reducing inter-band optical phonon scattering. However the increasing confinement, results in stronger LCS and LRS as the respective scattering potentials are higher closer to the interface. On the other hand, the decrease in m_{scat} means a reduction in the density of states, reducing scattering.

On the (100) orientation, $m_{conf} = 0.27m_0$ independent of N_{inv} which is in agreement with the values in Table 5.4 and Table 5.5. As discussed in section 5.7.3, the weaker confinement, as compared to the (110) orientation, results in smaller LH-HH sub-band splitting and large inter-band optical phonon scattering. However the weaker confinement has the benefit of weaker LCS and LRS. Then again, the increase in m_{scat} means an increase in the density of states, increasing scattering.

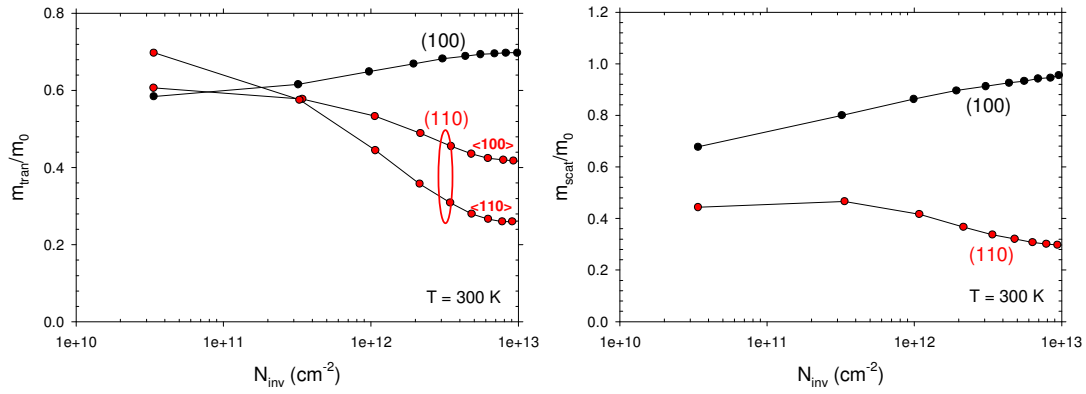

Figure 5.24a) m_{tran} in the HH sub-band as a function of N_{inv} The variation explains the difference in μ_{eff} between the (100) and (110) orientations b) m_{scat} as a function of N_{inv}. (calculations performed by Luca Donetti and Francisco Gamiz)

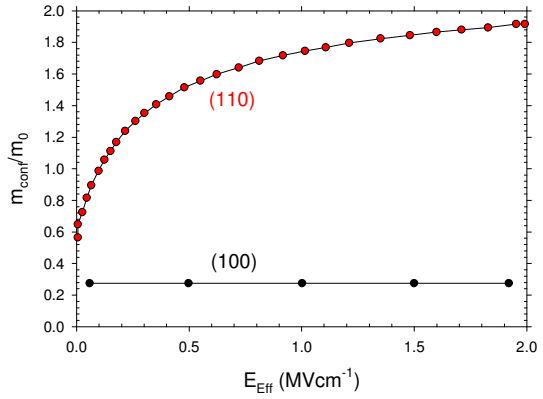

Figure 5.25 m_{conf} vs E_{eff} (calculations performed by Luca Donetti and Francisco Gamiz)

5.8 4 K effective mobility modelling

So far we have qualitatively been able to explain the variation in μ_{eff} in terms of the effective masses. However, due to the different contributions of m_{conf}, m_{scat} and m_{tran}, it is very difficult to ascertain the role of the various material parameters. Whilst slightly higher D_{it} on the (110) wafer than the (100) wafer has been measured, any difference in interface roughness between the two orientations is currently unknown,

and requires a quantitative analysis. Yang *et al.*[182-183] and Momose *et al.*[188] show oxidation of a (110) Si substrate results in a higher interface roughness whereas Yang *et al.*[181] and Nakamura *et al.*[180] show using transmission electron microscopy and from mobility measurements that the roughness is the same in their devices. On the contrary Sun *et al.*[202] assumes a smoother (110) interface in their modelling. The study by Chen *et al.*[206] shows the thicker the oxide, the rougher the interface. Another consideration is that roughness may be anisotropic. Although this has been observed to affect μ_{eff} at a GaAs/AlAs interface[207], the study by Sun and Plummer[208], shows roughness at a SiO_2/Si interface on a (110) orientation is isotropic.

By measuring μ_{eff} at 4 K, phonons are frozen out and the effects of Coulomb and roughness scattering can be more easily determined. Figure 5.26 shows the hole μ_{eff} measured at 4 K and Figure 5.27 shows m_{tran} and m_{scat} calculated at 4 K.

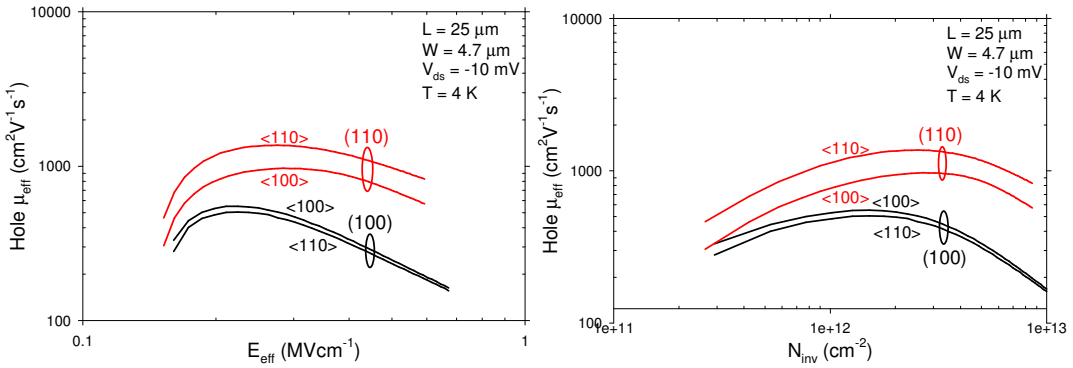

Figure 5.26a) 4 K hole μ_{eff} vs E_{eff}. b) 4 K hole μ_{eff} vs N_{inv}

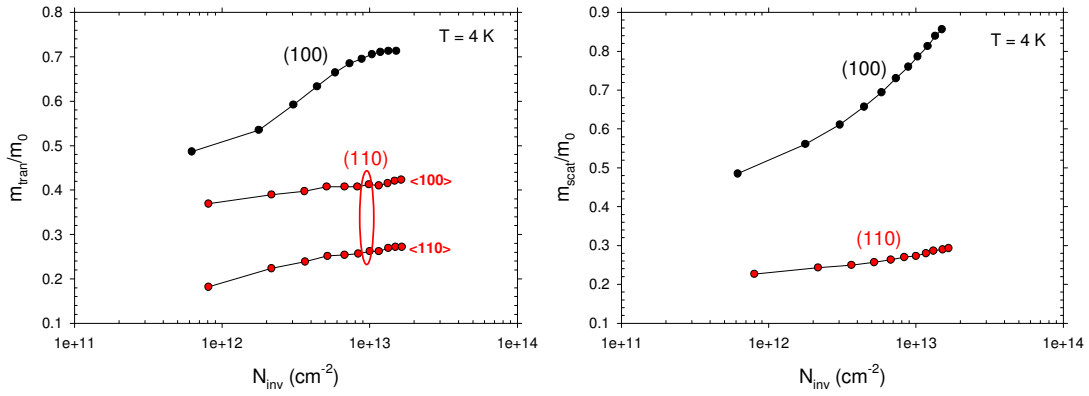

Figure 5.27a) m_{tran} as a function of N_{inv} b) m_{scat} as a function of N_{inv} at 4 K

Using the scattering theory in section 2.5, μ_{eff} measured at 4 K is modelled in terms of IIS, LCS and LRS using n_{imp}, Δ and Λ as fitting parameters. μ_{eff} is modelled up to N_{inv} ~$6x10^{12}$ cm^{-2} using constant values of m_{scat} and m_{tran}, within 15% of those calculated in Figure 5.27. These are shown in Table 5.6.

4 K effective masses used in modelling									
p-MOS HH band									
(100)					**(110)**				
g_v	**m_{conf}/m_0**	**m_{scat}/m_0**	**m_{tran}/m_0**		**g_v**	**m_{conf}/m_0**	**m_{scat}/m_0**	**m_{tran}/m_0**	
1	0.27	0.56	<110>	0.56	1	See Figure 5.25	0.23	<100> <110>	0.40 0.22
n-MOS									
(100)					**(110)**				
g_v	**m_{conf}/m_0**	**m_{scat}/m_0**	**m_{tran}/m_0**		**g_v**	**m_{conf}/m_0**	**m_{scat}/m_0**	**m_{tran}/m_0**	
2	0.91	0.19	<110>	0.19	4	0.32	0.32	<100> <110>	0.19 0.55

Table 5.6 4 K effective masses used in the modelling of 4 K hole $\mu_{eff.}$

To model IIS, we have to bear in mind that the ionised doping concentration decreases when cooling. Figure 5.28 shows an extraction of the doping profile at 4 K. Although W_{dep} = 120 nm was measured, measurement noise prevented reliable extraction beyond approximately 80 nm.

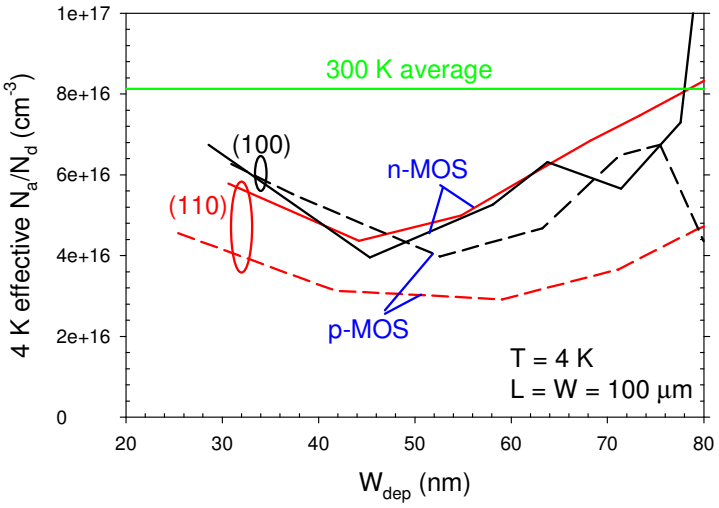

Figure 5.28 Doping profile extracted from CV at 4 K. 300 K average doping concentration shown for comparison

Intuitively we would expect Δ and Λ for n- and p-MOSFETs to be the same on a given wafer. Indeed, Ishihara *et al.* [38] and Pirovano *et al.*[36] stress that the validity of Δ and Λ must be judged on whether the values can explain both electron and hole surface roughness mobility consistently. For a (100) SiO_2/Si interface, reports of Δ range from 0.24 nm[209] to 0.55 nm[38] and Λ varies between 1 nm[36] and 2.6 nm[29]. Figure 5.29 and Figure 5.30 show examples of μ_{LCS} and μ_{LRS} calculated for different values of n_{imp}, Δ and Λ.

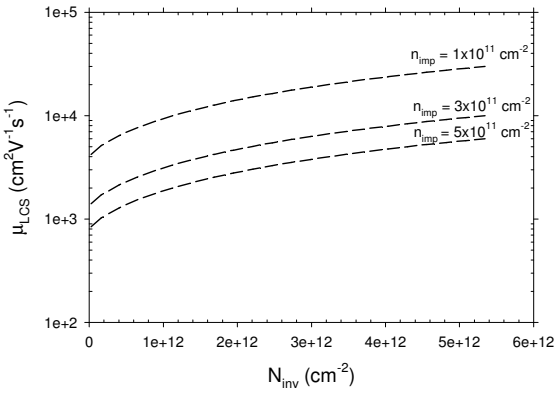

Figure 5.29 Calculated μ_{LCS} as a function of N_{inv} for different values of n_{imp} for a (100) n-MOSFET

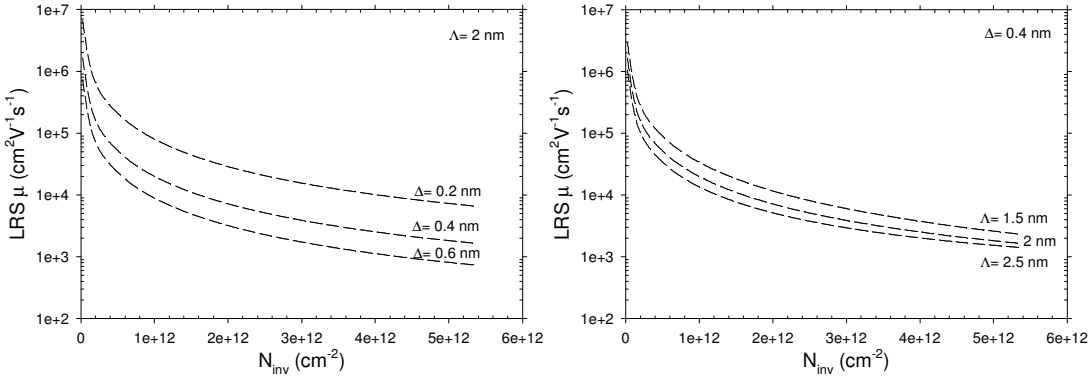

Figure 5.30 Calculated μ_{LRS} as a function of N_{inv} for different values of Δ and Λ for a (100) n-MOSFET

As expected, increasing either one of these parameters increases the relevant scattering rate, decreasing the mobility. The total mobility, μ_{Tot} has been calculated using Matthiessen's rule:

$$\frac{1}{\mu_{Tot}} = \frac{1}{\mu_{IIS}} + \frac{1}{\mu_{LCS}} + \frac{1}{\mu_{LRS}} \tag{5.2}$$

The modelling parameters for the (100) n- and p-MOSFETs are shown in Table 5.7 and the respective fits to the 4 K μ_{eff} data are shown in Figure 5.31 and Figure 5.32.

A value of $n_{imp} \sim 3x10^{11}$ cm^{-2} which is comparable to the extracted D_{it} near weak inversion (Figure 5.7), and constant doping of $6x10^{16}$ cm^{-3} enabled good fits to μ_{eff} of both n- and p-MOSFETs at low N_{inv}. One might expect n_{imp} at 4 K to be greater than the D_{it} measured at 300 K. Consider that in strong inversion the charged interface states exist between mid-gap and the Fermi-level (figure 2.10). At 300 K this energy difference is ~0.4 eV, calculated by equation (2.4). However at 4 K, this could be closer to 0.56 eV due to the shift in Fermi-level towards the majority carrier band edge, caused by the decrease in intrinsic carrier concentration. Thus more interface traps are charged over the wider energy range.

Values of Δ = 0.34 nm and Λ = 2 nm, which lie within the range reported in the literature, were necessary to fit the data at higher N_{inv}. Using similar parameters (Table 5.8), good fits to μ_{eff} on the (110)/<100> and <110> p-MOSFETs were obtained as shown in Figure 5.33 and Figure 5.34. An interesting result is that Δ and Λ agree with the (100) wafer within error suggesting the oxide interfaces are very similar for the two orientations. However we must be mindful of the assumptions used in these models and that the various fitting parameters can mask their shortcomings.

Modelling of the (110) n-MOSFETs, using the effective masses in Table 5.6 was unsuccessful necessitating very large fitting parameters. e.g. $n_{imp} \sim 5x10^{12}$ cm^{-2}. This is most likely due to occupation of the higher Δ_2 sub-bands, lowered by their non-

parabolicity. Detailed simulations of the 300 K and 4 K data are currently in progress by Dr. Luca Donetti to verify the fitting parameters.

	(100) 4 K modelling parameters			
	LCS	IIS	LRS	
	n_{imp} (cm^{-2})	N_a/N_d (cm^{-3})	Δ (nm)	Λ (nm)
n-MOS	$3.0 \times 10^{11} \pm 0.5x10^{11}$	$6.0x10^{16}$	0.34 ± 0.05	2.0 ± 0.3
p-MOS	$3.0 \times 10^{11} \pm 0.5x10^{11}$	$6.0x10^{16}$	0.34 ± 0.05	2.0 ± 0.3

Table 5.7 Fitting parameters used in the modelling of (100) electron and hole 4 K μ_{eff}

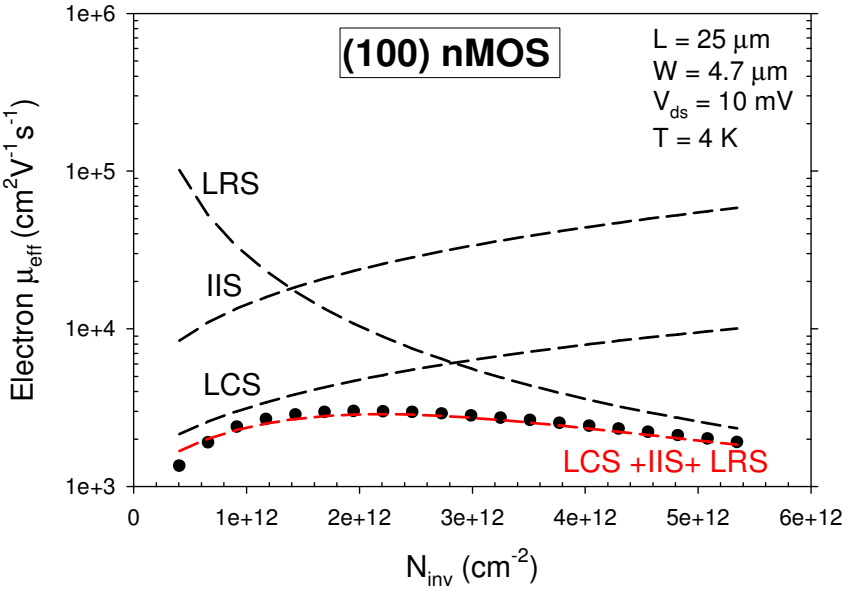

Figure 5.31 Modelling of the 4 K (100) electron μ_{eff} in terms of IIS, LCS and LRS

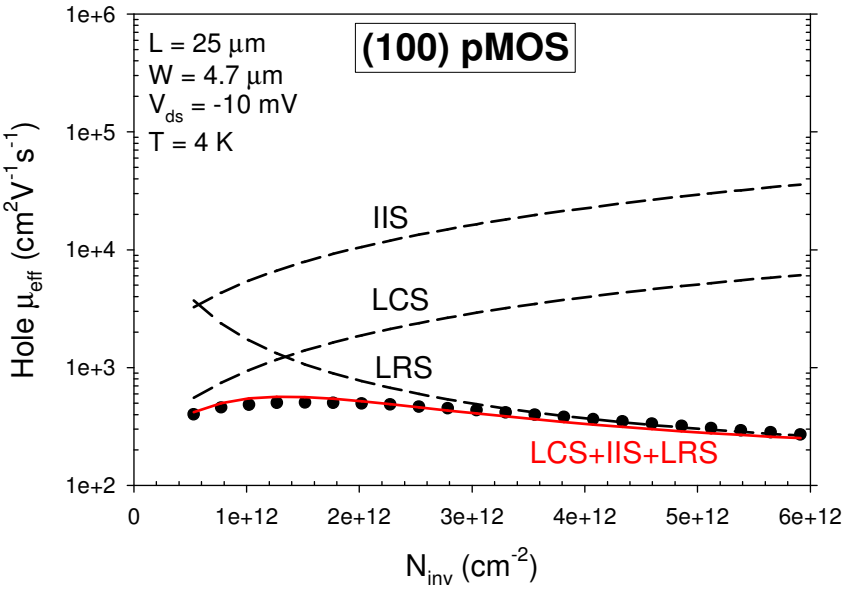

Figure 5.32 Modelling of the 4 K (100) hole μ_{eff} in terms of IIS, LCS and LRS

	p-MOS (110) 4 K modelling parameters			
	LCS	IIS	LRS	
	n_{imp} (cm^{-2})	N_a/N_d (cm^{-3})	Δ (nm)	Λ (nm)
<100>	$3.0 \times 10^{11} \pm 0.5x10^{11}$	$5.4x10^{16}$	0.32 ± 0.05	2.3 ± 0.3
<110>	$3.2 \times 10^{11} \pm 0.5x10^{11}$	$5.4x10^{16}$	0.38 ± 0.05	2.3 ± 0.3

Table 5.8 Fitting parameters used in the modelling of (110)/<100> and <110> 4 K hole μ_{eff}

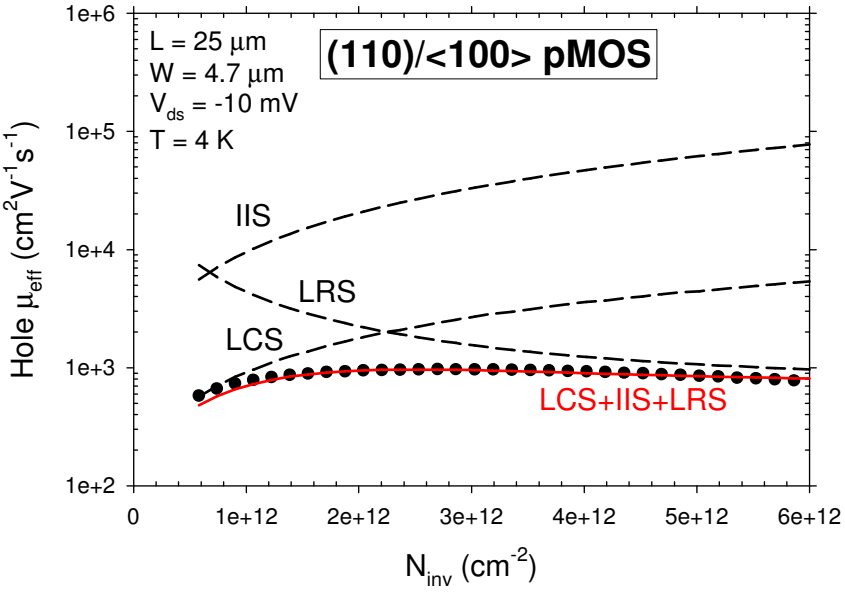

Figure 5.33 Modelling of the 4 K (110)/<100> hole μ_{eff} in terms of IIS, LCS and LRS

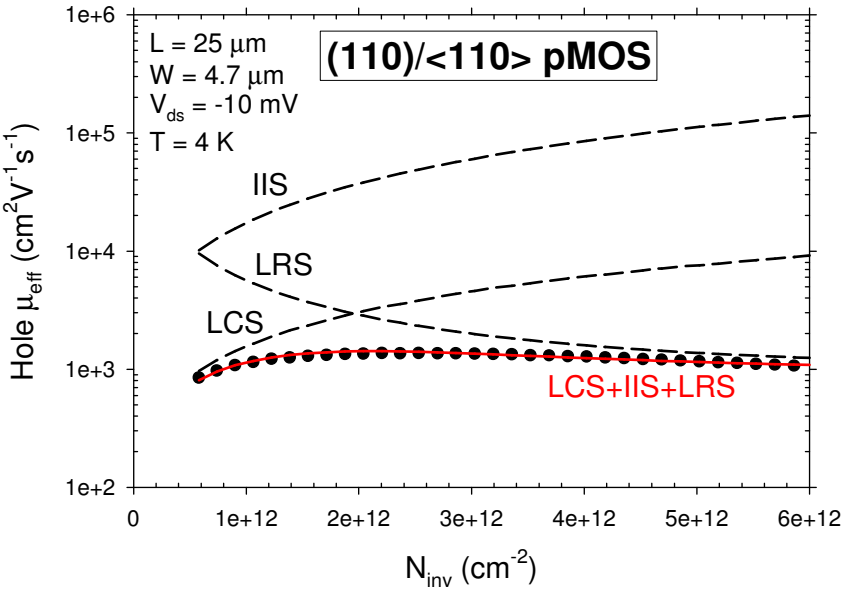

Figure 5.34 Modelling of the 4 K (110)/<110> hole μ_{eff} in terms of IIS, LCS and LRS

5.9 Summary

n- and p-MOSFETs with n+polySi/SiO_2 gate stacks, fabricated on (100) and (110) orientated wafers have been electrically characterised in detail. D_{it}, g_m, *S.S.*, V_t, R_{sd}, ΔL, μ_{eff} and the doping profile were extracted at room temperature. μ_{eff} was also extracted at 4 K. The main focus is on the analysis of μ_{eff} as a function of N_{inv}, substrate orientation and channel direction. The behaviour of the electron mobility can be explained relatively easily in terms of constant effective masses and sub-band splitting thanks to the simple conduction band-structure. The hole band structure is much more complicated and required novel sophisticated calculations of the effective masses of the dominantly occupied HH sub-band, to interpret the hole μ_{eff}. Subsequently, the dependence of hole μ_{eff} on N_{inv}, substrate orientation and channel direction could largely be explained by the variation in transport mass. Analytical modelling of the 4 K electron and hole mobility in terms of ionised impurity, local charge and roughness scattering mechanisms (phonons frozen out) revealed comparable Si/SiO_2 interface quality between the (100) and (110) orientations.

Chapter 6 : Si finFETs with high-κ dielectrics and metal gates

6.1 Introduction

In chapter 5, the electrical characteristics of planar MOSFETs on (100) and (110) surface orientations were analysed in detail. Much of the analysis is used in this chapter to interpret the mobility in state of the art finFETs. However, we now have the added complexity of both surfaces, whose physical properties may differ, being present on a single device and also the inclusion of high-κ dielectrics and metal gates.

6.2 Device overview

N-channel and p-channel finFETs were fabricated on separate wafers at NXP Semiconductors, Belgium using a VLSI-compatible process. The basic process flow is summarised as follows.

300 mm boron doped SOI (100) wafers (provided by SOITEC) of resistivity 10-15 Ωcm (corresponding N_a ~ 10^{15} cm^{-3}) were used as the starting platform. The thickness of the BOX was ~145 nm and the thickness of the SOI was ~ 88 nm. The

SOI was thinned to 65 nm using a wet etch to define the prospective fin heights, H_{fin}. Fins were then patterned by depositing a hard mask followed by immersion lithography. A dry etch (reactive ion etch) of the hard mask and Si was then performed, with the BOX acting as an etch stop layer. Figure 6.1 illustrates the patterned fins of a prospective finFET.

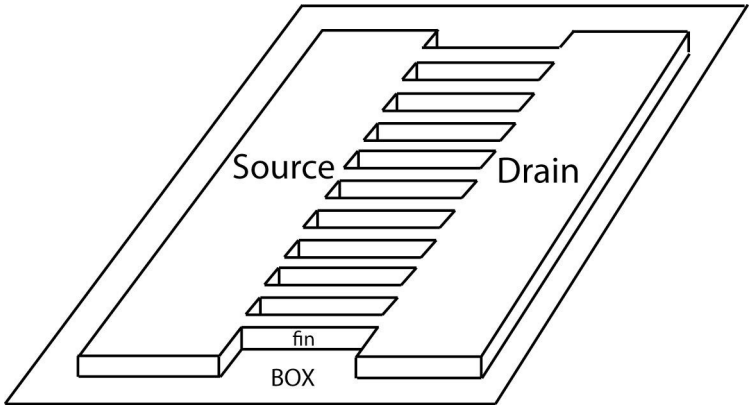

Figure 6.1 Illustration of the patterned Si fins (10 in parallel) of a prospective finFET, fabricated on a BOX.

Any native oxides were subsequently removed using HF based wet chemistry. The final patterning step was an anneal in H_2 to round the fin corners and smoothen the sidewalls, roughened during the dry etch.[210-211] (Occasionally this reduces H_{fin} by 2 nm).

Fins were defined along the <110> and <100> directions (parallel and 45° to the wafer flat respectively) to produce finFETs with (110) and (100) sidewalls. Fin widths, W_{fin} were varied from 1872 nm below 5 nm. The gate stack, which straddles the fin, was formed by a 1 nm SiO_2 interfacial oxide, followed by metal organic chemical vapour deposition (MOCVD) of 2.3 nm $Hf_{0.4}Si_{0.6}O$ and 5 nm TiN deposited by plasma enhanced atomic layer deposition and a poly-Si cap. After gate

patterning, source and drain extensions were implanted (As for n-channel, BF_2 for p-channel) and spacers were formed. Access resistance was reduced with 40 nm Si selective epitaxial growth. Implantation of As+P for the n-channel and B for p-channel followed by 10 nm NiSi formed the source/drain contacts. Finally a 1050 °c RTA was used to activate the dopants. A cross sectional TEM image of a 20 nm wide finFET is shown in Figure 6.2. Further information on the device processing are given in [212-213].

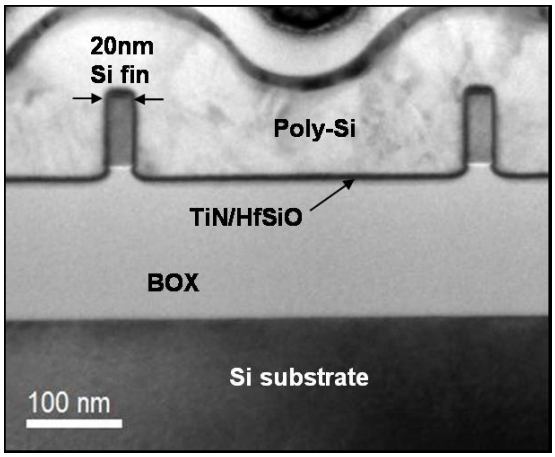

Figure 6.2 Cross sectional TEM image of a 20 nm wide finFET

Electrical measurements in this work were performed on finFETs of length 10 μm with 10 fins in parallel. Measuring long channel and multi-fin devices was necessary for a high signal-noise ratio, particularly for CV measurements. There were no electrical contacts to the device channels which meant only the C_{gc} branch of the split CV could be measured. In any case the light doping of the fins and the BOX meant the finFETs were fully depleted with N_{dep} no greater than 6.5×10^9 cm^{-2}. All devices exhibited large gate leakage currents necessitating corrections for I_d, a typical example of which has already been shown in figure 4.1. A big problem

during measurements was the breakdown of the gate dielectrics, manifested by excessive gate leakage. It was worse with decreasing W_{fin} and during low temperature measurements. This was a real nuisance as working finFETs with $W_{fin} < 16$ nm were not only scarce but also displayed large variations in I_d, making analysis difficult. The large variation was attributed to the devices having "broken fins".

6.3 Gate – channel capacitance and threshold voltage

6.3.1 n-finFETs

Figure 6.3a) shows C_{gc} for W_{fin} ranging from 1872 nm to 16 nm and Figure 6.3b) shows the associated CET as a function of W_{fin}. Measurement frequencies of 100 kHz – 1 MHz were used. The dielectric constant of the $Hf_{0.4}Si_{0.6}O$ was calculated as approximately 8 using equation (2.56) corresponding to the measured CET of 2.1 ± 0.1 nm. Note this is not too different from the value of 6.5 obtained from the Clausius-Mossotti relation (figure 2.12). From Figure 6.3a) a small decrease in C_{ox} with decreasing W_{fin} is observed, suggesting confinement is weaker on the (110) sidewalls compared to the (100) top surface. (CET is constant within extraction error.) An unexpected feature is the increase in V_t with decreasing W_{fin}, observed by the shift in C_{gc} to higher V_{gs}. For channel lengths of 10 μm, V_t was expected to be constant due to the light fin doping and correspondingly small N_{dep}. Figure 6.4 shows V_t extracted from the maximum slope of g_m, which confirms the

trend. Note the W_{fin} presented here, are large enough not to be affected by structural quantum confinement effects.

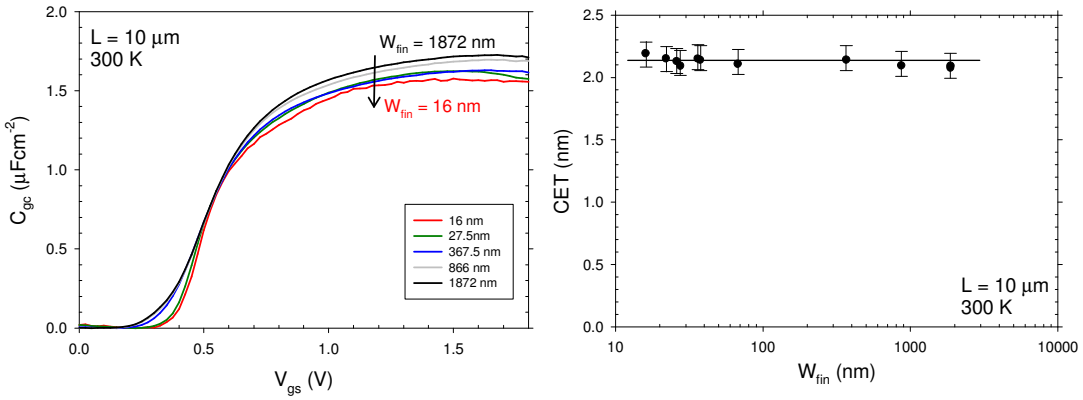

Figure 6.3a) C_{gc} characteristics, for n-finFETs with W_{fin} ranging from 1872 nm to 16 nm and L = 10 µm. b) Corresponding CETs.

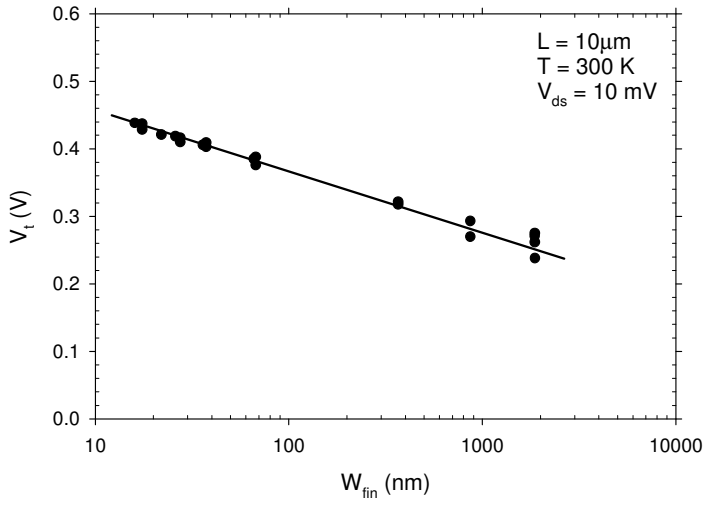

Figure 6.4 V_t for n-finFETs with W_{fin} in the range 16 nm – 1872 nm. V_t is extracted from the maximum slope of g_m.

6.3.2 p-finFETs

Figure 6.5a) shows C_{gc} for W_{fin} ranging from 1864 nm to 12 nm and Figure 6.5b) shows the associated CET as a function of W_{fin}. A CET of 2.1 ± 0.1 nm was obtained for all W_{fin}, i.e. same as the n-finFETs. Although some random variation is observed, C_{ox} and V_t is constant with W_{fin}, the former indicating uniform dielectric thickness on the top surface and sidewalls of the fins.

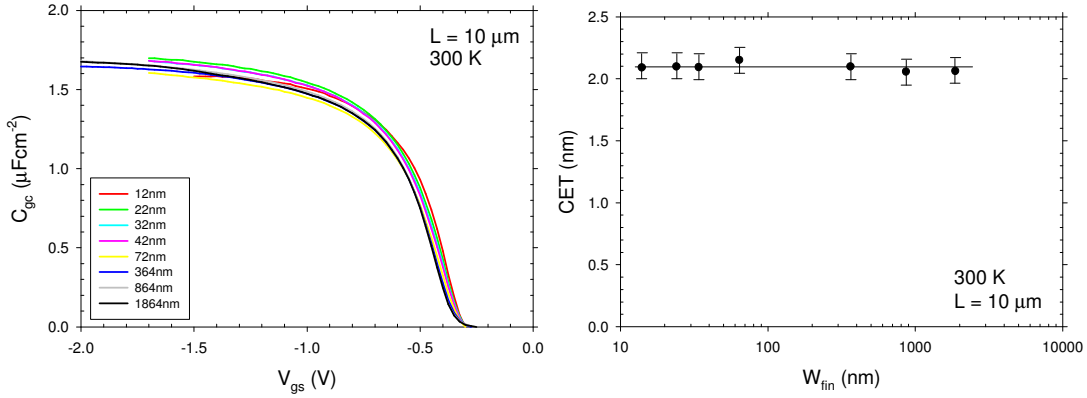

Figure 6.5a) C_{gc} characteristics, for p-finFETs with W_{fin} ranging from 1864 nm to 12 nm and L = 10 µm. b) Corresponding CETs.

Figure 6.6 shows V_t for the range of W_{fin}, extracted from the maximum slope of g_m. As expected, V_t is fairly independent of W_{fin}. A value of approximately 0.36 V was obtained which corroborates with the C_{gc} measurements.

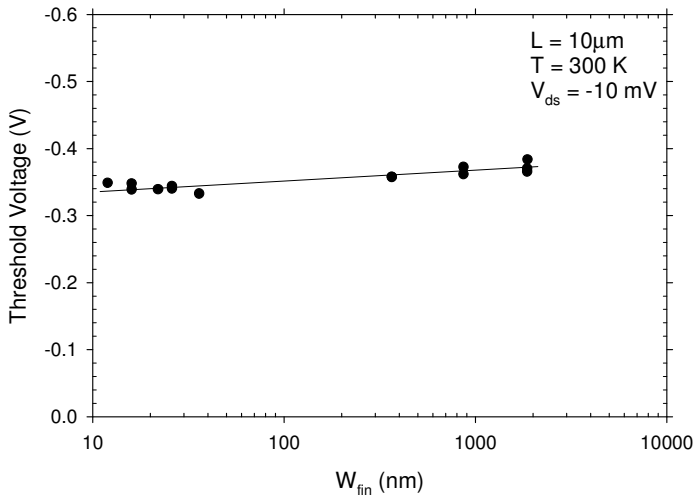

Figure 6.6 V_t for p-finFETs with W_{fin} in the range 12 nm – 1872 nm. V_t is extracted from the maximum slope of g_m.

6.4 Volume or surface inversion

The C_{gc} characteristics for both n- and p-finFETs are analogous to bulk MOSFETs, suggesting volume inversion is not present for the W_{fin} shown here. If volume inversion was present, a drop in the capacitance might be observed as carriers travel down the centre of the fin rather than at the interfaces. Simulations of the inversion charge distribution in the Δ_4 sub-bands in double gate (110) n-MOSFETs have been performed in [115, 214-216]. Silicon thicknesses of 5.2 nm or less are required for volume inversion to be maintained up to N_{inv} = 5x10^{12} cm^{-2}. (Volume inversion is observed for thicknesses of 9 nm but only up to 1x10^{12} cm^{-2})

On the contrary, Tsutsui *et al.*[217] surmise from mobility measurements, that volume inversion is not observed for thicknesses of 5 nm in double gate (110) p-

MOSFETs. Furthermore, calculations of the inversion charge distribution by Donetti *et al*.[31] show volume inversion is not observed for thicknesses as small as 4 nm.

6.5 300 K effective mobility

6.5.1 n-finFETs

Electron and hole μ_{eff} were extracted using equation (4.16a) with I_d-V_{gs} measured with $V_{ds} = \pm 10mV$. Figure 6.7 shows electron μ_{eff} for W_{fin} ranging from 16 nm to 1872 nm as a function of N_{inv}. Data from Takagi *et al*. on (100) and (110) SiO_2/Si bulk MOSFETs has been included as a reference.

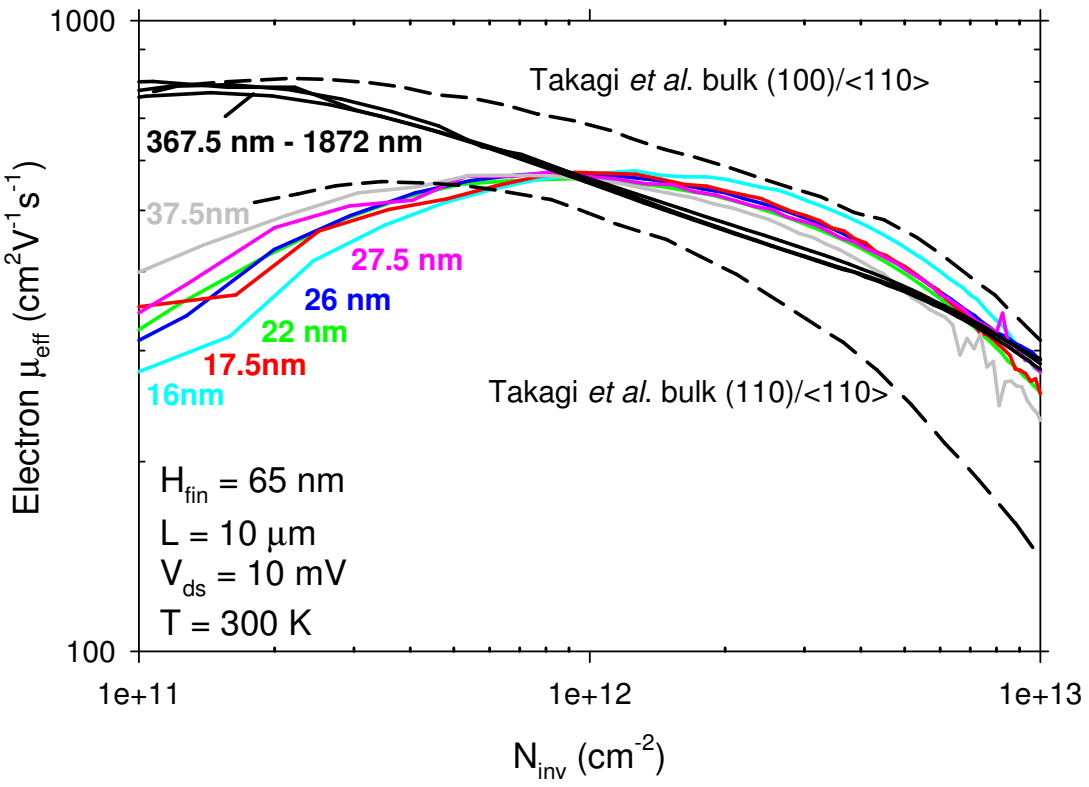

Figure 6.7 Electron μ_{eff} for W_{fin} ranging from 16 nm to 1872 nm. Takagi *et al.* (100) (N_a = 3.9x10^{15} cm^{-3}) [154] and (110) (N_a =2.8x10^{15} cm^{-3})[155] bulk MOSFET data included for comparison.

For $W_{fin} \geq 367.5$ nm, the (110) sidewalls make up less than 35% of the effective width. Such finFETs can be treated as essentially (100) SOI MOSFETs and are termed quasi-planar. μ_{eff} can be analysed in terms of transport along the (100) top surface and <110> channel direction. We can see that μ_{eff} in this set of finFETs is ~20% lower than Takagi *et al.*'s (100) data over most of the N_{inv} range and so now will discuss why this might be. Since the doping concentrations are comparable, ionised impurity scattering (IIS) is not responsible. The SiO_2 interlayer should ensure local roughness scattering (LRS) and local Coulomb scattering (LCS) are

comparable to those of the bulk MOSFET.- D_{it} of ~10^{11} cm^{-2} in weak inversion was measured by charge pumping measurements at NXP Semiconductors on bulk MOSFETs with the same gate stack. This measurement is in agreement with charge pumping measurements performed by Garros *et al*.[57] on a similar gate stack. Since the fin top surface is 65 nm from the BOX, Coulomb and roughness scattering from the Si/BOX interface is not likely to be the cause of mobility reduction. These mechanisms have been shown to be important 10 nm from the channel in SOI MOSFETs.[111, 114, 218] The influence of the remote TiN/HfSiO interface (3.3 nm from the channel) can also be neglected. This leaves high-κ related remote scattering mechanisms i.e. remote phonon (RPS) and/or remote Coulomb scattering (RCS). RPS from the $Hf_{0.4}Si_{0.6}O$ dielectric is likely to be of secondary importance for 3 reasons. Firstly, the small difference in static and high frequency permittivity (6.5 and 3.3 respectively from figure 2.12) results in a weak coupling strength between SO phonons and the inversion charge. Secondly, the SiO_2 interfacial layer decouples the phonons from the channel and reduces their effective scattering potential. Thirdly, Chau *et al*.[79] shows that a TiN gate is effective in screening phonon in a HfO_2 dielectric from coupling to the channel. O'Regan *et al.*[219] and Datta *et al*.[81] show that screening of the dielectric by carriers in the inversion layer reduces the strength of RPS at large electron densities (HfO_2). In line with these studies Shah *et al.*[220] and Casse *et al*.[51] show SO phonon plays a minor role in the electron mobility degradation of TiN/HfO_2 MOSFETs and that RCS is the primary cause. In the present case, remote charges from the HfSiO/SiO_2 interface, ~1 nm from the

channel are likely to be responsible. Any charges at the TiN/HfSiO interface are ~ 3.3 nm from the channel, therefore unlikely to play a significant role.

For $W_{fin} \leq 36$ nm, the top (100) surface only makes up less than ~28% of the effective width thus μ_{eff} can be analysed in terms of transport along the (110)/<110> sidewalls. Comparing μ_{eff} with Takagi *et al.*'s (110)/<110> data, a ~60% enhancement from N_{inv}= 5x10^{12} cm^{-2} is observed and is maintained with increasing N_{inv}. At low N_{inv}, μ_{eff} is lower than the bulk data, most likely due to RCS as discussed above. The electron mobility in (110)/<110> inversion layers is the lowest among the various silicon crystal orientations, since quantization effects mean the valleys, with the heaviest m_{tran} are the most populated - in this case, the Δ_4 valleys, whilst the low m_{tran}, Δ_2 valleys, are only scarcely populated. The enhancement of electron μ_{eff} at high N_{inv} suggests the presence of strain in the sidewalls of the fins. Since the devices did not intentionally receive any stress liners, stress induced by the metal gate must be responsible.

6.5.2 p-finFETs

Figure 6.8 shows hole μ_{eff} for W_{fin} ranging from 12 nm to 1866 nm as a function of N_{inv}. Data from Irie *et al.*[119] on (100)/<110> and (110)/<110> planar bulk SiO_2/Si MOSFETs has been included for reference with the quasi-planar and (110) dominated finFETs respectively. In contrast to the n-finFETs, the quasi-planar finFET and (100) reference are in close agreement which implies RCS and RPS are negligible in this case. The negligible RPS can be explained using the arguments

above. The discrepancy with the n-finFETs on the role of RCS is unclear. However it is akin to the experimental findings by Casse *et al.*[51], Weber *et al.*[221] and Lime *et al.*[222] who show holes are far less affected by RCS than electrons. For $W_{fin} \leq 26$ nm, hole μ_{eff} is in agreement with the (110) reference up to $2x10^{12}$ cm^{-2}, after which, it decreases. This is most likely due to the sidewalls having a larger roughness. This hypothesis is examined in more detail in section 6.7.

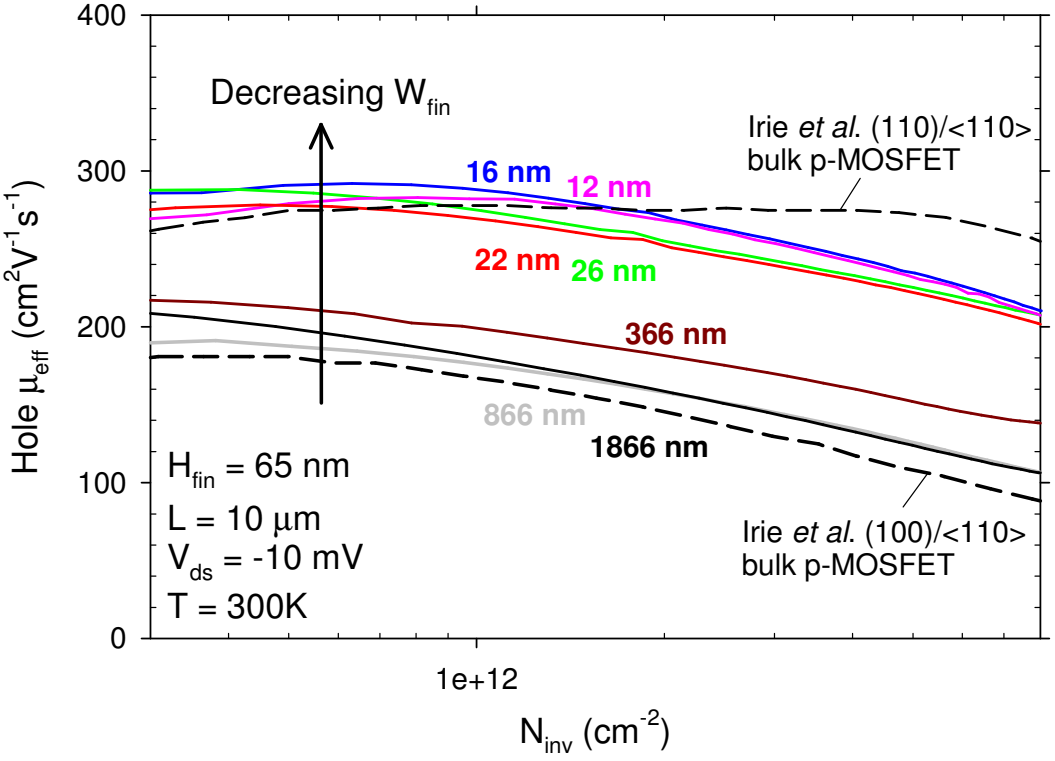

Figure 6.8 Hole μ_{eff} for W_{fin} ranging from 12 to 1866 nm. Irie *et al.*'s[119] planar bulk (100)/<110> and (110)/<110> p-MOSFET data is included for reference.

6.6 Strain characterisation

The results in this section were carried out by the device modelling group at DIEGM, Via delle Scienze, Udine, Italy, Nano-materials group CEMES-CNRS, France and NXP Semiconductors, Belgium.

In section 6.5.1 it was proposed that strain in the fin sidewalls induced by the metal gate was the likely cause of the enhanced electron mobility. Simulations of the impact of stress in the main device directions i.e. fin height (T_{fH}), fin width (T_{fW}) and along the channel (T_{fL}) on the sidewall mobility were performed by DIEGM. The stress impact was analysed by means of double gate electron and hole mobility simulations where stress was systematically applied along each of the directions. Figure 6.9 and Figure 6.10 show the simulated FinFET mobility change induced by each one of the three stress components. As seen, a non-trivial dependence of the mobility on the device stress components is predicted. Tensile and compressive stress along the channel enhances electron and hole mobility respectively. However compressive stress in the fin height increases the electron mobility while hardly effecting the hole mobility, thereby explaining the experimental mobility.

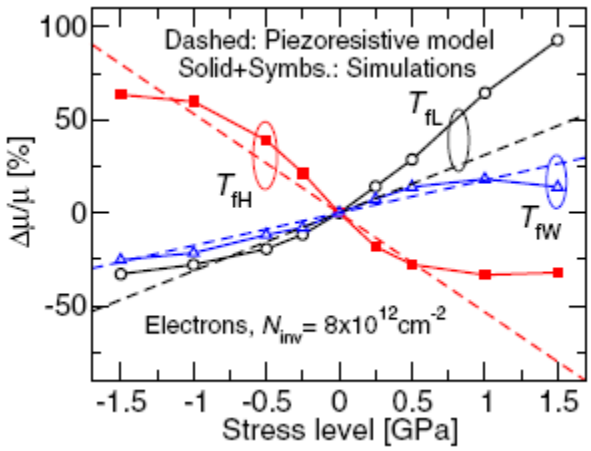

Figure 6.9 Simulated electron mobility change induced by stress components in the fin height, width and length directions. Simulation is for the (110) sidewalls of a n-finFET at N_{inv} = 8x10^{12} cm^{-2}. (Simulations performed at DIEGM. Figure sourced from [223])

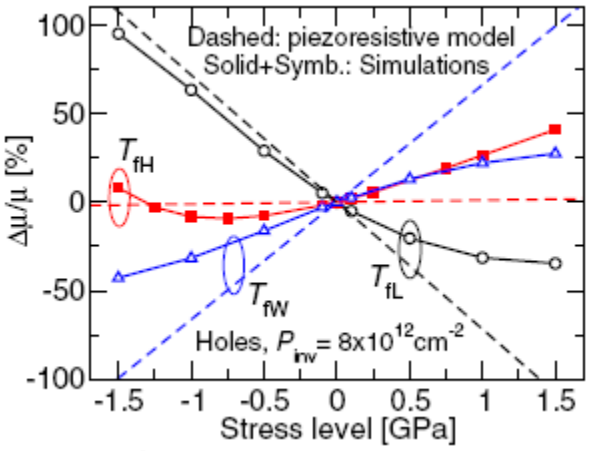

Figure 6.10 Simulated hole mobility change induced by stress components in the fin height, width and length directions. Simulation is for the (110) sidewalls of a p-finFET at N_{inv} = 8x10^{12} cm^{-2} (Simulations performed at DIEGM. Figure sourced from [223])

Figure 6.11 summarises the effect on mobility of the stress components.

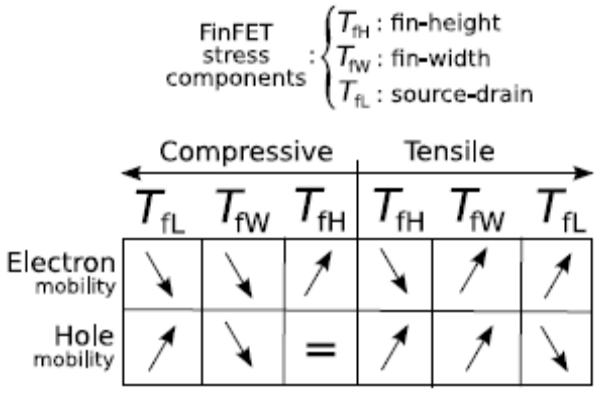

Figure 6.11 The impact on the electron and hole FinFET mobility of the three device stress components, according to mobility simulations at DIEGM. There are stress configurations that can simultaneously improve both electrons and hole mobility. Note a tensile T_{fL} for electrons and compressive T_{fL} for holes stress may be exploited to further enhance FinFET mobility. (Sourced from [223])

To gain a definitive understanding, direct measurements of the finFET strain were made with a novel holographic interferometry technique[224] at CEMES-CNRS. Figure 6.12 shows the measured strain pattern in the fin cross section. The holographic measurement shows a large compressive strain component in the fin height direction and also a weaker tensile strain component in the fin width direction. Strain along the channel was negligible for the long channel finFETs in this work. For a W_{fin} = 10 nm finFET, strain values of -0.8% in fin height direction and 0.3% in fin width direction were measured corresponding to a dominant fin height stress component of -1.1 GPa. From Figure 6.9 we see this is approximately the stress needed to explain the electron mobility enhancement.

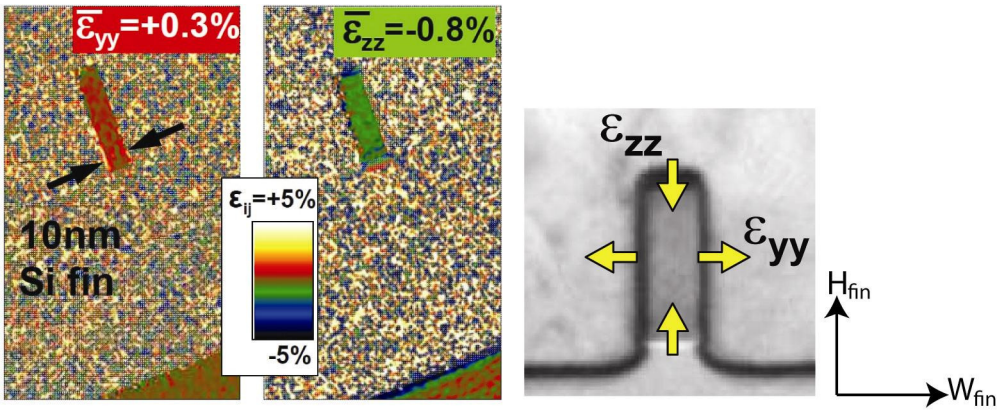

Figure 6.12 Holographic measurement of the strain pattern, induced by the metal gate in a 10 nm fin cross section. There is a large compressive strain component in the fin height direction (shown in green), and also a weaker tensile strain component in the fin width direction (shown in red). Strain in the channel direction is negligible in long channels. Measurement was performed at CEMES-CNRS, France. (Adapted from [223])

Calculations at DIEGM showed that the mechanism responsible for the electron mobility enhancement is strain-induced re-population of the Δ_2 valleys produced by the compressive T_{fH} stress. This causes a lowering of the Δ_2 valleys with respect to the Δ_4 valleys leading to a repopulation of the Δ_2 valleys, reverting the unstrained population situation. Since the Δ_2 valleys feature a low m_{tran}, mobility enhancements follows from this repopulation effect. Note the strain is antagonistic with respect to the sub-band splitting produced by confinement which lowers the Δ_4 valleys. Hence the stress-induced re-population is more effective at small than at large N_{inv}.[141] Figure 6.13 shows the occupancy of the Δ_2 and Δ_4 valleys as a function of compressive T_{fH} stress when N_{inv} = 8x10^{12} cm^{-2}. For T_{fH} = -1.1 GPa, 90% of electrons occupy the Δ_2 valleys.

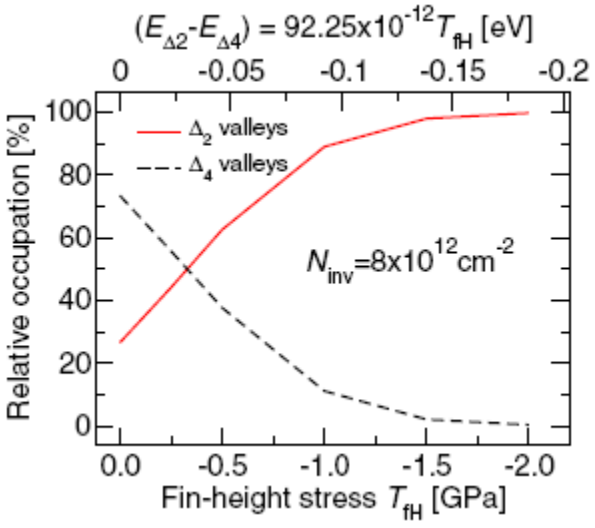

Figure 6.13 Occupancy of the Δ_2 and Δ_4 in (110) silicon at N_{inv} = 8x10^{12} cm^{-2} as a function of fin-height stress. The formula on the top axis expresses the relative energy shift of the Δ_2 valleys with respect to the Δ_4 valleys as a function of the fin height stress component. (Simulation performed at DIEGM. Figure sourced from [223])

Process simulations performed at NXP revealed that the large vertical compressive strain and weaker tensile strain in the fin width direction is induced by the large difference in the thermal expansion coefficients of the silicon channel and the TiN metal gate (2.5 and 9.4 respectively). The strain is formed by plastic relaxation of TiN gate during the cooling phase of the high temperature anneal. By comparison, the as-deposited strain due to intrinsic stress in TiN was found to be negligible.

Simulations of the sidewall mobilities at 300 K and 77 K were performed at DIEGM using a multi sub-band Monte Carlo simulator. Using the strain values in Figure 6.12, good agreement was obtained with the measured mobilities for n- and p-finFETs with $W_{fin} \leq 36$ nm. Data measured by the author at 77 K data, are not included in this thesis and the reader is referred to Serra *et al.*[223]

No simulations were performed on the effect of the stress on the top surface mobility. As the stress is predominantly applied perpendicular to this surface, it is reasonable to assume the mobility is unaffected.

6.7 4 K effective mobility

6.7.1 n-finFETs

By cooling to 4 K the effects of interface related charge and roughness can be analyzed, as phonons are frozen out. Figure 6.14 shows the 4 K electron mobility for n-finFETs with W_{fin} in the range of 16 nm to 1872 nm. For reference (100)/<110> and (110)/<110> bulk n+poly-Si/SiO_2/Si n-MOSFETs from section 5.5.2 have been included.

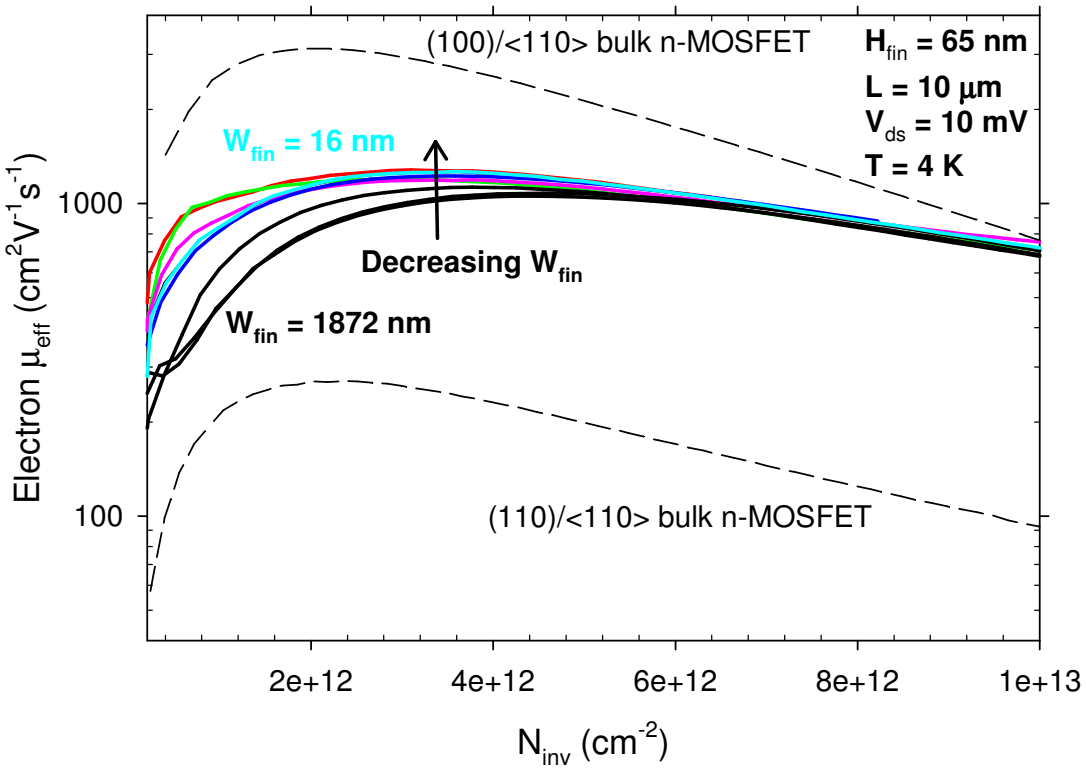

Figure 6.14 Electron μ_{eff} measured at 4 K for W_{fin} ranging from 1872 nm to 16 nm. Bulk (100)/<110> and (110)/<110> n-MOSFET data (dashed lines) included for comparison.

As the majority of electrons occupy the Δ_2 valleys on both the (100) top surface and (110) sidewall interfaces, with $m_{tran} = 0.190m_0$, we might expect μ_{eff} to be relatively independent of W_{fin}. However, at low N_{inv}, μ_{eff} is lower in the quasi-planar finFETs signifying a higher Coulomb scattering rate on the (100) top surface. Since there is no reason to expect that the magnitude of interface or remote charges should be higher on the top interface, this increase in scattering suggests the difference in confinement between the two interfaces maybe responsible. On the (100) interface, $m_{conf} = 0.916m_0$, whereas on the (110) interface, $m_{conf} = 0.190m_0$ although this latter value increases slightly due to energy band non-parabolicity. Thus electrons are confined closer to the (100) interface. Therefore the scattering rate is higher for a

given interface or remote charge density. At high N_{inv}, μ_{eff} is independent of W_{fin} demonstrating a comparable LRS rate between the top and sidewall interfaces. Since electrons are confined further from the (110) interface, the sidewalls must be physically rougher than the top surface for LRS to be the same. The origin of this could be due to the damage incurred by the dry etch. The H_2 anneal may not have fully restored the sidewall surfaces to match that of the top surface, not exposed to this etch. Interestingly, a reduction in interface roughness due to strain has been reported for biaxial tensile strained MOSFETs[225], however there is no evidence of a reduction due to strain here.

The large degradation of mobility in the quasi-planar finFET below the bulk (100)/<110> n-MOSFET particularly at low N_{inv} can be explained by high remote charge density, particularly as the bulk MOSFET has a higher doping concentration. The large difference in band structure between the (110) dominated finFETs and the bulk (110)/<110> n-MOSFET makes a qualitative comparison of physical parameters such as roughness difficult.

6.7.2 p-finFETs

Figure 6.15 shows the 4 K hole mobility for n-finFETs with W_{fin} in the range of 22 nm to 1872 nm.

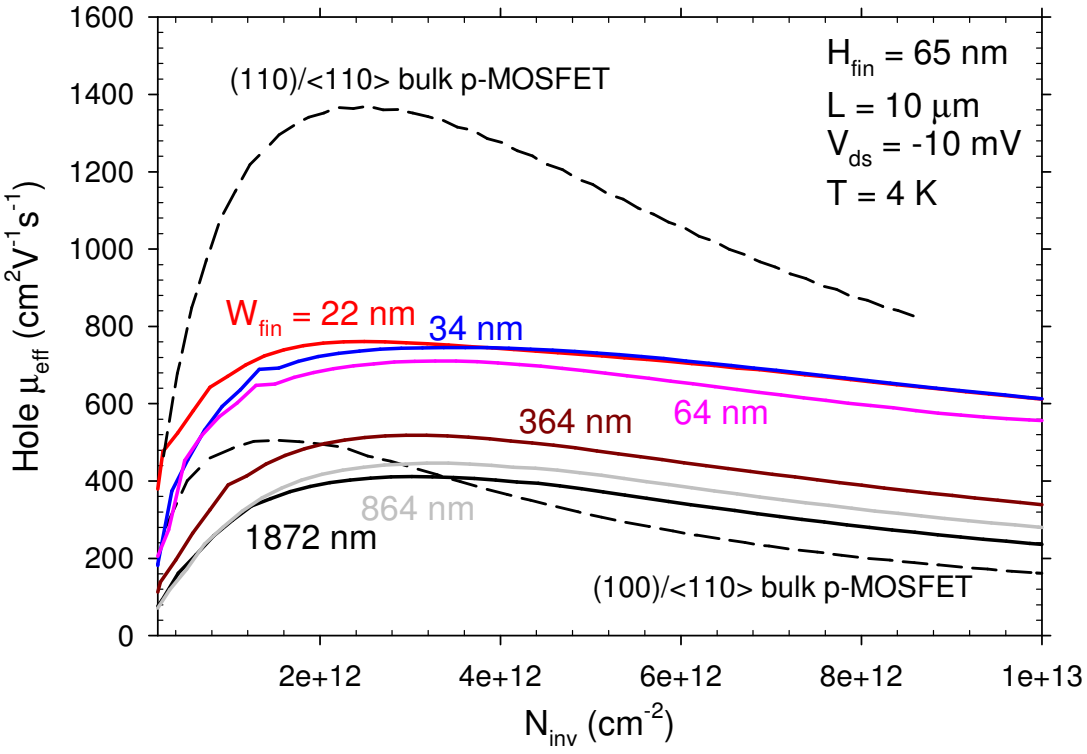

Figure 6.15 Hole μ_{eff} measured at 4 K for p-finFETs with W_{fin} ranging from 1872 nm to 22 nm. (110)/<110> and (100)/<110> bulk p-MOSFET data (dashed lines) included for comparison.

From the discussion on 4 K electron mobility a higher sidewall roughness should be observed for the p-finFETs since they underwent the same processing, with exception of the source and drain implants. However, due to the large difference in valence band structure between the (100)/<110> and (110)/<110> orientations, which is left unchanged by the strain, it is difficult to ascertain if roughness is larger on the sidewalls just by comparing μ_{eff} between the (110) dominated and quasi-planar finFETs. To assist understanding, the bulk n+polySi/SiO_2/Si (100)/<110> and (110)/<110> p-MOSFET data from section 5.6 have been included for comparison. (Corresponding room temperature μ_{eff} agrees with literature data at high N_{inv}. See figure 5.22) Although these bulk p-MOSFETs have a higher substrate doping

therefore IIS rates, their μ_{eff} is higher than that of the finFETs at low N_{inv} suggesting RCS is important at low temperature.

At high N_{inv} the quasi-planar finFETs exhibit a slightly higher μ_{eff} (as was the case at room temperature). This might be explained by the lower E_{eff} due to the lower doping therefore lower LRS. For $W_{fin} \leq 64$ nm, μ_{eff} remains significantly lower than the (110)/<110> bulk p-MOSFETs suggesting higher sidewall roughness, confirming the hypothesis to explain the electron μ_{eff}.

6.8 4 K modelling of quasi-planar finFETs

Following the procedure outlined in section 5.6, the same models can be applied to the 4 K electron and hole μ_{eff} in the quasi-planar finFETs (W_{fin} = 1872 nm), by treating them as (100)/<110> planar MOSFETs. As we suspect remote charges from the high-κ/SiO_2 interface are significant, an analytical model for RCS is required. We will adapt the model by Yang and Henson[37] who formulated a model for Coulomb scattering from ionised dopant impurities in a polysilicon gate in a n+polySi/SiO_2/Si MOSFET. Their analysis is based on ground sub-band occupation; Δ_2 minima for electrons and HH band for holes. In their analysis they model 300 K electron μ_{eff}. They derive the following momentum relaxation time;

$$\frac{1}{\tau_k} = \frac{m_{scat} e^4 N_{poly}}{8\pi\hbar^3 (\varepsilon_0 \varepsilon_r)^2} \int_0^{2\pi} \frac{P_0^2 \left(e^{-2qz_1} - e^{-2qz_2}\right)(1-\cos(\theta))}{2q\left(q + \bar{s}\left(P_{av} + \delta P_0^2\right)\right)^2} d\theta \qquad (6.1)$$

In their notation, z_1 is the physical thickness of the gate oxide and z_2-z_1 the width of the depletion region in the polysilicon gate when a gate voltage is applied. N_{poly} is the doping concentration of the gate.

$$P_{av} = \frac{8b^3 + 2b^2 q + 3bq^2}{8(b+q)^3} \tag{6.2}$$

$$\varepsilon_r = \frac{\left(\varepsilon_{Si} + \varepsilon_{SiO_2}\right)}{2} \tag{6.3}$$

$$\delta = \frac{\left(\varepsilon_{Si} - \varepsilon_{SiO_2}\right)}{2\varepsilon_r} \tag{6.4}$$

The screening function due to N_{inv} is given by;

$$\bar{s} = \frac{e^2 N_{inv}}{2\varepsilon_0 \varepsilon_r E_F} \tag{6.5}$$

By modelling the charge distribution as a delta function, δ_z at a high-κ/SiO_2 interfacial oxide interface as shown in Figure 6.16, we can write;

$$z_2 = z_1 + \delta_z \tag{6.6}$$

Substituting equation (6.6) into equation (6.1), replacing N_{poly} with n_r, a sheet density of charge and using Taylor expansion, we can write;

$$\frac{1}{\tau_k} = \frac{m_{scat} e^4 n_r}{8\pi\hbar^3 \left(\varepsilon_0 \varepsilon_r\right)^2} \int_0^{2\pi} \frac{P_0^2 \left(2qe^{-2qz_1}\right)(1-\cos\theta)}{2q\left[q + \bar{s}\left(P_{av} + \delta P_0^2\right)\right]^2} d\theta \tag{6.7}$$

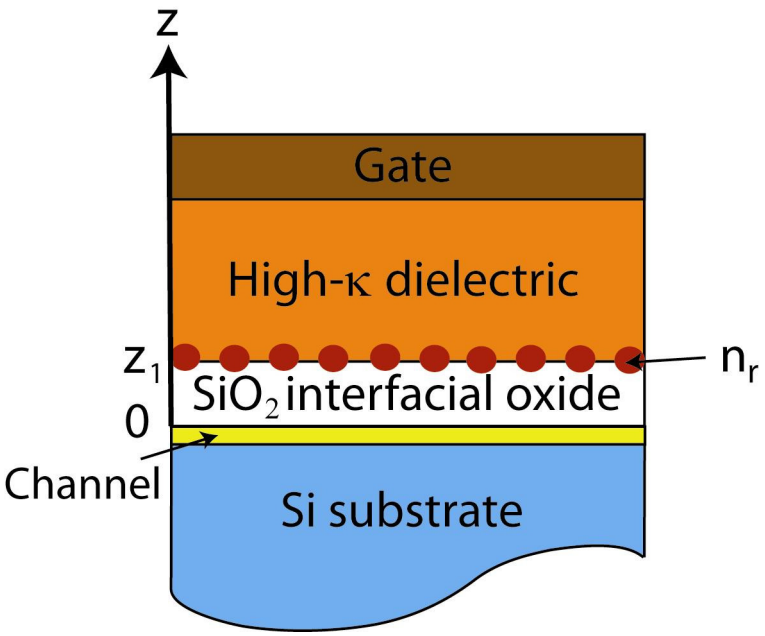

Figure 6.16 Schematic of a high-κ gate stack. Remote charge density, n_r is modelled as a sheet of charge at the high-κ/SiO_2 interface. Keeping with, Yang and Henson's notation, z_1 is the interfacial oxide thickness.

We can thus extract the roughness parameters of the (100) surface and quantify any remote charge. Using Matthiessen's rule;

$$\frac{1}{\mu_{Tot}} = \frac{1}{\mu_{RCS}} + \frac{1}{\mu_{IIS}} + \frac{1}{\mu_{LCS}} + \frac{1}{\mu_{LRS}} \tag{6.8}$$

The D_{it} value of $1\text{x}10^{11}$ cm^{-2} measured in weak inversion was used in the LCS model and the room temperature doping concentration of $1\text{x}10^{15}$ cm^{-3} used in the IIS model. n_r, Δ, Λ were used as fitting parameters to the experimental data. Intuitively we expect these to be similar for the n- and p-finFETs. The modelled 4 K electron and hole effective mobilities are shown in Figure 6.17 and Figure 6.18. The modelling parameters are shown in Table 6.1.

	4 K modelling parameters				
	RCS	LCS	IIS	LRS	
	n_r (cm^{-2})	n_{imp} (cm^{-2})	N_a (cm^{-3})	Δ (nm)	Λ (nm)
n-finFET	$8.0x10^{12} \pm 0.5x10^{12}$	$1.0x10^{11}$	$1.0x10^{15}$	0.41 ± 0.05	2.3 ± 0.3
p-finFET	$8.0x10^{12} \pm 0.5x10^{12}$	$1.0x10^{11}$	$1.0x10^{15}$	0.38 ± 0.05	2.3 ± 0.3

Table 6.1 Parameters used in the mobility modelling of quasi planar n- and p- finFETs

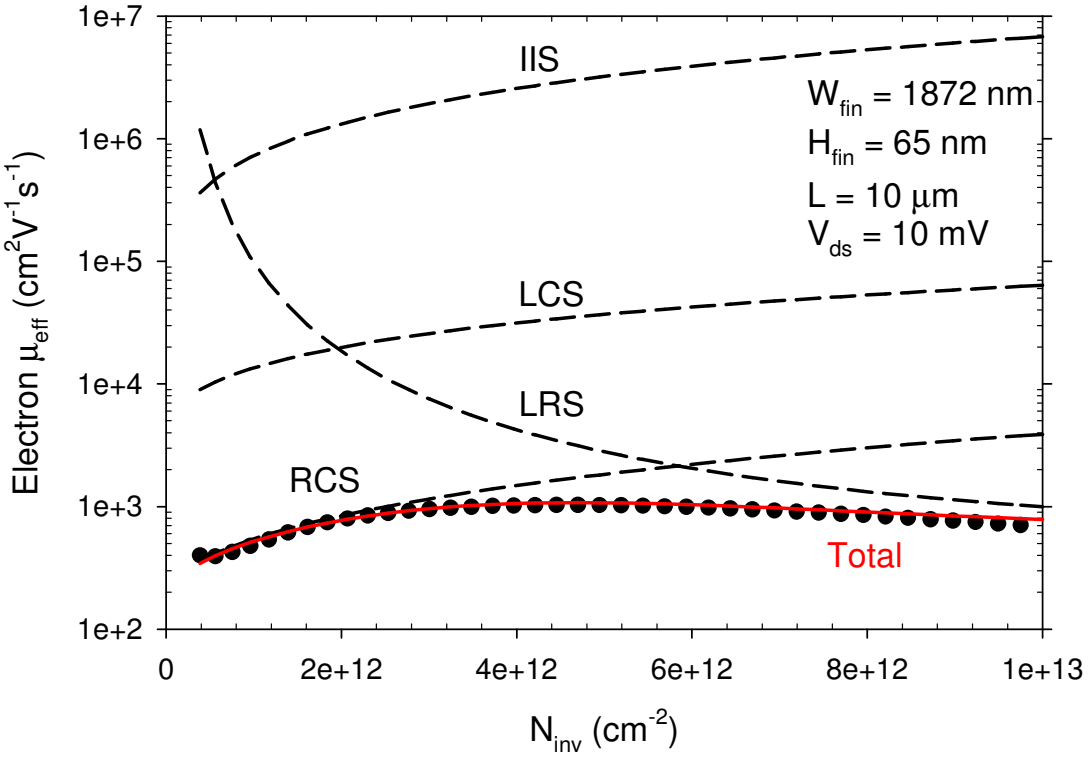

Figure 6.17 4 K electron μ_{eff} of a quasi-planar n-finFET (W_{fin} = 1872 nm) modelled in terms of ionised impurity, local Coulomb, remote Coulomb and local roughness scattering mechanisms.

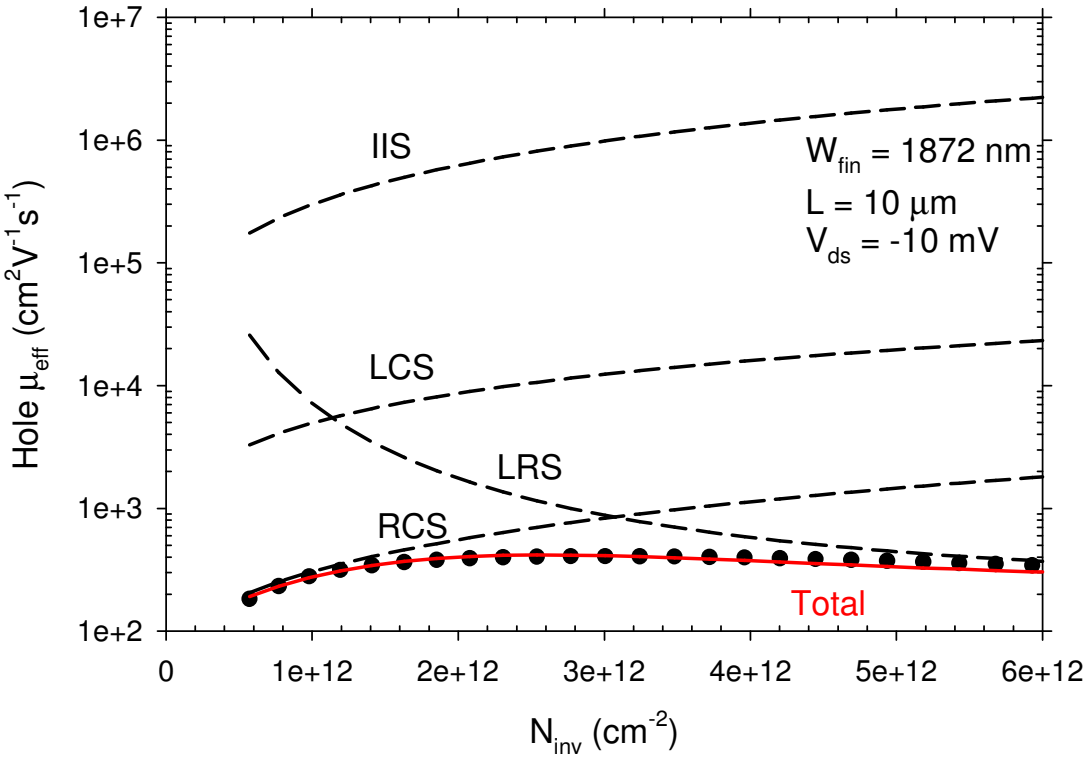

Figure 6.18 4 K hole μ_{eff} of a quasi-planar p-finFET (W_{fin} = 1872 nm) modelled in terms of ionised impurity, local Coulomb, remote Coulomb and local roughness scattering mechanisms.

Note the small impact of LCS and IIS on electron and hole μ_{eff}. In the RCS model, a value of $n_r = 8\text{x}10^{12}$ cm^{-2} was required to fit both sets of data at low N_{inv}, showing that RCS is the dominant Coulomb scattering mechanism. It still has an impact on mobility, particularly so for electrons at $N_{inv} = 1\text{x}10^{13}$ cm^{-2}. It is unclear why RCS is dominant at 300 K down to 4 K for electrons but only at 4 K for holes. This is also observed by Lime *et al.*[222] who state Coulomb scattering "contributes more efficiently at low temperature". The extracted values of n_r are not too different from that obtained by Kaushik *et al.*[64] Using an etching technique, they estimate n_r ~ $6\text{x}10^{12}$ cm^{-2} in devices with a $Hf_{0.5}Si_{0.5}O$ dielectric deposited by MOCVD and a 10 nm TaN/TiN gate electrode, exposed to a 1000°c RTA. (D_{it} in their case < $3\text{x}10^{11}$ cm^{-2}.) In section 6.7.1 it was speculated that the weaker confinement on the

strained (110) surface compared to the (100) surface was the reason for the higher electron mobility at low N_{inv}. The models show that the mobility is indeed a strong function of m_{conf}. Using, m_{conf} = 0.190m_0 as opposed to 0.916m_0 results in a 50% higher RCS calculated mobility and a 70% higher LCS calculated mobility at N_{inv} = $1x10^{12}$ cm^{-2}. At N_{inv} = $8x10^{12}$ cm^{-2} the LRS calculated mobility is higher by 22%. It should be pointed out that a TiN gate can modify the interface roughness. This is process dependent.[51, 226] The extracted values of Δ and Λ in the present work are in rough agreement with those obtained for the bulk poly-Si/SiO_2/Si MOSFETs in table 5.7. Thus it can be deduced this is insignificant for the gate stack in the present work.

Upon the author's request, a multi sub-band Monte Carlo simulation of the 300 K electron mobility of a quasi-planar n-finFET (W_{fin} = 1872 nm) was performed, using the remote charge density extracted at 4 K. The simulation and comparison to the measured data is shown in Figure 6.19.

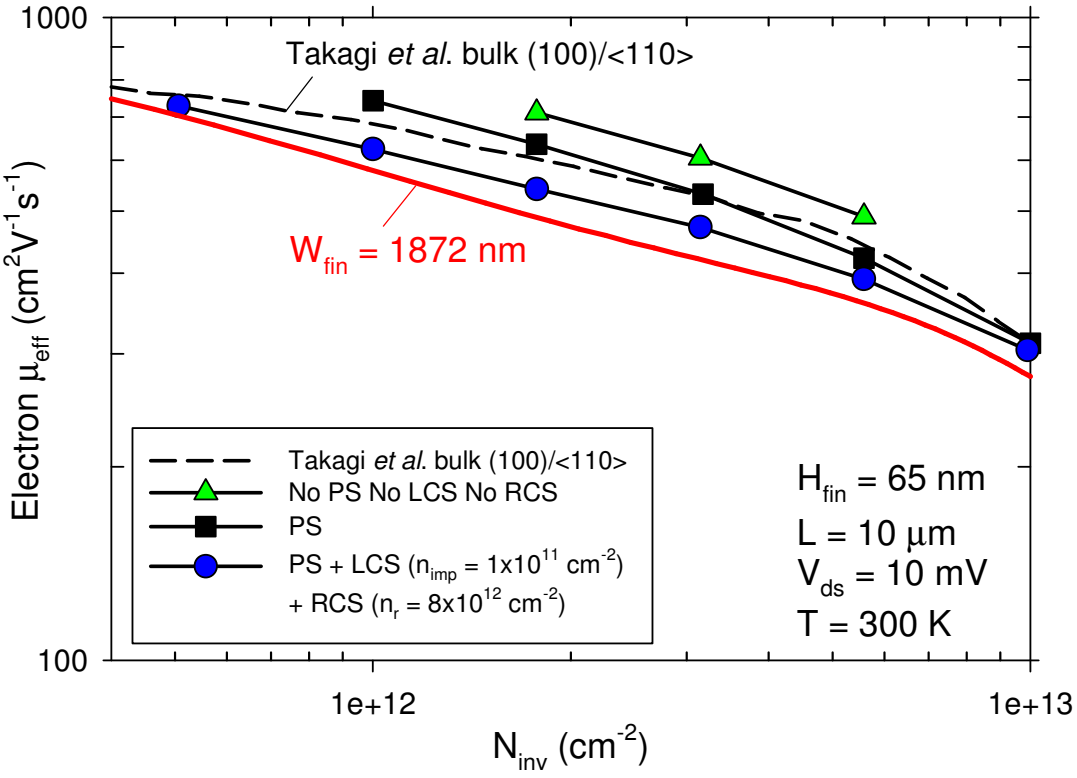

Figure 6.19 Multi sub-band Monte Carlo simulations of the 300 K electron mobility of a quasi-planar n-finFET (performed at DIEGM). The effects of phonon scattering (bulk and remote) PS, LCS and RCS are independently shown. LRS is included in all simulations. The remote charge density extracted at 4 K, is used in the modelling of RCS with the resulting mobility within 12% of the measured mobility. Takagi *et al.*'s bulk Si/SiO_2 (100)/<110> data is shown for reference.

It was found that accounting for all the scattering mechanisms (detailed in the figure), the simulated mobility agrees with the measured mobility to within 12%. Note also RCS accounts for the mobility degradation below the bulk SiO_2/Si reference, confirming the argument in section 6.5.1. This indicates the simple analytical approach developed here to extract remote charge density, is a reasonable approximation at room temperature.

6.9 Summary

This chapter presents detailed mobility analysis of n- and p-finFETs, with fin widths of 1872 nm (quasi-planar) down to 12 nm and TiN/$Hf_{0.4}Si_{0.6}O$/SiO_2 gate stacks. The finFETs have a (100) top surface and (110) sidewalls. Electron and hole mobilities were extracted at 300 K and 4 K. The 300 K (110) sidewall electron mobility showed a 60% enhancement over the (110) bulk MOSFET literature reference data. This was due to vertical compressive strain in the fin sidewalls induced by the difference in thermal expansion coefficients between the TiN gate and Si fin. This strain leaves the hole mobility unaffected.

The electron mobility of a quasi-planar ((100) dominant) n-finFET was found to be approximately 20% lower than the (100) bulk MOSFET literature reference. This was attributed to remote Coulomb scattering. On the other hand, the hole mobility was not degraded by remote charge and was in agreement with the literature (100) reference.

Analysis of the 4 K electron and hole mobility suggests the sidewall roughness is higher than on the top surface. This is probably due to the damage caused by the dry (reactive ion) etch used to pattern the sidewalls, which suggests that the H_2 anneal, used to repair the damage is insufficient.

A model for remote Coulomb scattering from the $Hf_{0.4}Si_{0.6}O$/SiO_2 interface was developed. Analytical modelling of the 4 K electron and hole mobilities of quasi-

planar finFETs was then performed in terms of remote charge scattering, ionised impurity, local charge and roughness scattering mechanisms. Remote charge densities of $8x10^{12}$ cm^{-2} were subsequently extracted. Roughness parameters at the SiO_2/Si interface were found to be comparable to literature values, indicating good top surface interface quality.

Chapter 7 : Conclusion

This thesis has provided greater understanding of the carrier transport in novel Si MOSFETs and finFETs, which industry is currently researching. The focus is on the accurate extraction and modelling of carrier mobility to assess the performance limiting mechanisms. The findings are highly relevant for the continuation of Si based technology.

The main results are summarised below.

7.1 Chapter 4

In chapter 4, the extraction of the effective channel mobility and possible errors have been analysed in detail. The analysis shows that the variation in the field along the channel is exactly compensated by the diffusion current in the limit $V_{ds} \to 0$. Blindly extracting the mobility at a drain bias of 50 mV, as is usually done, underestimates the mobility. A novel regression technique was proposed to extrapolate the drain conductance to zero drain bias in order to correct for the difference in drain bias between I_d-V_{gs} and C_{gc}-V_{gs} measurements. Thus, accurate mobility is obtained using the drift only expression with the drain conductance correction, providing the inversion charge is known accurately. However, accurate extraction in weak inversion is now limited by errors in deducing the inversion charge.

7.2 Chapter 5

In chapter 5, n- and p-MOSFETs fabricated on (100) and (110) substrate orientations were electrically characterised in detail. The MOSFETs had channel lengths of 25 μm and n+polySi/SiO_2 gate stacks which enabled detailed analysis of the mobility dependence on substrate orientation and channel direction without being concerned with high-κ dielectric related scattering mechanisms. Mobility measurements were performed at 300 K and 4 K, the latter for freezing out phonons and allowing qualitative and quantitative analysis of just Coulomb and interface roughness scattering mechanisms. The behaviour of electron mobility is well known and was explained using the constant effective masses corresponding to the conduction sub-band minima. On the contrary, due to the complex nature of the valence band, hole mobility is less well understood. Zone centre effective masses, which are usually reported, were unable to explain the observed mobility dependence on inversion charge density, substrate orientation and channel direction. Simulations of the relevant masses were performed, at 300 K and 4 K by Luca Donetti at Universidad de Granada, by averaging the mass calculations over the Brillouin zone, weighted by the Fermi distribution to obtain the effective masses as a function of inversion charge density. Using these masses, a qualitative description of the mobility was performed. Analytical modelling of the 4 K electron and hole mobility in terms of ionised impurity, local charge and roughness scattering mechanisms revealed comparable Si/SiO_2 interface quality between the (100) and

(110) orientations. Monte Carlo simulations of the 300 K mobility are currently in progress at Universidad de Granada for comparison.

7.3 Chapter 6

Chapter 6 is based on detailed mobility analysis of n- and p-finFETs, with fin widths of 1872 nm (quasi-planar) down to 12 nm and TiN/$Hf_{0.4}Si_{0.6}O$/SiO_2 gate stacks. The finFETs in this study have a (100) top surface and (110) sidewalls. Electron and hole mobilities were measured at 300 K and 4 K (additional work at 77 K is not shown in this thesis). For inversion charge densities above $5x10^{12}$ cm^{-2}, a 60% enhancement of the 300 K sidewall electron mobility was found over (110) bulk MOSFET literature reference data, which implied that the sidewalls were strained. The corresponding stress is due to a difference in thermal expansion coefficients between the TiN gate and Si fin which induced vertical compressive strain into the fin sidewalls. This strain serves to enhance the electron mobility and leaves the hole mobility unaffected. For inversion charge densities below $5x10^{12}$ cm^{-2}, the sidewall electron mobility was degraded below the reference due to remote charge scattering from the $Hf_{0.4}Si_{0.6}O$/SiO_2 interface.

The electron mobility of a quasi-planar n-finFET was found to be approximately 20% lower than the literature (100) reference. This was attributed to the remote charge scattering. On the other hand, the hole mobility was not degraded by remote charge and was in agreement with the literature (100) reference.

Analysis of 4 K electron and hole mobility suggests the sidewall roughness is higher than on the top surface. This is probably due to the damage caused by the dry (reactive ion) etch used to pattern the sidewalls, which suggests that the H_2 anneal, used to repair the damage is insufficient. Thus even higher mobilities may be realised if this is addressed.

A model for remote charge scattering from the $Hf_{0.4}Si_{0.6}O/SiO_2$ interface was developed by adapting an existing model for remote charge scattering from ionised impurities in a polySi gate. Analytical modelling of the 4 K electron and hole mobilities of quasi-planar finFETs was then performed in terms of remote charge scattering, ionised impurity, local charge and roughness scattering mechanisms. Remote charge densities of $8x10^{12}$ cm^{-2} were necessary to fit both the electron and hole mobility at low inversion charge densities. Extracted roughness parameters were comparable with values extracted in chapter 5 and literature values for the SiO_2/Si interface, thus showing good fin top surface interface quality. Upon the author's request, a Monte Carlo simulation of the 300 K electron mobility of a quasi-planar n-finFET was performed at University of Udine, using the extracted remote charge density. The simulated and measured mobility were within 12% of each other, showing that the parameters deduced at low temperature are in reasonable agreement with those at 300 K.

7.4 Further work

While this work has contributed to our understanding of the mobility limiting mechanisms associated with Si MOSFETs, finFETs and high-κ/metal gates, there is still considerably more to learn. For instance, low frequency (1/f) noise measurements and their modelling on the finFETs may provide further insight into the role of oxide charge trapping for corroboration with the mobility data. In addition, measurements on the 45° rotated finFETs (i.e. with sidewalls in the (100) plane) would enable analysis of the mobility on these strained (100) surfaces. Little has been published in these areas.

The Si MOSFETs on (100) and (110) wafers analysed in chapter 5 are part of a batch which contain buried channel pseudomorphic strained $Si_{1-x}Ge_x$ (x = 0.2 and 0.4) n- and p-MOSFETs which are also fabricated on these orientations and have channels in the full range of directions. Although SiGe has been intensively researched in the past for MOSFET applications, a full analysis of this batch following the analysis used for the Si MOSFETs in this thesis may provide more detailed understanding of the carrier transport and mobility limiting scattering mechanisms.

The impact of the high-κ/metal gate is still a hot topic amongst researchers, and there would be scope to further improve the model for remote charge scattering proposed here, especially with regard to analysing "higher-κ" dielectrics (e.g. Ti-based) and metal gate combinations. No study yet has been undertaken to

compare different metal gate materials and thicknesses for the purpose of inducing stress in finFETs and the subsequent impact on mobility. There is also considerable scope for further research on strained SiGe or pure Ge based finFETs. Such devices could have significantly higher mobilities and be of relevance for future technology nodes.

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