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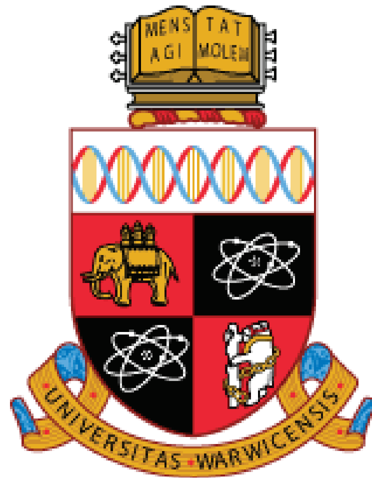

Epitaxial growth of relaxed Ge buffers on (111) and (110) Si substrates using RP-CVD

by

Van Huy Nguyen

Thesis

Submitted to the University of Warwick

in partial fulfilment of the requirements

for admission to the degree of

Doctor of Philosophy

Department of Physics

THE UNIVERSITY OF

WARWICK

Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. All experimental data presented was carried out by the author, or (where stated) by specialists under the author's direction.

Abstract

The continued scaling of Si metal oxide semiconductor field effect transistor (MOSFET) devices to enhance performance is reaching its fundamental limits and the need for new device architecture and/or new materials is driving research and development within the semiconductor industry. Germanium, with its much higher intrinsic carrier mobilities, has a considerable advantage over Si as a channel material and its compatibility with current complementary metal oxide semiconductor (CMOS) technology makes it a very promising candidate. There is currently significant technological interest in the epitaxial growth of high quality relaxed Ge layers directly on Si substrates for potential applications including: high-mobility metal-oxide-semiconductor field-effect-transistors (MOSFETs), infrared photodetectors, solar cells and III-V integration. The crystallographic orientation of the substrate also influences the inversion layer mobility in transistors; compared to (100) orientation, Ge grown on (111) and (110) substrates can considerably enhance the carrier mobilities for electrons and holes. The 4.2% mismatch between Ge and Si is, however, a major drawback for the growth of high quality epitaxial layers, as 3-dimensional islanding, surface roughening and the generation of a high density of defects can occur which are all detrimental to performance of prospective devices. In particular, epitaxial growth on (110) and (111) surfaces is more susceptible to the formation of extended stacking faults as the gliding sequence of the dissociated 30° and 90° partial dislocations is reversed with respect to that for the (100) surface. This means that the concept of a thick graded buffer for gradual strain relaxation is not as easily applicable in the case of (111) and (110) substrates.

In this work, we have investigated the growth of relaxed Ge films on (111) and (110) Si substrates by reduced-pressure chemical vapour deposition (RP-CVD) in an ASM Epsilon 2000 reactor using the high temperature/ low temperature growth technique, which comprises of a thin low temperature (LT) Ge seed, a thick high temperature (HT) Ge layer and subsequent in-situ high temperature H_2 anneal. We will show how the growth conditions influence both the presence and nature of defects within the Ge layers, their surface morphology and also the state of relaxation using transmission electron microscopy (TEM), atomic force microscopy (AFM) and X-ray diffraction (XRD) techniques.

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List of symbols

θ_{SiGe}: bowing parameter that quantifies the deviation from linear behaviour of Vegard's law

λ_a: adatom migration length

γ_{LS}: sum of the interface energy between the layer and the substrate

σ_L: epilayer surface energy

σ_S: substrate surface energy

ε: strain of a layer

$a_{x,y,z}$: lattice constants

E_h: elastic energy stored at the misfit interface

h: layer thickness

h^*: critical thickness

G: bulk shear modulus

ν: Poisson's ratio

$\underline{b}$: Burgers vector

$\underline{b}_{eff}$: effective Burgers vector

β: angle between the Burgers vector and the perpendicular line to the direction of the dislocation

E_r: strain energy relieved by a misfit dislocation

l: length of misfit dislocation

d: depth of epitaxial layer below a surface

v_g: glide velocity of a dislocation

B: arbitrary constant

E_g: activation barrier for glide

k: Boltzmann's constant

T: temperature

G_{ij}: interactive retarding force on a dislocation

σ_{ij}^I: additional contribution to the applied stress field due to interaction

n_j: number of intersected orthogonal dislocations

$\underline{b}_i$: Burgers vector of the intersecting dislocation

B_g: boundary defined by the intersecting dislocation threading arm

F_h: driving force on a threading dislocation dependent on layer thickness

F_d: tension force required to overcome the Peierls energy barrier

D: equilibrium separation between partial dislocations

F_p: repulsive force per unit length between the partials

d_f: minimum resolvable feature size

λ: wavelength of the light source

n: refraction medium

θ_l: half angle subtended by the objective lens

$\underline{g}$: diffraction vector

$\underline{u}$: line direction of dislocation

x,y,z: position of sample on the stage

φ: rotation of sample

ψ: tilt of sample

ω: incident angle of X-ray beam

2θ: angle between the incident and diffracted beam

Acknowledgements

I would like to thank my supervisors Prof. David Leadley and Dr. Maksym Myronov for all their support and encouragement throughout this work.

I would like to reserve special thanks to Dr Andy Dobbie who have guided and supported me with everything throughout my PhD career as a research fellow in the Ge Renaissance Project and also for carrying out the experimental XRD scans and analysis. Special thanks go to Andy and Maksym for providing me with samples as growth scientists.

I would also like to thank Dr Vishal Shah for teaching me a lot of things around the lab, many useful discussions and all the assistance that he's so willing to give. I want to thank Dr. Richard Beanland, Dr. Neil Wilson, Dr. Ana Sanchez for all the help on microscopy aspects and especially Steve York who came to my rescue whenever unexpected problems occurred whilst using the facilities. I also want to thank Dr David Norris who got me started on non-(100) TEM characterisation and Dr Thomas Walther for his initial discussion on the subject.

Many thanks go to all members of the Nano-Silicon Research Group, both new and old for their contributions and their distractions particularly: Prof Evans Parker, Prof Terry Whall, Tim Naylor, Dr Allen Liu, Dr Steve Thomas, and John Halpin.

Lastly, I would like to express my personal gratitude to my parents, sisters, my girlfriend and all my friends for all their support and patience throughout my academic career.

1 Introduction

The Semiconductor Industry Association (SIA) announced in January 2011 that worldwide semiconductor sales for 2010 reached a record $298.3 billion, a year-on-year increase of 31.8 percent from the $226.3 billion recorded in 2009 [1]. The majority of the semiconductor market is attributed to Silicon electronic devices and the rest to various optoelectronic applications [2]. It all started when the first transistors were invented by scientists at Bell Lab [3]. The core of the semiconductor industry has always been the production of metal-oxide-semiconductor field effect transistor (MOSFET). The MOSFET is effectively an on/off switch with four terminals: gate, source, drain and body. The gate is insulated from the channel and modulates the source to drain current to make the device function on and off. A complementary metal-oxide-semiconductor (CMOS) circuit consists of both n-channel and p-channel devices where electrons and holes are the primary carriers respectively. A diagram of a p-channel MOSFET is shown in figure 1.1.

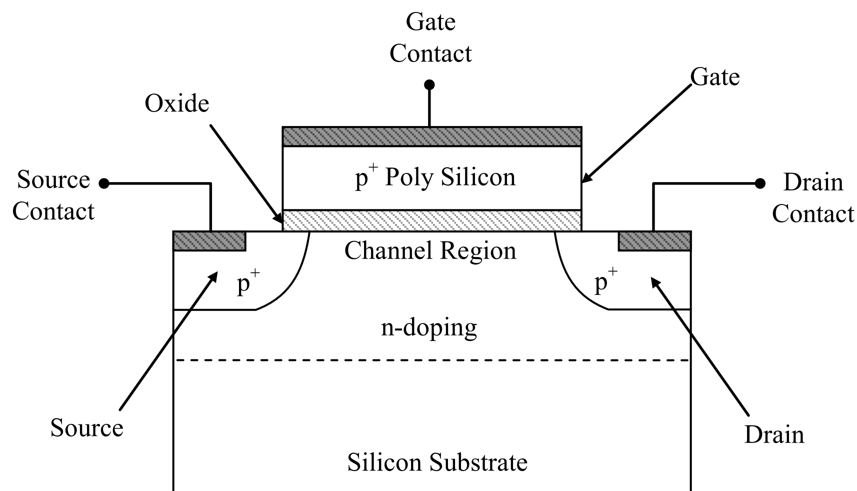


Figure 1-1 Schematic representation of a p-channel MOSFET.

Germanium was the material used to create the first transistor. However, Ge has been overshadowed by Si in the microelectronics revolution. In fact, the first commercially available integrated circuit (IC) was made using Si by Fairchild Semiconductor Corporation and it has been the material of choice for the industry ever since. The primary reasons for the dominance of Si are the natural abundance of this material, making it inexpensive for mass production, and the superior properties of the SiO_2 oxide. The oxide of silicon forms an excellent insulator between the conduction channel and the gate electrode in a MOSFET which can also be exploited as a mask during device fabrication [4, 5].

The semiconductor industry has been in steady growth ever since the observation by Intel co-founder Gordon Moore was made in 1965 that "the number of transistor on a chip doubles every two year". It has been the benchmark for increased performance of computer micro-processors year after year by reducing the dimensions of MOSFETs allowing ever more transistors to be packed together into a single chip (often referred to as *scaling*). Moore's law, as it has always been known, is plotted in figure 1.2 along with generations of Intel processors since 1970 [6].

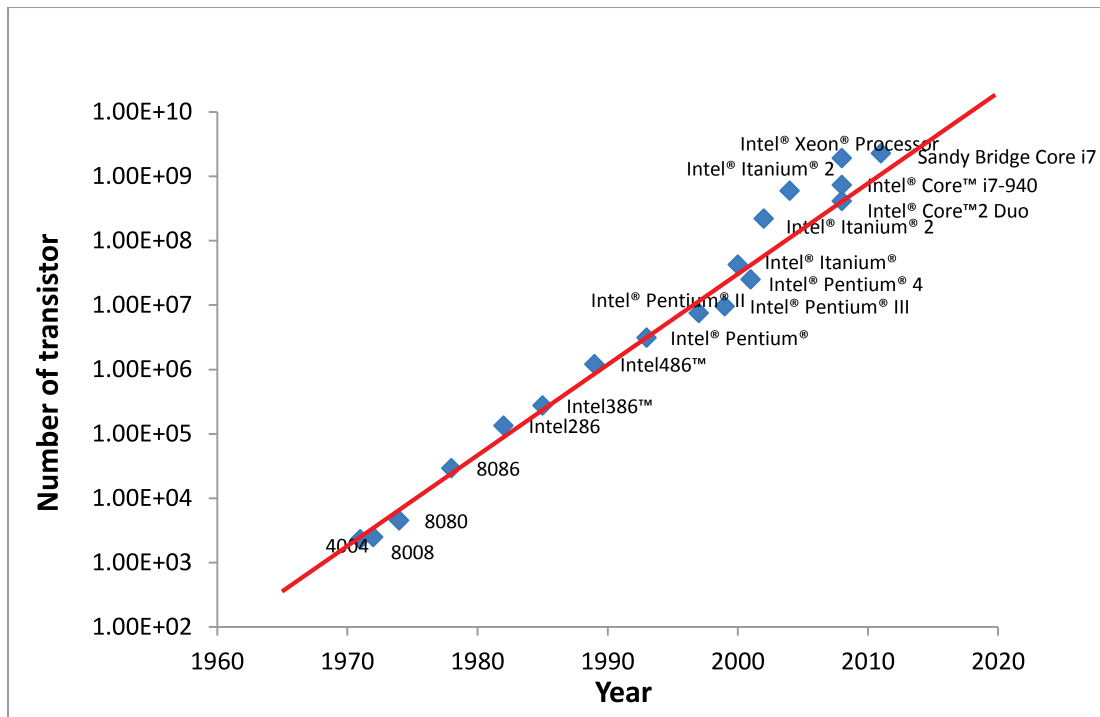


Figure 1-2 A graph showing Moore's law by plotting major generations of Intel® processors and the number of transistors contained versus release date. (Data taken from Intel® website) [7].

However, scaling of MOSFETs to improve chip performance and reduce selling price cannot continue forever unfortunately. Eventually, scaling will reach its fundamental limits as the power dissipation due to leakage current overcomes the output power because of short channel effects; also, economic reasons might prevent the manufacture of smaller electronic devices. According to various publications, taking into account the balance between the gain in drive current and the high leakage associated with ultrathin oxides then 10-12Å could serve as a practical limit [8]. Despite the device performance boundary being pushed closer and closer to the fundamental limit, there is still great optimism that the enhancement in the semiconductor industry can be continued. There has been numerous research being directed into new materials to boost the transistor performance that can be integrated with existing fabrication techniques and preferably scalable to some degree. Such options have been the introduction of strain engineering into existing semiconductor

materials and the renaissance of Ge as a channel material in high mobility transistors. Alternative crystallographic orientations such as (110) and (111) have also promised to yield higher hole and electron mobility enhancements compared to what is available from the industry standard (100) orientation. There have been significant interest on the growth of Ge on (110) and (111) Si substrates due to the higher electron mobility achievable in these orientations. Recent improvements in passivation layers have given rise to record hole and electron mobilities in Ge MOS of 725 cm^2/Vs on (110) and 1920 cm^2/Vs on (111) respectively. It is strongly suggested that high performance Ge CMOS is really feasible [9].

Ge can also be used as a *buffer* whereby a layer of Ge is grown on top of a Si substrate to be used as a template for further growth of different types of heterostructures as using Ge substrates can be very expensive. Apart from high mobility applications, Ge can also be used as infra-red photodetectors [10], Ge lasers [11], solar cells and III-V integration [12]. However, the growth kinetics and dislocation dynamics is less favourable for growing high quality relaxed Ge layers on (110) and (111) Si substrates than for (100) Si. In particular, the gliding sequence of partial dislocations in compressive Ge is reversed for (110) and (111) orientations leading to the formation of stacking faults, which are not observed in relaxed Ge grown on (100) Si.

This thesis sets out to explore the properties of Ge epitaxy as a high quality buffer in (110) and (111) crystallographic orientations. The next chapter will discuss the benefits that Ge can bring over its Si counterpart. Strain engineering and relaxation mechanisms along with dislocation formations in the epitaxial system will be

described in detail. Extra complications in epitaxy and characterisation from the alternative crystallographic orientations will also be explained. Chapter 3 will outline the experimental techniques that have been used to grow and characterise all the samples presented throughout later chapters. Chapter 4 will describe the development of high quality relaxed Ge buffers grown on (111)-oriented Si substrates. Similar investigation of relaxed Ge buffers grown on (110)-oriented Si substrates will be presented in chapter 5. The main conclusions of the work done for this thesis are summarised in chapter 6, together with some proposed directions for further investigations that can be done with the work presented in this thesis.

2 Theoretical Discussion

2.1 Germanium

Despite its early prominence at the birth of the electronics revolution, Ge could not overcome the dominance of Si as the primary semiconductor material. However, developments over the last few years have prompted Ge to be the most promising material to replace Si in complementary metal oxide semiconductor (CMOS) circuit. Ge possesses electron and hole bulk mobilities that are approximately two and four times higher than those of Si (table 2.1). It is perceived by many as a candidate that will maintain the growth of CMOS technology and associated devices well beyond the end of silicon and also take the technology into new performance territories.

Property	Silicon	Germanium
Lattice constant (Å)	5.43102	5.6579
Energy band gap (eV)	1.12	0.66
Electron bulk mobility (cm^2/Vs)	1450	3900
Hole bulk mobility (cm^2/Vs)	450	1900
Electron effective mass, m^*/m_0	$m_l^* = 0.98$ $m_t^* = 0.19$	$m_l^* = 1.164$ $m_t^* = 0.082$
Hole effective mass, m^*/m_0	$m_l^* = 0.16$ $m_t^* = 0.49$	$m_l^* = 0.044$ $m_t^* = 0.28$
Melting temperature (° C)	1400	950

Table 2.1 Basic properties of Si and Ge [13].

There have been numerous reports on p-channel Ge MOSFETs with hole mobilities much higher than those in Si [14, 15]. However, at this stage, the results for n-channel Ge MOSFETs are less promising requiring further research in this area [16]. Ge also has a lattice constant close to that of GaAs so it can also open up potential in optoelectronic applications, its good sensitivity in the infra-red spectrum enables highly efficient integratable detectors and is electro-optic properties can be essential for optical modulations.

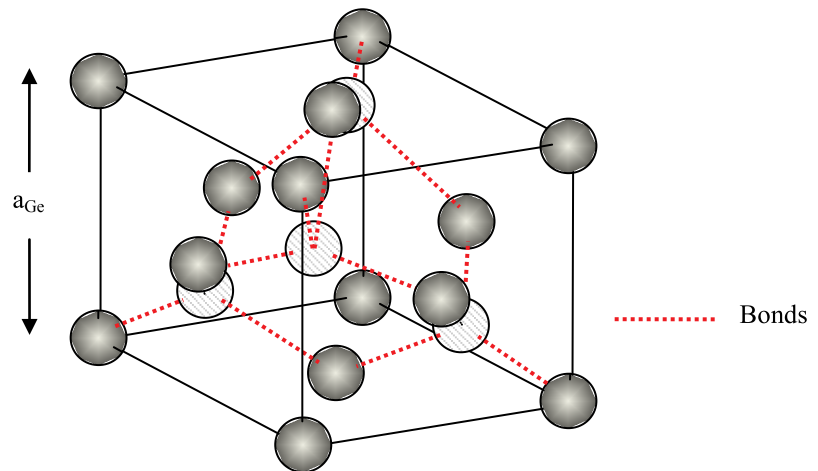


Figure 2-1A schematic of the face centred diamond cubic crystal system of Ge. White face centred unit cell interpenetrates the grey face centred cubic unit cell.

Both Ge and Si are group IV materials and have similar crystalline diamond lattice structures in which each atom is covalently bonded to four neighbouring atoms in a tetrahedral arrangement (figure 2.1). Bulk silicon and germanium have lattice parameters of 5.431 Å and 5.658 Å respectively (table 2.1) so there is a 4.2% lattice mismatch between the two. Ge can form a random $Si_{1-x}Ge_x$ alloy with Si over the full composition range. The relaxed lattice parameters of the binary alloy $Si_{1-x}Ge_x$ are not described by Vegard's Rule (linear interpolation) [17]. It is well known that the

interpolation between the lattice constants of silicon, a_{Si}, and germanium, a_{Ge}, and can be more suitably formulated by the parabolic law for any alloy composition [18]:

$$a_{Si_{1-x}Ge_x} = a_{Si}(1-x) + a_{Ge}x + x(1-x)\theta_{SiGe} \quad (2.1)$$

where θ_{SiGe} is the bowing parameter that quantifies the deviation from linear behaviour.

Kasper et al. have also shown that the actual lattice parameter of the $Si_{1-x}Ge_x$ alloy differs slightly from the original Vegard's law by a small correction factor. The difference in melting temperature between Ge and Si (table 2.1) along with the lower dopant activation energies in Ge would allow the thermal budget for device processing to be substantially reduced.

2.2 Epitaxial growth

2.2.1 Basics of epitaxy

Epitaxy is the term that describes layer-by-layer deposition of material so that it extends the crystalline substrate in a planar manner. Deposition occurs when there are molecular exchanges between a source and the substrate surface. When mobile atoms/molecules are deposited on the surface, they are called *adatoms*. These atoms are free to move on the surface until they are bonded /incorporated into the crystal structure of the substrate. Epitaxial growth proceeds by the planar incorporation of adatoms on the surface of the substrate. The movement or mobility of an adatom is

characterised by its migration length, λ, which is the average distance an adatom moves before being fully incorporated. This migration length is dependent on many factors during growth. The most important factors are the chemical species of the source and the temperature of the substrate. An example of this is the difference in chemical bond strength between Ge and Si which makes the migration length of Ge greater than that of Si. The migration length also depends on the energy barriers between the adjacent surface incorporation sites. Therefore, a rise in substrate temperature significantly increases the kinetic energy of the adatom making it easier to overcome these energy barriers and increase the migration length as well. Crystallographic orientations also affect the migration length as closer packed crystal planes have a lower energy barrier and hence a lower λ. The common crystallographic planes have increasing migration lengths in the order (100) < (110) < (111) [19] (more on alternative crystallographic orientations in section 2.4).

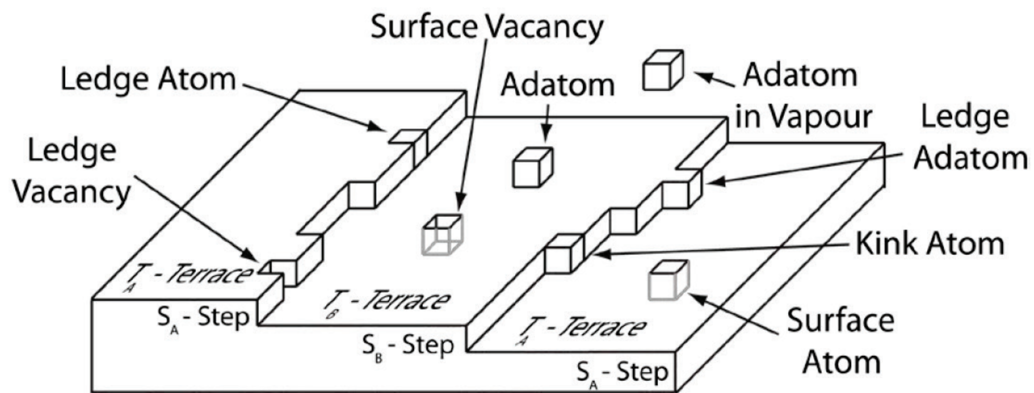


Figure 2-2 Diagram of typical adatom sites on vicinal Si substrate. [Taken from Hudson] [20].

The surface of Si substrates are vicinal, meaning that they are not completely flat but consists of many terraces separated by atomic steps as shown in figure 2.2. Layer-by-layer growth occurs by extension of the terraces if the adatom migration length is

greater than the terrace width [20]. A dimer is the temporary rebonding of two surface dangling bonds. A single step having an upper terrace with dimerisation parallel to its edge is referred to as type A, S_A, with the terrace above it labelled T_A. A single step with upper terrace of dimerisation perpendicular to its edge as a type B step, S_B, terrace T_B. If the potential well associated with the surface step is deeper than a surface site away from a step then when an adatom loses enough kinetic energy it incorporates into the surface step and is termed a ledge atom (figure 2.2). The sites for adatom incorporation are (from most preferential to least): bulk vacancy, surface vacancy, ledge vacancy, kink vacancy and step vacancy.

2.2.2 Growth modes

Homoepitaxy is defined as the epitaxial growth of a layer which is the same species or composition with the underlying substrate. *Heteroepitaxy* occurs when the layer is either a different species or alloy content. There are three basic growth modes by which heteroepitaxial growth can adopt: *Frank-van der Merwe*, *Volmer-Weber* and *Stranski-Krastanov*. The balance of the free energy between the surfaces and interface involved determines the mode of growth [21]:

$$\gamma_{LS} + \sigma_L < \sigma_S \qquad (2.2)$$

where γ_{LS} is the sum of the interface energy between the layer and the substrate, σ_L is the epilayer surface energy, σ_S is the substrate surface energy.

For homoepitaxial growth, there is no lattice mismatch between the substrate and epilayer so $\gamma_{LS} = 0$ and $\sigma_L = \sigma_S$. When equation (2.2) is satisfied then the two dimensional Frank-van der Merwe growth method will proceed [22]. In the other case, a heteroepitaxial layer can undergo formation of isolated three dimensional islands in Volmer-Weber growth [23] when the strain in the layer causes equation (2.2) to be untrue from the start (ie. $\gamma_{LS} + \sigma_L > \sigma_S$). However, at the beginning of deposition, when a layer is under strain but equation (2.7) is still satisfied then the layer will initially proceed with 2D growth but then will switch to 3D growth as γ_{LS} increases the strain energy is sufficient to negate the situation, this process is called a Stranski-Krastanov growth mode [24]. Figure 2.3 presents the schematics of the growth modes.

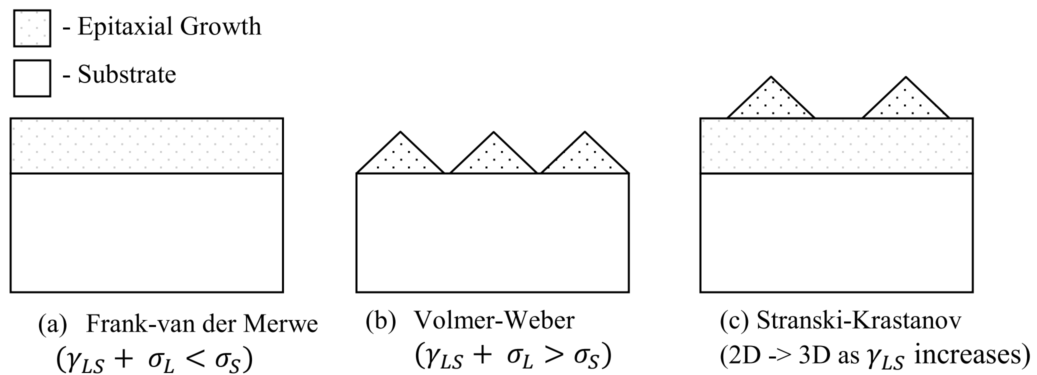


Figure 2-3 Schematic representation of the basic growth modes: (a) Frank-van der Merwe, (b) Volmer-Weber, (c) Stranski-Krastanov. [Adapted from Nash] [25].

2.3 Strain relaxation and dislocations

2.3.1 Introduction:

The mismatch and the miscible SiGe alloy can be utilised to fabricate strained layers to improve device performance. A layer can either be in compressive or tensile strain where an in-plane compression of the strained layer will be accompanied by an extension of the lattice in the growth direction and vice versa (figure 2.4).

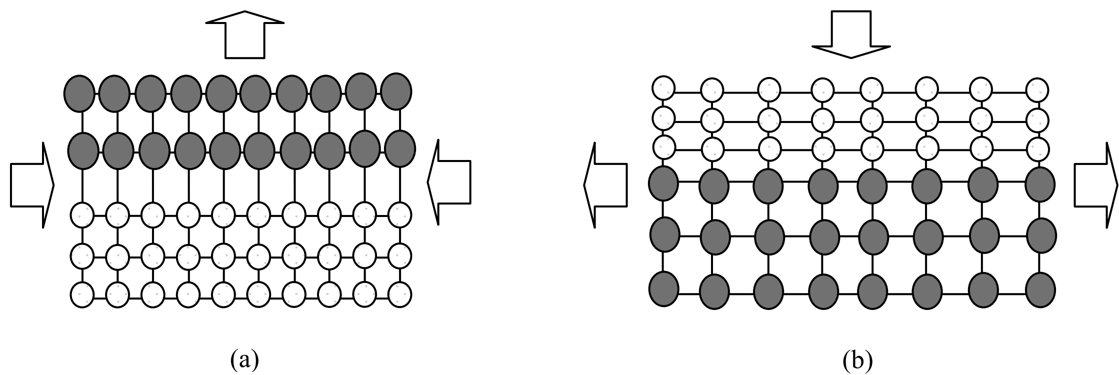


Figure 2-4 Schematic of layers under strain (a) compressive and (b) tensile. Layer with larger lattice constant is shown in black and the smaller lattice constant layer is in white.

The strain, ε, with respect to the underlying substrate can be expressed in terms of the in-plane lattice constants of the layer, a_{layer}, the unstrained lattice parameters of the layer, $a_{layer\,(bulk)}$ and the substrate, $a_{substrate}$:

$$\varepsilon = \frac{a_{layer} - a_{layer(bulk)}}{a_{substrate}} \quad (2.3)$$

When ε is positive, the layer is under tensile strain, while when ε is negative, the layer is under compressive strain. If a layer is biaxially strained, the out-of-plane

lattice constant, a_z, will compensate for any distortion in the in-plane lattice parameter, a_x or a_y, leading to the tetragonal distortion of the cubic lattice seen in figure 2.4.

The growth of a strained layer has an associated elastic energy, E_h, stored at the misfit interface between the two layers, given by the expression [26]:

$$E_h \approx 2G\left(\frac{1+\nu}{1-\nu}\right)h\varepsilon^2 \qquad (2.4)$$

where ε is the strain in the layer (equation 2.2), h is the thickness of the layer, G is the bulk shear modulus and ν is Poisson's ratio. This energy stored gets bigger as more material is deposited under strain until it reaches a critical thickness, h^* (see section 2.3.6). As the layer reaches critical thickness it will relax towards its bulk lattice constant. This relaxation of the strained layer will give rise to deformations in the crystal lattice which displaces material and form discontinuities at the misfit interface and in the lattice structure. Such discontinuities are called *dislocations* (see section 2.3.3). The relaxation process of mismatched fcc materials can occur through two main mechanisms: *surface roughening* and *dislocation dynamics*.

2.3.2 Strain relaxation via island formation and surface roughening

It has been found experimentally that partial elastic relaxation of an island permits a reduction in elastic free energy outweighing the increase in surface energy, due to the increased surface area, even though the strain energy at intervening cusps is locally higher [27]. A migration of germanium atoms occurs toward the tops of islands where the local lattice parameter is greater. When the built-up strain can no longer be accommodated solely by elastic relaxation, plastic deformation inevitably occurs with dislocation formation preferentially occurring at the highly strained cusps. The large misfit between Ge and Si can give rise to epitaxial layer relaxation via surface roughening or islanding. Uniform strained layers are unstable against modulation of the surface profile [28, 29]. Studies made by Tersoff et al. showed that strain-induced surface roughening is the dominant mechanism for the introduction of dislocations in strained layers at high misfit [30]. Roughened surface or island nucleation can lead to large local stresses where the barrier to nucleation of dislocations is extremely small [31]. By enhancing or suppressing the strain-induced surface roughening using either temperature, surfactants or compositional grading one can completely change the surface morphology and mode of relaxation of epitaxial layers.

2.3.3 Basics of dislocations

2.3.3.1 Crystal defects

All real crystals contain discontinuities within the lattice structure which disturbs the local regular arrangement of the atoms. All of the crystal defects can be classified dimensionally as:

- Zero-dimensional or *point defects*. In a pure crystal there are two types of point defects, namely a vacancy in which an atom is missing at a lattice site or an interstitial where an atom resides between lattice points. These are intrinsic point defects (intrinsic meaning the same material). Impurity atoms in a crystal can be considered as extrinsic defects: substitutional atoms that displace the original atoms at their lattice site; and interstitial, impurity atoms at non-lattice point sites.
- 1-dimensional line defects or *dislocations*. There defects are normally known as dislocations and are lines within the crystal that separates planes of atoms that have slipped over each other resulting in plastic deformation of the crystal. Dislocations are terminated planes of atoms in a crystal [32]. Their presence is very important in the physics of strain relaxation in semiconductor epitaxy and will be discussed in detail in the following sections.
- 2-dimensional or *planar defects*. These planar defects can be *stacking faults* (discussed in section 2.3.6), *twins* or *microtwins* where the periodic ordering of planes in the crystal has been disrupted.

- 3-dimensional or *volume defects*. These are large volume regions of missing atoms in the crystal where the regular crystallinity is broken such as *precipitates*, *voids* and *bubbles*.

The presence of defects can significantly modify the properties of crystalline materials, sometimes preferable. However in this work, only dislocations and stacking faults are discussed in detail.

2.3.3.2 Dislocations and Burgers vector

A *pseudomophic* epitaxial layer is a layer that has the exact same structure with the underlying substrate. When a pseudomophic layer increases in thickness, the strain energy stored within it increases (equation 2.4). If this energy is large enough for it to break the atomic bonds at the interface between the layer and the substrate, it deforms the crystal causing the layer to relax towards its bulk lattice constant. This deformation displaces material along the interface which creates line discontinuities called *misfit dislocations* gliding along the interface.

A dislocation is characterised by its line direction and its *Burgers vector*. The Burgers vector of a dislocation describes the magnitude and direction of the distortion of crystal lattice caused by the deformation. Burgers vector analysis can be used to characterise a dislocation, its motion and interactions with other dislocations [33]. The Burgers vector of a dislocation is calculated by performing a Burgers circuit around the dislocation. A Burgers circuit can be determined by drawing a clockwise atom-to-atom path in a crystal containing a dislocation which forms a

closed loop around that dislocation. Then after the same circuit is drawn in the perfect reference crystal (see figure 2.4) the vector required to close this latter circuit from finish (F) to start (S) is defined as the Burgers vector $\underline{b}$. This convention used for $\underline{b}$ is called the FS/RH convention [34]. This convention also defines the positive line sense or direction of a dislocation. Dislocations that have the same line direction but opposite Burgers vectors (or opposite line directions but same Burgers vector) are said to be physical opposites. Dislocations which are physical opposites of each other can annihilate and restore the perfect crystal if brought together (see section 2.3.5).

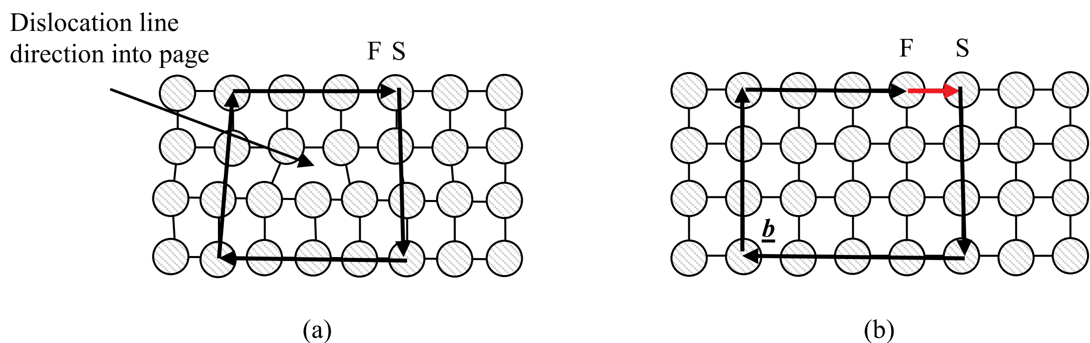


Figure 2-5 Schematic showing FS/RH Burgers circuit drawn around (a) a real crystal containing a dislocation, (b) a perfect reference crystal.

There are two primary types of dislocations called edge and screw dislocations. When the Burgers vector is perpendicular to the line direction of the dislocation (figure 2.5) it is called an edge dislocation. When the Burgers vector is parallel to the line direction of the dislocation it is called a screw dislocation. In general cases the dislocation line lies at an arbitrary angle to its Burgers vector having both the edge and screw characters and these are termed mixed dislocations. The Burgers vectors defined in the simple cubic crystal in figure 2.5 are the shortest lattice translation

vectors which join two points / atoms in the lattice. A dislocation whose Burgers vector is a lattice translation vector is known as a *perfect dislocation*.

A dislocation is a termination or boundary of a crystal lattice where material is displaced relative to each other. Therefore, a dislocation cannot terminate freely within the lattice sites meaning that they must annihilate with each other, form closed loops or terminate at a free surface. The dislocation that is formed at the interface between two mismatched heteroepitaxial layers is termed a misfit dislocation. A misfit dislocation normally consists of two components: interface containing misfit segment and its threading arm (threading dislocation). The misfit dislocations act to relieve the strain in the layer by the deformation of the crystal lattice they induce. However, only the component on the growth plane and orthogonal to the line direction of the dislocation would contribute to any effective relaxation. This component is called an effective Burgers vector, $\underline{b}_{eff}$.

$$\underline{b}_{eff} = \underline{b} \cos \beta \qquad (2.5)$$

where $\underline{b}$ is the Burgers vector of the dislocation and β is the angle between the Burgers vector and the perpendicular line to the direction of the dislocation lying on the growth plane.

2.3.4 Dislocation motion

In order to carry on the relaxation process, dislocations have to propagate within the crystals. Misfit dislocations can increase in length though a process called *glide*. Glide occurs through the sliding of planes of atoms, which allows the threading

component to propagate through the crystal, lengthening the misfit dislocation at the interface, allowing the layer to relax. The glide of a dislocation usually occurs on the plane with the highest density and in the direction of the closest packed atoms as it would have the lowest energy barrier for motion, the *Peierls energy barrier* [35]. The Peierls stress is the applied stress required to overcome the lattice resistance to the movement of a dislocation in an otherwise perfect lattice. For the Si-Ge system (or any diamond like structure), the highest density atomic planes are the {111} planes and the closest packed atoms are along the <101> directions. Thus, misfit dislocations will form along the <110> directions where the {111} glide planes intersect with the growth plane (see figure 2.6). The orientations of the glide planes are of course different for different growth orientations, these will be described in more details in section 2.4.

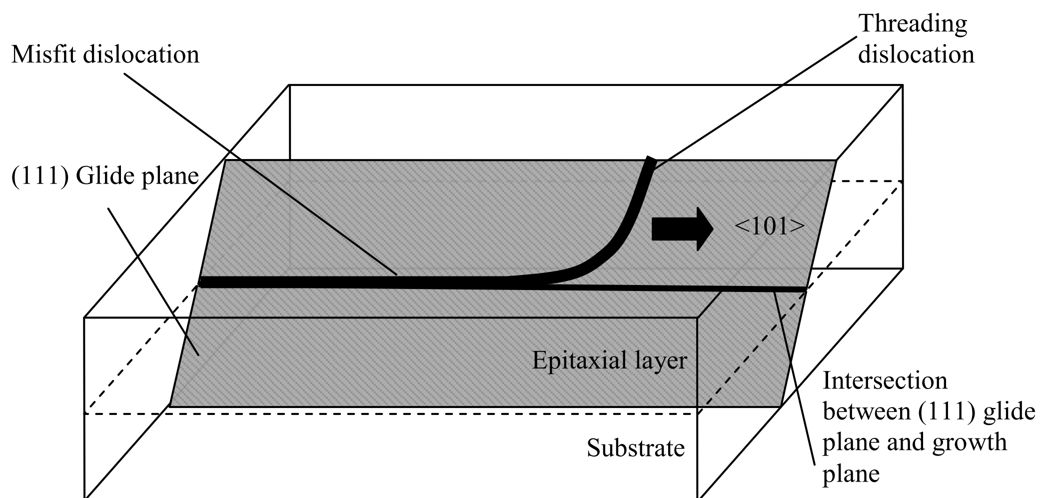


Figure 2-6 Gliding for the threading arm of a misfit dislocation on the (111) glide plane along the <101> directions.

The strain energy relieved, E_r, by a misfit dislocation of length, l, at an epitaxial layer depth below a free surface, d, is given by [34]:

$$E_r = 2G\varepsilon \frac{(1+\upsilon)}{(1-\upsilon)} \underline{b}_{eff} ld \qquad (2.6)$$

The most common type of dislocations in Ge has a Burgers vector given by $\underline{b} = \frac{a}{2}$ <110> which is the shortest lattice translation vector. This is classified as a mixed dislocation and can only glide on one plane. Due to the elastic strain energy in the layer it is favourable to have a smaller Burgers vector of this form. Such Burgers vectors form an angle of 60° with the dislocation line direction, commonly referred to as a *60° perfect dislocation*.

Another type of dislocation can form with a Burgers vector at 90° to the dislocation line, edge dislocation. This type of dislocation principally can relieve more strain than the 60° dislocation due to its Burgers vector being the same as the effective Burgers vector. However, it is unable to glide along the preferred {111} planes so the extension of the misfit to relieve strain can only occur through a much higher energy process known as *climb*. This is the reason why 60° dislocations are the dominant type of dislocations in germanium even though they are less efficient at relieving strain. Thus, for the sake of the work done in this thesis, only gliding motion of dislocations is discussed, readers are recommended to read references [33, 34] for more understanding on the climb process of dislocations.

The glide of a dislocation is normally thermally activated and is related to the mismatch strain. The glide velocity of a given dislocation is expressed as [36]:

$$\upsilon_g = B\varepsilon \exp\left(-E_g/kT\right) \qquad (2.7)$$

where υ_g is glide velocity, B is an arbitrary constant, ε is the mismatch strain, E_g is the activation barrier for glide, k is Boltzmann's constant, T is temperature in Kelvin.

Dislocations can continue to glide until:

(a) sufficient strain has been relieved in the layer or

(b) the misfit dislocation reaches the edge of the wafer where it will terminate directly or

(c) an orthogonal misfit dislocation blocks its path rendering it pinned (trapped) or

(d) two threading dislocations that are physical opposites meet and mutually annihilate each other forming a continuous misfit dislocation.

It is preferential for threading dislocations to mutually annihilate or misfit dislocations to reach the edge of wafers so that the surface will be free of defects. It has been shown there is a clear link between the number of threading dislocations reaching the surface of a sample and leakage current, leading to degraded performance of electronic devices [37]. When numerous dislocations become pinned, the pile up could lead to increased surface undulation [38] which again is detrimental to device performance.

2.3.5 Dislocation nucleation and interaction

2.3.5.1 Dislocation nucleation

In order for a layer to reach a desired level of relaxation, a sufficiently high number of dislocations within the material is needed. Typical (100) Si substrates are very high quality with a very low *threading dislocation density* (TDD) ~ 10^2 cm^{-2} whereas a TDD ~ 10^7-10^{11} cm^{-2} has been suggested to be needed to relax a high composition (x > 0.7) strained $Si_{1-x}Ge_x$.layer. If there are not enough threading dislocations to start with in the strained layer, full relaxation through gliding can only be achieved if more dislocations are nucleated. There are three mechanisms by which dislocations can be nucleated depending on the growth conditions and the material properties: homogeneous nucleation, heterogeneous nucleation and dislocation multiplication [39].

Homogeneous nucleation is the spontaneous nucleation of a dislocation half loop from a point source at the surface of the wafer due to the residual strain in the layer when other types of relaxations are not sufficient to relax the layer. The activation energy for this mechanism has been calculated to be around ~40eV [40]. Due to the high level of energy required, this type of nucleation is only likely to occur under conditions of high strain f ~ 0.02 or high growth temperature.

Heterogeneous nucleation only occurs for low quality layers with a high density of defects such as voids, precipitates [41] and point defects. These types of defects can act as free surfaces to nucleate further dislocations in the layer. Another source of

heterogeneous nucleation of dislocation has been suggested to be excessive surface roughness incurred during growth [42].

The *multiplication* mechanism is the process by which some dislocations initially present in the layer act to rapidly increase the number of dislocations and so quickly relax the layer. The rate of multiplication depends entirely on the amount of dislocations ready-formed by other means whilst numerous multiplication mechanism have been summarised by Vdovin [43], only the modified Frank-Read (MFR) mechanism proposed by LeGoues [44] is discussed in this thesis (see section 2.3.6) as it is deemed the most widely accepted multiplication process.

2.3.5.2 Dislocation interaction

A misfit dislocation induces local distortion of the atomic bonds along its length creating a strain field around it [45]. Although the degree of the stress is quite large it is localised so the misfit dislocation still contributes to the total relaxation of the strained layer. Dislocations are free to glide in a perfect crystal but can be blocked by impurities or defects so there could be interactions between dislocations and some orthogonal misfit with its associated strain field (likelihood depending on dislocation density). The strain field can also be created from surface undulation of the strained layer and is another mechanism of layer relaxation.

The threading arms of the misfit dislocations can interact with either the strain field or with the orthogonal misfit itself. It needs a higher degree of driving strain to overcome the strain energy barrier of the distorted arrangement of the atoms. A

model has been proposed by Freund [46] to describe the process of pinning (see figure 2.6). It is assumed that the strain field creates a retarding force on the dislocation. The interactive retarding force G_I is described as [46]:

$$G_I = -\int_{B_g} \sigma_{ij}^I n_j \underline{b}_i dx_3' \qquad (2.8)$$

where σ_{ij}^I is the additional contribution to the applied stress field due to dislocation interaction, n_j is the number of intersected orthogonal dislocations, $\underline{b}_i$ is the Burgers vector of the intersecting dislocation, and B_g is the boundary defined by the intersecting dislocation threading arm, integrated in a direction orthogonal to the intersecting misfit within the glide plane.

If the strain energy in the lattice is too low for the gliding dislocations to overcome the barrier, the strain field will act to pin the dislocations in a blocking regime [47]. This will create a pile-up site of threading dislocations at the strain field [30]. In general, for layers with greater excess stress the outcome of this type of interaction is dependent on the relationship between the dislocation Burgers vectors, the depth at which the encounter occurs, the material composition of the layer and the unrelieved misfit strain present. The retardation force is at its maximum when the Burgers vectors between two dislocations are perpendicular to each other. In this case, the strain field will force the dislocation to propagate in a thinner channel region (see figure 2.7) with thickness h^*. The threading segment will now glide at a slower speed due to the reduced driving force in the thinner region. When the Burgers vectors are parallel, the retardation force should be at a minimum and a threading dislocation can

cause an orthogonal misfit to split forming into two separate dislocations each with a 90º bend [47].

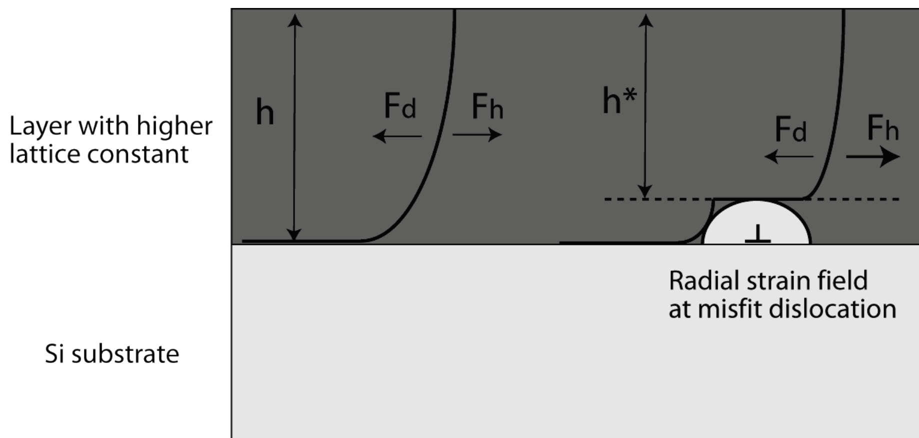


Figure 2-7 Interaction between a gliding threading dislocation and the strain field of an orthogonal misfit dislocation. The threading segment can either become pinned or continue gliding in a thinner channel with thickness h*. (Adapted from Freund) [46].

When the Burgers vectors of two threading arms are anti-parallel on the same plane gliding towards each other it would cause an annihilation of the threading segments connecting the misfit dislocations together When the TDD is high (>10^{8} cm^{-2}) the probability of annihilation is high and is the main source of TDD reduction. When TDD is low (<10^{5} cm^{-2}) the main TDD reducing mechanism is glide of threading dislocations until they reach a free surface and the dislocation glides out of the system leaving behind a perfect 60° misfit dislocation [48].

2.3.6 Modified Frank Read multiplication mechanism

The interaction between two orthogonal misfit dislocations having parallel Burgers vectors can undergo a splitting reaction forming two corner dislocations. The

intersection of such type becomes the source for a multiplication mechanism widely known as the modified Frank Read (MFR) mechanism [44].

The original Frank Read mechanism described the process in which pinned dislocations can unpin themselves by bowing into the substrate and forming a loop around the orthogonal dislocation pinning it under the influence of shear stress. This would eventually close upon itself to form a complete dislocation loop and would reform the initial dislocation as well as creating another loop. More dislocation loops can be formed in this way as long as sufficient stress in the layer remains.

In the MFR mechanism, the process involves two split corner dislocations that are mutually repulsive. This repulsion will force the corner dislocations to bow into the substrate in a manner similar to that of the original Frank Read mechanism, figure 2.8(a). However, in this case, the two orthogonal dislocations bow on separate glide planes locked together by a line through the intersection. This bowing will form half loops around both dislocations, figure 2.8(b, c), and further extension of these loops will continue until the two segments unite to form a common closed loop connecting the two glide planes and another pair of intersecting misfit dislocations, figure 2.8(d, e). This loop continues to grow in size until the top of the loop reaches the surface of the sample, thus forming two threading dislocations that will glide away to create two new misfit dislocations on the same glide planes as the original misfits, but which are spatially separated in the layer, figure 2.8(f, g). On the other hand, the new pair of intersecting misfit dislocations will undergo the same process to produce more dislocations provided that sufficient misfit stress remains, figure 2.8(h). The resulting dislocation network is schematically shown in figure 2.8(i).

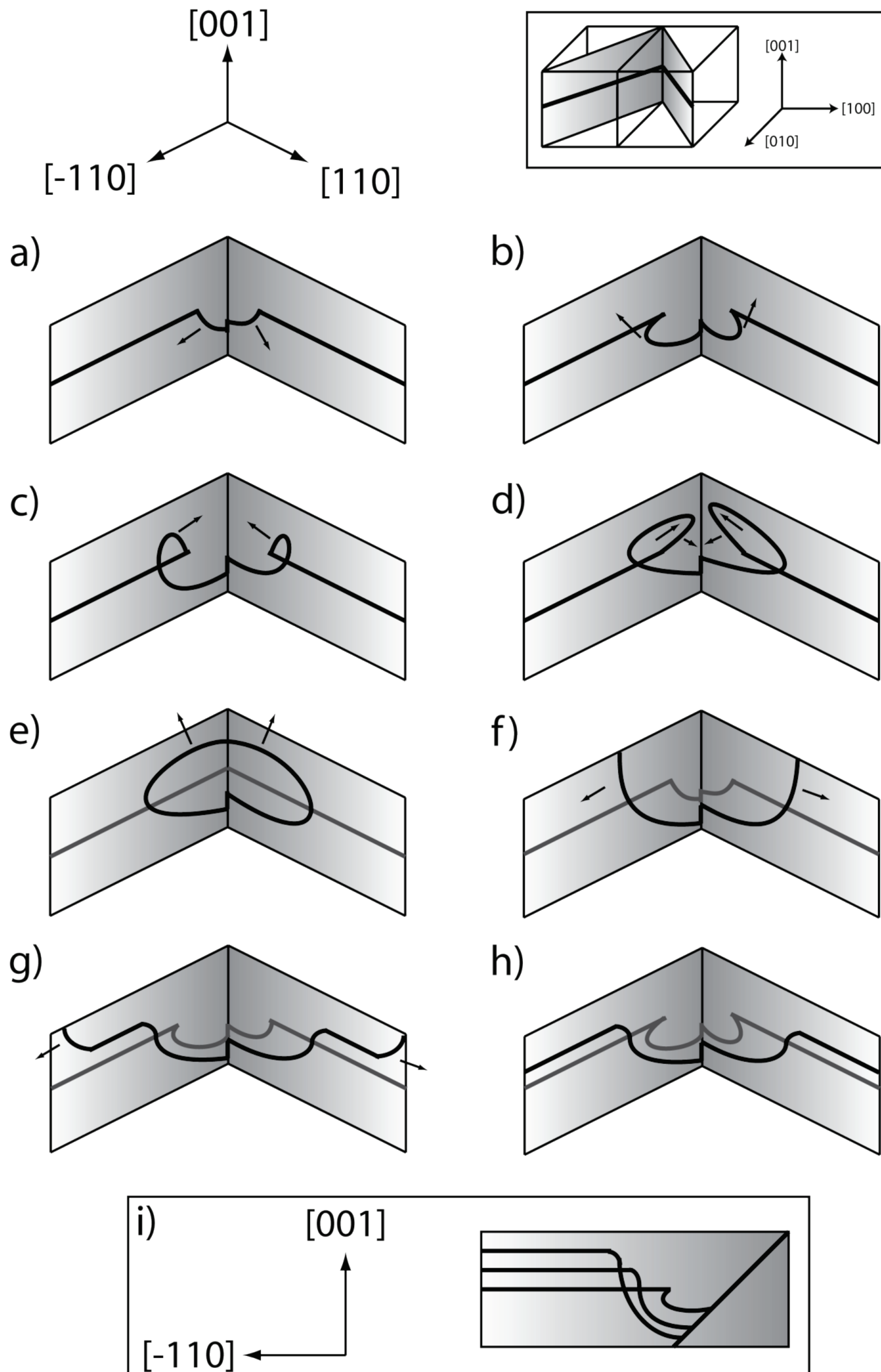


Figure 2-8 Schematic of the modified Frank Read dislocation multiplication mechanism. (Taken from Shah) [49]

This multiplication mechanism can allow for rapid relaxation of the layers as numerous dislocations can be formed for very low activation energy of ~4eV, much less than homogeneous nucleation. This increases the threading dislocation density exponentially around the intersection site, but because they all lie on the same plane, it tends to lead to annihilation of threading defects reducing TDD. The presence of these dislocation networks, however, can lead to surface roughening as a result of the pile up of misfit dislocations if the stress is not big enough. Many mobile threading dislocations will become trapped at the same misfit pile-up resulting in threading dislocation pile-up. Fitzgerald et al. [50] showed that the surface undulation resulting from misfit pile-ups is itself responsible for dislocation pinning by reducing the thickness of overlying material to less than the critical thickness required to drive dislocation motion. Thus, the process of MFR requires that the intersecting misfits dislocation are pinned at a long enough distance apart to allow sufficient stress to bow the dislocations creating threading segments and new dislocations rather than becoming a pile up site.

2.3.7 Critical thickness

As growth of an epitaxial layer proceeds, the strain energy increases in proportion to the thickness of the layer (see equation 2.4). This increase in energy will eventually reach a critical level where the layer will start to relax. The corresponding thickness of the layer at this stage is called a critical thickness, h_c, The strain energy (see equation 2.4) will be relieved when misfit dislocations form to initiate relaxation. Numerous mathematical models have been formulated to describe this process but

only the two most popular theories are discussed in this section, the Matthews-Blakeslee model and the People-Bean model.

2.3.7.1 Matthews and Blakeslee Mechanical Equilibrium Theory

The Matthews-Blakeslee model [51] considers the force acting on a *pre-existing* threading dislocation from the substrate. An imbalance of the force equilibrium on the threading dislocation will cause it to start gliding at the mismatch interface, creating misfit dislocations (see figure 2.9).

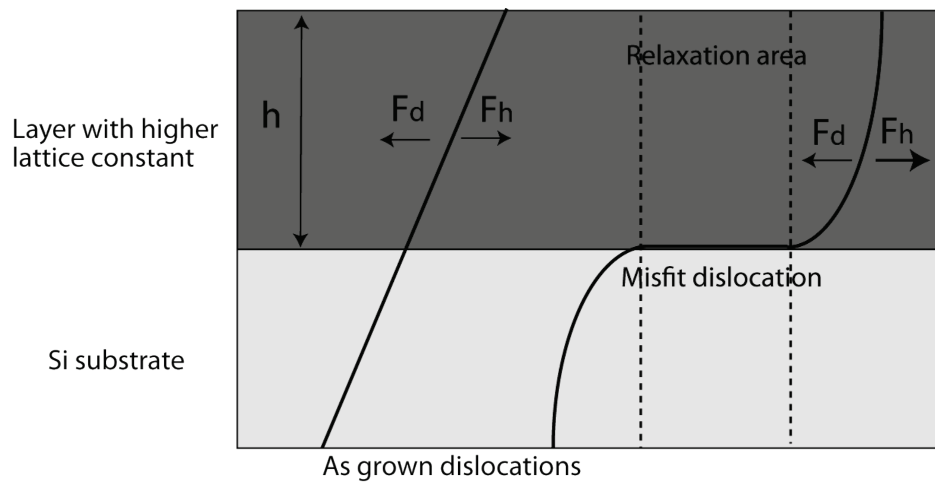


Figure 2-9 A critical thickness model proposed by Matthews and Blakeslee considering the mechanical equilibrium of pre-existing threading dislocations. (Adapted from People and Bean)[26].

Sufficient strain at the misfit interface will exert a driving force, F_h, on the threading dislocation which will increase with thickness (derived from equation 2.4) [26]:

$$F_h \approx G\left(\frac{1+\nu}{1-\nu}\right)bh\varepsilon \qquad (2.9)$$

where b is the magnitude of the Burgers vector. There is also a tension force acting on the threading dislocation where it represents the force, F_d, required to overcome the Peierls energy barrier and displace material forming misfits. This force is given by [26]:

$$F_d \approx \frac{Gb^2(1-\nu cos^2\theta)}{4\pi(1-\nu)} \ln\left(\frac{h}{b}\right) \qquad (2.10)$$

where θ is the angle between the Burgers vector and the dislocation line. Misfit dislocation will start to form when the driving force exceeds the tension force on the pre-existing threading dislocation. The critical thickness is the thickness at which F_h is equal to F_d. Equating (2.9) and (2.10) would give the thickness as:

$$h^* \approx \frac{b(1-\nu cos^2\theta)}{4\pi(1+\nu)\varepsilon} \ln\left(\frac{h^*}{b}\right) \qquad (2.11)$$

However, because this model relies on and is valid when relation is via the pre-existence of threading dislocations, when Si substrates become much better in quality the result is a deviation from critical thickness predicted by Matthews and Blakeslee.

2.3.7.2 People and Bean Energy Balance Theory

People and Bean reviewed the work by Matthews and Blakeslee and came up with an improved description of critical thickness [26, 52] . In this theory, the critical thickness is the thickness at which the areal activation energy is big enough to initiate dislocation nucleation in an initially dislocation free layer. Dislocation

nucleation requires a higher activation energy compared to gliding so the People-Bean critical thickness is somewhat higher than those predicted by Matthews and Blakeslee. It is considered that the dislocations must be nucleated from a free surface, where they would terminate assuming there are no impurities within a layer. Homogeneous nucleation of a dislocation half loop from a point source at the surface is proposed to be the mechanism in this model (see figure 2.10).

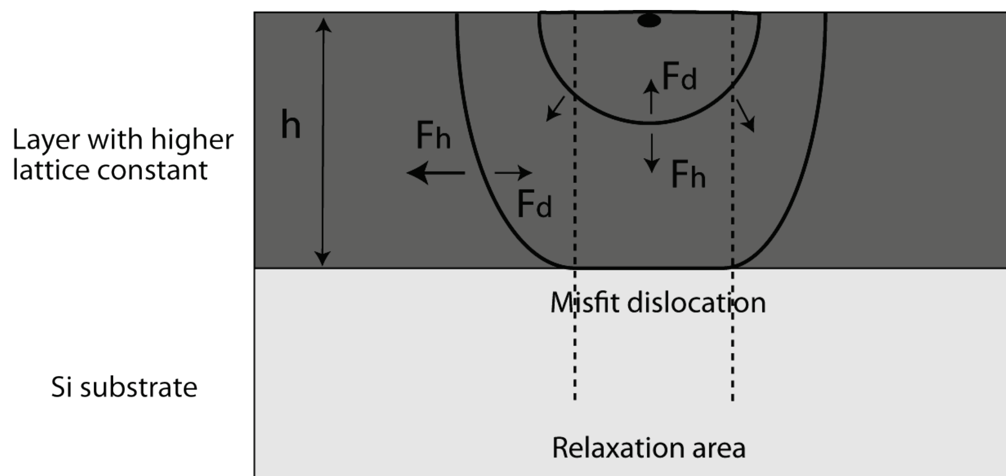


Figure 2-10 The critical thickness model proposed by People and Bean considering the energy balance for dislocation half loops. (Adapted from People and Bean) [26].

When the thickness of a layer increases, the strain energy increases to nucleate dislocation half loops expanding on the {111} glide planes until they reach the misfit interface. At this point, the loop will form threading segments that will be subjected to driving and tension forces. If the strain energy is sufficient the threading dislocation arms will glide apart, lengthening the misfit dislocation, relaxing the layer. The areal energy density required to form a single dislocation half loop is given by [26]:

$$E_d \approx \left(\frac{Gb^2}{8\pi\sqrt{2}a}\right) \ln\left(\frac{h}{b}\right) \qquad (2.12)$$

where a is the lattice constant of the strain layer. The People-Bean critical thickness at which the first misfit dislocation is nucleated is given by:

$$h^* \approx \left(\frac{1-\nu}{1+\nu}\right)\left(\frac{b^2}{16\pi\sqrt{2}a\varepsilon^2}\right)\ln\left(\frac{h^*}{b}\right) \qquad (2.13)$$

The Matthews-Blakeslee and the People-Bean critical thicknesses for a Ge layer grown on a varying composition $Si_{1-x}Ge_x$ layer were calculated and plotted in figure 2.11 below. The figure shows three theoretical regions representing the states of relaxation of the Ge layer. The region below the red curve for Matthews-Blakeslee is *stable* meaning the material lacks sufficient energy for dislocations to glide and thermal treatment is not likely to encourage significant relaxation. The region above the black curve for People-Bean is *unstable* in which dislocations can nucleate and relax the layer even with low temperature growth. The region in between the two curves termed *metastable* is where the growth temperature becomes important to the relaxation of the layer, with lower temperature growth suppressing the gliding of dislocation hence there might be no relaxation.

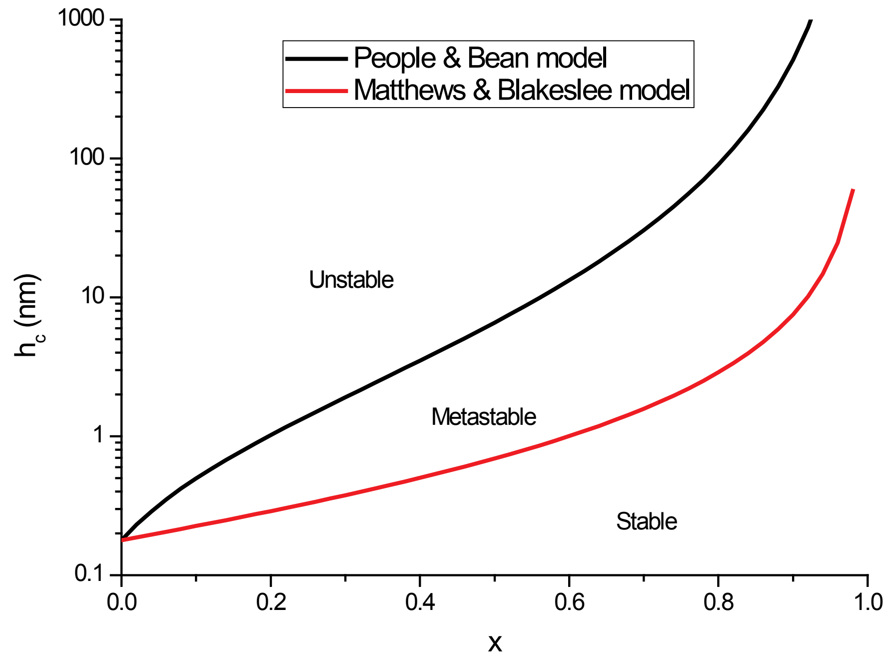


Figure 2-11 Graph showing critical thickness regimes for a strained Ge layer on a $Si_{1-x}Ge_x$ layer of Matthews-Blakeslee (red curve) and People-Bean (black curve) : *Stable* below red curve, *Unstable* above black curve, *Metastable* in between the curves.

2.3.8 Partial dislocations and stacking fault formation

The most likely Burgers vectors for dislocations in a face-centred cubic structure (ie. Si and Ge) are the shortest lattice translation vectors of the type $\frac{1}{2}$<101>. Thus for Ge, the 60° dislocations with Burgers vector type $\frac{1}{2}$<101> leave behind a perfect crystal when they glide as they displace the lattice by a whole number of lattice positions and so are termed perfect dislocations. However, it is normally more energetically favourable for a perfect dislocation to glide on the {111} planes via an intermediate path. This means that the perfect dislocation can split into two partial dislocations which would appear as single dislocations with Burgers vector shorter than $\frac{1}{2}$<101>.

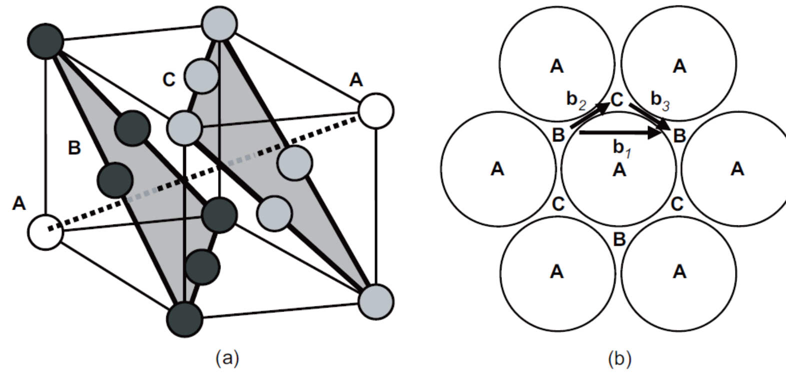


Figure 2-12 Hard sphere representations of (a) the stacking of {111} planes in face-centred cubic structure and (b) the top down view of the stacking sequence. (Taken from Cottrell) [53]

A hard sphere representation of the face-centred cubic structure is shown in figure 2.12. The {111} planes are labelled as A, B, C and are stacked on top of each other in a three-fold "ABCABC" stacking sequence along the [111] direction normal to the plane. Each atom of the lattice B must sit on each hollow site created by three A atoms, the C atoms again must in turn sit on the hollows created by three B atoms (a site that is not directly above the A atoms). Gliding of a perfect 60° dislocation must normally be of a whole number of lattice spacing, meaning from a B site to another B site along the direction of Burgers vector b_1 (see figure 2.12). However, motion along this path is not energetically favourable compared to a split in displacement via the C sites. The shorter displacements have Burgers vector $\underline{b}_2$ and $\underline{b}_3$ which are displacements by a fractional number of lattice spacing and termed Shockley *partial dislocations* [33]. The dissociation (split up) of the $\underline{b}_1$ Burgers vector is expressed as:

$$\underline{b}_1 \rightarrow \underline{b}_2 + \underline{b}_3$$

$$\frac{1}{2}[101] \rightarrow \frac{1}{6}[112] + \frac{1}{6}[2\bar{1}1] \qquad (2.14)$$

Perfect 60° dislocations dissociate into 30° and 90° Shockley partial dislocations with Burgers vector $\frac{1}{6}[112]$ and $\frac{1}{6}[2\bar{1}1]$ respectively. If a Burgers vector circuit is performed around the two partial dislocations it would yield a Burgers vector of a perfect dislocation (equation 2.13). These partial dislocations also glide on the {111} planes but the order at which they glide depends on the order at which the bonds break. This in turn depends on the type of strain configuration of the system (compressive or tensile) and also on the crystallographic orientation of the growth plane (sees section 2.4). The partials glide in particular orders as they can't glide past each other.

In order to decide on the proper sequence at which the partial dislocations glide it is necessary to consider the detailed atomic arrangement as in figure 2.12. This method is rather complex and a more convenient way to determine the gliding sequence for partial dislocations was originally proposed by Thompson [54]. The method called Thompson tetrahedral construction was used to represent the {111} glide planes and the <110> glide directions to work out the proper sequential arrangement of the partial dislocations. Readers are referred to Hirth and Lothe [34] for a more detail explanation.

When two partial dislocations are formed on the same {111} glide plane, they will create a region between them called a *stacking fault*. A stacking fault is a planar, two-dimensional dislocation where the normal stacking sequence is disrupted. The stacking sequence of {111} planes outside the partial dislocations will be

“ABCABCABC” and between the partial dislocations will be “ABCACABC” (see figure 2.13)

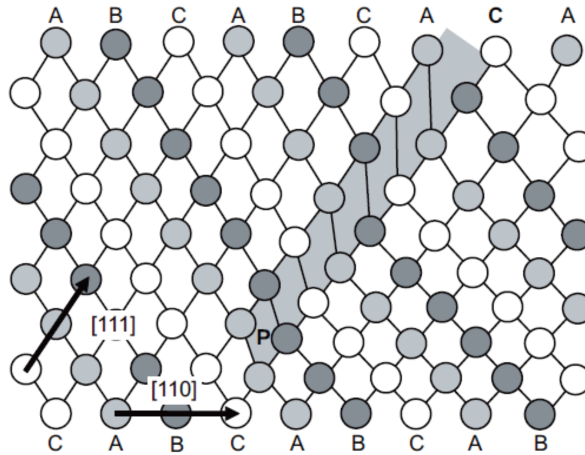


Figure 2-13 Schematic diagram of a stacking fault region (shaded area) caused by a partial dislocation at point P with line direction running into the page. (Adapted from Kosevich) [55]

The stacking fault energy provides a force that tends to pull the dislocations together. However, the partial dislocations themselves are mutually repulsive so an equilibrium separation between the partials will be established when the repulsive and attractive force balance. The approximate equilibrium separation, d, is given by [32] :

$$D = \frac{Gb^2}{4\pi F_p} \qquad (2.15)$$

where F_p is the repulsive force per unit length between the partials. In this case, the repulsive force is equated to γ, the attractive force per unit length. Due to this balance, the stacking faults equilibrium size in SiGe system has been reported to be around 0.3-0.5 nm [56].

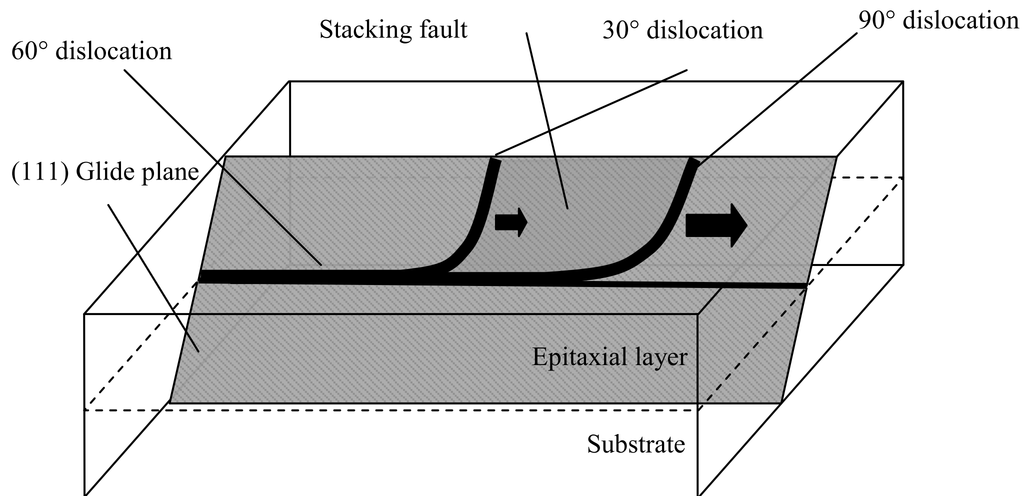


Figure 2-14 Formation of an extended stacking fault as the leading partial dislocation experiences a larger shear force and glide away from the trailing partial.

In *tensile* strained layers grown with a conventional (100) growth direction the 90° Shockley partial dislocation leads the 30° partial. However the 90° always experiences a larger shear force (due to cos θ term in equation 2.9) so it glides away from the 30° partial dislocation creating an extended stacking fault (figure 2.14). On the contrary, in *compressive* strained (100) layers the 30° Shockley partial dislocation leads but the 90° still has a larger shear force acting on it so it glides at a faster rate. However, because of the mutual repulsion between the partials the 90° dislocation is not able to pass the 30° so the stacking fault remains in its equilibrium size without extending. This is often ignored as the equilibrium size of the stacking faults is very small and thus just regarded as a 60°dislocation.

Stacking faults are not desirable in heteroepitaxial for potential device fabrication as they behave in the same way as threading dislocations, acting as leakage paths and reducing device performance.

2.4 *Alternative crystallographic orientation*

The band structure that a carrier experiences in an inversion layer depends strongly on the crystallographic orientation of the surface [57]. It has been theoretically predicted that growth of layers on (110) or (111) substrate orientations resulting in a change in band structure can lead to a higher mobility achieved by the surface channel [58]. Substrate orientation can also change the behaviour of dislocations in the growth of heteroepitaxial layers due to the differences in the resolved shear stress onto the various glide planes.

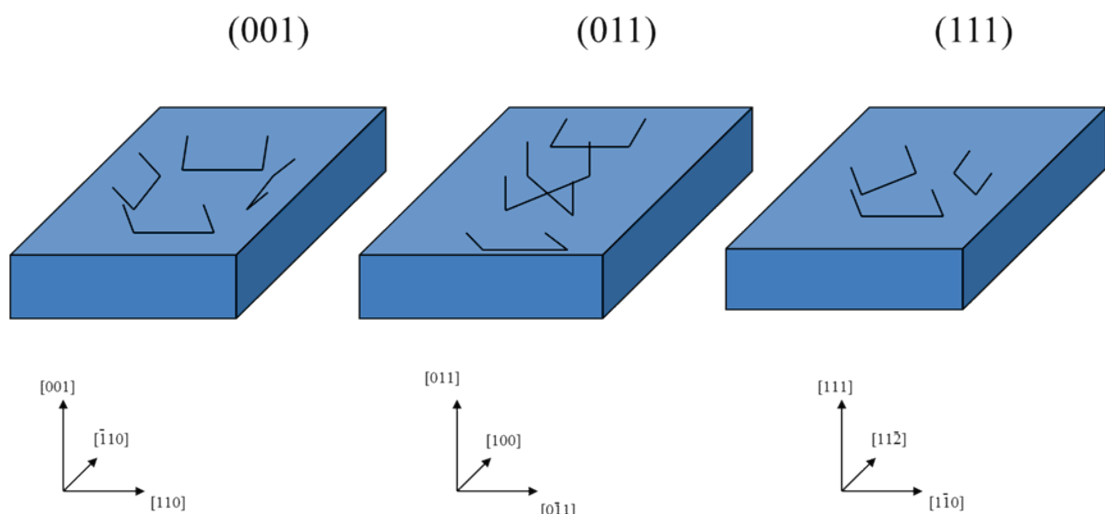


Figure 2-15 Schematic representations of the {111} glide planes associated with each substrate orientation.

Figure2.15 shows the difference in {111} glide planes of the three substrate orientations (100), (110) and (111). In the familiar case of (100) substrate orientation, the four sets of symmetrical{111} planes are inclined at an angle of 60° to the surface plane and dislocation glide on these planes all contribute to the relaxation of the layers as they are all inclined. Only dislocations which have nucleated along an

inclined plane can relieve the interfacial misfit because they have a non-zero edge component of the Burgers vectors. For (110) growth orientation, there are only two sets of {111} planes that are inclined at 30° to the growth plane, the other two {111} planes are perpendicular to the (110) plane and thus do not contribute to layer relaxation. The (111) growth plane has three other {111} glide planes that are inclined at 60° to the surface and run along the <110> directions.

Tensile strained layers grown on (110) and (111) Si substrates have the 30° partial dislocation leading so the stacking faults remain narrow. But this thesis is only concerned with compressive strained Ge overlayers.

Compressively strained layers grown on (110) and (111) Si substrates behave very differently. Whilst the 30° partial dislocation always leads in the compressively strained (100) case, the situation is reversed for the (110) and (111) system. The 90° Shockley partial always leads and it still experiences the larger shear force so it glides away from the 30° creating a stacking fault. Hence, epitaxial growth of compressive strain layers on (110) and (111) orientation is very susceptible to stacking fault formation. During growth, 3-dimensional islanding, high surface roughness and generation of a high density of defects can occur and all these are detrimental to the performance of a device. This is a big challenge to overcome to produce good quality buffer or channel layers for fabrication of high mobility devices and other potential applications.

3 Experimental Techniques

This chapter describes the experimental techniques used to carry out the research in this thesis. These techniques include chemical vapour deposition (CVD) growth and characterisation by such means as transmission electron microscopy (TEM), atomic force microscopy (AFM), selective defect etching and high resolution x-ray diffraction (HR-XRD). The TEM was used primarily to study the microstructures, to determine the thicknesses; the XRD was used to examine the strain configurations in samples and the AFM was used to study the surface morphology and to determine the surface roughness of grown materials. The operating principals of the techniques are discussed along with relevant background theories and implementations.

3.1 Chemical Vapour Deposition (CVD)

CVD growth is the process where gaseous chemicals, known as precursors, are passed through the chamber and react with the surface of the substrate wafer to form adatoms which incorporate into the crystal. CVD allows for very fast growth rate (of the order of tens of nanometres per minute) and uniform structures. It is thus regarded as the ultimate industrial tool, capable of mass-producing high-purity crystalline materials. There are many different types of CVD systems which operate at various ranges of growth temperature (100° C - 1300°C) and growth pressures (atmospheric to ultra-high vacuum) [59]. An ASM Epsilon 2000 reduced pressure CVD (RP-CVD) is used to produce all wafers investigated in this study. A schematic of a RP-CVD is shown in figure 3.1 below.

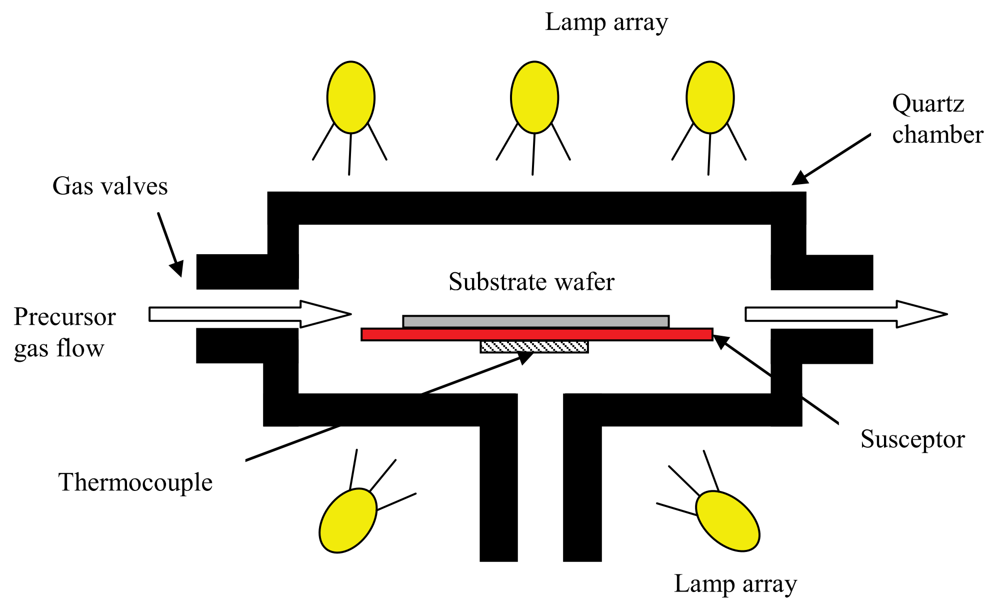


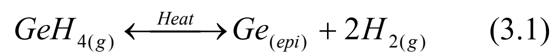
Figure 3-1 Schematic of the cross-section of a typical CVD system.

In RP-CVD, the temperature is very critical as it controls the sticking coefficients of the reactants in the precursors. The growth chamber pressure is also very important in maintaining a desired growth rate. During growth, a wafer sits in a quartz chamber which allows the wafers to be heated by an array of infra red radiation lamps (quartz is transparent to infra-red radiation). The temperature during growth is monitored by thermocouples below the wafer and will automatically adjust the output of the lamp array. Precursors and carrier gas flow rates are controlled by a set of valves that open and shut automatically according to growth recipe inputs. Chamber pressure can also be controlled accurately and consistently throughout the growth process.

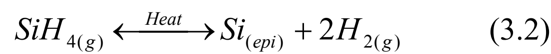
Even though high quality Si substrates are used, a thin layer of native silicon dioxide is unavoidably formed on the surface of substrate wafer almost all of the time. Thus prior to growth, Si substrates must undergo surface preparations to desorb the oxide.

When the wafer is inserted into the growth chamber it receives an *in-situ* bake at 1150°C to get rid of any surface oxide. After desorption, hydrogen carrier gas is allowed to flow into the chamber and the hydrogen passivated surface wafer will be ready for growth.

The most common types of precursors used for growth of germanium and silicon are germane (GeH_4) and silane (SiH_4) which react with the surface of the wafer to form mobile Ge and Si adatoms that can incorporate into the Si substrate crystal according to the equations:



$$GeH_{4(g)} \xleftrightarrow{Heat} Ge_{(epi)} + 2H_{2(g)} \qquad (3.1)$$



$$SiH_{4(g)} \xleftrightarrow{Heat} Si_{(epi)} + 2H_{2(g)} \qquad (3.2)$$

Gas flow rates are normally measured in standard cubic centimetres per minute (sccm) and standard litres per minute (slm). Other types of precursors that can be used are digermane (Ge_2H_6) for Ge deposition or dichlorosilane (SiH_2Cl_2) for Si deposition which would allow deposition at lower temperatures than germane and silane. These precursors are all undoped and the choice of precursors depends on the growth temperature.

Hydrogen plays an important role when used as a carrier gas for epitaxial growth by CVD. It acts as a *surfactant* to ensure a smooth layer is grown. A surfactant is a chemical that acts to reduce the surface free energy and therefore modify the atomic diffusion at surfaces and steps leading to improved 2D growth. The hydrogen gas influences the growth rate at low temperature as it limits the rate of bonding of silane

(silane can only bond with the substrate once the hydrogen has been desorbed). So low temperature growth is in the hydrogen desorption limited regime where as the high temperature growth is in gas flow limited regime. Nitrogen, on the other hand, enhances growth rate when used as a carrier gas as it is not a surfactant and does not terminates surface sites.

3.2 Transmission Electron Microscopy (TEM)

An ordinary optical microscope has a fundamental limit on the resolution that can be achieved during imaging. Its resolution is limited by the diffraction limit imposed by the wavelength of optical light. The minimum feature size resolvable by a microscope is governed by:

$$d = \frac{\lambda}{2(n\ sin\theta)} \qquad (3.3)$$

where d is the resolvable feature size, λ is the wavelength of the source, n is the refraction medium and θ is the half angle subtended by the objective lens. The term (n sinθ) is normally called a numerical aperture (NA) which modern optics can reach to about 1.4 hence the resolution limit is ~ d=λ/2. The wavelength of light ranges from 380-740 nm giving resolvable feature limits at ~200nm which is impractical considering the scale of semiconductor features of interests. For example, fabricated MOSFET channel widths and depths of grown heterostructures are of the order of 1-50nm and surface undulations as low as 1-2nm prove impossible for optical microscopy. Another drawback to the optical microscope is its small depth of field,

which is the depth of the object it can focus on at a given time. This term is inversely proportional to the square of NA which makes it impractical for optical microscopes to sufficiently focus on very small objects (order of a few nanometres).

A transmission electron microscope operates in a way similar to that of an optical microscope. A TEM forms an image using highly accelerated electrons with very short wavelength (~0.003 nm) which would improve resolution significantly allowing detail imaging at high levels of magnifications (up to x500k). A TEM can be used to perform a high resolution thickness study of crystalline material layers, strain variation across the heterostructures and also defect morphology within the grown sample. A JEOL JEM-2000FX TEM was used for this study and its basic structure is described below in section 3.2.2. A TEM can be operated in two different modes: (a) bright field imaging mode, (b) annular dark field mode.

3.2.1 Sample preparation

Specimen preparation is of great importance to this technique as transmission of electrons through a specimen necessarily requires electron transparency, in relation to the Si and Ge material system this equates to a thickness of a few hundreds of nanometres. When an electron passes through a solid it may be scattered once, several times or not at all. This depends on the thickness of the specimen as the thicker the sample is, the more likely it is for multiple scattering to occur. The sample needs to be thin enough (few hundred of nanometres) so most of the electrons can pass through (electron transparency).

There are many ways in which a TEM sample can be prepared and the exact techniques depend on individuals. Although there are many alternatives, the main steps remain broadly similar which can include gluing of samples, grinding to thin down followed by polishing the samples and finally ion milling to give electron transparency. Good preparation of TEM samples often lead to high quality images being obtained for those samples so it is very important that this step is done properly. However, TEM sample preparation is a laborious task and is very time consuming. Typical (100) samples are a lot easier to cleave and prepared compared to those for (110) and (111). Preparations can be for cross-sectional (XTEM) or plan view (PVTEM) analysis.

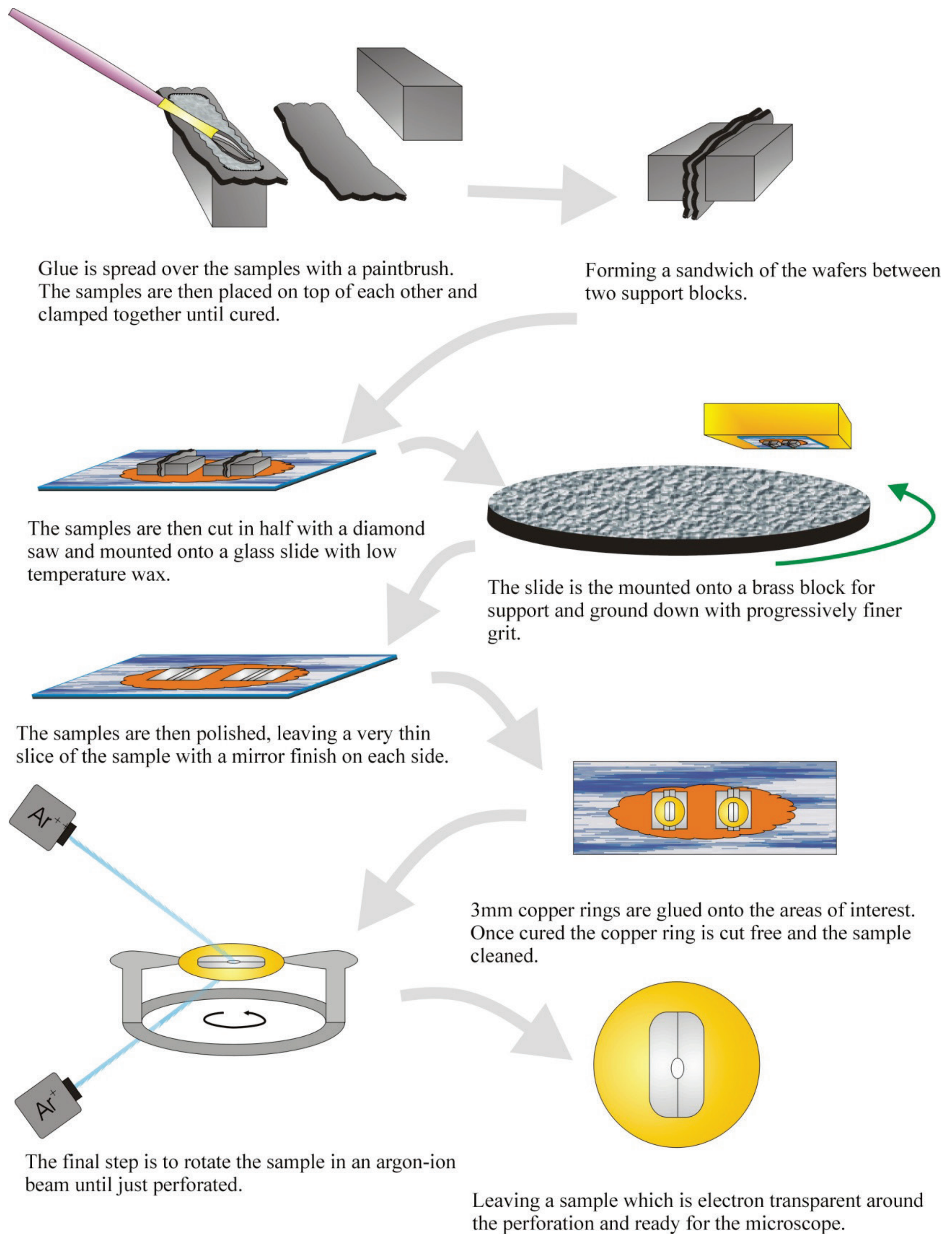


Figure 3-2 The typical process of a cross-sectional TEM sample preparation. (Taken from Capewell 2002) [60].

All the TEM images in this thesis were taken along the [110] viewing direction unless otherwise stated. Therefore the hereafter instruction for cleaving is for making samples to be viewed along the [110] direction. For a typical XTEM (100) specimen preparation, two rectangular sample pieces of approximately 2cm x 1cm are cleaved along the <110> directions using diamond scribers. For samples grown on (110) and (111) substrates, cross-sectional TEM sample preparation procedures are almost the same except for the initial cleaving stage. These non-standard orientation samples have to be cleaved/ cut in such a way that its cross-section will still be viewed along one of the <110> directions. Figure 3.3 indicates how these samples would be cut before being glued together for further preparation. For (110) and (111) samples, a diamond wire saw is needed to cut the samples in the desired directions for [110] direction cross-sectional viewing in the TEM later.

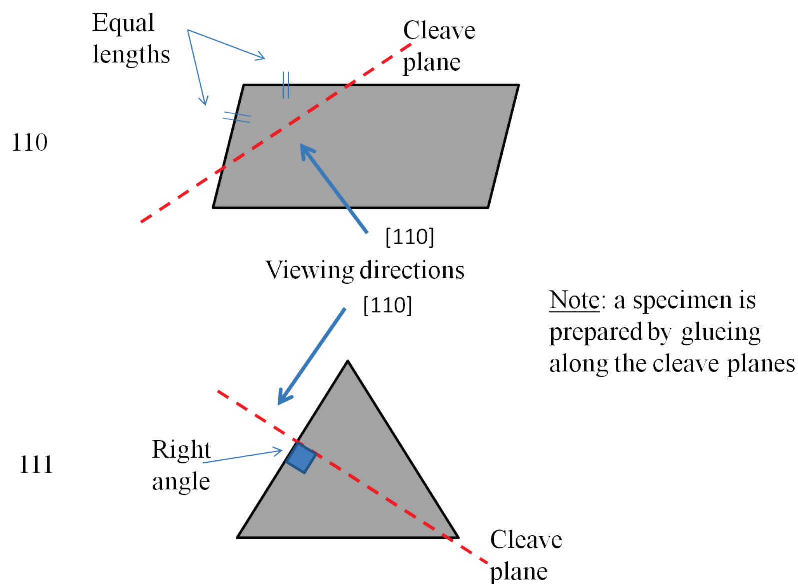


Figure 3-3 Schematic for cleaving of (110) and (111) TEM sample preparations.

The samples are then glued face to face together using Araldite adhesive and rubbed together to ensure an even distribution of the glue and make sure there are no bubbles

in between the samples. Two Si support blocks are then attached to the sides of the sample sandwich and the whole structure clamped together. It is then baked on a hot plate or in an oven at ~200°C for one hour and is allowed to cool. The specimen is then cut in half along its length using a diamond coated blade saw. This process reduces the amount of material to be ground away and produces an almost flat surface to be mounted on a glass slide using a temperature resistant wax (dissolvable in Acetone). The glass slide containing the sample is then mounted on a brass support block and the sample is ground down to ~ 150 µm in thickness using progressively finer grit papers of 240, 400, 1200 (where a higher number indicates a smoother grinding pad) and then the 2400 and 4000 papers are used to polish the specimen. The sample is then flipped over, again mounted on a glass slide and ground in the same manner down to approximately 15µm in thickness before polishing to create a mirror finish. At this stage thin areas of the sample would appear orange if held under a bright light. After the sample has been polished, a copper ring with a 2mm x 1mm slot is glued onto the sample using Araldite with the slot surrounding the area of interest. This is then allowed to cure overnight (or at least 4-5 hours) at room temperature. Once the glue is cured, the residual material around the ring is removed; the copper ring is then detached from the glass slide and rinsed in a hot acetone bath.

In the final preparation stage, the sample is thinned further to achieve electron transparency by ion milling in a Gatan Precision Ion Polisher (PIPS) using an ionised beam of argon. The beam is accelerated at ~5.5kV and directed at the interface between the two sample pieces to erode the specimen whilst being continuously rotated. For cross-sectional TEM samples, the guns are normally aligned as one gun

at ~4° from the top and the other at ~2° from the bottom of the sample. For plan-view TEM samples, both guns are aligned at ~2-3° from the top of the sample (substrate containing part covered by the ring). The sample rotation is normally kept at a minimum for the machine at around 5rpm. When the specimen is just perforated, a region of electron transparency is produced around the perforation of a few hundred μm^2. Readers are recommended to read Goodhew (2001) [61] for a good guide on sample preparation.

3.2.2 Operation of a TEM

The structure of the TEM described here is for the JEOL JEM-2000FX but the main features are common to most TEM systems. A TEM operates in an evacuated high vacuum column ($<10^{-7}$ mbar) to minimise electron interaction with matter. A set of turbo molecular, diffusion and ion pumps maintains this vacuum whilst isolation valves between different chambers allow samples to be loaded without venting the system. The column consists of: a source of electrons, electromagnetic (EM) condenser lenses, sample holder, EM objective lens, EM projector lenses and a phosphor imaging screen with a charged couple device (CCD) camera mounted below (figure 3.4).

The source is an electron gun which consists of a fine tungsten wire filament connected to the cathode of a high voltage supply. The electrons are accelerated towards the grounded anode. The voltage can be varied but during this study, a 200 kV voltage was used throughout. The filament is heated to produce thermionic emission by inducing a current which is set so that it is just saturated to produce a

uniform beam of electrons. A Wehnelt cap shields the electron gun and produces a focussing effect of the electron beam.

The electron beam emitted at the top of the column is collimated and passes through a condenser aperture to limit the beam's width ranging between 50 – 100 µm in diameter. The first condenser lens helps forming a well defined *virtual electron source* of variable spot size on the specimen, whilst a second condenser lens allows the illuminated beam area or intensity of the beam to be controlled.

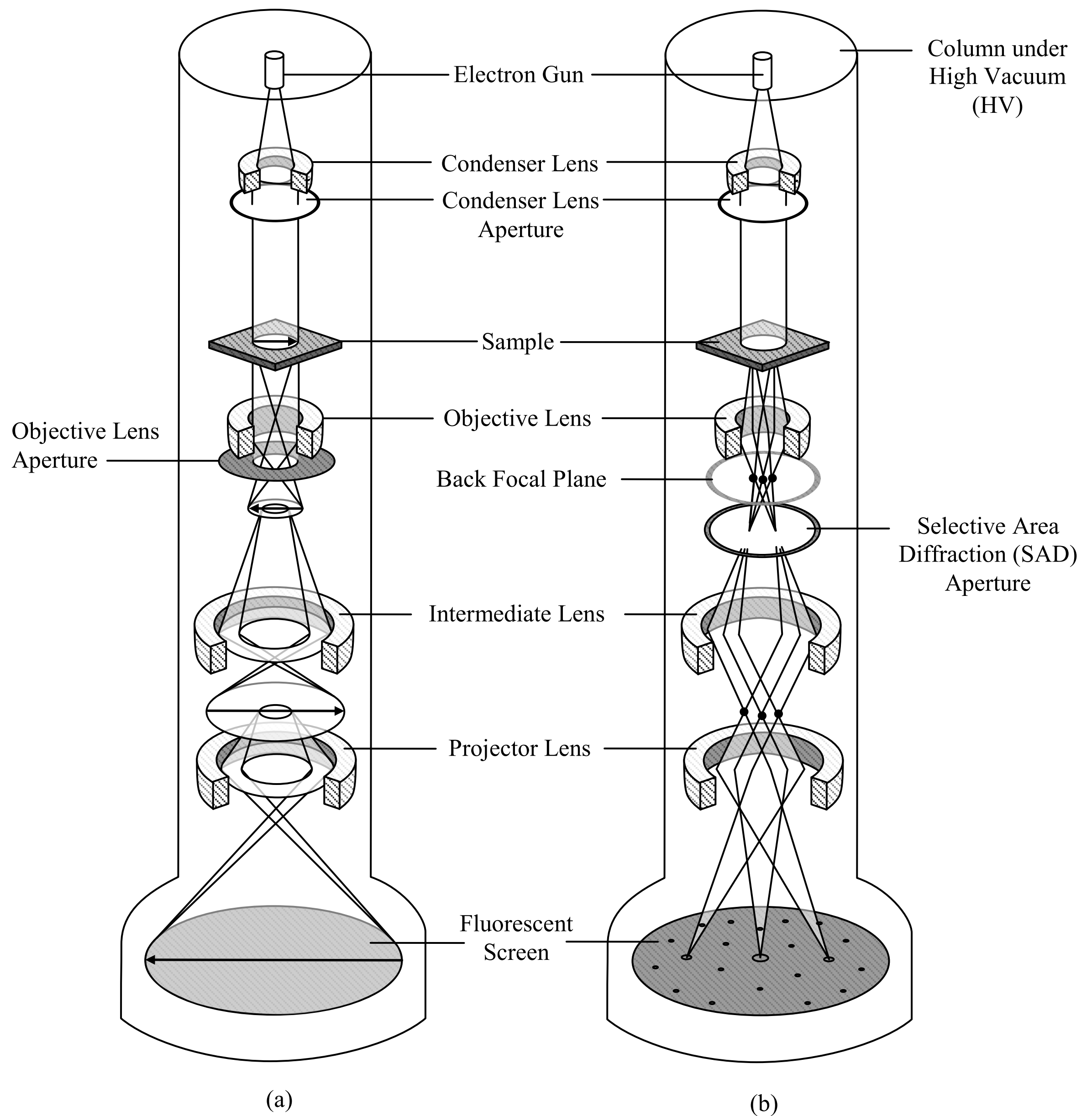


Figure 3-4 Schematic of a Transmission Electron Microscope (TEM) in (a) normal imaging mode (b) diffraction imaging mode. (Used with permission from Nash's thesis) [25]

The sample is normally held by a double tilt holder which gives the ability to tilt the sample in two orthogonal directions; this is of major importance as the crystallographic orientation of imaging is critical to analysis. After passing through the sample, the objective lens is used to produce a real magnified image of the specimen at up to x50 magnification and is also used to focus the final image. There

is a objective lens aperture that can select specific diffraction conditions and its size is a trade-off between intensity and contrast in the desired image.

The TEM can be operated in two modes: (a) normal imaging mode and (b) diffraction imaging mode (figure 3.1). In the normal mode, the selective area diffraction (SAD) aperture after the objective lens is removed but in diffraction mode the SAD aperture is inserted to select the area of the sample to contribute to the diffraction pattern. The beam is then passed through a set of projector lenses to correct for aberrations and magnify the image further. The image is then shown on the phosphor screen where different set up of the desired image can be obtained. This phosphor screen can be lifted up to expose the image to a CCD camera mounted below to be recorded digitally.

3.2.3 Image contrast and diffraction conditions

A good image is produced when there is a clear contrast between the different layers and from dislocations and defects. Image contrast in the TEM can be achieved with the following factors: different atomic density (eg. between Si and Ge); variations in the atomic planes caused by dislocations and strain and selective diffraction conditions with sample tilting. The former two factors are dependent on the samples so the use of selective *diffraction condition* would provide the best contrast in TEM images.

Electrons passing through the sample are often partially diffracted under Bragg condition by the different crystal planes within the sample giving a *diffraction*

pattern. The main electron beam is split into these reflections and during normal imaging the projection of the sample seen is a superimposition of all the reflections. Diffraction mode is achieved by adjusting the strength of the projector lens to focus multiple electron beams from different reflections so that diffraction spots are formed on the screen representing different crystallographic planes. Tilting the sample will allow selection of certain crystal planes for diffraction. In order to achieve the best contrast, the correct *two beam diffraction condition* must be selected. A microscopist can either utilise the diffraction aperture or *Kikuchi lines* to identify specific diffraction conditions [62].

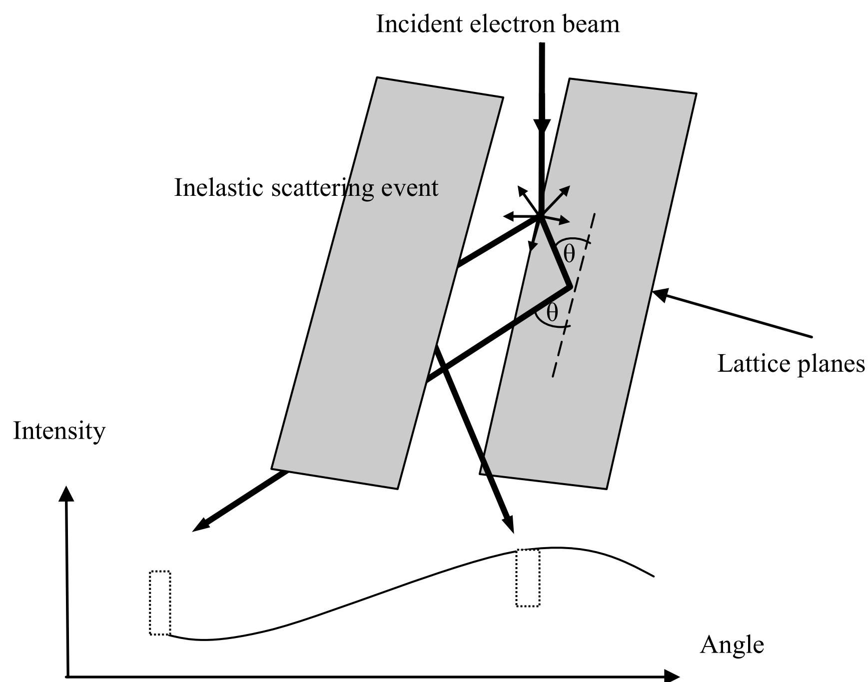


Figure 3-5 Representation of the formation of Kikuchi lines with higher and lower intensity compared to background.

Elastically scattered electrons that have met the Bragg condition for diffraction form the diffraction pattern that can be seen in a TEM. However, when electrons penetrate a fairly thick part of a crystalline sample, another feature called Kikuchi lines can be seen under diffraction mode without the diffraction aperture. Kikuchi lines have

either higher or lower intensity than the background (see figure 3.5). Kikuchi lines are pairs of long lines which form a web-like pattern criss-crossing the diffraction pattern, caused by inelastically scattered electrons. When electrons are inelastically scattered in a sample they can create new (instantaneous) sources of electrons within the sample. Because they have lost coherence with the incident waves, these sources produce electrons that have many different wavevectors (same magnitude) compared to the incident beam. Inelastically scattered electrons give rise to a general background intensity of the diffraction pattern. However, a number of electrons from these secondary sources will be incident at the Bragg angle of specific planes and undergo diffraction. The angular separation 2θ results in the intersection of the Kikuchi lines with the beam centre and corresponding reciprocal lattice point giving rise to the pair of Kikuchi lines (see figure 3.5). Kikuchi lines would move as the crystal is rotated as there will always be planes that diffract the electrons at the Bragg angle. A microscopist can use these lines as guides to orientate the crystal and to correctly identify specific diffraction conditions.

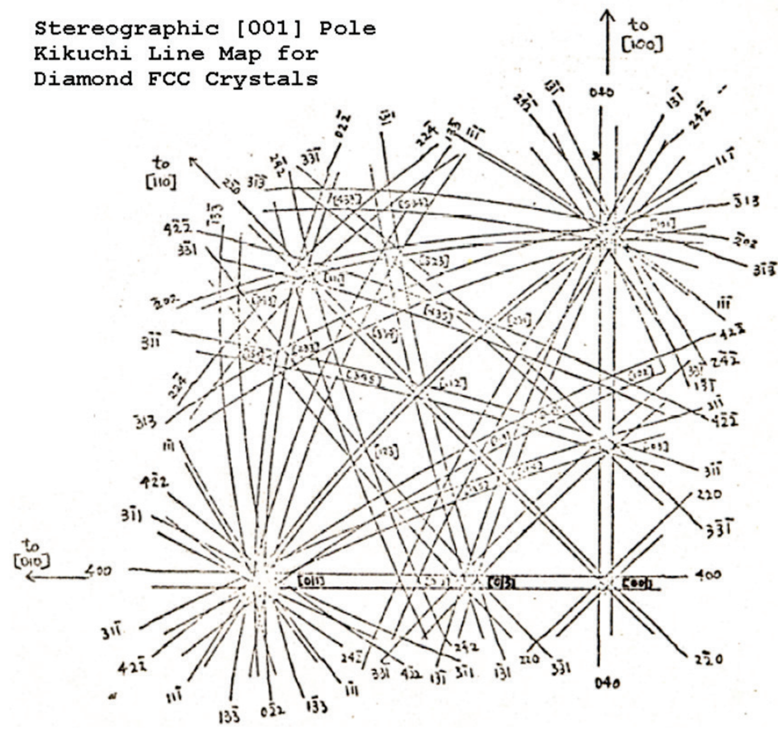


Figure 3-6 A schematic of the stereographic projection for diamond fcc crystal around the [001] pole with Kikuchi lines. [63]

The resulting diffraction condition of [hkl] (certain numbers for h,k,l representing diffraction conditions) only has two spots, the [000] spot representing the main electron beam that passes straight through the sample and another [hkl] spot corresponding to the desired diffraction plane. Contrast is then achieved by using the objective lens aperture to select one spot and allow it to form the final image. The electrons from the other beam are thus blocked so that features diffracting from that plane would appear dark in the image. For *bright field imaging*, the [000] straight through spot is selected. *Dark field imaging* is achieved when the diffracted spot is selected by the objective aperture.

The contrast of a dislocation in the TEM is determined by the relationship between its Burgers vector, $\underline{b}$, and the diffraction vector $\underline{g}$. The diffraction vector $\underline{g}$ is the line

joining the direct beam and the diffracted spot. The position of each reflection depends on the orientation of the sample with respect to the beam and the type of dislocation that the beam passes through. When g is chosen to be perpendicular to b (g . b=0) the dislocations will not be seen on the TEM. This is therefore termed the *invisibility criterion*. Figure 3.7 will show this effect for two different diffraction vectors.

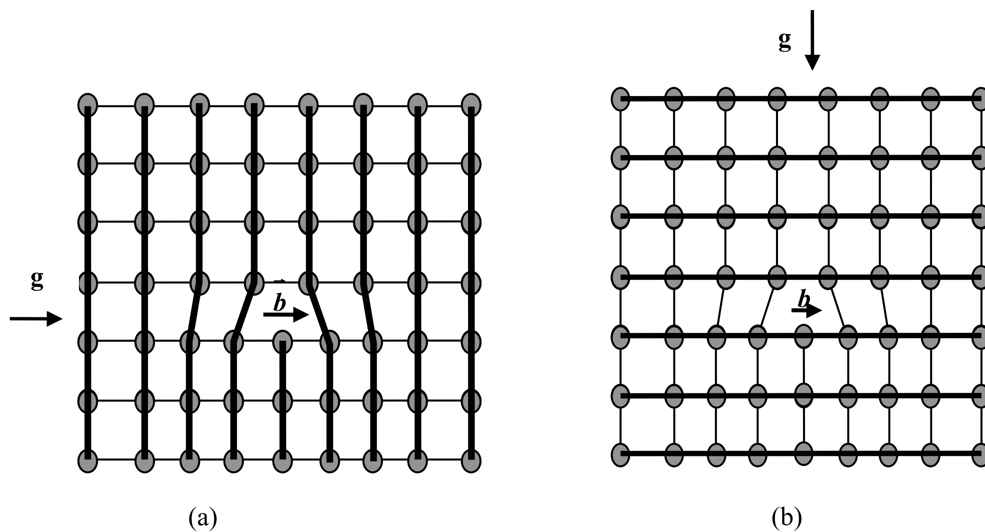


Figure 3-7 Schematic representation of the invisibility criterion in (a) g is parallel to b (g . b≠0) and the edge dislocation is visible; (b) g is perpendicular to b (g . b=0) and there is little distortion in the lattice.

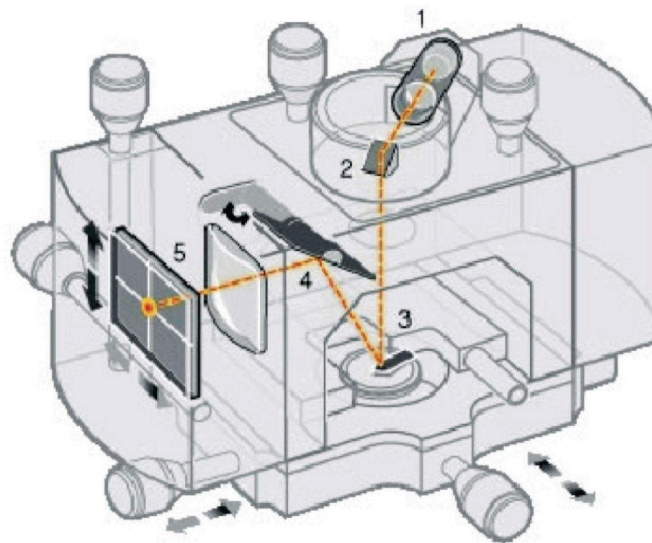
However, for the SiGe system, the dislocations are generally a mixed type having both edge and screw components (see section 2.3.3.2). The screw component of a dislocation forms on the (111) plane and its Burgers vector will be at an angle to the line direction u of the dislocation. This modifies the invisibility criterion so that the dislocations will only be invisible if g . (b x u) =0 *and* g . b =0. Often both

conditions can never be satisfied simultaneously so it is considered that a dislocation is invisible if $\underline{g} \cdot (\underline{b} \times \underline{u}) < 0.5$ *and* $\underline{g} \cdot \underline{b} < 0.5$.

Also, length distortions will occur when the sample is tilted away from the major pole axis in diffraction mode as in real space the sample is being viewed at an angle. Thus only the [000] straight though beam should be viewed and selected if one wants to ensure accuracy in the thickness measurements of layers. Strain contrast imaging is achieved when the [000] and [004] spots are chosen and dislocation contrast is achieved when the [000] and [224] spots are chosen. For a comprehensive description of the principles and operations of the TEM, the reader is referred to Agar (1974) [64].

3.3 Atomic Force Microscopy (AFM)

Atomic Force Microscopy (AFM) is an atomic scale technique used to form very high magnification surface morphology maps of a sample. Topographical features can be scanned to provide the root-mean-squared (RMS) roughness of the sample and the total height range (Z-range) roughness of the surface. The RMS roughness values quantifies the density of surface features of the sample whilst the Z-range provides information about the magnitude of these features. All of the samples in this work were carried out using the NanoNIS controller [65] and data analysed using the Gwyddion software [66]. Figure 3.8 shows a schematic diagram of the AFM head containing the essential working parts of an AFM.



Labels:

1. Laser
2. Mirror
3. Cantilever
4. Tilt Mirror
5. Photodetector

Figure 3-8 Schematic diagram of the Digital Instrument Nanoscope III AFM head. (Image taken from Veeco training manual) [67]

There are two main imaging modes in AFM: *contact mode*, where a silicon nitride tip is brought into "soft-contact" with the sample, and *tapping mode*, where a tip oscillates at the resonant frequency without touching the sample. All the images obtained for this work were done by contact mode AFM so only this operation is described in detail for this section. The reason for using contact mode AFM in this work is because this technique is very robust for hard samples such as Ge and Si heterostructures used and also consumes fewer tips.

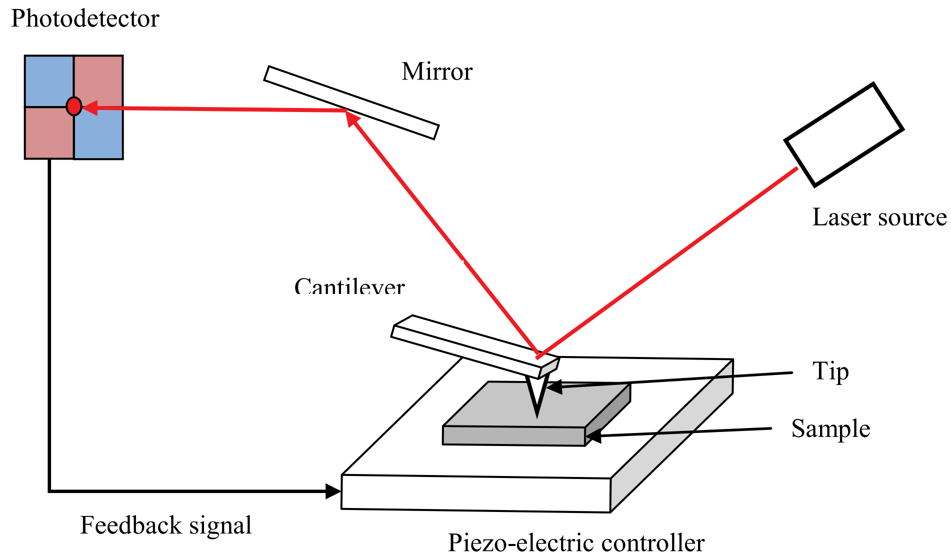


Figure 3-9 Simplified diagram describing the working principle of contact mode AFM.

In contact mode, the tip is allowed to slowly approach the surface of the sample. The tip reaches "soft contact" when it is close enough to feel a mutual repulsion force between the probe tip and the atoms on the surface due to overlap in their atomic orbitals without actually making contact [68]. The sample is the rastered underneath the tip by the high precision piezo-electric controller with up to 0.2 nm resolution vertical and approximately 4nm lateral resolution (depending on tip). As the sample is moved relative to the tip the surface features then imposed a large enough force on the tip to bend the cantilever. This change in deflection of the directed laser onto the cantilever and mirror is then picked up by the photodetector (see figure 3.9). The Nanoscope software then registers this change in position of the laser and sends a feedback signal to the piezo-electric controller to change the height of the stage and maintains a constant force between the tip and the sample. This mode of operation is termed a *constant force mode* and is used for all the samples in this work. A topographical map of the surface can be constructed using the data from the

deflection of the cantilever as well as the height change of the sample as it rasters laterally. The raw cantilever deflection can be used to construct a detailed, qualitative map whilst quantitative information must come from height changes of the sample. Scan areas of up to 100 μm x 100 μm can be achieved with typical scan rate of 1Hz. A clean sample surface is essential as debris build up at the tip can result in a generally lower image resolution as well as image distortions. The raw data then undergoes a series of processing before the final topographical representation of the surface is obtained. These processes can include plane fitting (levelling the image plane), flatten (eliminate noise, tilt), etc... After the processing, information about the sample such as the rms roughness, Z-range and especially the qualitative morphology could be obtained. Several images of different areas of the samples were taken and only average values were presented here. The quality and accuracy of the information depends on various factors such as image scan size, scan rate, image resolution and the resolution of the tip, etc...

3.4 High resolution X-ray diffraction (HR-XRD)

High resolution X-ray diffraction is used to characterise the strain and composition of a layer. It measures the in-plane and out-of-plane lattice constants of crystalline layers which would then be analysed to provide information about the strain state and compositions. Simply put, X-ray diffraction (XRD) is a practical application of Bragg's law being combined with high precision angular positioning. All the XRD done in this work were performed by the Philips PW1835 diffractometer.

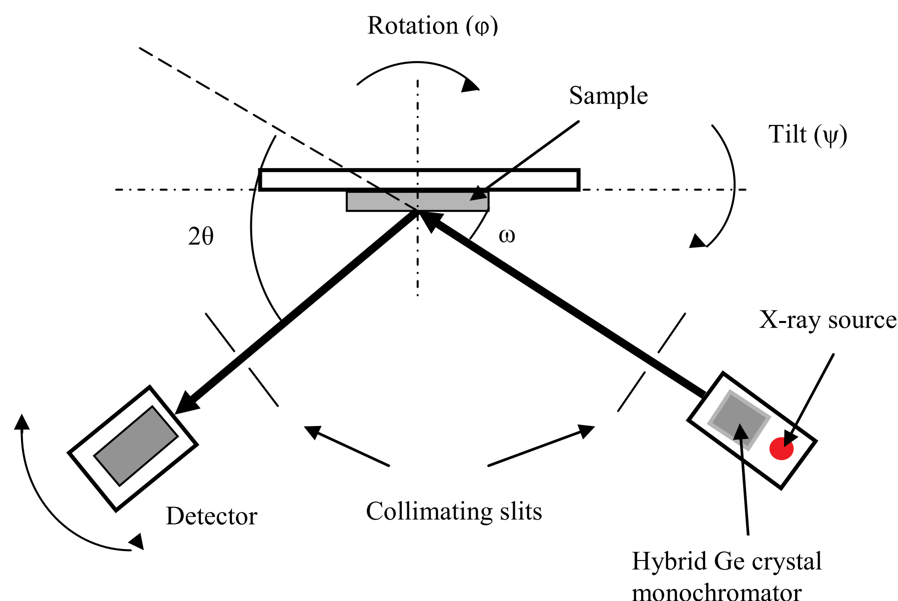


Figure 3-10 Schematic diagram of a typical high resolution X-ray diffractometer along with all the principal angles and degrees of freedom.

A typical XRD system consists of an X-ray source and a detector which can rotate around a sample stage with high degree of accuracy (~0.0001°) (see figure 3.8). A source of high power copper is used ($CuK\alpha_1$ λ= 1.540597Å) operating at 40kV /40mA. There is a hybrid Ge crystal monochromator at the source to produce a high intensity monochromatic X-ray and a collimating slit to collimate the divergent beam. The collimated beam is directed at the sample mounted on a stage orientated with five degrees of freedom including the x,y,z corresponding to the position of the sample, the rotation, phi (φ) and the tilt of the sample, psi(ψ) (see figure 3.10). The position and angles of the sample on the stage will be set up to ensure maximum diffraction counts along with the intended diffraction angles.

When the X-ray beam is incident on the crystalline sample it will be diffracted by planes of atoms. The planes of atoms are then represented by *reciprocal lattice*

points when the diffraction pattern is formed. Mapping of the reciprocal lattice can give characteristic information about the lattice parameters of the crystal. Omega (ω) is the incident angle of the X-ray beam and 2theta (2θ) is the angle between the incident and the diffracted beam (figure 3.10). The ratio between these two angles ω/2θ is measured when moving the detector together with the stage. A rocking curve (RC) is measured when ω is kept constant and the ratio ω/2θ is varied as the detector is moved around a specified crystal reflection. A reciprocal space map (RSM) consists of a series of RCs with different ω values to give a characteristic mapping of the sample lattice. The RCs and RSM are then processed and analysed using the specialist software for XRD, PANalytical X'pert Epitaxy. However, there are two physical factors that limit the accessible reflections of an RSM, the X-ray wavelength and the incident angle. The range of accessible reflections is limited by the wavelength (λ) of the source to a region $<2/\lambda$. The mappable area is also restricted by the incident angle which must be greater than zero ($\omega>0$) and less than the total exit angle ($\omega < 2\theta$) (see figure 3.11).

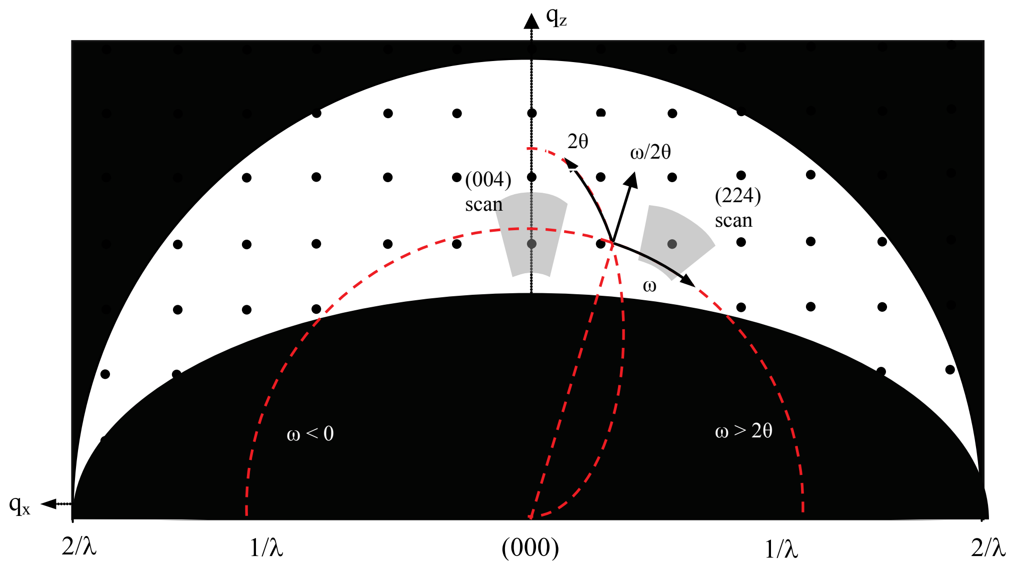


Figure 3-11 Schematic diagram showing the reciprocal lattice points, the scanning directions and the accessible reflections (dark areas are inaccessible) from a (100) crystalline sample. RSM mapping around the (004) and (224) reflections are also shown. (Adapted from Bowen) [69]

The characterisation of the epitaxial layers grown on (100) Si substrates requires collection of symmetric [004] and asymmetric [224] scans [70] (as shown in figure 3.11). Two scans are required to enable the calculation of the in-plane and out-of-plane lattice constants. The [004] scan allows direct determination of the out-of-plane lattice spacing whilst the [224] scan consists of components from both, allowing the extraction of the in-plane lattice parameter when combined with the [004] scan. The use of the two different reflections can compensate for other factors which affect the characterisation analysis of the samples such as the tilt or twist of epitaxial layers compared to the substrate [71]. Relaxation and composition values can be calculated from the relative peak positions of the different layers compared to the Si substrate peaks in the RSM [69].

3.5 Selective defect etching

Selective defect etching is a widely used technique designed to reveal the threading and misfit dislocations of epitaxial layer. This is a very useful technique for defect densities in the range of 10^4-10^7 cm^{-2} which is out of range for other techniques such as plan-view TEM where the detection limit is $>10^7$ cm^{-2} of defect density. The densities of threading and misfit dislocation or stacking faults are very critical to the performance of semiconductor devices as these can act as sources of leakage during device operation [72].

Selective etchants have differential etch rates between the bulk and dislocations. The strain field associated with a dislocation can result in a different etch rate compared to the bulk material, this results in preferential etching around the dislocation [73]. If the preferential etch rate is higher than the bulk etch rate, it will create *etch pits*

around the dislocations. If the preferential etch rate is lower than the bulk etch rate, hillocks are formed around the dislocations [34]. These pits and hillocks which represent the numbers of dislocations in the epitaxial layers can be viewed through a differential interference contrast microscope (see section 3.6). The etch pit density (EPD) can then be calculated which gives the TDD of the layer (one assumes one etch pit corresponds to one threading dislocation).

The basic components of etching solutions are:

- An oxidising agent (eg. HNO_3, H_2O_2, CrO_3 etc..), and in some special cases an additional oxidising substance is used to enhance selectivity and etch rate such as I_2, Br_2, Ag..
- A complexing agent such as HF to dissolve the oxide
- A diluent which can be acetic acid or water or both

Defect etching is a chemical dissolution process where the oxidising agent begins by oxidising the surface of the sample. The complexing agent then dissolves this oxidised surface and exposes the sample to further oxidation thus etching the sample. The diluent acts as an etch rate control. Table 3.1 below lists the common etchants that are used for Si, $Si_{1-x}Ge_x$ and Ge defect delineation.

Etchants	Composition	Ratio
Secco [74]	$(K_2Cr_2O_7 + H_2O) : HF$	1:2
Schimmel [75]	$(CrO_3 + H_2O) : HF$	1.3:1
Iodine [76]	$(HF : HNO_3 : CH_3COOH) + I_2$	5:10:11
Wright [77]	$(HF : CrO_3 : H_2O) + HNO_3$, $Cu(NO)_3$, HAc	2:1:2
HCl gas [78]	In-situ HCl gas using RP-CVD	

Table 3.1 Recipes of standard etchants used for Si, SiGe and Ge.

Whatever the etchant is used, selective defect etching requires a modification of the surface potential between the perfect crystalline material and the defects. The etching is not only influenced by the strain field at the dislocation sites but also depends on the composition of the etchant. Other parameters which also influence the etching behaviour of etchants are the temperature, the crystallographic orientation, doping, strain variations and the layer composition.

Etch rates were determined by measuring the thickness of material that has been removed by etching. This was done by covering half of the sample with a chemical resistive Apiezon W black wax. The sample was then submerged in the etchant for a certain amount of time and rinsed in DI water to remove excess etchant on the surface of sample and then dried using a N_2 gun. The wax was subsequently removed by rinsing the sample in xylene, then iso-propanol and rinsed with DI water. Removing the wax would reveal a step between the selectively etched and unetched regions. This step height could be measured using a Talystep, which is a mechanical profiler, to give the etch depth of the sample. Several samples etched and measured for different times would give the etch rate for that particular etchant.

4 Epitaxial Growth of Ge Buffers on (111)-Oriented Si Substrates

4.1 Introduction

Compared to (100) orientation, Ge grown on (111) substrates can enhance the carrier mobility for electrons. However, there are epitaxial challenges (table 4.1) that need to be solved to improve the quality of Ge buffers grown on (111)-oriented Si substrate.

Properties		**Si_{1-x} Ge_x or Ge on (100) Si**	**Si_{1-x} Ge_x or Ge on (111) and (110) Si**
Quality of starting wafer		High quality, low defect level	More defective, difficult offcut
Epitaxial growth	Stacking fault formation	Not susceptible to stacking fault formation [79]	Tendency to form stacking faults and twins [80-82] (~10^9 cm^{-2})
	Surface roughness	Low (<1nm rms) [80]	High (30-60 nm rms) [80]
	TDD	Low ($<10^7$ cm^{-2}) [80]	High (10^8 – 10^9 cm^{-2}) [80]
	Growth rate	High [83]	Low [83]

Table 4.1 Epitaxial challenges of $Si_{1-x}Ge_x$ / Ge growth on (111) and (110) Si substrates.

For (100) growth orientation, employing graded $Si_{1-x}Ge_x$ buffers can often minimize the density of the defects as strain relaxation occurs gradually and predominantly by dislocation glide rather than nucleation of new or additional dislocations. Some groups have tried to study the epitaxial process of growing $Si_{1-x}Ge_x$ buffers on different crystallographic surfaces but the concept of gradual strain relaxation is not easily applicable in the case of (111) oriented surfaces due to the tendency of stacking fault formation [81, 84]. Another way of reducing defect densities of direct growth of Ge layers on Si surfaces is reported to use Sb in surfactant mediated epitaxy by molecular beam epitaxy[82, 85-87], but the setback is due to the danger of incorporating Sb as a dopant in the surface layers. Recently, Hartmann *et al.* reported on the characteristics of thick relaxed Ge layers grown on (100), (110) and (111) Si substrates by reduced-pressure chemical vapour deposition (RP-CVD) [80] using a low temperature/ high temperature (LT/HT) process [88]. Their report was primarily focussed on the properties of the Ge layers at various high temperature (HT) layer thicknesses (up to 2.5µm) on the same low temperature (LT) layer (100nm thick). The roughness values of the Ge layers grown on (111) substrates were found to be typically 60 times higher than similar layers on (100). Also, the threading defect densities for layers grown on (111) were ten times higher than those grown on a (100) Si substrate. Other methods include selective growth techniques such as aspect ratio trapping (ART) and epitaxial lateral overgrowth (ELO) [89, 90] which is also quite common in III-V growth [91].

This chapter will present the results for the investigation of fully relaxed Ge layers grown on (111) Si substrates using the LT/HT growth method by reduced pressure chemical vapour deposition. This involves the deposition of a thin, low temperature

Ge seed layer to plastically relax the strain followed by a thicker, high temperature Ge layer that serves to reduce the threading dislocation density (TDD). The TDD can be further reduced by post-growth annealing. This chapter is focussed on varying the thickness of the low temperature (LT) Ge seed to try and suppress the surface roughness as a means to improve the quality of thick relaxed Ge buffer on (111) Si substrate. Two different high temperature (HT) layer thicknesses have also been grown on these various seed layers to make relative comparisons in terms of surface morphology, strain relaxation, stacking fault and threading dislocation densities. Further investigations were also conducted to understand the initial stages of LT to HT growth transition and subsequent growth mechanisms.

4.2 Experimental details

All the epitaxial Ge layers in this study were grown on 100mm n^- (111)-oriented Si substrates by RP-CVD in a ASM Epsilon 2000 using GeH_4 as a gaseous precursor diluted in H_2 carrier gas. An 1150 ^{0}C bake was initially performed on all wafers for two minutes in H_2 in order to desorb any native oxide on the Si substrates prior to epitaxial deposition. In this investigation, Ge was grown using a fixed GeH_4 precursor flow rate and chamber pressure such that the GeH_4 partial pressure was held constant at ~1.3 Pa for both LT and HT. Previous study on growth of relaxed Ge layers on (100) Si substrate using these growth conditions have produced high quality relaxed Ge buffer on (100) Si [79]. The growth temperatures for the LT and HT layers were kept constant at 400 ºC and 670 ºC respectively with no Ge growth occurring during the temperature ramp between these steps. Post growth *in-situ* annealing was carried out at 830 ºC for 10mins in H_2 (see figure 4.1).

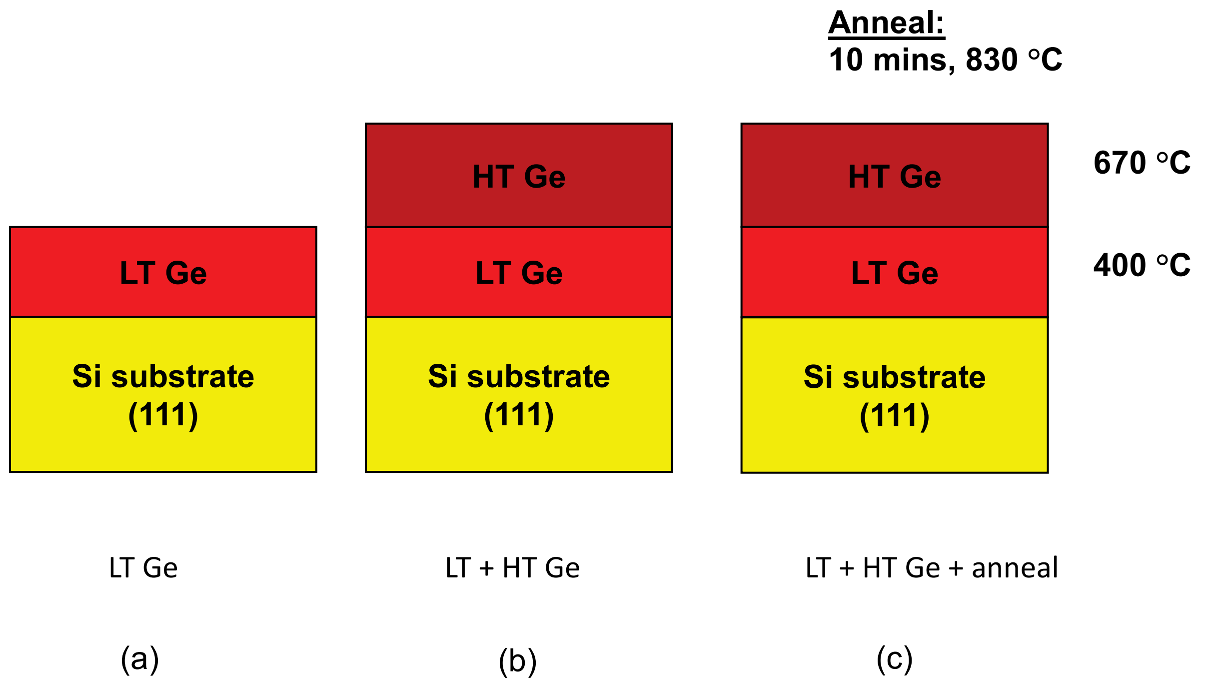


Figure 4-1 Schematic diagram of sample growth with: (a) low temperature (400°C) seed layer only, (b) high temperature (670°C) layer on top of LT seed and (c) with in-situ annealing at 830°C.

As there are a lot of growth parameters that can be varied to achieve a full systematic study, this thesis only focuses on examining different layer thicknesses of the LT seed and HT layers. The different thicknesses of the layers were achieved by varying the deposition times for each layer. The main aim of this investigation is to assess the importance of the LT, HT layers and the annealing on the quality of the final structure such as surface roughness, TDD and stacking fault density. A range of LT seed layers were initially grown on (111) orientations to look at how the growth and strain relaxation evolved as the layer gets thicker. Thick HT relaxed Ge layers of two different thicknesses were grown on these LT Ge seeds with and without *in-situ* annealing to examine the final quality of the buffer. Further follow up work was carried out with annealing at 670 ºC HT growth temperature to look at the initial stages of HT layer growth.

The microstructure and dislocation network of the Ge layers was analyzed using both cross-sectional and plan view transmission electron microscopy (TEM) with a JEOL 2000FX operating at 200 kV. All cross-sectional TEM samples were viewed along a <110> direction unless otherwise stated. TEM specimens were prepared by conventional mechanical back thinning and polishing to ~20μm. The samples were then thinned further to achieve electron transparency by Ar ion beam polishing with 5.5 kV energy incident at an angle of 2 - 4° to the surface. The surface morphology of the Ge layers was examined by atomic force microscopy (AFM) using a Veeco Multimode AFM with a NanoNIS controller operating in contact mode. AFM was also used to determine the root mean square (rms) roughness values of the samples with typical scan size of 10μm x 10μm. High resolution X-ray Diffraction (HR-XRD) was used to examine the macroscopic degree of relaxation (with respect to Si substrate) and crystallinity of the Ge layers. All XRD measurements were done using a Phillips X'pert MRD Pro single crystal high resolution X-ray diffractometer by Dr Andrew Dobbie under direction of the author.

4.3 Growth of low temperature Ge seed layers

This section focuses on the growth of LT Ge seed layers on (111) Si substrate. In the first part of the investigation, only the low temperature Ge seed thin layer is grown at various thicknesses at 400°C to examine the morphology and dislocation formation as it relaxes the strain in the Ge film grown on Si (111). Different thicknesses of the layers were achieved by varying the deposition times as shown in table 4.2 above (LTa-1, LTa-2 and LTa-3). The purpose of this thin seed layer is to initiate the

relaxation of epitaxial Ge within a certain thickness. Investigations of how defects are formed and the surface morphology of the layers will give an understanding of how it affects the growth of high temperature layers later.

Wafer (*111*)		Growth temperature (°C)	Deposition times (s)	Thickness measured (nm)
Name	**ID**			
LT-a1	11-067	400°C	240	10
LT-a2	10-370	400°C	410	35
LT-a3	10-147	400°C	820	70

Table 4.2 Low temperature Ge seed layer wafer numbers and deposition times along with measured thicknesses.

4.3.1 Microstructure

Cross-sectional TEM images for samples LTa-1, LTa-2 and LTa-3 are shown in figure 4.2. TEM images were processed from raw data using the ImageJ software. For each sample, several images were taken and only the best quality images with typical characteristics are shown here in this thesis. The thicknesses of the Ge seed layers in samples LTa-1, LTa-2 and LTa-3 were measured by cross-sectional TEM to be at ~ 10 nm, ~ 35 nm and ~ 70 nm respectively.

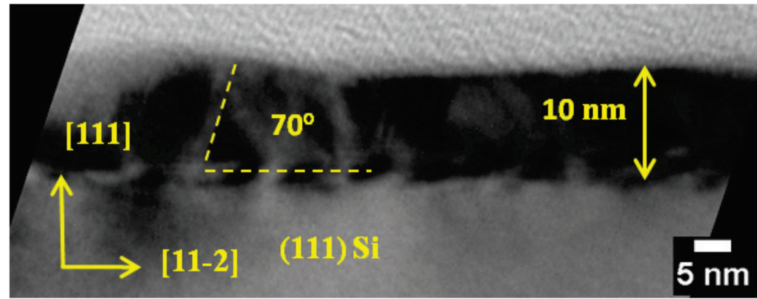


Figure 4-2a Cross-sectional TEM image of 10 nm Ge seed layer grown on (111) Si substrate (sample LTa-1).

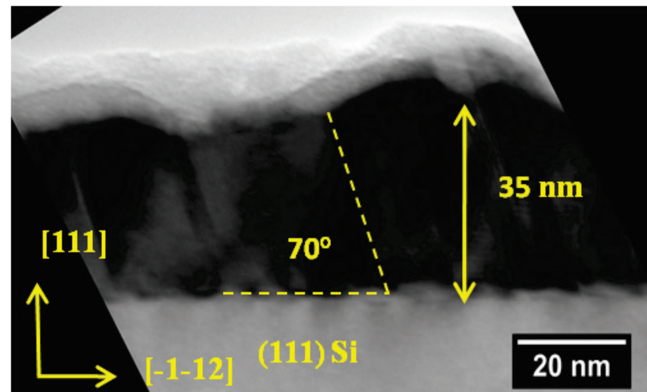


Figure 4.2b Cross-sectional TEM image of 35 nm Ge seed layer grown on (111) Si substrate (sample LTa-2) with several inclined stacking faults at 70° to the Ge/Si interface.

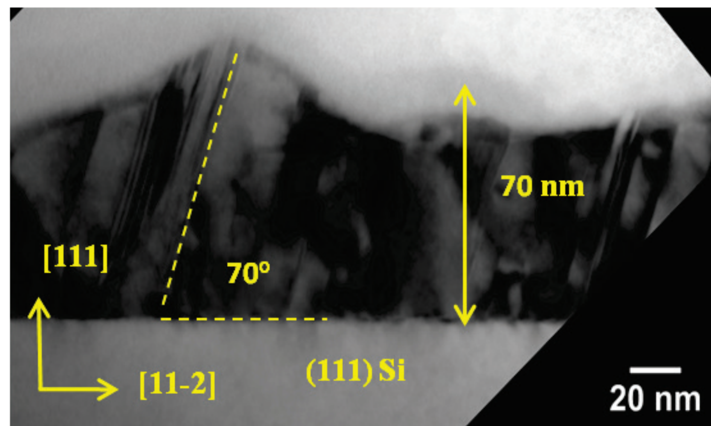


Figure 4.2c Cross-sectional TEM image of 70 nm Ge seed layer grown on (111) Si substrate (sample LTa-3) with numerous inclined stacking faults at 70° to the Ge/Si interface.

Figure 4.3 shows a plot of LT layer seed thickness against deposition times to give the corresponding growth rate of approximately 0.1 nms^{-1} at 400 ºC and is lower compared to the corresponding growth rate on the (100) surface of 0.3 nms^{-1}.

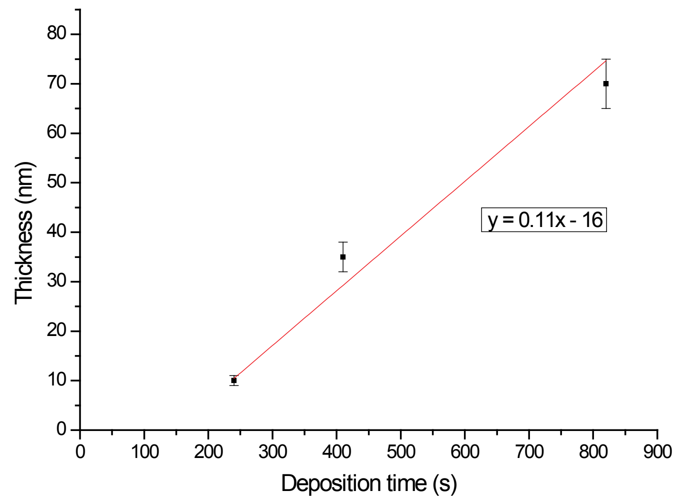


Figure 4-3 Plot of LT layer thicknesses against deposition times to give a Ge growth rate of 0.1 nms^{-1} at 400 °C.

It can be seen that LTa-2 and LTa-3 samples have a high density of stacking faults, twins and threading dislocations penetrating the surface from the Ge/Si interface. The inclined stacking faults/twins lie along two of the three {111} planes typical of (111)-oriented growth (section 2.5). Two inclined stacking faults/twins make angles of ~ 70° and ~ 50° with respect to the Ge/Si interface and ~ 60° between themselves. The stacking fault component from the other plane was not observed under cross-sectional TEM.

The high density of stacking faults observable under cross-sectional TEM is better illustrated under plan-view. Plan-view TEM also shows the typical arrangement of the {111} glide planes for (111) growth (figure 4.4). The stacking fault features were seen lying along three particular directions which might be the [1-10], [-101] and

[01-1] directions indicating the intersections of the {111} glide planes with the (111) growth plane. Threading dislocations can also be observed but they appear to be pinned by the network of stacking faults and become undistinguishable where the faults overlap.

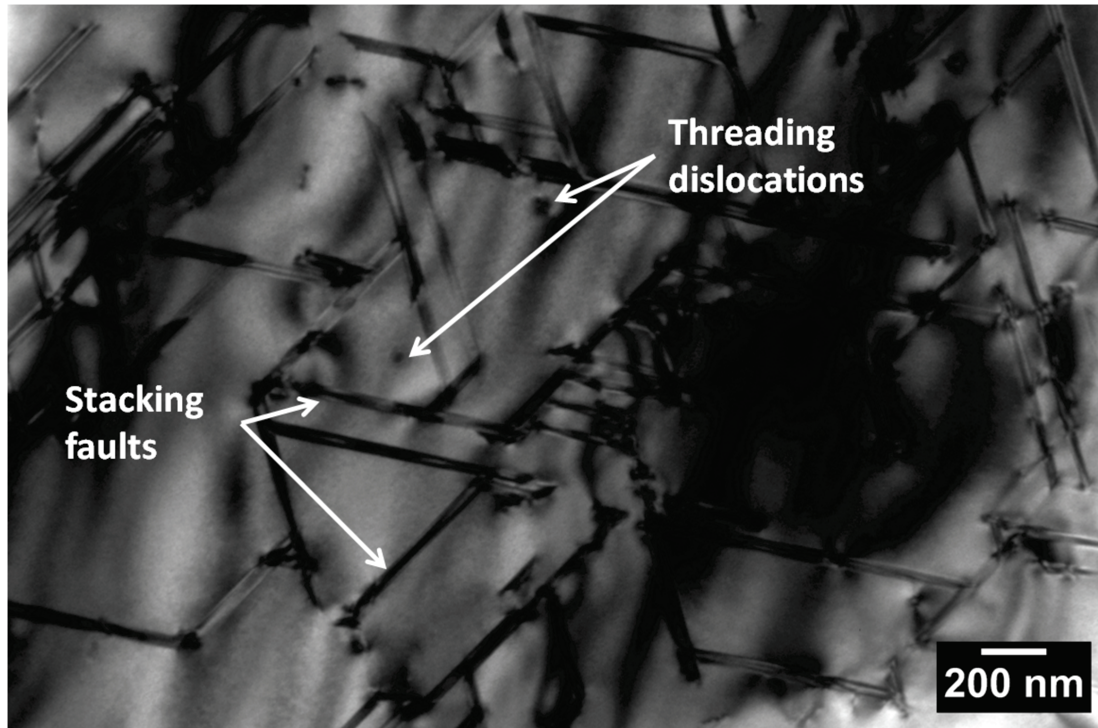


Figure 4-4 Typical Plan-view TEM image of stacking fault lines oriented along the intersections of {111} glide planes with the (111) growth plane. Several threading dislocations appear in close proximity with the dense network.

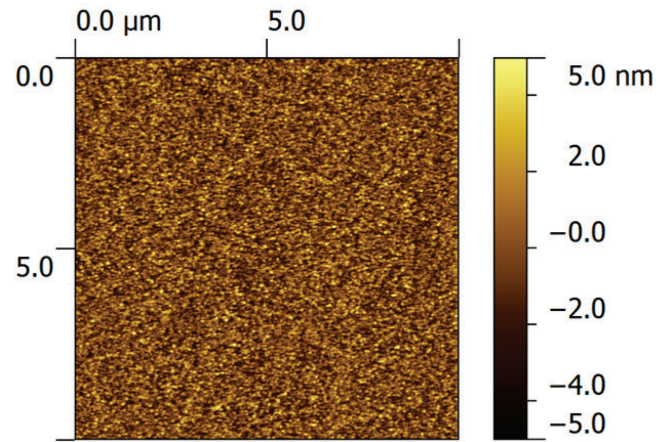
The observation of stacking faults in these layers is consistent with previous studies of relaxed Ge layers on (111) Si [80]. As Ge is grown on top of Si, compressive strain is acted on the layer, and the gliding sequence of these partials in (111) orientation has led to formations of extended stacking faults. The stacking faults were formed due to the dissociation of 60° a/2<110> strain-relieving dislocations into pairs of 90° and 30° Shockley partial dislocations (see section 2.4.6). In the case

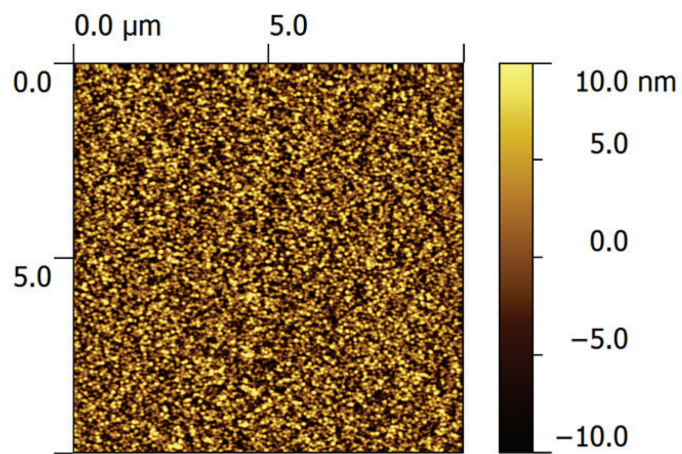
of relaxation of compressive strain on (111) Si substrate, the 90° always leads the 30° partial when they glide. However, the 90° partial dislocation experiences a larger shear force compared to the 30° partial and glide apart hence the formation of extended stacking faults. This is in contrast with strain relaxation of Ge layers grown on (100) Si where stacking faults are kept from ever dissociating widely due to the reverse of gliding sequence of Shockley partial dislocations where the 30° partial leads and the 90° trails closely behind [92].

For LTa-1, only a few stacking faults were observed for this 10nm layer under cross-sectional TEM (figure 4.2a). The layer also seems to be smoother compared to the other two seed layers. It is not entirely clear whether this layer contains any fewer defects than the other two since PVTEM has been performed on this sample but could not reveal the layer structure.

4.3.2 Surface morphology

The surface of the Ge seed layers grown on (111) Si substrate appear very smooth for the 10nm LTa-1 sample where an rms roughness of 1.4 nm (Z-range: 13 nm) was measured by AFM. As the samples got thicker, there was also an increase in surface roughness to 5 rms (Z-range: 38 nm) for LTa-2 (35 nm thick) and 12.5 rms (Z-range: 87 nm) for LTa-3 (70 nm thick). The AFM images for all the seed layers are shown in figure 4.5. The surface morphology of the Ge seed layers showed the presence of short-range wavelength (~ 0.1 μm), periodic undulations and this is demonstrated by a section plot through an AFM scan in figure 4.6.





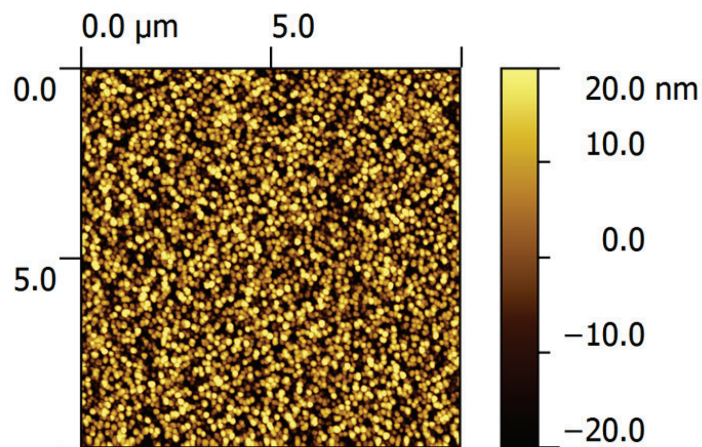


Figure 4-5 AFM images of (111) seed layers showing short-range wavelength, periodic undulations: (a) LTa-1 (10 nm), (b) LTa-2 (35 nm), (c) LTa-3 (70 nm).

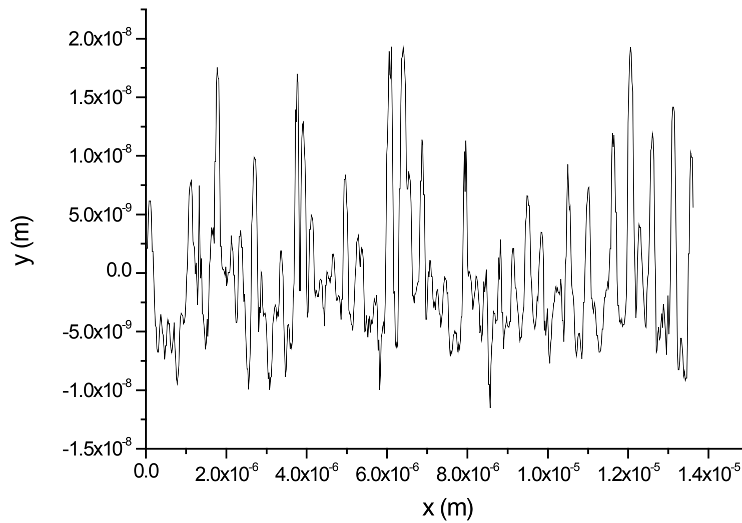


Figure 4-6 Section plot through an AFM scan of a seed layer to show the short-range wavelength, periodic undulations that appear in all the LT seed layers.

As the thickness of the Ge seed increases, one would expect the surface roughness of the layers to increase in a similar manner to Ge layers grown on Si (100) substrates [93]. The plot of rms roughness and Z-range versus layer thickness in figure 4.7 demonstrates the linear increase as a function of Ge seed layer thickness.

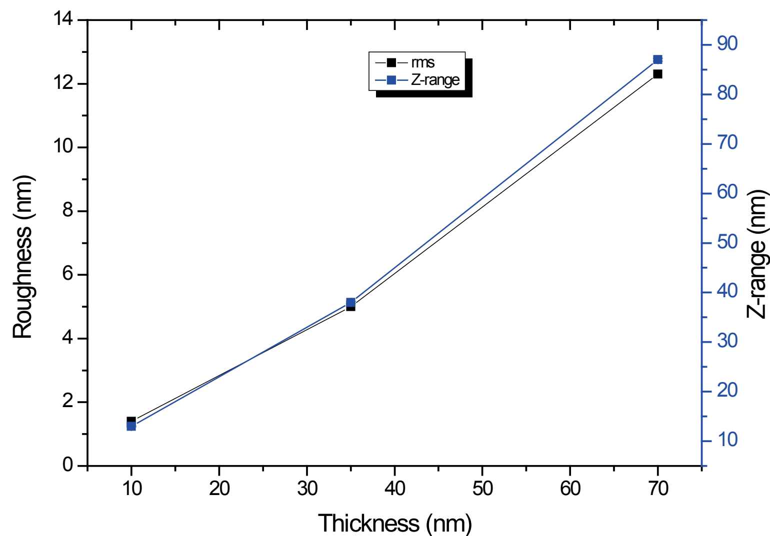


Figure 4-7 Plot of surface rms roughness (black) and Z-range (blue) versus Ge seed layer thickness showing an almost linear dependence.

4.3.3 Relaxation

X-ray diffraction was performed on the seed layers to examine the state of strain relaxation in the layers prior to the HT layer deposition. The measurements were done using a Phillips X'pert MRD Pro single crystal high resolution X-ray diffractometer. Analysis of the raw data was carried out using the X'Pert Epitaxy software. Figure 4.8 shows and reciprocal space map (RSM) of the 70 nm Ge seed layer grown on (111) Si substrate.

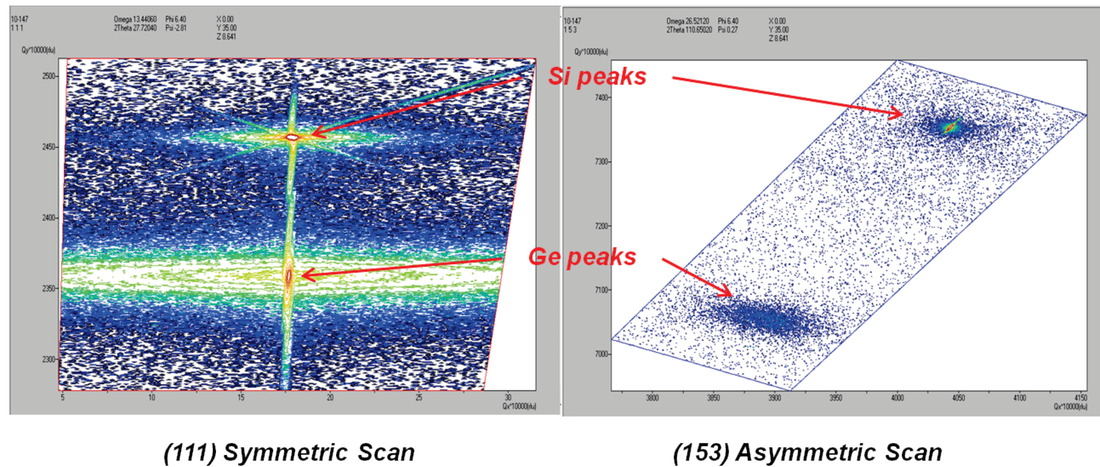


Figure 4-8 (111) symmetric and (153) asymmetric scans of the 70 nm Ge seed layer with respect to the underlying (111) Si substrate showing the Si and Ge peaks very clearly.

The relaxation of this Ge seed layer with respect to (w.r.t.) the Si substrate was calculated to be ~ 97.9 %. This is quite close to the full relaxation value of 100% and is expected of this layer since it is quite thick and has a dense network of dislocations to relieve the mismatch strain.

Similar observation is made with the RSM scans for the 35 nm seed layer. However, the peak intensity is very low in the (153) asymmetric scan with the Ge peak layer

only just detected. The relaxation value was determined to be ~ 90.5 %. The relaxation values of these seed layers agree with the observation made by Capellini [94] about strain relaxation of high content compressive strained $Si_{1-x}Ge_x$ on (100) Si substrate where the layers were still in partial strain for thicknesses up to 200 nm.

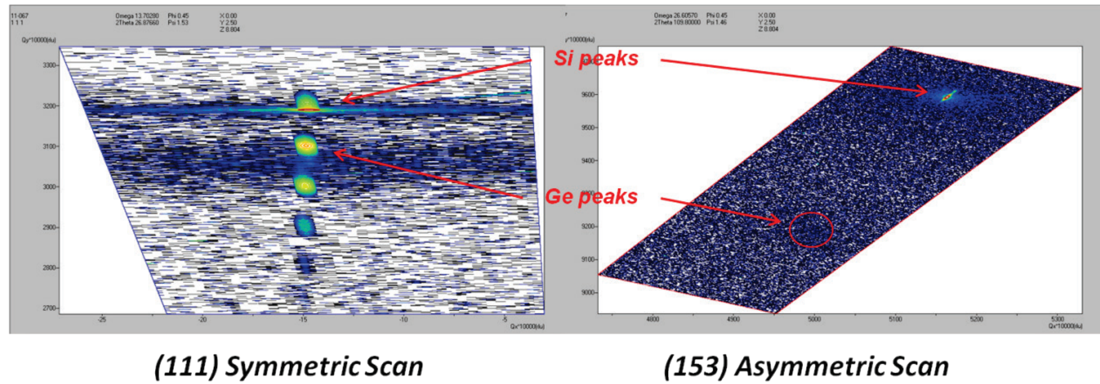


Figure 4-9 (111) symmetric and (153) asymmetric scans of the 10 nm Ge seed layer with respect to the underlying (111) Si substrate.

Figure 4.9 shows the XRD scans for the 10 nm seed layer. The symmetric scan shows the Si substrate peak and five more peaks, which could be due to the Ge layer and fringe peaks. However, if the highest intensity peak corresponds to the Ge layer, then it lies *closer* to the Si substrate than those of the thicker seed layers LT-a2 and LT-a3 implying that the *out-of-plane* (111) lattice spacing is actually less than the two thicker seeds i.e.LT-a1 is under *less* compressive strain. This is a reasonable assumption considering the work done by Capellini. There appears to be a very faint layer peak on the asymmetric scan – this might correspond to the Ge layer but it is difficult to determine the relaxation of Ge layer with any confidence. However, by extrapolating the two values of the thicker layer relaxation and using the data shown by Capellini, a relaxation value of ~ 85% was estimated for LT-a1 (figure 4.10).

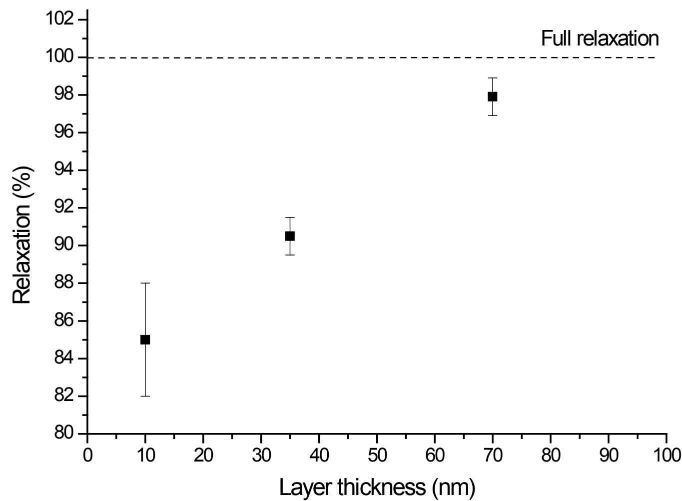


Figure 4-10 Plot of relaxation as a function of Ge seed layer thickness.

4.4 Growth of high temperature Ge layers

A temperature of 670°C was used to grow thick Ge layers on top of the Ge seeds. This temperature increased the growth rate of epitaxial Ge from 0.1 nms^{-1} to about 1.2 nms^{-1} for (111) substrate orientation. From previous studies of relaxed Ge layers grown on (100) Si substrate, the thick high temperature layer would act to reduce the TDD from the seed and to enhance the overall growth rate of the buffer [95]. Even though the LT and HT regions can be qualitatively identified by the level of defects, there isn't a clear interface between these regions. Therefore, the total Ge layer thickness was measured and the HT layer thickness was obtained by subtracting the known value of the LT seed. Table 4.3 lists the different wafers that have been grown at different deposition times plus wafers with in-situ annealing at 830 °C.

Wafer *(111)*		Growth temperature (°C)	Deposition times (s)		Thickness measured (nm)	
Name	**ID**		**LT**	**HT**	**LT**	**HT**
HT-a1	10-371	400°C / 670°C	820	410	70	500
HT-a2	10-148	400°C / 670°C	820	820	70	1000
HT-a3	12-007	400°C / 670°C	410	410	35	475
HT-a4	11-068	400°C / 670°C	240	410	10	460
HT-a5	12-005	400°C / 670°C	240	820	10	900
HT-a1 (A)	10-372	400°C / 670°C + 830°C anneal	820	410	70	500
HT-a2 (A)	10-149	400°C / 670°C + 830°C anneal	820	820	70	1000
HT-a3 (A)	12-008	400°C / 670°C + 830°C anneal	410	410	35	475
HT-a4 (A)	11-069	400°C / 670°C + 830°C anneal	240	410	10	460
HT-a5(A)	12-006	400°C / 670°C + 830°C anneal	240	820	10	900

Table 4.3 Wafer numbers, deposition times and thicknesses of HT Ge layers grown on (111)-oriented LT Ge seeds.

4.4.1 Microstructure

When thick (~500 nm) Ge layer, sample HT-a1, was grown at 670°C on the thickest Ge seed of 70nm there are numerous stacking faults and twins that have extended from the interface way beyond the seed layer, penetrating the surface. These defects are hugely detrimental to future device performance as they are a significant source of leakage current during device operation.

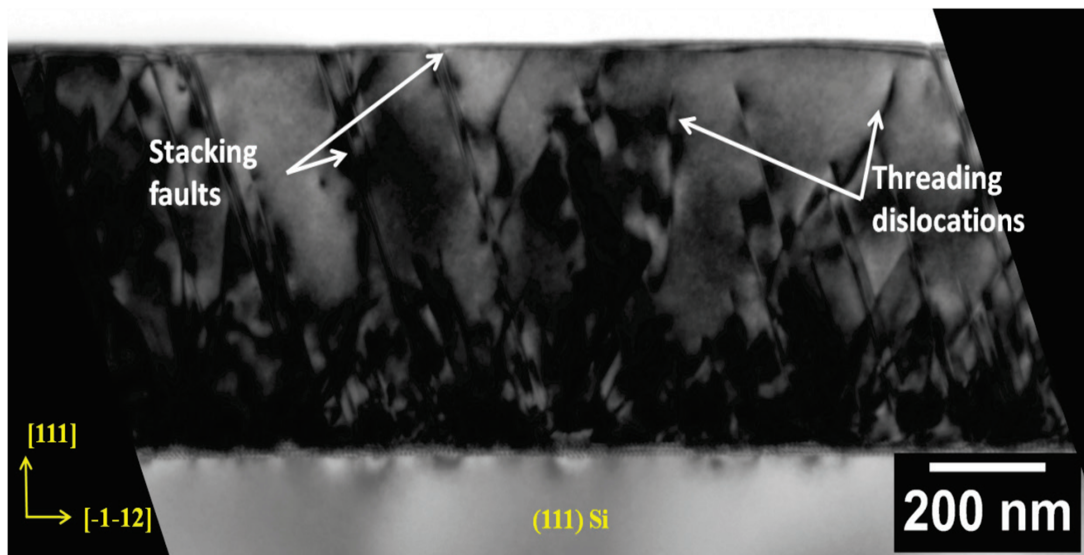


Figure 4-11 Cross sectional TEM of 500 nm of HT Ge layer on 70 nm seed (HT-a1). A lot of stacking faults can be seen to have emerged from the interface and penetrate all the way to the surface of the sample. A few threading dislocations can also be observed in the dense network of defects.

Figure 4.11 shows the presence of such stacking faults/twins in sample HT-a1 under cross-sectional TEM, which is similar to those reported in previous work of thick Ge layers on (111) Si by Hartmann et al. [80]. The inclined stacking faults again can be seen lying at a 70° and 50° angles to the surface representing two of the {111} glide planes typical of (111) surface growth (see section 4.3.1 and 2.5).

Similar observation can be made with the thicker HT Ge layer (~ 1000 nm), sample HT-a2 (figure 4.12).

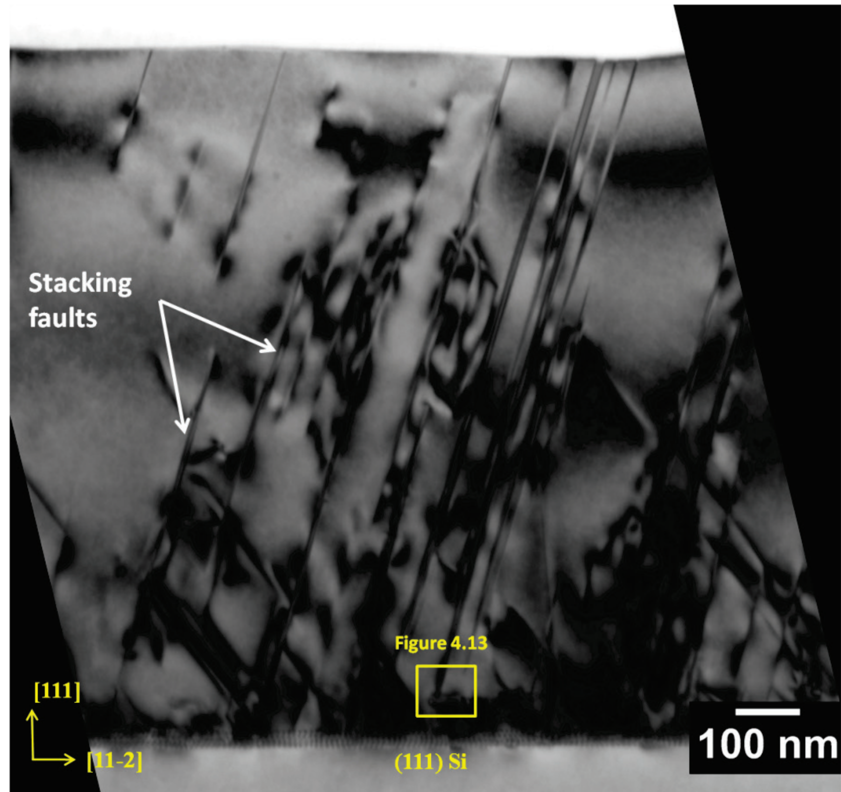


Figure 4-12 Cross sectional TEM of 1um HT layer on 70nm seed(HT-a2). A similar network of stacking faults/ twins is observed compared to the 500 nm thick HT layer (HT-a1).

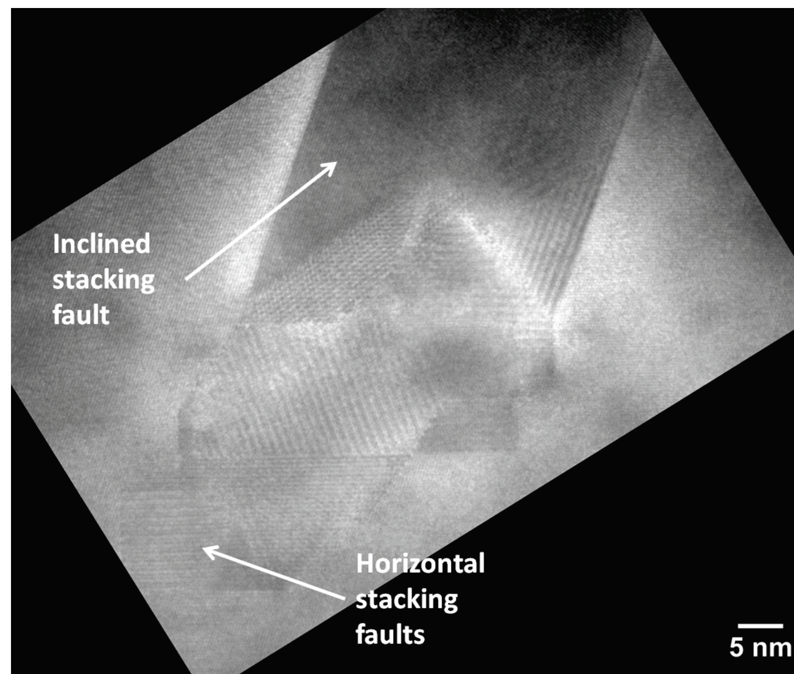


Figure 4-13 Cross sectional TEM of stacking fault overlapping in sample HT-a1. The inclined stacking fault has overlapped with the horizontal fault creating a region with different planar faults.

The 35 nm seed was also examined by growing a thick ~ 500 nm HT Ge layer on top of it, sample HT-a3 and HT-a3 (A). This buffer structure also suffers from a network of stacking fault observable under cross-sectional TEM showing no sign of improvement in buffer quality.

Apart from the inclined stacking faults and twins, horizontal stacking faults were also observed to form within ~ 100 nm from the interface for thick HT Ge grown on 70 nm and 35 nm seeds. Within this 100 nm area near the interface, high density of stacking faults and twins have led to numerous stacking fault overlaps from different planes (see figure 4.13).

Stacking fault features were again seen lying along the expected [1-10], [-101] and [01-1] directions for the thick HT Ge layers grown on the 70nm seed under plan-view TEM indicating the preferential surface crystallographic orientations (figure 4.14, 4.15). These directions are again the intersections between the {111} gliding planes and the (111) growth surface. Several threading dislocations were also observed in the vicinity of the stacking faults, although their close proximity to the stacking faults makes it difficult to determine an accurate TDD value. In these samples, only the stacking fault densities (SFD) were estimated. These dislocations are likely to become pinned and unable to contribute towards strain relaxation, resulting in the nucleation of additional dislocations.

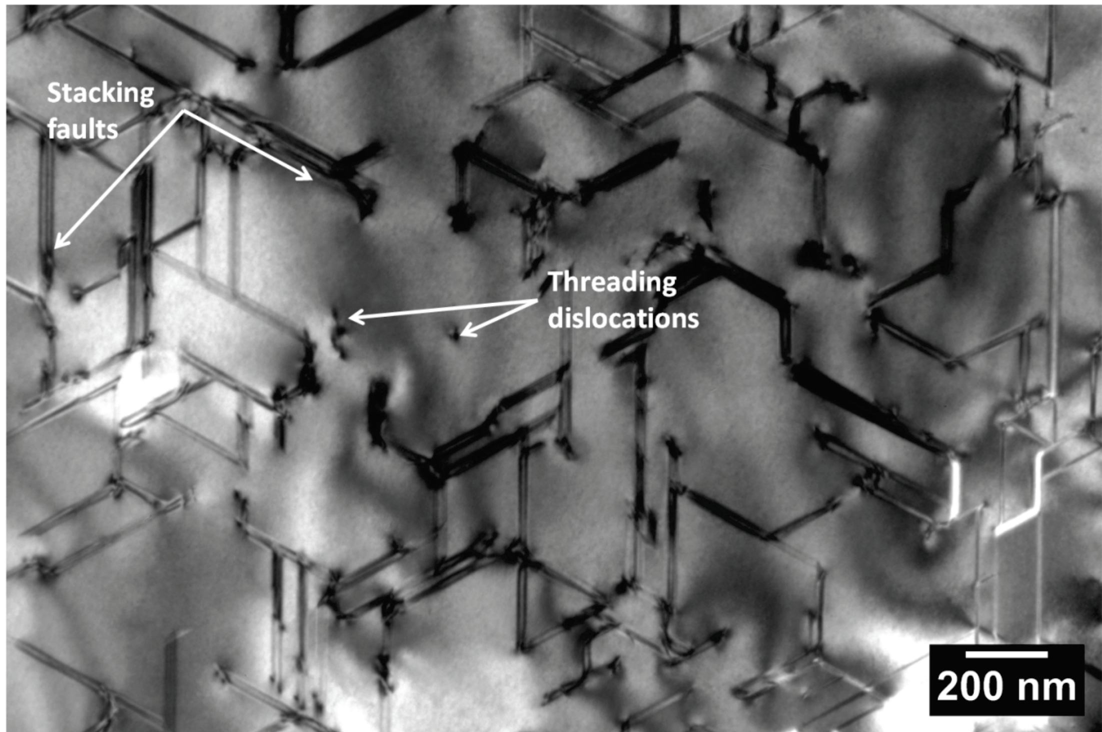


Figure 4-14 Typical plan view TEM image of HT layer on 70 nm seed layer. A dense network of stacking faults can be seen blocking each other and pinning the threading dislocations around them.

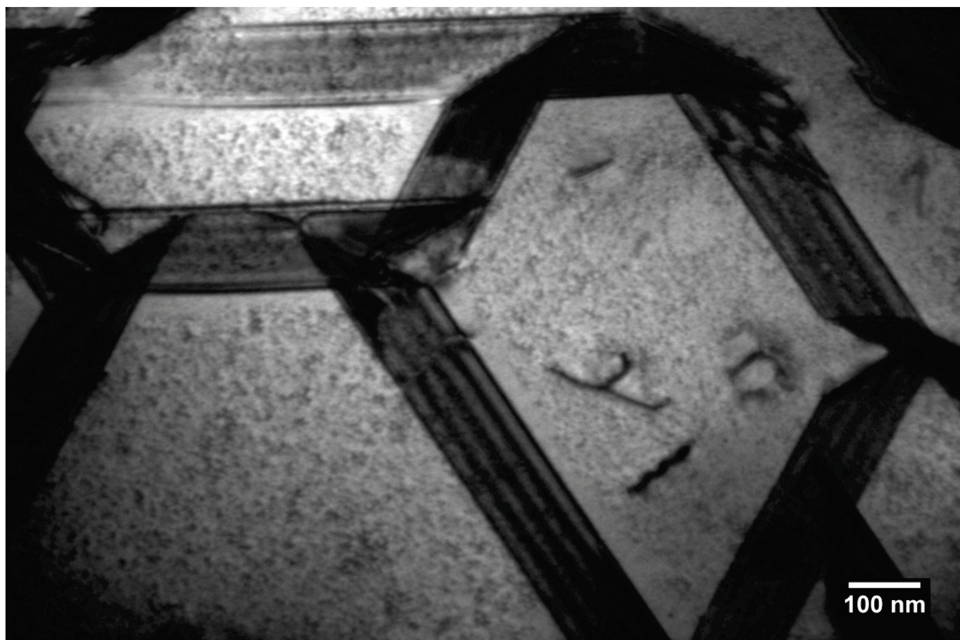


Figure 4-15 A close up image of the stacking fault network observed for HT layer grown on 70 nm seed.

For Ge layers grown directly on (100) Si substrate, where the majority of defects reaching the surface are threading arms of misfit dislocations, the TDD can be further reduced by post growth annealing at high temperature. The same does not apply for Ge layers grown on (111) Si substrate. High temperature *in-situ* annealing did not seem to be able to reduce the defect density in these layers with stacking fault densities estimated at ~ 1.5 x 10^9 cm^{-2} for HT-a1 and HT-a1 (A). There was still a significant proportion of stacking faults observed under cross-sectional TEM of the annealed structure of sample HT-a1 (A) (figure 4.16). The same can be said for sample HT-a2 (A) and HT-a3 (A) with their SFD estimated at 8.5 x 10^8 cm^{-2} and 1 x 10^9 cm^{-2} respectively.

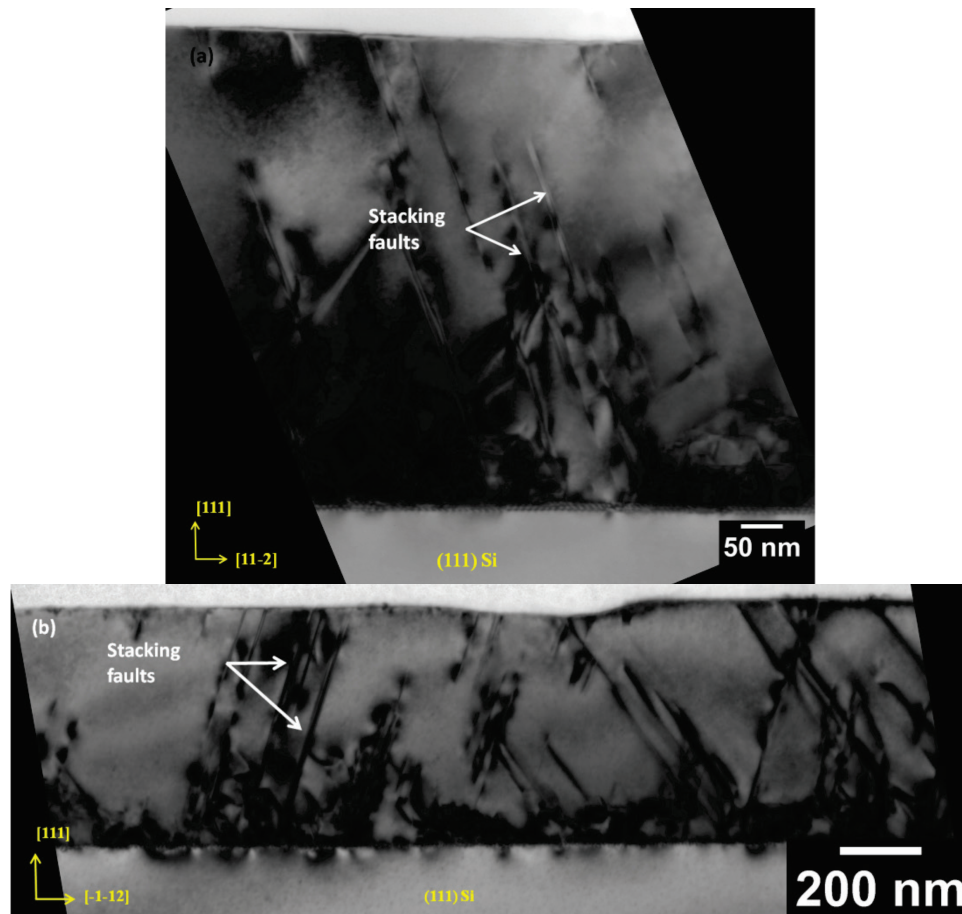


Figure 4-16 Cross sectional TEM of : (a) sample HT-a1 , (b) sample HT-a1 (A) with post growth annealing at 830 °C showing no improvement in defect density compared to the unannealed structures.

A series of TEM images using different diffraction conditions have been taken to find out the invisibility criterion of the stacking faults and its associated partial dislocations. The diffraction conditions examined include **g** values of: 022, 0-22, 222, 2-22, 311, 331, 400 and -400. Images for these conditions show slightly different contrasts from one another with only the **g** = 222 condition giving a complete disappearance of the stacking faults and partials (see figure 4.17). Using the images, **g . b** analysis have shown that the Burgers vectors for the partials bounding the stacking faults are of the type : 1/6 [-12-1] and 1/6 [11-2]. These Shockley partial dislocations were dissociated from ½ [01-1] type of 60° dislocation.

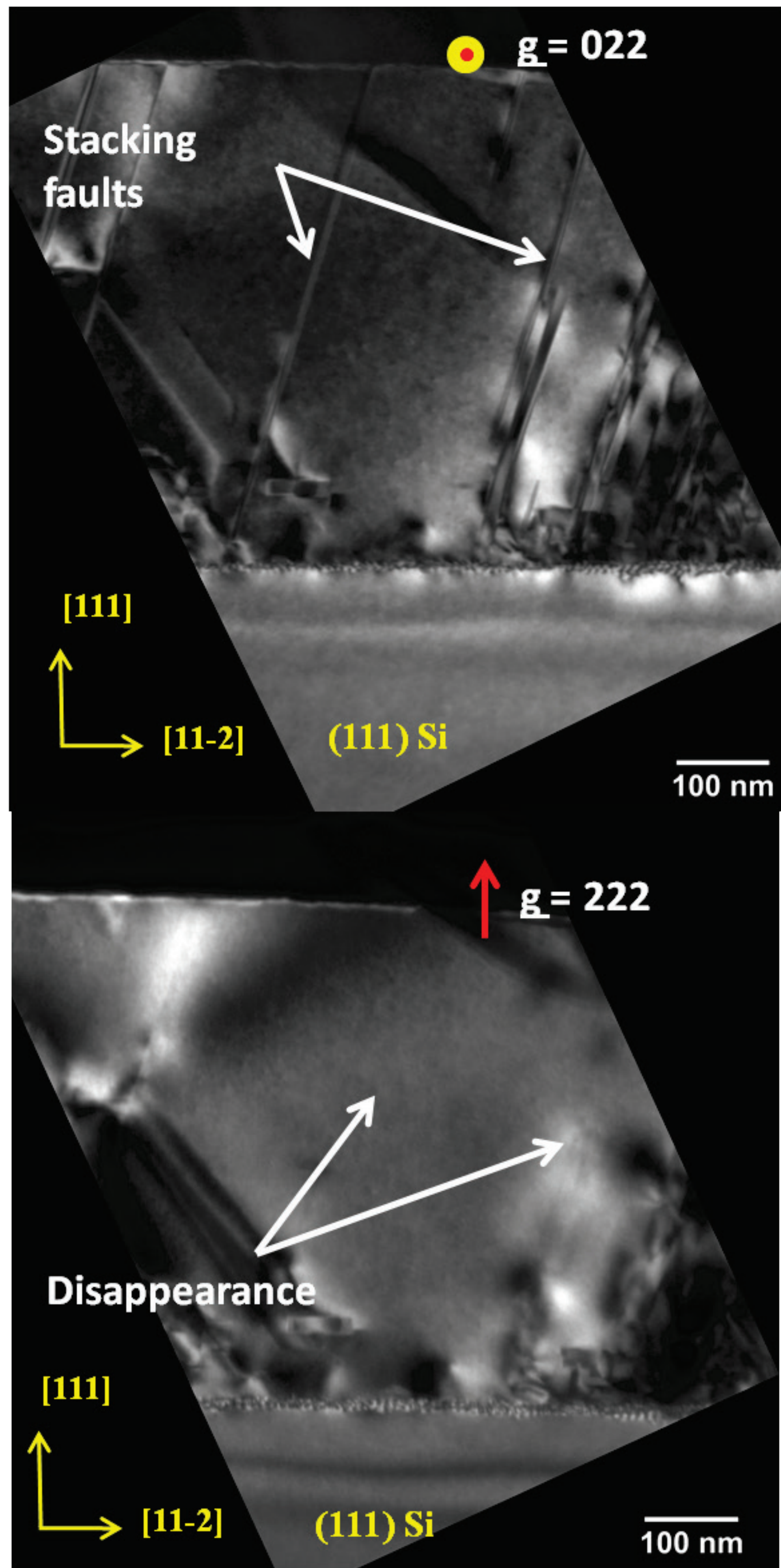


Figure 4-17 Dark field TEM Images of HT-a1 (A) taken using two different diffraction conditions: (top) g = 022, showing the "normal" network of stacking faults; (bottom) g = 222, showing the disappearance of these stacking faults due satisfaction of the g . b = 0 invisibility criterion.

However, when the thick HT Ge layer is grown on the thin 10nm seed (HT-a4), no extended stacking faults can be observed under cross-sectional TEM for this layer. Instead, the majority of defects appear to be confined to a region ~ 100 nm from the Ge/Si interface. There are occasional threading dislocations observed to scatter within the layers (figure 4.18a). The surface looks to be smooth, and free of defects, which is desirable for device fabrication. There are also regions below the Ge/Si interface where Si seems to have out diffused and now contains Ge.

This layer was also annealed at 830 °C (HT-a3 (A)) but the observation of changes in microstructure and defect density is minimal in cross-sectional TEM where no stacking faults can be seen (figure 4.18 b). The thickness of the HT layers was calculated to be ~ 460 nm. This thickness is slightly less than that of the HT layers grown on 70 nm seed at ~ 500 nm even though both samples were grown with identical deposition time at 410 s. This could be due to the difference in initial growth of the high temperature layer where the seed layers of various thicknesses form islands and coalesce differently (see section 4.5).

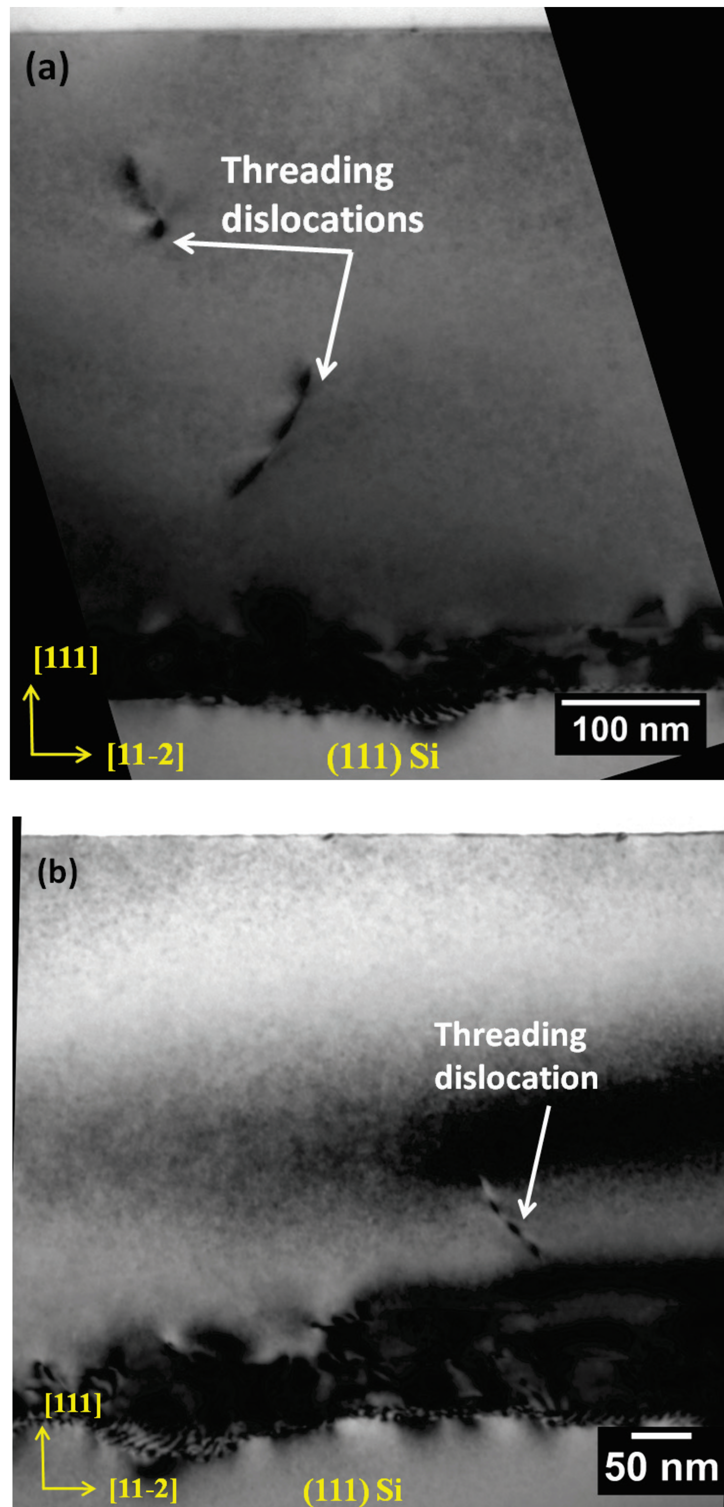


Figure 4-18 Cross sectional TEM of ~ 460 nm HT layer on 10nm seed layer: (a) unannealed, (b) annealed. The layers look to be entirely devoid of stacking faults/twins, only a few threading dislocations can be seen scattered within the layers. The majority of defects can be seen to be confined within ~ 100 nm of the interface.

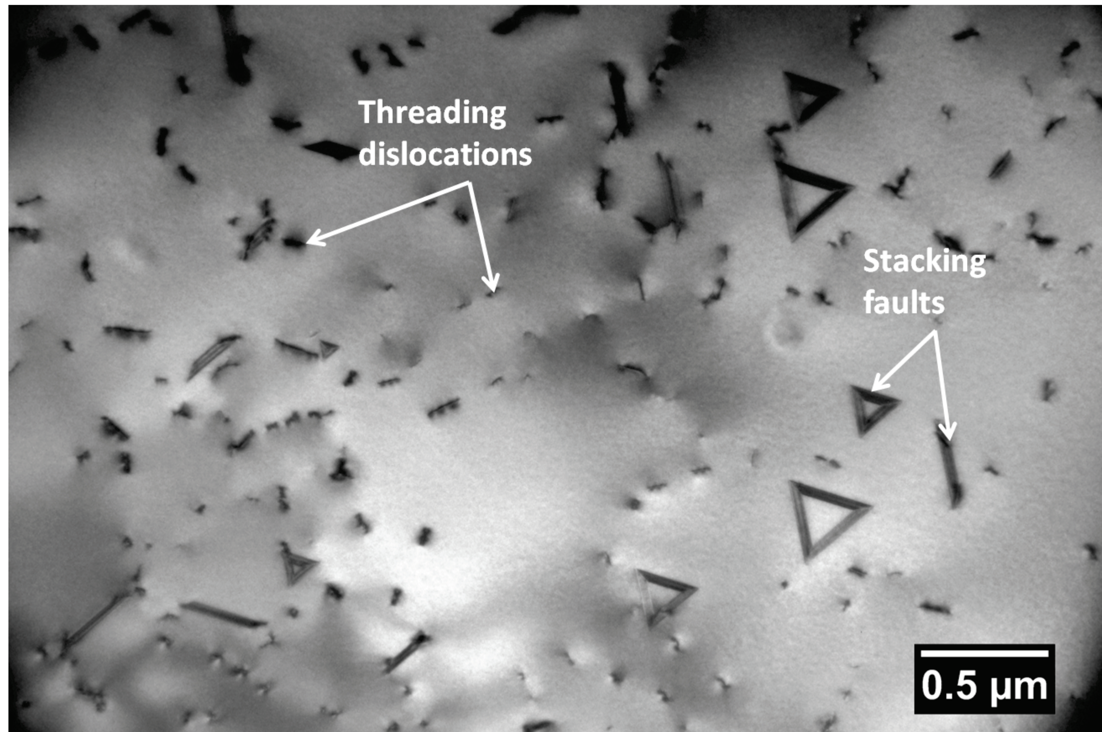


Figure 4-19 Plan view TEM of ~ 460 nm HT layer grown on 10nm seed without annealing. The sample reveals several stacking faults within the ~ 12 μm^2 area of the image indicating a very low density. The majority of defects is threading dislocations.

These layers were also examined by plan-view TEM to further study the dislocation and stacking fault network near the surface. For the HT Ge layer grown on the 10 nm seed without annealing, there are several stacking faults that can be seen under plan-view TEM that were not seen in cross-sectional TEM (figure 4.19). Threading dislocations can also be seen penetrating the layer in random directions with TDD ~ 6.1 x 10^8 cm^{-2}. The density of the stacking faults (SFD) was calculated to be ~ 8.1 x 10^7 cm^{-2}. The stacking faults here were treated as individual features and were not calculated as line density.

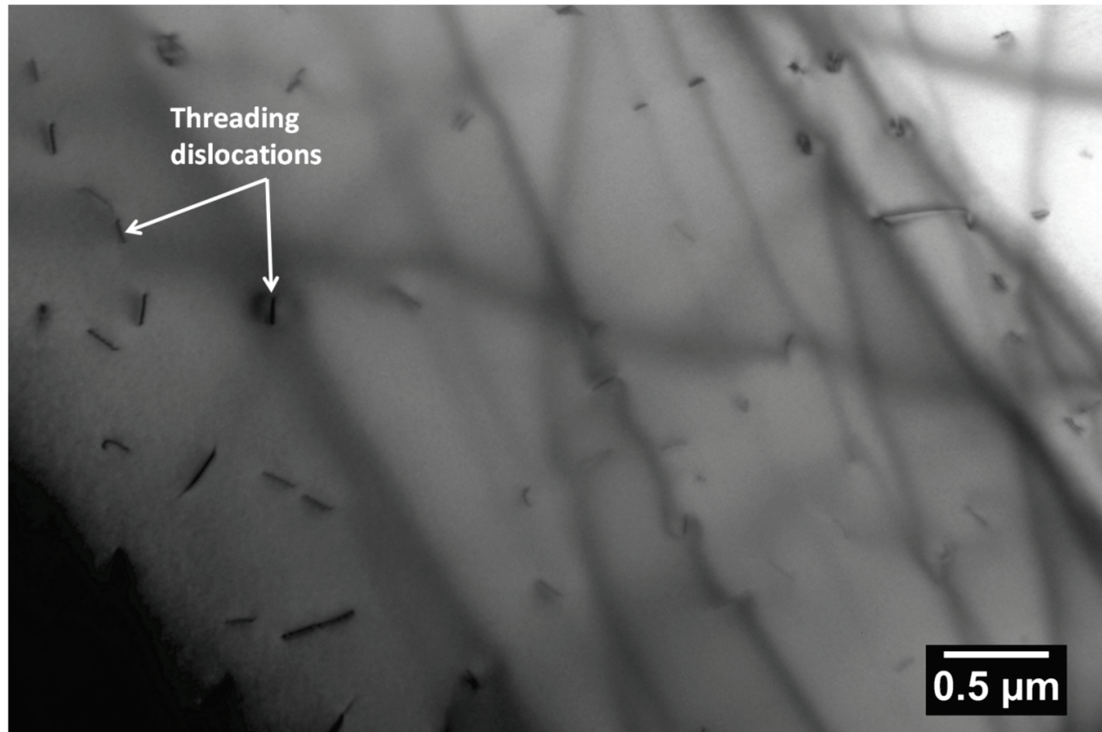


Figure 4-20 Plan view TEM of ~ 460 nm HT layer grown on 10nm seed after *in-situ* annealing. The sample shows exclusively the appearance of threading dislocations indicating a density < 10^7 cm^{-2} for stacking faults.

The plan-view TEM image of the annealed layer is shown in figure 4.20. Several images were taken with the sample and none showed any presence of stacking faults within the layer. One immediately sees the significant changes in the density of stacking faults as it drops from ~ 8.1 x 10^7 cm^{-2} to ~ <10^7 cm^{-2} (the detection limit of PVTEM) following annealing. The TDD also drops from ~ 6.1 x 10^8 cm^{-2} to ~ 2.0 x 10^8 cm^{-2} as thermal assistance promoted dislocation gliding and enhanced the annihilation of threading dislocations.

HT Ge layers of ~ 900 nm thick with and without annealing, HT-a5 and HT-a5 (A), have also been grown on this 10 nm LT Ge seed to see if there is a significant change in defect density of the buffer. However, PVTEM analysis of both unannealed and

annealed structures give TDD value almost matching those for the ~ 460 nm thick HT layers with no presence of stacking faults.

Figure 4.21 plots the estimated SFD of the annealed HT layers against the seed thickness that they were grown on. One can immediately see the significant change in SFD for the buffer grown on the 10 nm seed.

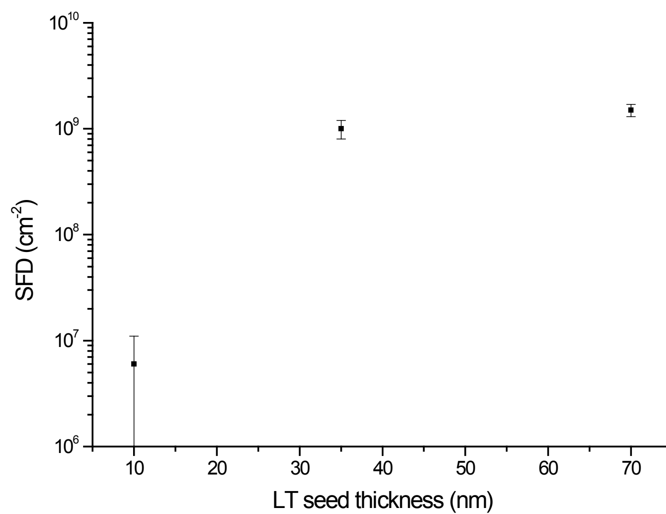


Figure 4-21 Plot of estimated stacking fault density of the HT layers versus the seed thickness that they were grown on.

4.4.2 Surface morphology

AFM images of the HT Ge layers grown on the 70 nm seed revealed very rough surfaces with rms values at 20.5 nm (Z-range: 200 nm) and 22.5nm (Z-range: 220 nm) for HT-a1 and HT-a1 (A), respectively, compared to the original seed layer rms of 12 nm. Typical 10x10 µm scans of the layers are shown in figure 4.22.

It can be seen that the short range undulations that were observed for LT seed layers have disappeared. The morphology now have longer range wavelength at ~ 1.5 µm compared to the seeds (figure 4.23).

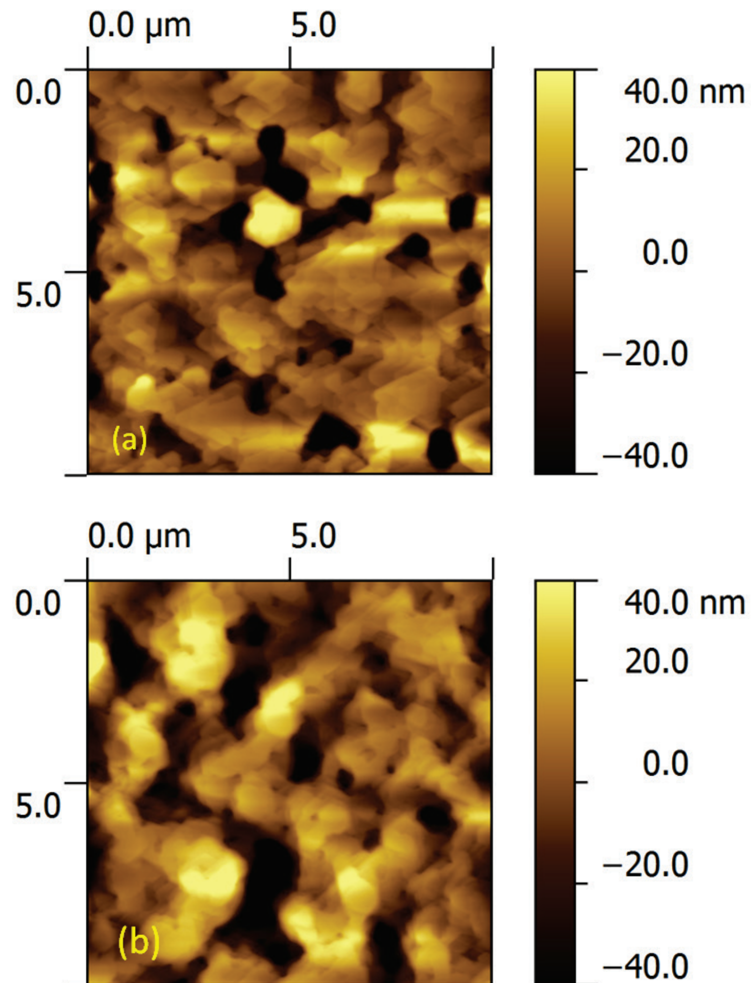


Figure 4-22 AFM images of thick 500 nm Ge layer grown at 670°C on 70 nm seed : (a) unannealed HTa1 and (b) annealed HTa1 (A).

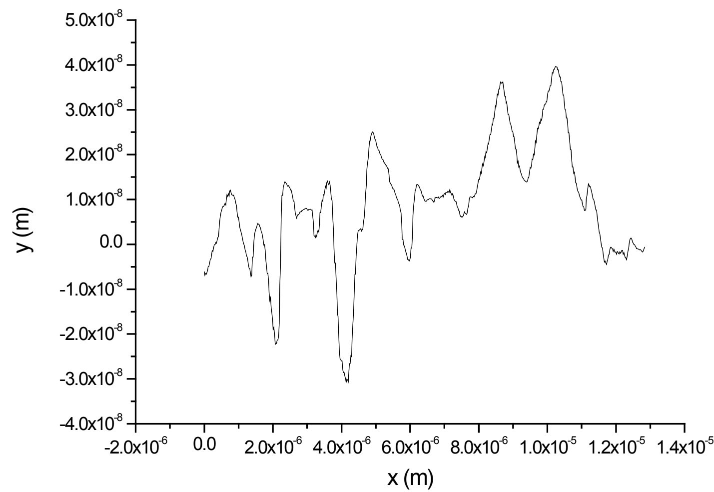


Figure 4-23 A plot of a line section through an AFM scan of sample HT-a1 showing the typical long range wavelength of HT Ge layers grown on the 70 nm seed.

The surface roughness was very similar for unannealed and annealed layers. The surface features also remained the same, confirming the insignificance of thermal assistance in the reduction of stacking faults density. Surface features on these layers included large (~ 1 µm across) irregular dark features and did not appear to have any crystallographic orientation. Apart from these dark features, the surface could be seen to have terraces with edges that orientate in similar directions with stacking faults observed in plan view TEM of these samples. These features could be attributed to the surface steps caused by surface penetration of the stacking faults (figure 4.24).

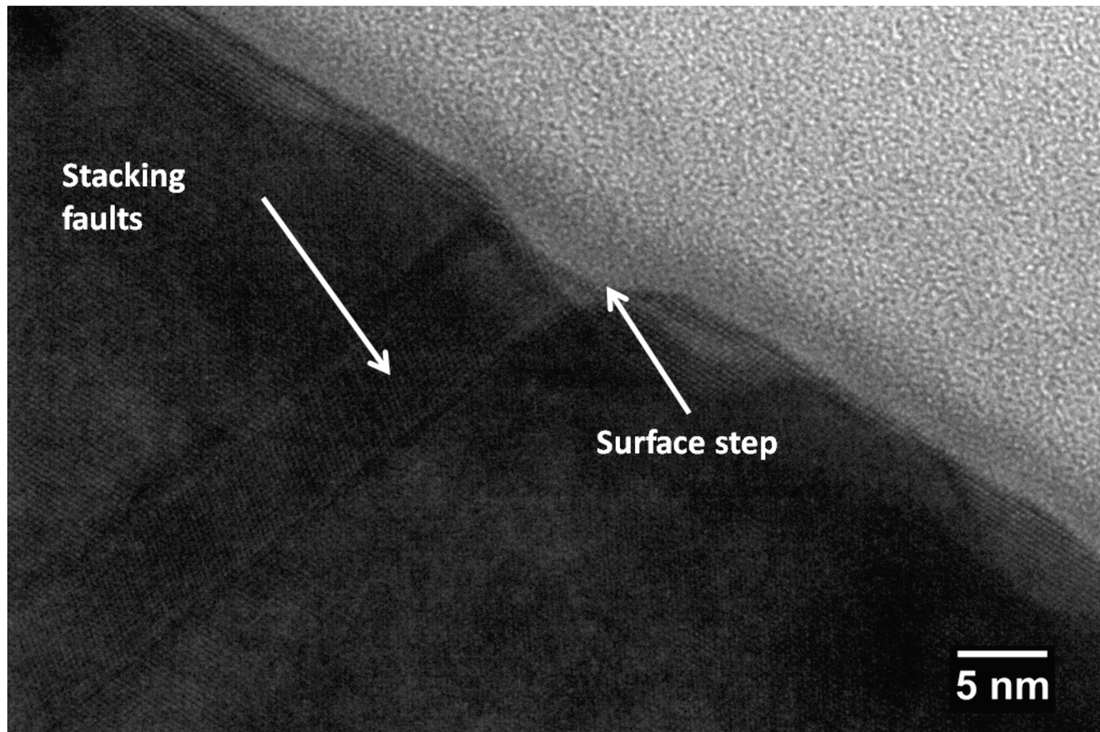


Figure 4-24 Cross sectional TEM image of a stacking fault penetrating the surface and creating a surface step which contributes to the overall roughness of the layer.

For HT Ge layers grown on the 35 nm seed, the surface was a lot smoother with rms values measured at 2.3 nm (Z-range: 11 nm) and 2.7 nm (Z-range: 20 nm) for HT-a3 and HT-a3 (A) respectively. Even though the surface was smoother, the morphology was still similar to that of the HT layers grown on the 70 nm seed. Figure 4.25 shows an AFM scan of sample HT-a3 revealing terraces with the same shaped-edges as HT-a1. This is expected as both these sets of samples suffered from high densities of stacking faults.

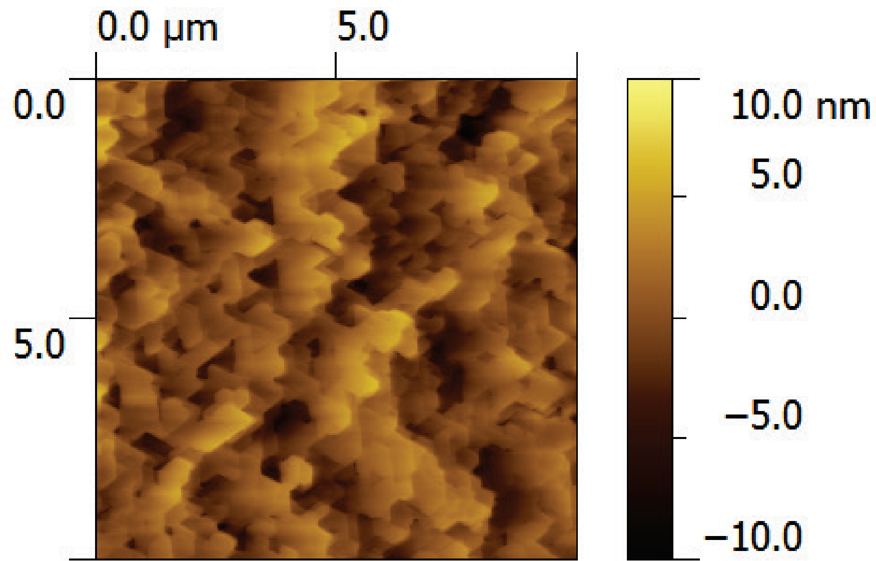


Figure 4-25 Typical AFM image of 500 nm HT layer grown on 35 nm seed, HT-a3.

There were significant differences in the surface morphology of thick Ge HT layers grown on the 10 nm seed compared to those grown on the 70 nm and 35 nm seeds. The surface appeared to show a set of regular wavy striations with no dark pits observed. The rms roughness was also smooth at 3 nm (Z-range: 20 nm) and 2.1 nm (Z-range: 18 nm) for unannealed and annealed samples HT-a4 and HT-a4 (A) respectively (figure 4.26). For the ~ 1um thick HT layers, HT-a5 and HT-a5 (A), the rms roughness improved further to ~ 1.7 nm (Z-range: 7 nm) and ~ 1.3 nm (Z-range: 5 nm) respectively. This level of surface rms “smoothness” is comparable to layers grown by MBE surfactant mediated epitaxy [82] and approximately thirty times less rough than those grown by CVD [80] reported in literature.

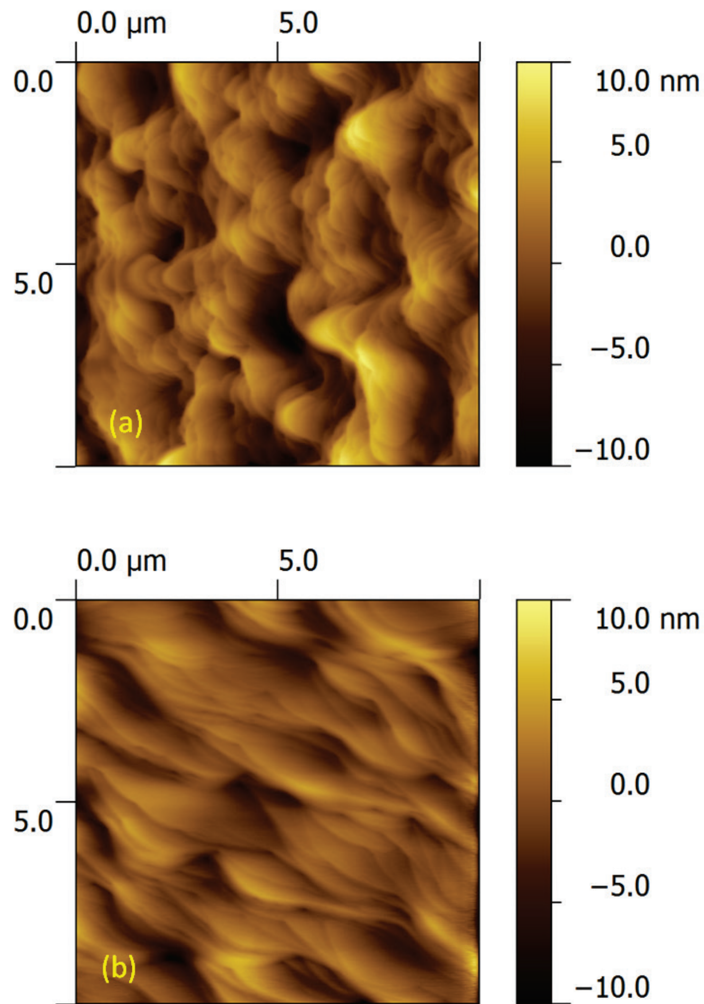


Figure 4-26 AFM images of (a) unannealed and (b) annealed HT layer grown on 10nm seed.

For HT layers grown on the 70 nm and 35 nm seeds, thermal annealing actually slightly increased the rms roughness of the layers (figure 4.27). On the contrary, there was a drop in rms roughness after annealing for HT-a4 (A) and HT-a5 (A) confirming that the majority of defects in these layers were threading dislocations which were effectively reduced after thermal annealing.

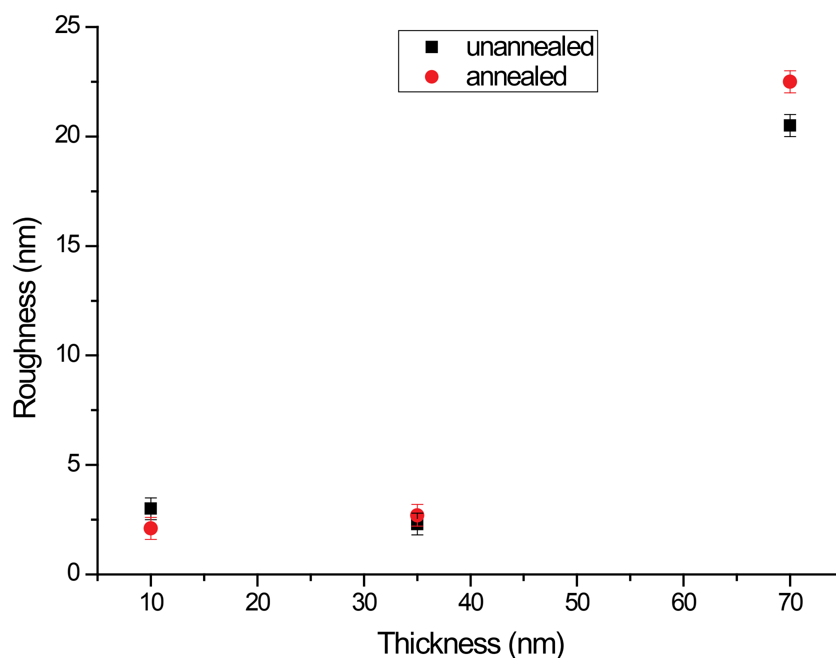


Figure 4-27 A plot showing the rms roughness of ~ 500nm HT Ge layers grown on three different seed thicknesses along with the annealed layers.

4.4.3 Relaxation

X-ray diffraction measurements were also performed on all the HT thick Ge layers and it was confirmed that the layers are monocrystalline and fully relaxed (figure 4.28). In fact, the Ge layers were found to be slightly over-relaxed with respect to the Si substrate. All the layers have similar relaxation values of ~ 103 – 104 % indicating that the layers were under slight tensile strain. This can be attributed to the differences in thermal expansion coefficients of Ge and Si, and is typically observed for Ge layers grown on Si substrates [96].

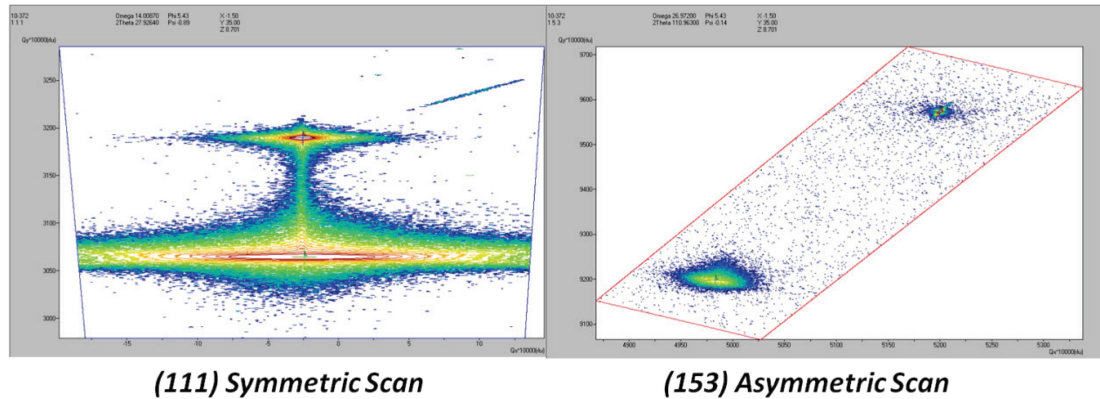


Figure 4-28 A typical RSM of a thick HT Ge layer grown on the LT Ge seed showing relaxation value ~ 103 % w.r.t. Si substrate. The layer is under slight tensile strain.

4.4.4 Etch pit density

Etch pit density measurements were carried out on the samples to try and determine the TDD of the layers more accurately. However, commonly used etchants, including both Schimmel [9, 75] and an Iodine-based etchant [76, 97], did not reveal the presence of defects. These etchants have been proved to reveal defects in a range of materials from Si, SiGe and Ge layers grown on (100) Si substrates; however, it appears that the selectivity is lost when etching the (111) surface. It might have been that the etch rate on the dislocations on (111) orientation is not preferential for these etchants (ie. same as bulk etch rate) leading to the non-observation of pits/ hillocks. Further work is necessary to develop an etchant able to reveal defects in Ge layers on (110) and (111) Si substrates effectively.

4.5 Growth mechanism

This section describes a follow-up work to study the initial growth of the high temperature layer in attempt to explain the growth mechanism involved and the reason for the improvement in buffer quality observed in the previous sections. The samples that were grown for this experiment are listed in table 4.4 below.

Wafer ID *(111)*		**Growth temperature (°C)**	**Deposition times (s)**	**Thickness of islands (nm)**
Name	**ID**			
LT-a1 (A)	11-269	400°C + 670°C anneal	240	30
HT-a6	11-270	400°C / 670°C	240 (LT) + 80 (HT)	115
LT-a3 (A)	12-009	400°C + 670°C anneal	820	70

Table 4.4 Wafers grown for investigation into the initial stages of HT layer growth.

Before the HT layer is grown, the LT layer is exposed to temperature ramping from 400 °C up to 670 °C and kept at the HT growth temperature without Ge deposition for ~ 10 minutes. An *in-situ* annealing experiment of the thin seed (~ 10 nm) layer at 670 °C would represent the growth evolution of the seed as the HT layer is grown. A sample of the LT seed layers was annealed at 670 °C (LTa1 (A)), the growth temperature of the HT layer, for ~ 7 minutes without any additional Ge deposition to investigate the changes in surface morphology and layer structure (LT-a1 (A)).

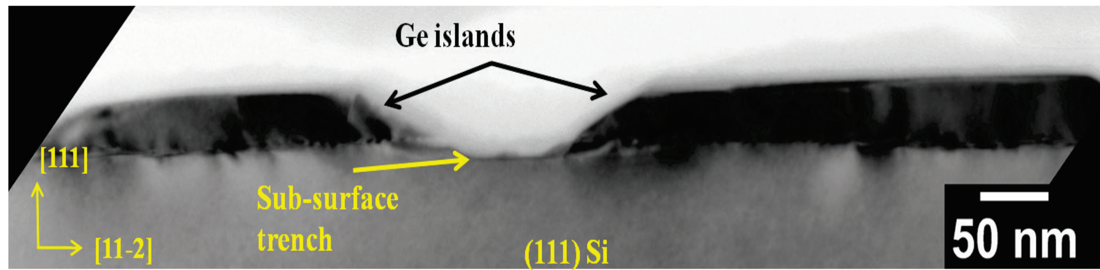


Figure 4-29 Cross sectional TEM image of (111) seed layers after in-situ annealing at 670 °C. Ge islands have formed from the partially strained layer due to mass transport. Formation of sub-surface trenches results from the out-diffusion of Si atoms.

The thin (~10nm) seed still had residual strain left in the layer and *in-situ* annealing has transformed the continuous layer into 3D islands (see figure 4.29). The island formation due to the thermal assistance is similar to the report by Kovacevic [98]. Upon subsequent annealing of Ge layer on Si, self-assembled growth of nanostructures Ge islands on the Ge layer occurred. This effect has also been seen in other systems when mass transport from the grown layer under strain resulted in 3D islanding [99-102]. The side facets of the island are at angles of ~ 29.3° with the (111) growth plane which correspond to {113} surfaces. This is the preferential growth surface, as the growth rate on (113) is higher than that for the (111) surface [83]. This will lead to the HT Ge layer being deposited in between the island faster than on the top surface which should eventually lead to a smoother layer. The islanding of the Ge layer also leads to "trenches" in the Si substrate between the Ge islands [103, 104]. These trenches/voids can be seen to be below the Ge/Si interface (see figure 4.29) and could be caused by the out-diffusion of Si atoms due to the redistribution of substrate material in high stress regions [105]. Additional AFM analysis showed that many of these islands had coalesced and were not well aligned to any crystallographic direction (figure 4.30). The islands were calculated to cover ~ 60% of the surface area.

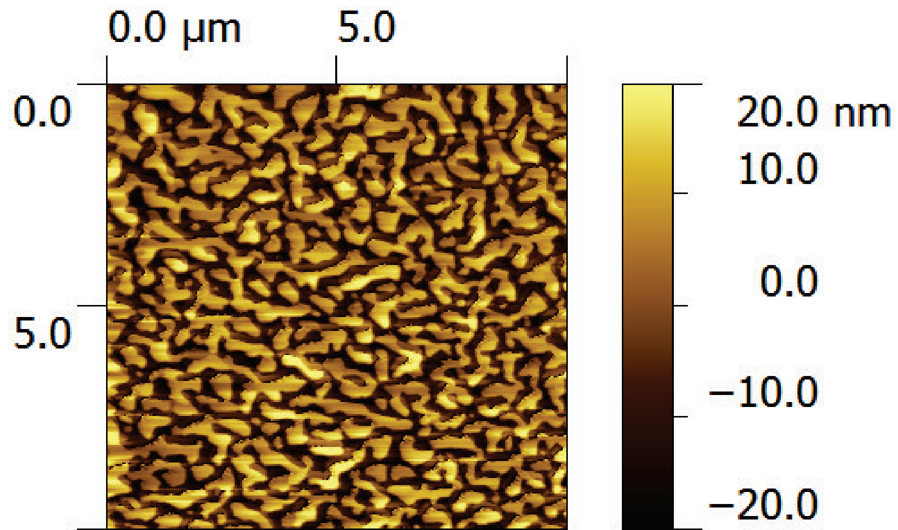


Figure 4-30 AFM image of the 10 nm Ge seed annealed at 670 °C showing elongated islands formation with {113} sidewall facets.

A thin deposit (~ 100 nm) of HT Ge was grown on the 10 nm seed layer to investigate the initial growth of high temperature Ge layer on this thin seed (HT-a6). Figure 4.31shows a TEM image of the buffer structure after deposition of ~ 100 nm HT Ge. The deposition of HT Ge has resulted in lateral growth of the Ge islands which were originally located on the sides of the sub-surface trenches. The trenches now have grown-in Ge and are several times deeper compared to the annealed LT seed layer only indicating that the Si out diffusion process continues during the initial growth of HT Ge.

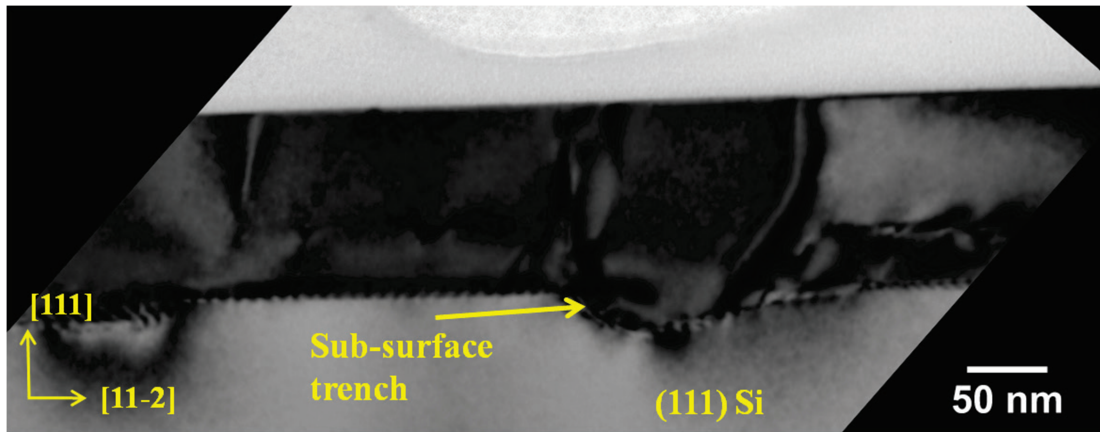


Figure 4-31 Cross sectional TEM image of thin (~ 100 nm) HT Ge grown on the 10 nm Ge seed.

The higher growth rate on {113} surfaces than on {111} has led to a smoothing effect as the subsequent HT Ge is deposited [106]. There are a few threading dislocations that can be seen within the layer which can annihilate during the continued growth of thicker (~ 500nm) HT Ge or the final post-growth anneal. At this point, most of the islands from the 10 nm seed have coalesced covering ~ 81% of the surface area (figure 4.32).

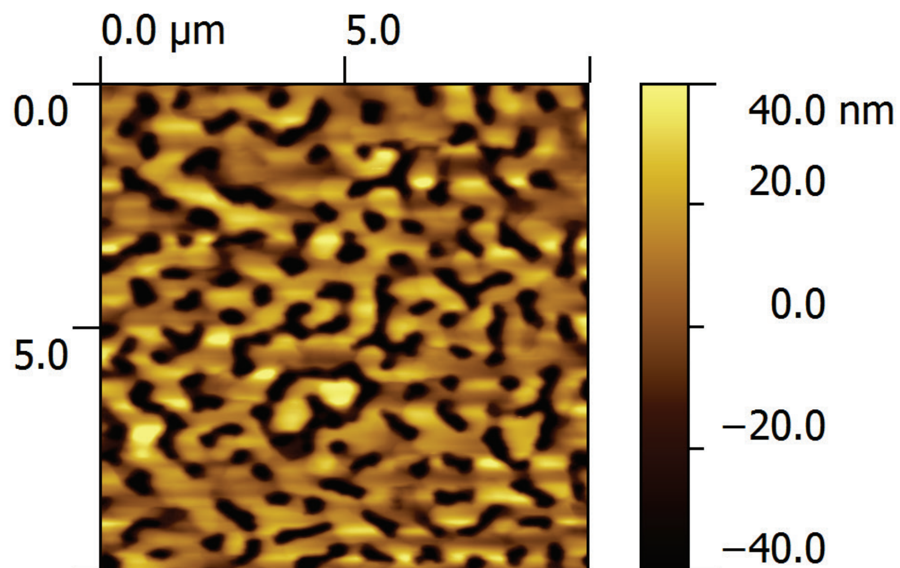


Figure 4-32 AFM plot of ~ 100 nm of HT Ge grown on the 10 nm seed showing the islands starting coalesce at the initial stage of thick HT layer growth.

Sample LT-a3 (A) had the thicker 70 nm seed that was measured to be ~ 97.9% relaxed, so the amount of residual strain was a lot less than for the 10 nm seed layers just discussed. Thus, after annealing at the growth temperature, sample LT-a3 (A) did not show any islanding (figure 4.33) . This is the main difference compared to the 10 nm seed and might be the reason why stacking faults could not annihilate during the initial stage of HT layer growth leading to a high SFD for HT layers grown on the 70 nm seed.

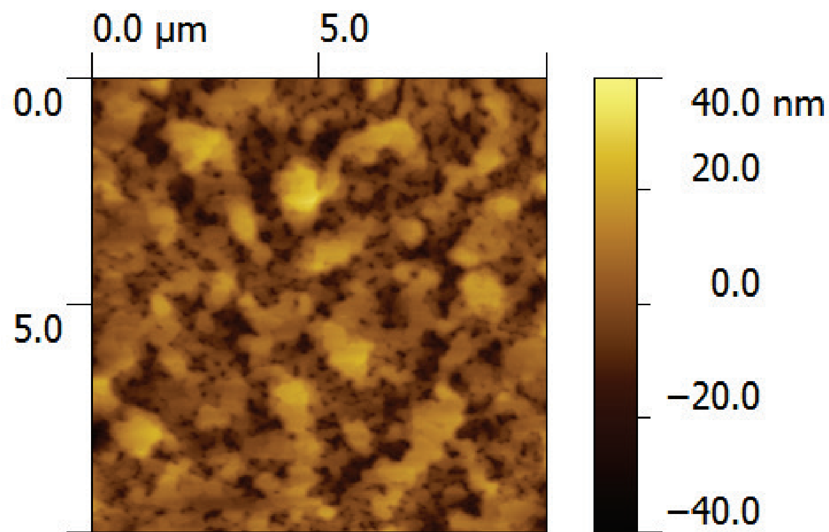


Figure 4-33 AFM scan of the 70 nm seed after annealing at 670 °C, the HT growth temperature, showing the lack of islanding leading to a high density of stacking faults observable in the HT layers grown on this seed.

Figure 4.34 shows a schematic overview of the main steps in the growth mechanism of thick Ge layers grown on (111) Si substrate by RP-CVD that give rise to the high quality of the buffer (lower stacking fault density, lower TDD and smoother surface).

(a) Initially, the LT Ge seed partially relaxes via the formation of misfit dislocation (⊥) at the Ge /Si interface with several threading arms penetrating the surface.

(b) The residual compressive strain in the seed drives the formation of large dome-shaped islands and creates sub-surface trenches in the Si substrate, which can act as a

source of dislocation nucleation and, most importantly, can promote dislocation annihilations within the confinement of the islands.

(c,d) After the initial deposition of a HT Ge layer the surface is smoothened and mobile dislocations annihilate leading to a lower TDD density. The coalescence of the island also lead to further dislocation annihilation as the dislocations previously reached the sidewalls of the islands have now met with those from neighboring islands.

(e) After a significant thickness of HT Ge deposition the lower growth rate on the (111) surface and adatom mobility to minimize the surface energy eventually leads to a completely smooth surface.

This growth process will be less likely to occur in the thicker seed layers due to less residual compressive strain to drive the initial islanding process in the seed layer. Also, there wouldn't be many individual islands and trenches as it would need a much larger energy to form such high aspect ratio islands due to the initial thickness of the seed. Therefore, this would mean the strain-relieving dislocations will not be well confined and have a much lower annihilation probability, resulting in highly defective buffers such as those in figures 4.11, 4.12.

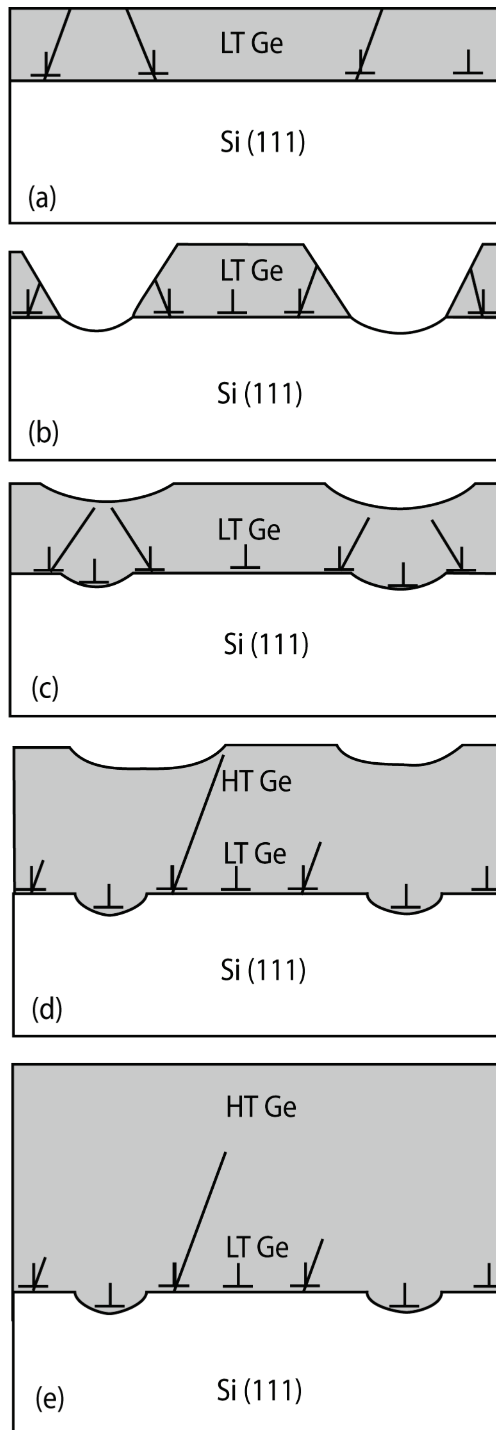


Figure 4-34 Schematic of the growth mechanism involved for thick relaxed Ge layers grown on (111) Si substrate by RP-CVD. (a) initial seed layer, (b) island formation due to thermal annealing at 670 °C growth temperature, (c) coalescence of islands leading to further dislocation annihilation, (d) continued growth of HT Ge layer, (e) smooth final buffer achieved due to preferential growth rates.

4.6 Comparison with related work

Technique	Substrate Orientation	Total Ge Thickness (µm)	Relaxation (w.r.t. Si substrate) (%)	RMS Roughness (nm)	TDD (cm^{-2})	Stacking Fault Density (cm^{-1})	Ref.
Surfactant-mediated MBE	111	1.0	102	Not reported	$\leq 10^7$	Very low density	[107]
RP-CVD	111	2.5	106	40 - 50	2×10^9	High density, visible in XTEM	[80]
RP-CVD	100	4.7 2.5 1.1	102 105 104	0.44 ~ 1 0.7	7×10^5 6×10^6 1×10^7	None None None	[108] [109] [93]
RP-CVD	111	~1.0 ~ 0.5	~103	1.3 2.1	3×10^8	Very low density, not visible in PVTEM ($<1 \times 10^7$)	This work

Table 4.5 Comparison of the quality of the Ge buffer investigated in this work with previously published literature.

Table 4.5 summaries this work in comparison with published literature that is closely related. A very important parameter of a Ge buffer is the thickness. This determines the deposition time needed and the amount of material used during growth which ultimately affects the cost and ease of integration. Thus the buffers need to be as thin as possible without compromising the quality. A lot of groups have tried to grow thicker buffers in order to reduce TDD as thicker buffer induces more dislocation annihilation and thus lower TDD. This is demonstrated by the work using RP-CVD on (100) Si substrate listed in table 4.5. Compared to previously published results [80], the layers this work have achieved ~ 40 times smoother surface, ~ 1 decade reduction in TDD value and have almost completely suppressed the formation of stacking faults in a Ge layer that is 2.5 times thinner. The TDD value of

these layers are not quite as low as those achieved by surfactant-mediated MBE (TDD value ≤ 1×10^{7} cm^{-2}) which represent some of the highest quality (111) Ge layers ever reported [107]. However, surfactant-mediated MBE grown layers suffer from incorporation of dopants into the layer surface so while these layers may be structurally superior they are electrically inferior and would not be feasible for device fabrication.

Other techniques that have been investigated for growth of Ge layers (111)-oriented Si substrates, not listed in the table, include: aspect ratio trapping (ART) and epitaxial lateral overgrowth (ELO) [89, 90] which is also quite common in III-V growth [91]. However, these techniques require selective growth using masks such as SiO_2 to promote dislocation annihilations onto the sidewalls and are very difficult to integrate into mass production required for commercial devices.

4.7 Summary

In this work, we have demonstrated an approach to grow thick, high quality relaxed Ge layers on (111) Si substrate by RP-CVD using a low temperature/ high temperature technique. The LT Ge seeds grown contained a high density of stacking faults and twins resulting from the lattice mismatch of Ge and Si along with the opposite gliding sequence of Shockley partial dislocations compared to (100) orientation. The roughness of these seed layers increased significantly as its thickness increased. The seed layers were all under partial compressive strain and the strain approached full relaxation as the layer increase in thickness.

Thick HT Ge layers grown on the “thicker” 35 nm and 70 nm seeds exhibited a high density of stacking faults and threading dislocations ($\geq 10^9$ cm^{-2}) penetrating throughout the buffer which is quite typical for (111)-oriented growth. The surface steps created by the stacking faults also add to the high surface roughness of these samples (up to ~ 22 nm rms).

However, the residual compressive strain in a thin (~ 10 nm) LT seed results in the HT layer growth proceeding via an intermediate islanding step that serves to promote dislocation annihilation. The threading dislocation density was reduced to ~ 3×10^8 cm^{-2} and almost entirely suppressed the formation of stacking faults. The higher Ge growth rate on the {113} sidewalls of the islands than on the {111} top surface resulted in a smoothing effect that led to a low value of rms surface roughness of ~ 1.3 nm.

The results represent a significant enhancement in the overall quality of (111) relaxed Ge layers grown by an industry compatible RP-CVD process.

5 Relaxed Ge buffer on (110) Si substrate

Following the previous Chapter discussing (111) growth for enhancement of electron mobility, this Chapter will address the (110) orientation with regard to improved hole transport. Hole mobility enhancement is predicted to be highest with (110) substrate orientation so the need for a high quality buffer grown on a (110) Si substrate is of major importance [110, 111]. Record hole mobility of 725 cm^2/Vs has been reported on a Ge pMOS with improved passivation layers [9] (see section 4.1). Numerous papers have reported on the growth of $Si_{1-x}Ge_x$ / Ge on (110) Si substrates using different techniques including CVD [80] and surfactant mediated epitaxy by MBE [85]. Growth of lattice mismatch Ge on (110) Si substrate suffers from the same problem as those grown on (111) oriented surface (section 4.1 for epitaxial challenges). This chapter will present the result of the growth of Ge on (110) Si substrates by reduced pressure chemical vapour deposition using the low temperature seed / high temperature thick layer approach and subsequent effects of adjusting the seed layer growth parameters.

5.1 Experimental details

All the samples that were used in this study were grown on (110) Si substrates by RP-CVD in the exact growth conditions provided in section 4.2. The low temperature/ high temperature growth method has also been employed in a similar manner (see figure 4.1).

All the experimental techniques used for this chapter are the same as those reported in the previous chapter (see section 4.2) including TEM, AFM and HR-XRD.

5.2 Growth of low temperature Ge seed layers

5.2.1 Microstructure

This section describes the growth of low temperature Ge seed layers on (110) Si substrates. From the previous chapter, it can be seen that the seed layer plays a major role in the quality of the final buffer. Therefore, it is highly likely that the seed will again influence the growth of HT Ge layers on (110) Si. The deposition times for the Ge seed were varied, shown in table 5.1 (LTb-1, LTb-2, LTb-3), to achieve different thicknesses for the layers.

Wafer *(110)*		**Growth temperature (°C)**	**Deposition times (s)**	**Thickness measured (nm)**
Name	**ID**			
LT-b1	11-064	400°C	410	20
LT-b2	10-143	400°C	820	55
LT-b3	10-364	400°C	1640	150

Table 5.1 Deposition times and thicknesses of Ge seed layers grown on (110) Si substrate.

The thicknesses of these layers were measured by cross-sectional TEM operating at 200 kV. All cross-sectional TEM samples were viewed in the <110> direction and in bright field imaging unless otherwise stated. Figure 5.1 shows typical cross-sectional TEM images of samples LTb-1, LTb-2 and LTb-3 grown on a (110) Si substrate. From the TEM images the thicknesses of the LT Ge seed layers were calculated to be: 20 nm, 55 nm and 150 nm for LTb-1, LTb-2 and LTb-3 respectively.

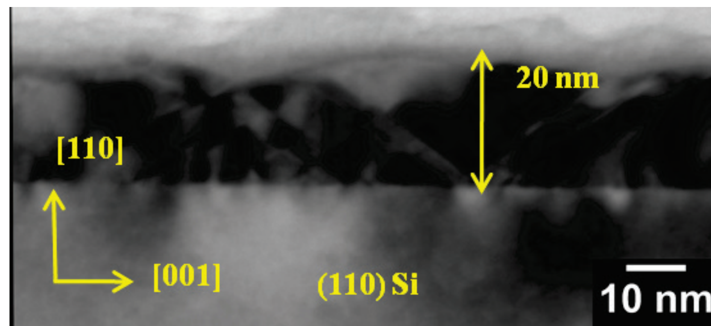


Figure 5-1a Cross-sectional TEM image of 20 nm Ge seed layer grown on (110) Si substrate (sample LTb-1).

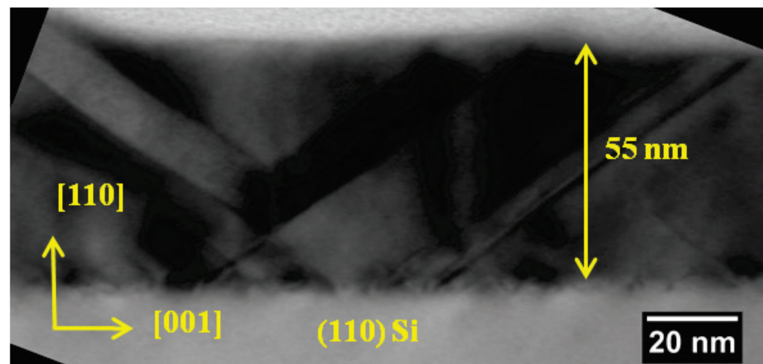


Figure 5.1b Cross-sectional TEM image of 55 nm Ge seed layer grown on (110) Si substrate (sample LTb-2).

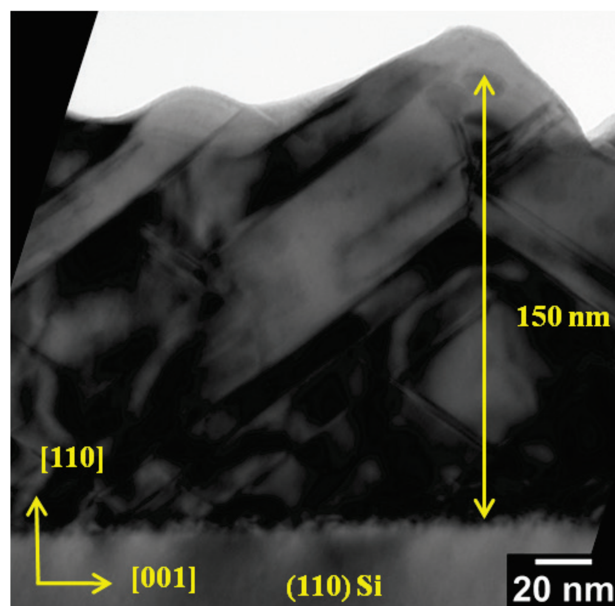


Figure 5.1c Cross-sectional TEM image of 150 nm Ge seed layer grown on (110) Si substrate (sample LTb-3).

The TEM images revealed a high density of stacking faults and twins formed in all the seed layers. The stacking faults lie on two sets of {111} planes, characteristic of (110) growth direction, that are inclined at an angle of ~ 30° to the surface (figure 5.2). The other two sets of {111} planes are oriented at 90° to the surface (see section 2.5) and so dislocations gliding along these planes are not expected to contribute to strain relaxation [112, 113].

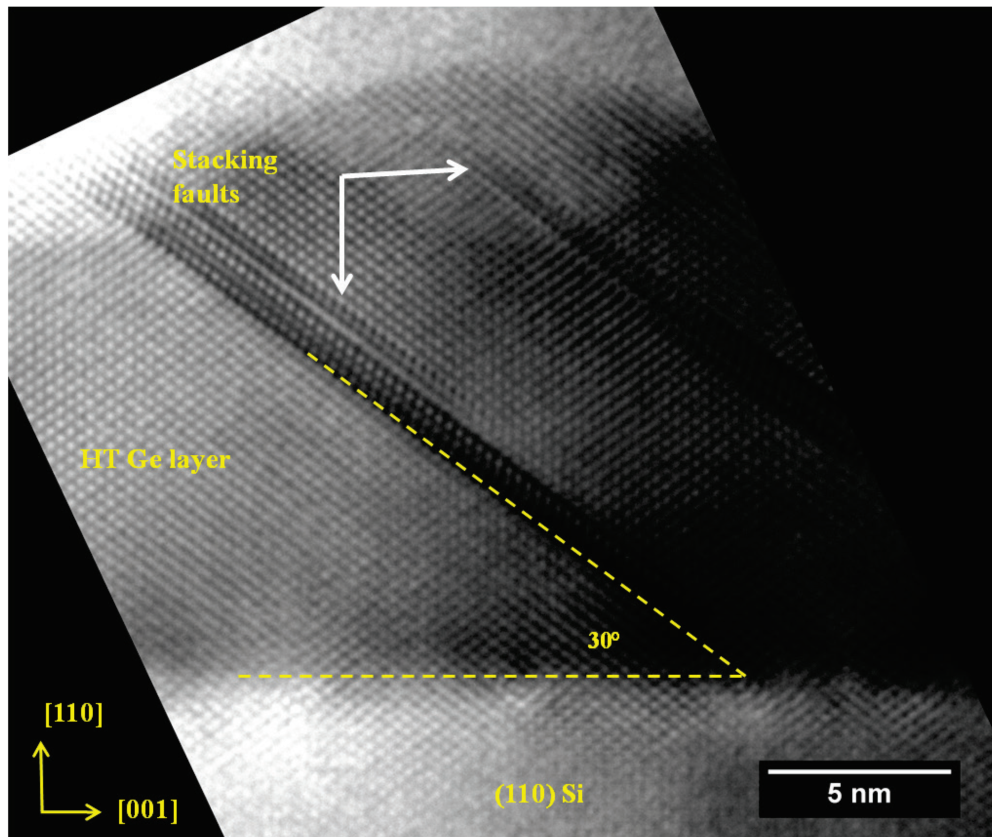


Figure 5-2 A high resolution cross-sectional TEM image of stacking faults in the thin seed, LT-b1.

The high density of stacking faults can also be observed under plan-view TEM in figure 5.3. The plan-view image shows a network of stacking faults that represents the intersections of the {111} glide planes with the (110) growth plane. The inclined stacking faults are seen at an angle to the plan-view top down [-1-10] direction therefore they reveal several fringes. On the other hand, the dislocations that form on

the {111} planes that are oriented at 90° to the surface are seen as faint, narrow lines in figure 5.4. Threading dislocations can also be seen but they are again in very close proximity with the stacking fault network making TDD calculation difficult.

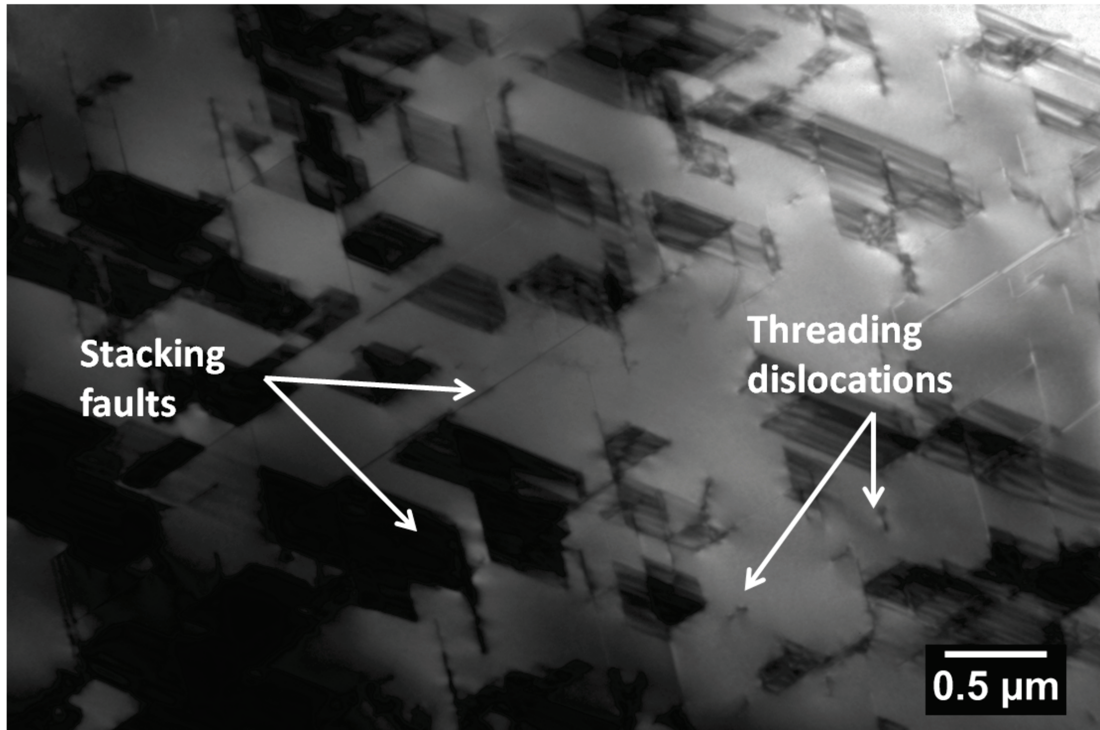
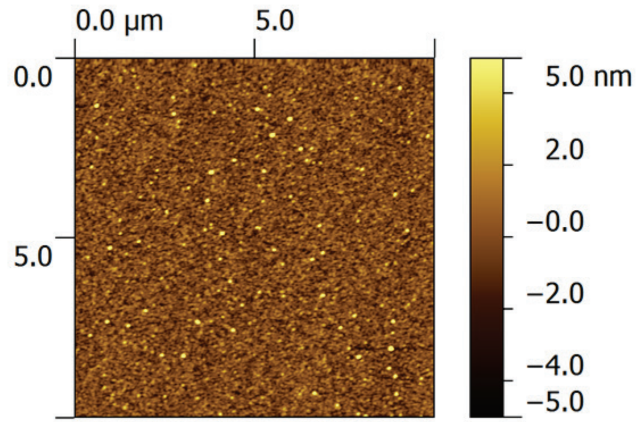


Figure 5-3 Typical Plan-view TEM image of stacking fault lines oriented along the intersections of {111} glide planes with the (110) growth plane. Several threading dislocations appear in close proximity with the dense network.

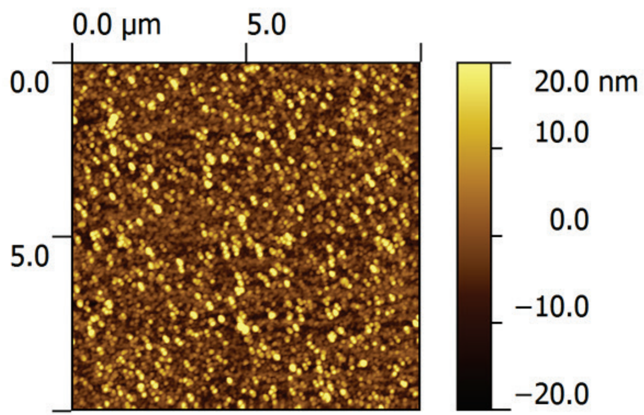
The stacking fault formation can be explained by the same process that occurred for the (111) surface epitaxy. The reverse in gliding sequence of the dissociated Shockley partials compared to (100) orientation has led to the formation of extended stacking faults in these layers.

5.2.2 Morphology

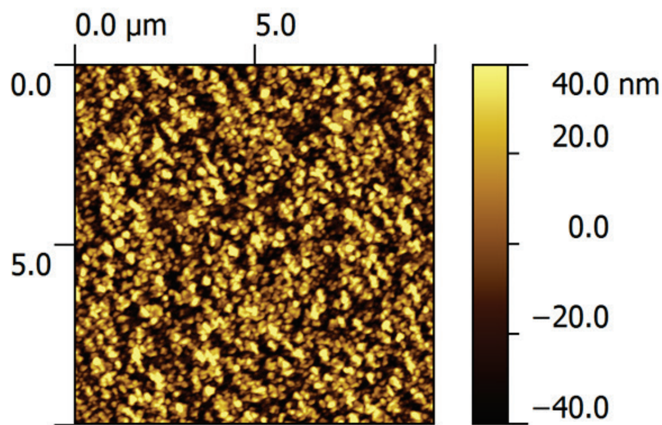
For the 20 nm and 55 nm layers, the surface appeared quite smooth in the cross-sectional TEM (figure 5.1a,b) while there was significant surface undulation occurring with the 150 nm thick seed layer (figure 5.1c). This is confirmed by AFM measurements on the samples where the rms roughness increased from 1 nm rms (Z-range: 28 nm) for the 20 nm seed layer (LTb-1) to 6.6 nm (Z-range: 50 nm) for the 55 nm seed (LTa-2) and then to 22.5 nm rms (Z-range: 150 nm) for the thickest 150 nm layer (LTb-3). The surface morphology of the Ge seed layers showed the presence of short-range, periodic undulations very similar to those presented in chapter 4 for Ge seed layers grown on (111) substrate. Figure 5.4 shows AFM scans for the three seed layers.



(a) 1.0 nm rms



(b) 6.6 nm rms



(c) 22.5 nm rms

Figure 5-4 AFM images of (110) seed layers showing short-range, non-periodic undulations: (a) LTb-1 (20 nm), (b) LTb-2 (55 nm), (c) LTb-3 (150 nm).

The plot below in figure 5.5 demonstrates the same linear dependence between surface roughness and LT seed layer thickness with (111)-oriented layers in previous chapter. As the thickness of LT Ge seed layer increased, so would the roughness of the layers.

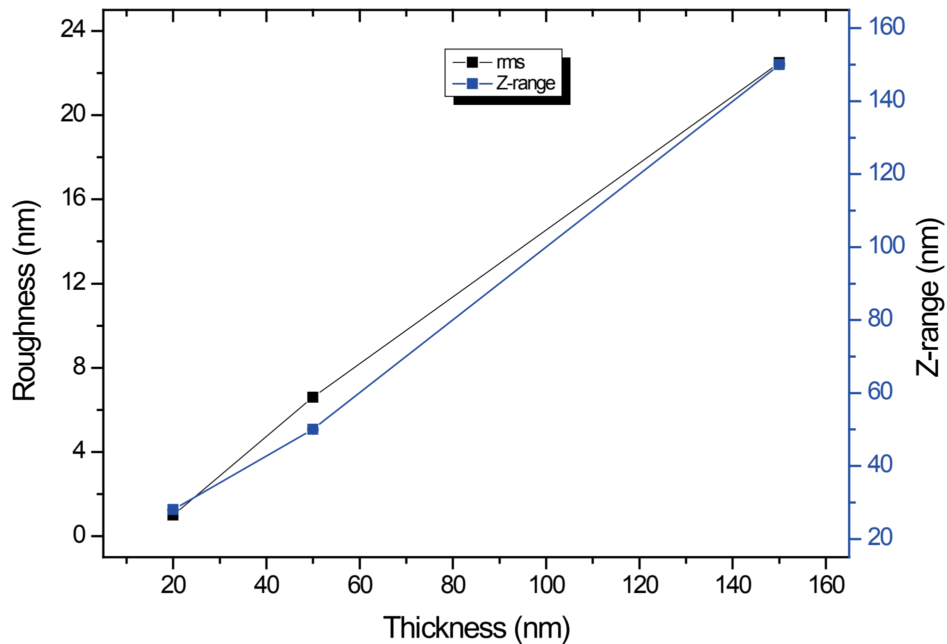


Figure 5-5 Plot of surface rms roughness (black) and Z-range (blue) versus Ge seed layer thickness showing an almost linear dependence.

5.2.3 Relaxation

X-ray diffraction was performed on the 20 nm and 55 nm seed layers to confirm if these layers should be in partially strained states similar to those observed in the previous chapter. No scan was done for the 150 nm as it was thought that this layer would be nearly fully relaxed. The XRD scans later confirmed that the LT-b1 and LT-b2 were at ~93% and 85% relaxed respectively.

5.3 Growth of high temperature Ge layers on (110) Si substrate

The high temperature Ge layers were grown using the same conditions as those in section 4.4. The samples that were grown for investigation are shown in table 5.2 below. It was decided that growth on the 150 nm thick seed layer would not be investigated as the layer was too rough so subsequent HT layer growth would lead to a low quality buffer in a similar manner to those investigated in chapter 4. Thus only the comparison between HT layers grown on the 55 nm and 20 nm seeds would be made in this section.

Wafer (*110*)		**Growth temperature (°C)**	**Deposition times (s)**		**Thickness measured (nm)**	
Name	**ID**		**LT**	**HT**	**LT**	**HT**
HT-b1	10-356	400°C / 670°C	820	410	55	425
HT-b2	10-144	400°C / 670°C	820	820	55	950
HT-b3	11-065	400°C / 670°C	410	410	20	400
HT-b1 (A)	10-366	400°C / 670°C + 830°C anneal	820	410	55	425
HT-b2 (A)	10-145	400°C / 670°C + 830°C anneal	820	820	55	950
HT-b3 (A)	11-066	400°C / 670°C + 830°C anneal	410	410	20	400

Table 5.2 Wafer numbers, deposition times and thicknesses of HT Ge layers grown on (110)-oriented LT Ge seeds.

5.3.1 Microstructure

For the 55 nm seed, two deposition times of 410s and 820s were used to grow the HT Ge layers which give HT layer thicknesses of 425 nm and 950 nm for samples HT-b1 and HT-b2 respectively. The cross-sectional TEM images in figure 5.6 shows that stacking faults were still present in the HT Ge layer of sample HT-b1 in high

density. However, the stacking faults are mainly confined within about ~100nm of the interface. Several threading dislocations were seen to have extended from the interface penetrating though the thick Ge layer. This observation is similar to the study made by Hartmann et al. on thick Ge layers grown on (110) Si substrate [80].

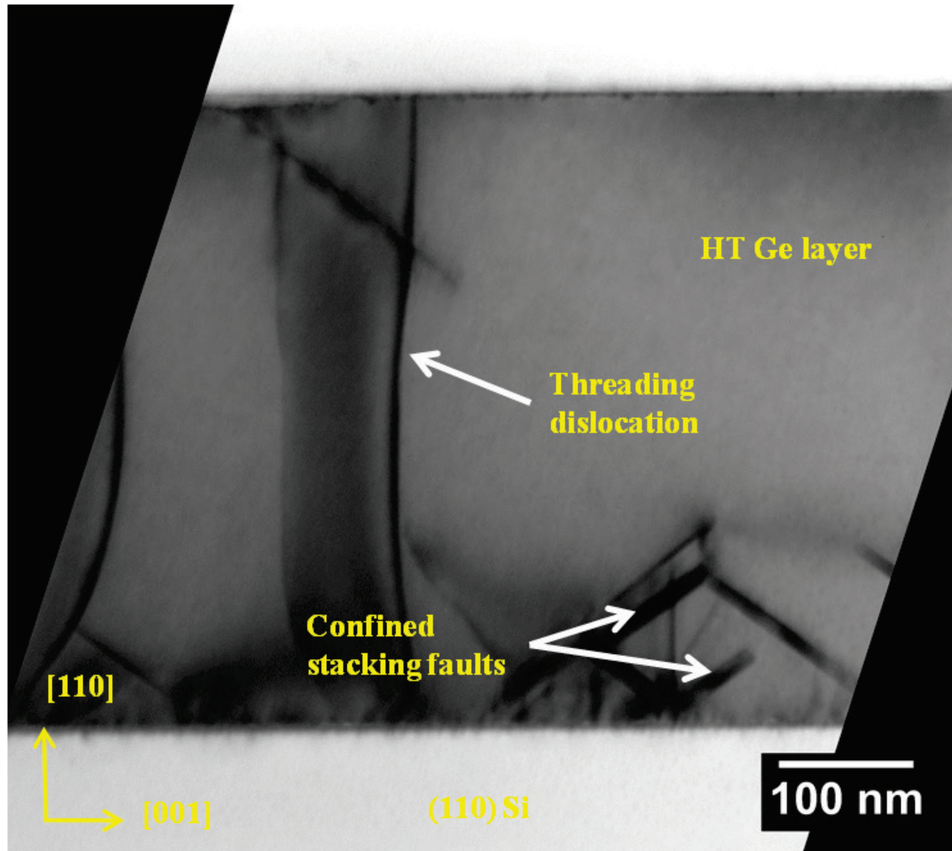


Figure 5-6 Cross-sectional TEM image of unannealed ~ 450 nm HT Ge layer grown on (110) Si substrate, sample HT-b1

Similar observation in cross-sectional TEM is made for the thicker, ~900 nm HT Ge layer of sample HT-b2. With the thicker HT layer, the stacking faults were still confined within ~ 100nm of the interface without extending further towards the surface. Threading dislocations however were seen penetrating the surface throughout the layer. Exact quantifications of their densities in the samples will be summarised later.

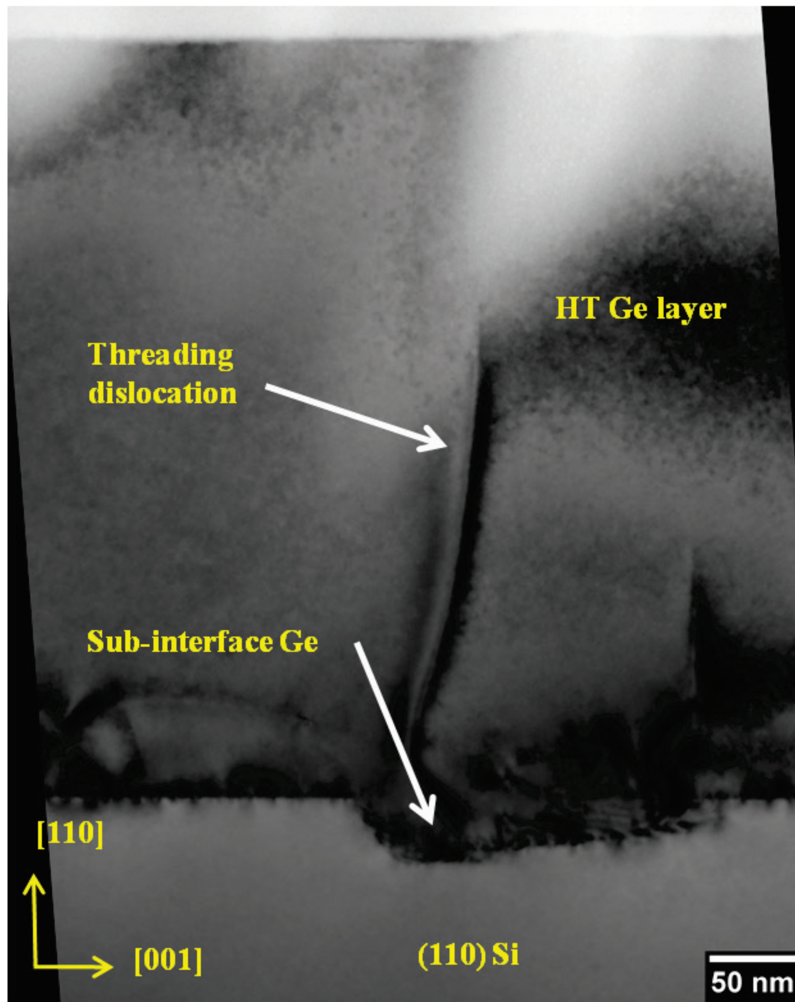


Figure 5-7 Cross-sectional TEM image of Ge buffer grown using the 20 nm seed on (110) Si substrate. The image shows a couple of threading dislocation penetrating the surface and a sub-interface trench containing Ge.

Figure 5.7 shows a typical cross-sectional TEM image of the HT layer grown on the thin 20 nm seed, HT-b3, with the HT layer measured to be ~ 400 nm thick. When compared with previous structures, this sample showed no confined stacking faults network near the interface. Instead, there is a dense network of misfit dislocations that give rise to threading dislocations that penetrate all the way to the surface. However, at the interface, there are occasional sub-interface trenches that contain Ge, this is similar to what was observed with growth using the thin 10 nm seed on (111) Si substrate which again could be due to the out diffusion of Si onto preferential sites

of islands at the initial stage of the high temperature layer growth. There is also evidence of dislocation annihilations within ~ 50 nm of the interface indicating the onset of high temperature growth when the islands have coalesced (see section 4.5).

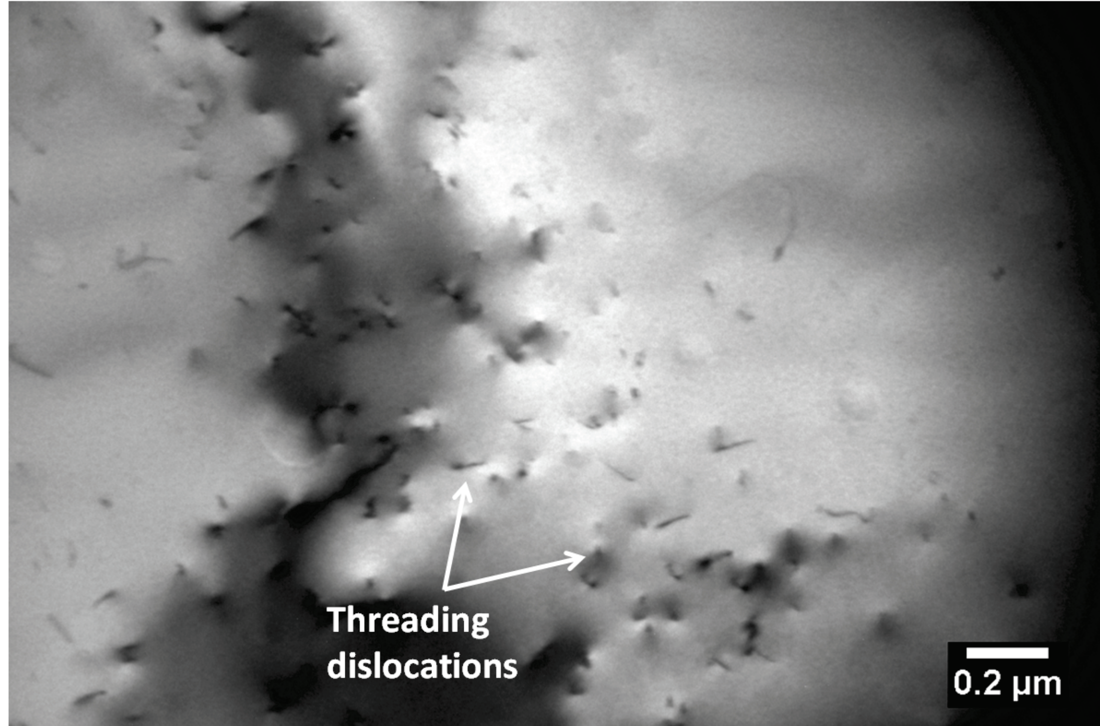


Figure 5-8 Typical plan view image of threading dislocations network in an HT Ge layer grown on (110) Si substrate with no stacking faults observed to penetrate the surface, ie. sample HT-b3.

The network of threading dislocations is better observed under plan view TEM. Figure 5.8 shows a typical PVTEM of sample HT-b3 where the threading dislocations were seen as dark spots and lines in the image. There is no observation of stacking faults in plan view TEM, as they are deep within the layer near the interface where the thickness of specimen prevents clear images of that part of the layer to be taken. The same can be said for the other layers that were grown on the 55 nm seed, HT-b1 and HT-b2.

The microstructure of the Ge buffer was similar for the annealed structures. However, the densities of threading dislocations were reduced significantly. Thermal annealing of the buffer has led to a lower TDD value, as expected because the majority of defects are threading dislocations. The plots below in figure 5.9 and figure 5.10 summarise the TDD of the HT layer and their annealed samples.

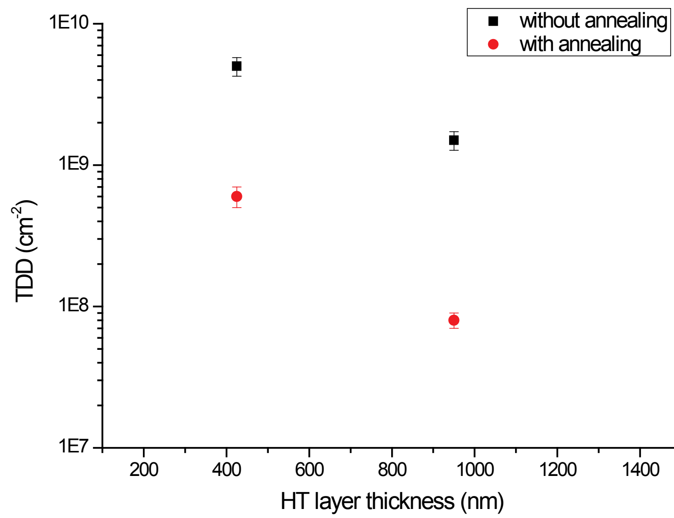


Figure 5-9 Plot of TDD of sample HT-b1, HT-b2, HT-b1 (A) and HT-b2 (A) against HT layer thickness. A lower TDD was observed for the thicker HT Ge layer whilst in-situ annealing reduced TDD in both sets of samples.

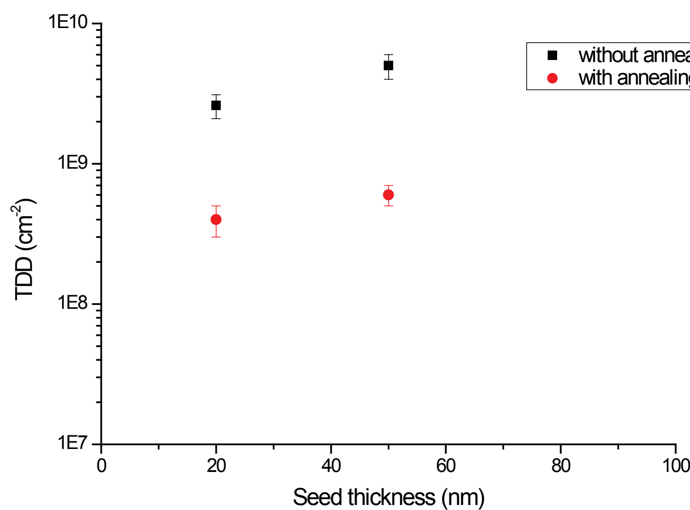
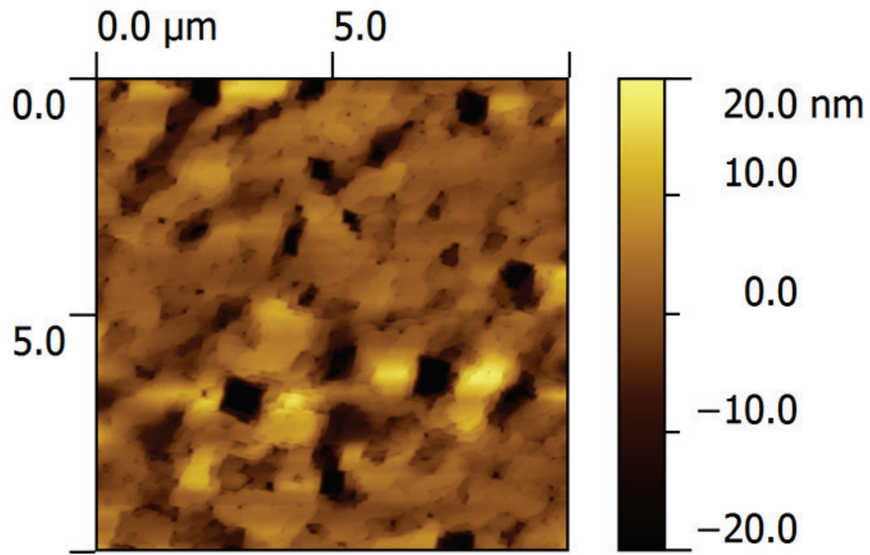


Figure 5-10 Plot of TDD of sample HT-b1, HT-b3, HT-b1 (A) and HT-b3 (A) against LT layer thickness. Similar values of TDD were observed whilst in-situ annealing reduced TDD in both sets of samples.

The plots show that there was an expected improvement in terms of TDD when a thicker (~ 900 nm) HT layer was grown on the 55 nm seed giving a value of 8×10^7 cm^{-2} (figure 5.9). The growth of HT Ge layer of similar thickness (~400 nm) on two different LT seed thicknesses (20 nm and 55 nm) didn't offer a significant improvement in term of buffer quality (figure 5.10). The TDD for these layers, HT-b1 (A) and HT-b3 (A), are comparable at 6×10^8 cm^{-2} and 4×10^8 cm^{-2} respectively.

5.3.2 Morphology

AFM was performed on the high temperature layers to study the surface morphology and surface roughness. The morphology of HT layers grown on the 20 nm seed is very similar to those grown on the thicker 55 nm seed. Typical 10x10 µm scans of the layers are shown in figure 5.11. It can be seen that the short range undulations that were observed for LT seed layers have disappeared. The unannealed sample surface now has square like features that might have arisen due to surface bunching of the threading dislocations (figure 5.14a). These square features are aligned at 45° to the orthogonal [100] and $[0\,\bar{1}\,1]$ directions. These directions are the intersections of the {111} planes with the (110) growth plane giving the preferential crystallographic orientations for the surface. However, after annealing, the number of dark square features has reduced significantly (figure 5.14b) and this is consistent with the decreased TDD measured in the previous section. This reduction in TDD has also led to a smoother surface roughness. Table 5.3 summarises the rms roughness of the grown layers.



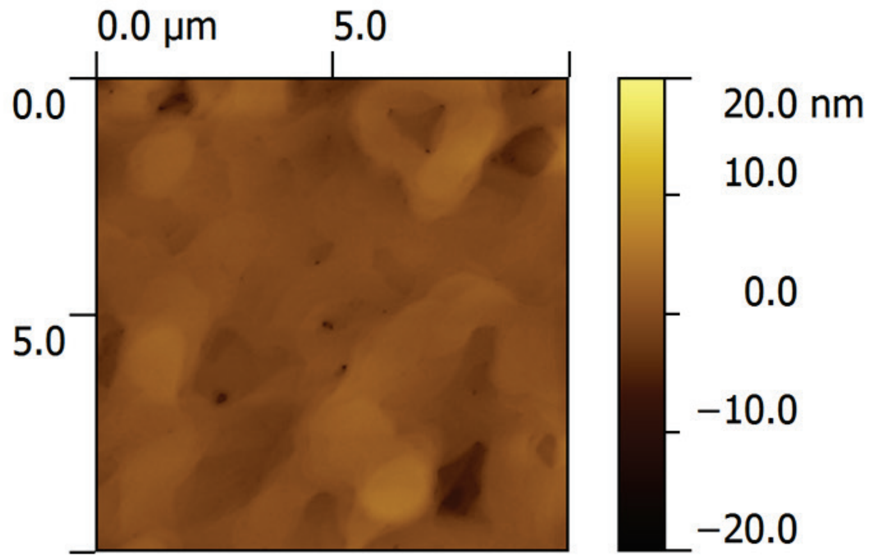


Figure 5-11 AFM images of: (a) the ~ 425 nm unannealed HT layers grown on (110) Si substrates, sample HT-b1 and (b) the annealed structure, sample HT-b1 (A).

Wafer *(110)*		Thickness measured (nm)		Rms roughness (nm)
Name	**ID**	**LT**	**HT**	
HT-b1	10-356	55	425	6.0
HT-b2	10-144	55	950	2.2
HT-b3	11-065	20	400	7.7
HT-b1 (A)	10-366	55	425	1.6
HT-b2 (A)	10-145	55	950	1.8
HT-b3 (A)	11-066	20	400	1.8

Table 5.3 Summary table of the surface roughness measured for the relaxed Ge buffers grown on (110)-oriented Si substrates.

It can be seen that before annealing the ~ 400 nm HT layer grown on both the 20 nm and 50 nm seeds have similar roughnesses, whereas the thicker 900 nm HT layer had a much lower rms value and is about three times smoother. After *in-situ* annealing the roughness of all three layers is reduced to approximately the same value. This could be seen as a much larger improvement for the thinner HT layers, but is better interpreted as all the layers reaching the same limiting value which the longer growth time of thicker layer allowed it to get closer to before annealing.

5.3.3 Relaxation

The thick HT layers also were measured by XRD to confirm the state of relaxation in these layers. The scans showed that all the thick layers were indeed crystalline and fully relaxed w.r.t. Si substrate at ~ 103%. Again, they are slightly over-relaxed and become tensile strained similar to what were observed in the previous chapter. A typical scan is shown in figure 5.12 below.

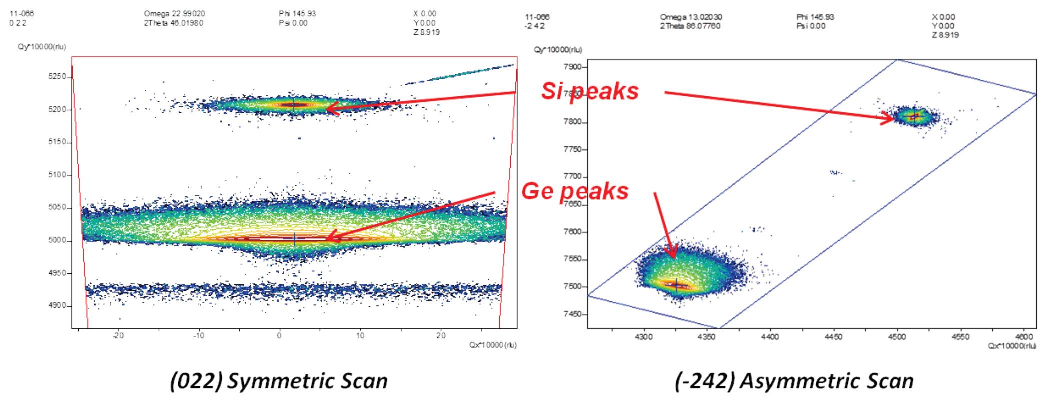


Figure 5-12 An XRD scan of sample HT-b3 (A) showing the typical relaxation state of thick HT Ge layers grown on (110) Si substrate.

5.4 Comparison with related work

Table 5.4 compares this work with other closely related work on growth of Ge buffer layers on (110)-oriented Si substrates. Again, comparing this work to the previous work done on RP-CVD the 1µm buffer ,which is 2.5 times thinner than the one reported, has achieved a surface that is more than 10 times smoother with a TDD value a decade lower. Surfactant mediated MBE was very effective at reducing the stacking fault density in (111)-oriented Ge layers; however, Ge layers grown on (110) Si substrates don't suffer as much from stacking fault so this technique didn't offer much improvement in buffer quality. The comparable thickness of the 1µm buffer of this work has even offered a slightly smoother surface compared to the work reported by Wietler listed in the table [85].

Other techniques that have been studied on (110) substrate orientation are similar to those mentioned in section 4.6 including: aspect ratio trapping (ART) and epitaxial lateral overgrowth (ELO) [89, 90]. Again, these techniques require selective growth and are not feasible on large scale production needed for commercial devices.

Technique	Substrate Orientation	Total Ge Thickness (μm)	Relaxation (w.r.t. Si substrate) (%)	RMS Roughness (nm)	TDD (cm^{-2})	Stacking Fault Density (cm^{-1})	Ref.
Surfactant-mediated MBE	110	1.0	102	2.7	N/A	Very low density, not visible in XTEM (<$1x10^8$)	[85]
RP-CVD	110	2.5	106	20 - 30	8×10^8	High density, visible in XTEM	[80]
RP-CVD	110	~1.0 ~ 0.4	~103	1.8 1.8	8×10^7 $4x\ 10^8$	Very low density, not visible in PVTEM (<$1x10^7$)	This work

Table 5.4 Comparison of the (110)-oriented buffers grown in this work with other closely related published literature.

5.5 Summary

Despite the significant enhancement in buffer quality achieved for (111)-oriented growth using a thin, partially strained LT seed layer, the same cannot be said with the (110)-oriented buffer investigated in this study. There wasn't a significant enhancement in either TDD or surface roughness of the layers when using a thin LT Ge seed compared to a buffer using a thicker one.

The two buffers with comparable thickness grown on two different seed thicknesses of 20 nm and 55 nm gave TDD of $4x10^8$ cm^{-2} and 6 $x10^8$ cm^{-2} respectively. Both of these layers also had similar surface rms values around 1.6-1.8 nm. The best quality buffer that was observed in this study was the 1μm thick layer which had a lower TDD value compared to the other two layers at $8x10^7$ cm^{-2} which resulted from a higher probability of threading dislocation annihilations in the thicker material. The

majority of defects observed in TEM for all the buffers grown on (110)-oriented Si substrate were threading dislocations along with a network of stacking faults and misfits that were mainly confined within about ~100 nm from the Ge/Si interface.

Three seeds of different thicknesses were investigated in this chapter, two of which were used for further HT Ge layer growth studies. The three seeds contained high densities of stacking faults inclined at ~ 30° to the interface which were evident of the intersection between the {111} glide planes and the (110) growth surface. Surface roughness increased with increasing seed layer thickness with significant surface undulation observed for the 150 nm seed.

6 Conclusion and Further Work

6.1 Conclusion

In this investigation, we have shown the epitaxial challenge associated with growth of thick relaxed Ge layers on (110) and (111) Si substrate by RP-CVD using a low and high temperature growth process. The samples examined were grown using a low and high temperature process by RP-CVD. The low temperature seed layers were grown at 400°C which plastically relaxed the strain due to the 4.2% mismatch between Ge and the Si substrate. The thick high temperature layers were grown at 670°C to reduce the defect density through glide and annihilation and smooth the layer. Finally in situ H_2 annealing at 830°C was used to thermally assist the annihilation of defects. The surface morphology of the Ge layers grown was studied by contact-mode AFM and the dislocation network was investigated by TEM. Strain relaxation in the layers was confirmed by XRD.

For Ge seed layers grown on (110) Si, it was shown that the surface roughness increased with layer thickness. However, when the thick high temperature layers were grown, the roughness did not follow the same trend. The thicker the buffer, the smoother the surface. The optimal surface roughness for high temperature layer after annealing was found to be around 1.6-1.8 nm rms.

The TEM images showed a dense network of characteristic stacking faults forming in the low temperature seed layer. The density of defects was reduced significantly as the stacking faults were confined within ~100nm of the interface when a high temperature Ge layers was grown on top of the seed layers. Only threading

dislocations were seen penetrating the layers all the way to the surface but the density was found to decrease from $1x10^9$ cm^{-2} to $8x10^7$ cm^{-2} for the 1μm thick buffer after annealing.

For the case of (111) orientation, the stacking faults were again seen forming in the thin seed layers. And for most of the samples examined, they could not be confined in a region near the interface despite the growth of thick high temperature Ge. Numerous stacking faults have extended all the way to the surface of the sample and this could be detrimental to performance of devices. The surface roughness of high temperature samples without annealing was found to be very close to those with in situ annealing due the planar nature of the stacking faults.

Finally, we have proved our objective of finding the effect that varying the seed layer thickness has on the epitaxy of Ge layers using the low temperature/high temperature technique. A Ge seed layer thickness of 10nm has given us a significantly lower density of stacking faults in the thick high temperature layer grown on top of it (not observable under plan-view TEM, ie $<10^7$ cm^{-2}). Also, the surface roughness was seen to be very low at around 1.2 nm rms. This has been a major find and it can be used as an industry favoured buffer for further growth of high performing device fabrication in CMOS technology and III-V integration in (110) and (111) orientations.

6.2 *Further work*

This work is by no means a complete systematic study of all the growth parameters possible with RP-CVD available for experimentation. There are also many other aspects in characterisation and analysis that could still be improved or added to enhance the scientific quality of the study.

1) The experiment only used variation in layer thickness by different deposition times to allow for simplicity in the investigation. However, other parameters could be used such as gas flow rate and chamber pressure that can also change the thickness of layers and may or may not influence the growth mechanism.
2) There were only three seed layers grown for each orientation which was not enough to say for definite that the thinnest seed grown was the optimal thickness for this LT/HT technique to grow Ge buffers. A few more samples of both LT seeds and HT layers grown on them could be investigated to give a clearer picture of the dependence of Ge buffer quality on seed layer thickness.
3) It was shown that when the stacking fault density was reduced significantly and the majority of defect was threading dislocation then in-situ annealing could reduce the TDD further. Thermal cyclic annealing and rapid thermal annealing (RTA) have been performed on other buffer growth techniques which yielded even TDD values a lot lower than the unannealed buffers which could be applied to the buffers investigated in this work to further improve the quality.
4) All SFD and TDD were estimated using XTEM and PVTEM images which have detection limits. A further work into defect etchants to find one that is selective to (110) and (111) orientation would be very beneficial. A definite SFD value

would allow for better comparisons with other reported work as well as further investigations for these buffers.

5) Many other characterisation techniques could be used to provide further insight into the growth mechanism of the HT layers on thin LT seeds. *In-situ* TEM used by MBE systems [47] could give real-time imaging of the formation of Ge islands and how dislocations interaction within the seeds as well as at the start of HT Ge growth.
6) X-ray pole measurement on the LT seed layers could better determine the density and type of the dislocations within these layers.
7) Electronic measurements for devices fabricated using these buffers would give a clear indication of the quality of the buffer and its feasibility for applications.

A high quality buffer grown on (111)-oriented Si substrate has been achieved leading to more exciting work that could be done to further improve it. The work reported here shows that the non-(100) orientation buffers are certainly worthy of at least further study, as previously the poor quality observed had led to them being dismissed as promising alternative material. If further experimentation achieves even better results, the buffer could quite realistically become an *industry favoured* platform for various device applications.

7 References

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