Electro-Thermo-Mechanical Study of Membrane Devices for Smart IC Technologies

Syed Zeeshan Ali

Sidney Sussex College

University of Cambridge

August 2007

Dissertation submitted for consideration to the University of Cambridge towards the degree of Doctor of Philosophy

Acknowledgement

I would like to express my thanks to my supervisor Dr. Florin Udrea for his constant support, help and guidance throughout my studies, and his encouragement to tackle new tasks. I would also like to thank my advisor Professor Bill Milne for his support.

Also, I would like to acknowledge the support of the Cambridge Commonwealth Trust, Cambridge Semiconductor Ltd, and ETRI (from the Korean Government) who helped provide funding during my studies.

Also thanks to Professor Julian Gardner, Dr. James Covington, and Mr. Takao Iwaki from the University of Warwick who gave lots of input in the design for the micro-hotplates.

I would also like to acknowledge the support of all my colleagues at the HVM lab who provided an excellent atmosphere to work in and gave lots of help and advice. Thanks also to the staff at Cambridge Semiconductor Ltd for their help and support.

Finally, a big thanks to my friends and family, especially my brother and parents for their encouragement, advice and prayers throughout my studies.

Declaration

This thesis contains the results of my research work undertaken between October 2003 and August 2007 as a student at the Cambridge University Engineering Department. This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration except where specifically indicated in the text.

No part of this thesis has been ever submitted in whole or part towards any other degree.

This thesis contains approximately 32,000 words and 146 figures

Syed Zeeshan Ali
University of Cambridge

Syed Zeeshan Ali

Electro-thermo-Mechanical Study of Membrane Devices for Smart IC Technologies

Summary

Silicon on Insulator membranes are increasingly finding applications in many semiconductor devices and circuits. This thesis studies thermal and mechanical behaviour of two very different membrane based devices: Smart Gas Sensors and Membrane Power Devices. Both the devices are CMOS compatible and can easily be integrated with circuitry in a smart IC. The same fabrication process has been used for both these devices – a standard SOI CMOS process, followed by Deep Reactive Ion Etching (DRIE).

Gas sensors need a micro-hotplate to heat the sensing material for better sensitivity and faster response time. The use of a membrane greatly reduces the power consumption of the heater. In lateral SOI power devices the membrane can greatly enhance the breakdown voltage and switching time. However, this comes at the expense of higher temperatures within the device – which can significantly reduce the lifetime. While in gas sensors it is desirable to have a high temperature for a given amount of power, in power devices the aim is to have a low operating temperature.

Novel tungsten based SOI micro-hotplates are presented. A thorough thermal analysis of the power consumption (via conduction, convection and radiation), transient time and temperature uniformity of the micro-hotplate is presented by extensive simulation and analytical analysis. Following the study, micro-hotplate devices were fabricated at a commercial foundry. The measured results were analysed and matched with the simulations. The devices have very low power consumption (14 mW at 600°C), fast response time (2 ms for 600°C), good mechanical stability and excellent uniformity within a wafer and from wafer to wafer.

Contents

Chapter1: Theory and Background 3

Membranes 3

Applications: 4
Fabrication 5

Smart Devices 7

Smart Sensors 7
Smart Power Devices 8

SOI Technology 8

Fabrication 9
SOI in micro-electronic circuits 11
SOI in MEMS and Sensors 13
Challenges 14

Micro Gas Sensors 15

Basic Principles 15
Sensing Materials 16
Selectivity and Drift 18

Membrane Power Devices 19

Summary 20

Thesis Outline 21

Chapter2: Gas Sensors – Initial Design and Analysis 22

Micro-hotplates in Literature 22

Proposed structure for Micro-hotplates 25

Aspects of Micro-hotplate Design 27

Power Consumption 27
Conduction: 27
Convection 42
Radiation: 52
Transient Time 53
Temperature Uniformity 55

Conclusions 75

Chapter3: Gas Sensors – Fabrication and Measurement........................76

Standard Micro-hotplate Design 76

Heater Design.. 78
Micro-hotplate Variations:.. 85
Fabrication.. 88

Measurement and Analysis 90

Pre-Etch Measurements: 90
Thermal Characterization and Analysis.. 95
Calibration... 95

Power Consumption 99

Transient Time 110

Effect of Membrane Types 115

Aluminum: 118

Different Temperature Sensors:... 120

Heater Sizes: 121

Mechanical Characterization 122
Conclusions 127

Chapter4: Membrane Power Devices............ Error! Bookmark not defined.

Overview .... Error! Bookmark not defined.

Self Heating Analysis .... Error! Bookmark not defined.

2D Simulations...**Error! Bookmark not defined.**
3D Simulations...**Error! Bookmark not defined.**
Full Chip and Packaging:...**Error! Bookmark not defined.**
Comparison with measurements:...............................**Error! Bookmark not defined.**
Mathematical Analysis...**Error! Bookmark not defined.**
Thermo-Mechanical Simulations for Packaging........... Error! Bookmark not defined.

2D Simulations...**Error! Bookmark not defined.**
3D simulations ....**Error! Bookmark not defined.**
Conclusions .... Error! Bookmark not defined.

Chapter5: Conclusions and Further Work...130

List of Publications 135

Appendix A: Fabricated Chips for Tungsten Micro-hotplates 136

Appendix B – Thermal Conductivity of Thin Silicon............................140

References...141

Chapter 1

Theory and Background

Membranes

Membranes, in microelectronics, refer to a very thin layer of material isolated from the rest of the chip, formed by etching away part of the substrate. Membranes have a structure as shown in Figure 1, and the membrane itself can be made of any material such as silicon, silicon oxide, silicon nitride, or more commonly, can be made of two or more layers of different materials.

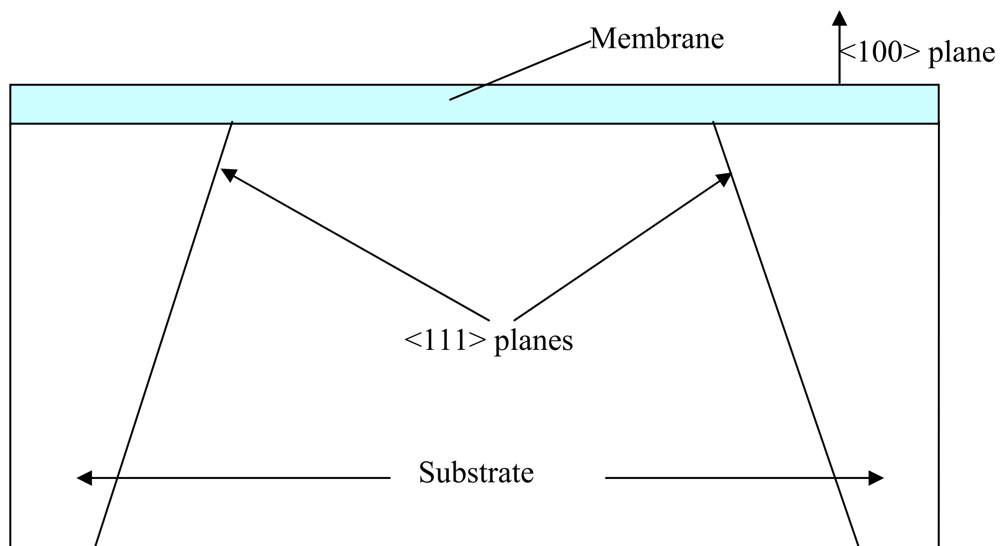


Figure 1: A membrane structure – a thin layer supported by a substrate

Another type of membrane structure is as shown in Figure 2. These are known as suspended membranes or micro-bridges and are supported by only 2 or 4 beams, as compared to the previous structure which is supported at the entire circumference.

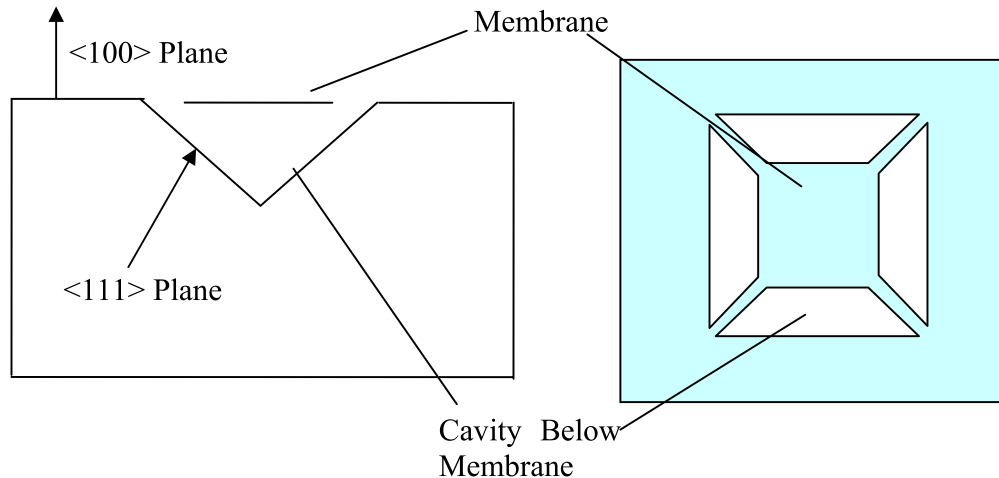


Figure 2: Structure of a suspended membrane

Applications:

Membranes have found applications in many different fields, a few of which will be briefly described.

Pressure sensors are one of the most successful devices employing membranes, with total sales of several hundred million euros annually [1]. Their applications include automotive systems, industrial process control, medical diagnostics, and environmental monitoring [2]. They consist of a membrane as part of a sealed cavity formed by bonding to another substrate. The differential pressure on the two sides of the membrane causes it to deflect. The deflection can be measured by placing piezoresistors within the membrane, which change their resistance when the membrane is under stress. Alternatively the membrane can act as one electrode of a capacitor, whose capacitance changes when the membrane deflects.

Silicon based microphones are another application that uses membranes. The thin membrane vibrates due to sound, and this can be sensed by piezoelectric, piezoresistive or capacitance measurements [3].

Infra-Red (IR) detectors employ membranes to improve the sensitivity of the measurements. IR detectors work by absorbing infra red heat. This raises the temperature of the device which can be measured to determine the IR absorption. Placing the detector on a membrane thermally isolates it. Therefore for a given amount of heat absorbed, the rise in temperature is higher, resulting in better response for the device [4,5].

Gas sensors and Power devices are two other very important applications of membranes, and it is these that will be discussed further in this thesis. Gas sensors require a micro-heater to raise the temperature of the sensing element. The micro-heater is embedded in a membrane to reduce the power losses[6]. Making lateral power devices on membranes can greatly increase the breakdown voltage of the device, and also reduces the switching time[7].

Fabrication

The main process step in the fabrication of membranes is the etching of the substrate. The etching starts from the back side of the chip or wafer for a conventional membrane structure, but from the front side for a suspended membrane. The etching can be by either wet or dry etching.

Wet etching uses liquid chemicals[2], EDP (Ethylene Diamine Pyrocatechol) and KOH (potassium hydroxide) being the most common. Both of these materials have high etch rates for silicon, but low etch rates for silicon nitride and silicon oxide. 50% wt KOH at 80°C has an etch rate of 1.4µm/min. A solution of 750mL EDP, 120g pyrocatechol and 100mL water has an etch rate of 0.75µm/min at 115°C [8]. KOH is cheaper, but has a comparatively higher etch rate for silicon oxide than EDP. The etch rates for silicon oxide are 100 times smaller than silicon when using KOH, and about 5000 times smaller for EDP. Both these etchants are anisotropic, meaning that they etch some crystal planes of silicon faster than others. This results in sloped trenched walls similar to the structures showed in Figure 1.

Dry etching uses a plasma to etch the substrate. It is formed by applying a high voltage, high frequency AC signal between two electrodes to ionize the gas. The ion species either react with the substrate silicon to etch it (plasma etching), or bombard the

surface and physically remove atoms (Reactive Ion Etching (RIE)) [2]. In RIE, an AC bias is also applied to the wafer.

Deep Reactive Ion Etching (DRIE) is a form of RIE that can be used to form structures with high aspect ratios [9]. There are two methods to do this. One approach cools the wafer to cryogenic temperatures (for example -120°C [10]). This causes gases to condense on the sidewalls, and hence protects them from the reactive ions.

The other method is patented by Robert Bosch GmbH [11]. This method is more commonly used and consists of alternate etch and deposition of protective polymers on the side walls of the trench. First, RIE is used to etch a small amount of the silicon. Then a 10 nm protective material (a fluorocarbon polymer) is deposited to cover the sidewalls, as well as the trench bottom. In the next RIE cycle, the plasma etches through the polymer at the bottom of the trench, while the polymer covering the sidewalls remains. Several repeated cycles result in trenches with high aspect ratios.

Etch-Stops:

Etch-stops are needed to stop the etching of the substrate, otherwise the etching process would continue and simply form a hole in the chip rather than a membrane. The simplest technique is to use another material that does not react with the etchant. For example, both silicon oxide, and silicon nitride have very low etch rates compared to silicon for KOH and EDP [6] as well as RIE and are often used as etch stops. Therefore growing, or depositing a layer of either material before the etch process would stop the etching when it reaches the oxide or nitride layer. This would result in the formation of a silicon oxide, or a silicon nitride membrane. Alternately, if a silicon membrane is needed, then the top silicon can be heavily doped with boron. Boron doped silicon has lower etch rates for both EDP and KOH, and hence can be used to form silicon membranes. With KOH it etched 20 times slower than silicon, while with EDP it etches 50 times slower [8].

For suspended membranes, etch-stops are not required, as the anisotropic etching stops once the etchant hits the <111> crystal planes.

Smart Devices

A smart device is a device such as a sensor or a power device that has been integrated along with its associated circuitry in the same chip (called a smart IC). The circuitry might be simple signal conditioning circuitry with some amplification, or might have complex interface circuits including control circuitry, analog to digital converters, and even a small microprocessor. Such a device has many advantages over a standalone device.

Since some or most of the associated circuitry is integrated with the sensor, fewer additional electronic components are required for system integration, and this results in lower overall system cost and size. The smaller size is a big advantage in portable or aerospace applications.

Smart Sensors

An example of a smart device is a smart microsensor (or "smart sensor" for short) fabricated with the interface circuitry on the same chip. Besides the advantage of cost and size, smart sensors can also have better accuracy. Some sensor signals, especially for capacitance sensors are so small, that they have to be conditioned on chip, otherwise, taking the signals out of chip would add noise, and significantly reduce the accuracy of the sensor. In addition, smart sensors often have circuitry to offset the effects of cross-sensitivities, such as to temperature and humidity. They may even incorporate passive sensors to cancel out cross-sensitivities [12].

Smart sensors can also have self-test as well as self-calibration capability. Most sensors tend to drift in time, and need to be calibrated. Sensors which have self-test capability can greatly reduce the cost of calibration. In safety critical systems, one cannot afford to have a faulty sensor. Smart sensors with self-test capability are therefore very useful in such applications.

Integrating the sensor with its associated circuitry is not straightforward. Many of the materials and processes ideally suited for the sensor structure are often not compatible with standard CMOS processes used for circuit fabrication. Often the structures have to be fabricated on the chip after the circuits have been made by the CMOS process. In such

a case, care has to be taken to protect the circuits. For example high temperatures (400-500°C or greater) during processing can greatly degrade the circuits on the chip.

Smart Power Devices:

Power devices can also be integrated with control circuitry to form smart power ICs [13]. This can greatly reduce the overall size of the system with applications such as mobile devices and battery chargers. Other features such as on chip current and temperature sensors can also be included.

One of the main challenges in smart power devices is to isolate the power device from the control circuitry. Charge from the power device can potentially affect the working of the control circuitry. Also, processes have to be properly adapted to fabricate both the power device as well as the control circuitry.

SOI Technology

SOI (Silicon on Insulator) technology offers the possibility of building electronic devices in a thin layer of silicon that is electrically isolated from the thick semiconductor substrate through the use of a buried insulating layer [14]. This reduces undesirable effects caused by the presence of the bulk silicon, and allows excellent isolation between individual device cells. The use of SOI technology can result in an electrical performance gain of 25-35% over bulk CMOS technology.

Research and development of SOI materials started several decades ago to develop devices less susceptible to radiation for use in space applications. However, it was only in 1998 that SOI became a mainstream technology, when the first SOI product (a 64-bit PowerPC microprocessor) was shipped by IBM (International Business Machines) [15]. At present SOI technology is being used in a number of high-end micro-processors from AMD (Advanced Micro Devices) and IBM.

Fabrication

Several techniques have been developed for the fabrication of SOI wafers. Silicon on sapphire was one of the earliest techniques used and consists of a thin single-crystal silicon layer grown on sapphire using chemical vapour deposition from silane glass. This has now been replaced by other techniques: SIMOX, wafer bonding, and smart cut.

In SIMOX (Separation by IMplantation of OXygen), the silicon substrate is implanted with a high dose of high energy oxygen ions, and then annealed at high temperature for several hours. This creates an oxide layer just beneath a thin silicon layer (Fig 3).

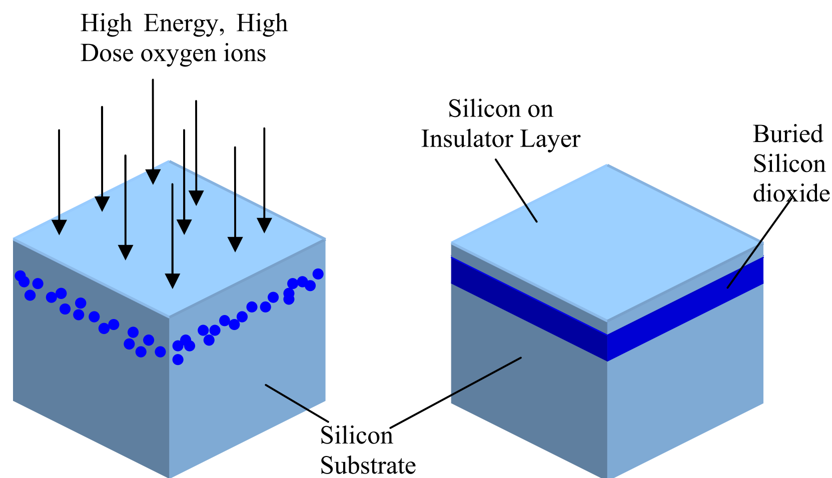


Fig 3: The SIMOX Process

In wafer bonding (Fig 4), an oxide layer is grown on two silicon wafers. When brought into contact with each other they are attracted by Van der Wall's forces and bond together. This is followed by annealing and polishing of the top wafer to leave behind a thin silicon on insulator layer.

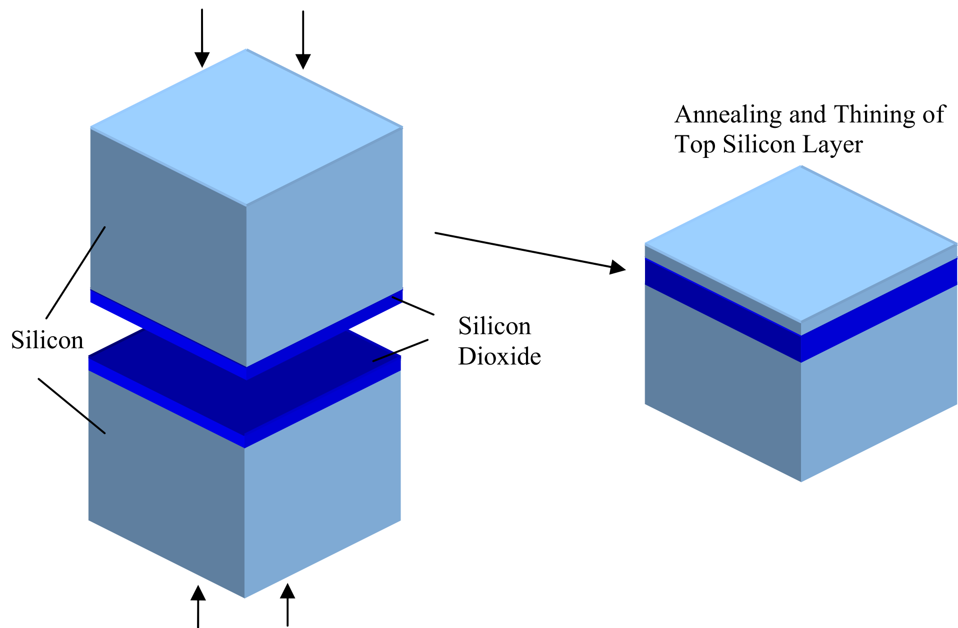


Fig 4: The Wafer Bonding Process

Smart-cut is similar to wafer bonding. However, before bonding, the top wafer is implanted with a high dose of hydrogen ions. After bonding, a heat treatment at 400-600°C divides the wafers along the line of implanted hydrogen ions, leaving behind a thin, uniform silicon on insulator layer (Figure 5). The Smart-Cut process is used by Soitec[16] for the fabrication of SOI wafers (sold under the Unibond brand name), and result in wafers with extremely uniform SOI layers.

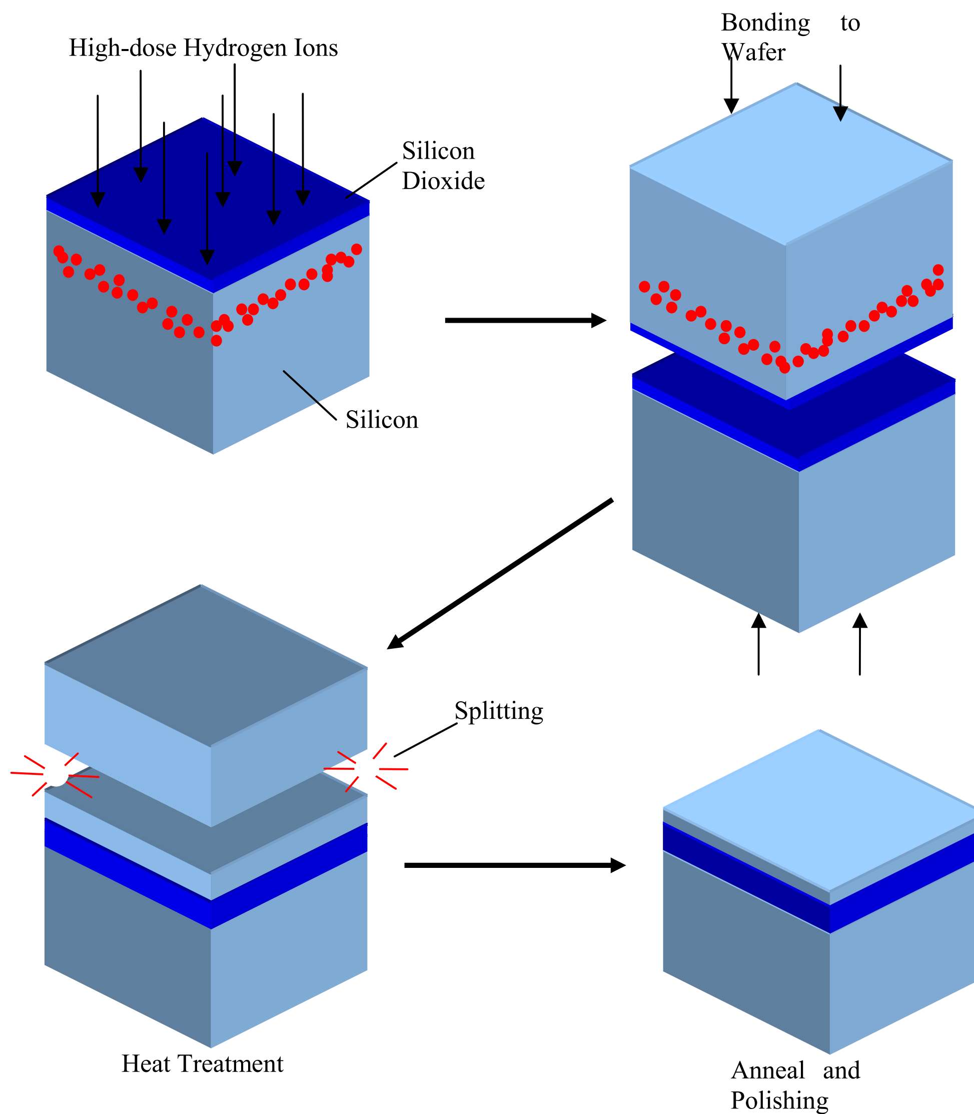


Figure 5: The Smart-Cut process

SOI in micro-electronic circuits

SOI technology offers many advantages for micro-electronic circuits and devices:

Enhanced Device Isolation:

In bulk CMOS technology, transistors are isolated from each other by the use of reverse biased p-n junctions. In SOI, enhanced isolation can be achieved vertically by the buried oxide and laterally by trench etching, or by LOCOS (LOCal Oxidation of Silicon)

in which the silicon between devices is oxidized to form an insulation between them (Figure 6). This is possible in SOI devices since the silicon layer is very thin (usually less than 5μm), and the isolating structures can physically connect to the buried oxide layer. This method of isolation is also more compact, resulting in a higher packing density of the devices, and hence smaller chips.

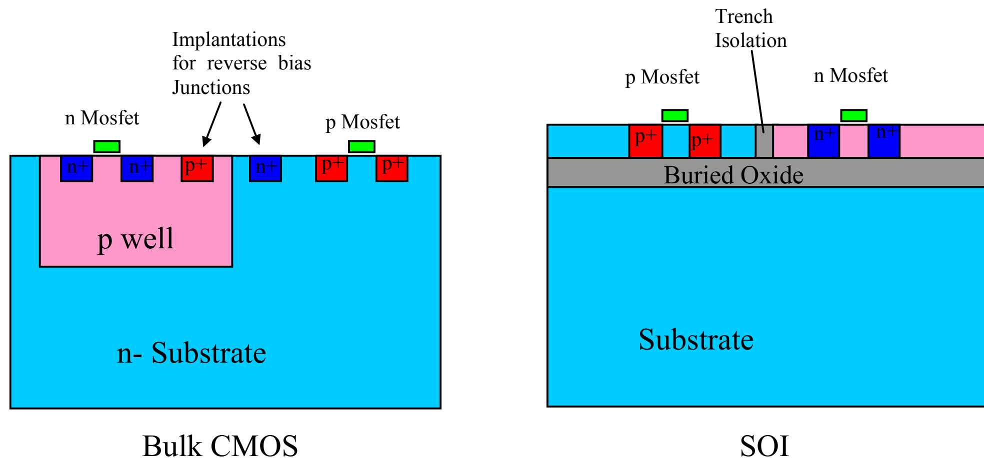


Figure 6: Device Isolation in Bulk CMOS and SOI Technology

Lower Parasitic Capacitances

In bulk CMOS, the presence of the substrate results in large parasitic capacitances. In particular area junction capacitances (between the heavily doped n+/p+ implant regions and the substrate) can be significant. In SOI technology, the presence of the buried oxide layer between the device and the substrate greatly reduces these capacitances. The lower parasitic capacitance allows for faster circuits, and operation at higher frequencies.

Reduced Short Channel Effects:

As MOSFETs are scaled down, the channel length becomes comparable to the depletion width of the drain and source regions. This results in 'shortening' of the channel, and reduction of the threshold voltage of the device, making device behaviour unpredictable. This effect is much reduced in SOI technology because in the thin silicon there is less area for the depletion region to extend to.

High Temperatures:

Circuits in SOI technology can typically operate at much higher temperatures (upto 200°C or even higher) compared to bulk CMOS devices because of better device isolation, and elimination of latch-up (which generally occurs at high temperatures).

Lower Power Consumption:

In bulk CMOS, there are significant leakage currents in the substrate, as well as to neighbouring devices. In SOI technology, due to good isolation, these leakage currents are much reduced. Therefore SOI technology is more power efficient.

Less Susceptible to Radiation

SOI devices are also much less susceptible to radiation [17]. In bulk CMOS, ionizing radiation (such as an alpha particle), can induce charges in the substrate, which can travel up to the device, causing a current surge, potentially resulting in latchup. In SOI technology, the buried oxide stops the charge propagation from the substrate to the device. For radiation to cause any problems, it must strike on the thin SOI layer – the chances of which are much lower than in the larger volume of the bulk chip.

SOI in MEMS and Sensors

MEMS (Micro Electro Mechanical Systems) and microsensors usually require the fabrication of mechanical structures on chip. This often involves the deposition of different material layers followed by suitable patterning and etching to realize these structures. SOI wafers have two extra layers (the SOI layer and the buried oxide layer) in addition to the silicon substrate. The presence of these two layers means that if these two layers are used for the design, then the structures can be created with fewer fabrication steps.

The properties of silicon and silicon oxide are ideally suited for use in MEMS. Silicon has good mechanical properties, and can be used as the structural layer for the fabrication of structures such as cantilever beams and micro-bridges, while the oxide acts as a sacrificial or isolation layer. Both these materials are used extensively in the

semiconductor industry for integrated circuits. Because of this their properties are very well known, therefore the development of devices using these materials is much quicker.

Both of these materials also have excellent etching selectivities with respect to each other making it easier to form structures. In particular, membrane structures can be readily fabricated on SOI technology. The buried oxide layer forms a natural etch stop for both wet and dry etching processes eliminating the need for the deposition of a separate etch stop layer.

In addition to this, circuits built on SOI technology can operate at higher temperatures (e.g. $200^{o}C$ and over) as compared to those built on bulk silicon. This allows smart devices fabricated using SOI technology to operate in high temperature environments.

Challenges

In spite of its many advantages, SOI technology does pose some challenges in development.

1. Silicon dioxide is a good thermal insulator, with a thermal conductivity which is 100 times less than silicon (silicon dioxide has a thermal conductivity of 1.4 W/mK compared to 150 W/mK for silicon at room temperature). This results in higher temperatures for circuits fabricated on SOI devices, and can result in overheating and reliability issues.
2. The body of the transistors in ultra thin SOI are usually floating. This can give rise to parasitic effects.
3. SOI wafers are also more expensive than bulk CMOS wafers. However the cost is usually offset by the fact that SOI allows denser packing of devices, and thus more chips per wafer.

Micro Gas Sensors

There has been considerable research activity in the past two decades in the development of silicon based gas sensors. Such sensors can be used in safety applications, such as smoke alarms, and detection of gas leakage. In the automotive industry, they can be used to monitor gases in car exhausts or to control the air quality in the cabin. Other applications include analytical instruments, environmental monitoring, medicine and industrial process control.

Basic Principles

The underlying feature of most silicon based gas sensors is that the target gas undergoes a reversible chemical reaction with a gas sensitive material [1]:

$$A_{gas} + B_{solid} \leftrightarrow AB$$

This results in a change in some physical property of the sensitive material, which is used to measure the gas concentration. Gas sensors are usually classified according to the physical property measured. Some categories of gas sensors are:

Chemoresistive Sensors:

Chemoresistive gas sensors consist of a gas sensitive material, which undergoes a change in resistance in the presence of a gas. The gas sensitive material is usually either a metal oxide or a polymer. High temperatures are usually required for oxides (e.g. 400°C), and these are achieved by means of a heater placed on a thin insulating membrane for lower power losses.

Chemocapcitive Sensors:

Chemocapcitive sensors work by sensing the changes in the capacitance of a material when exposed to a gas. Usually the gas sensitive material is a dielectric between two metal electrodes. The electrodes can be either inter-digitated, or two horizontal plates, with the top plate made of a porous metal. Exposure to gas causes a change in the di-electric constant, which results in a change in capacitance that can be measured and used to determine the gas concentration.

Micro-calorimeter

Micro-calorimeters are usually used to detect combustible gases such as methane and carbon monoxide. They work by sensing the change in temperature caused by the chemical reaction of a gas (usually combustible). The micro-calorimeter consists of a micro-heater, and a catalyst, such as palladium, and operates at a high temperature, usually above 500°C. The catalyst catalyses the combustion of the gas, a reaction which releases heat energy. The energy released causes the temperature to rise, which is detected by a thermal sensor and used to determine the gas concentration.

ChemFETs

These are field effect transistors, consisting of a gate made of a conducting gas sensing material. The presence of a gas causes a shift in the threshold voltage of the sensor, which is used to determine the gas concentration. The advantage of these sensors is that they can operate at room temperature, and thus require much lower power than chemoresistors. However, they are strongly influenced by changes in temperature.

Resonant Sensors:

These consist of a gas sensitive layer deposited at the end of a cantilever beam. These beams are made to vibrate, either by piezo-electric, or thermo-mechanical actuation. The resonant frequency of the beam depends, among other factors, on the mass of the beam. In the presence of a gas, the gas is adsorbed onto the gas sensitive layer, increasing the mass. This results in a change in the resonant frequency. This change in resonant frequency can be measured and used to determine the gas concentration. Resonant sensors require relatively more complex control circuitry than other types of gas sensors.

Sensing Materials

Sensing materials used for gas sensors are typically either porous metal oxides or organic materials. Metal oxides are more popular due to their better stability [1]: They do not degrade quickly, and are less affected by poisoning. However, metal oxides require much higher temperatures than organic materials.

Metal Oxides

Porous tin oxide is the most common material used for chemoresistors. The porous form of the material is used in order to increase the surface area in contact with the gas. In air, non-stoichiometric tin oxide is an n-type semiconductor, with electrons as the main charge carriers. Oxygen reacts on the surface of the tin oxide to form negatively charged ions. The negative charge on these ions is provided by free electrons within the tin oxide. This therefore reduces the electrons in the tin oxide, and results in a lower bulk conductivity.

When exposed to a reducing gas, such as carbon monoxide (CO), ammonia (NH_3), or any hydrocarbon is present, these react with the adsorbed oxygen, and return the electrons to the tin oxide. The electrons cause a reduction in the inter-grain barrier in the tin oxide. Predominantly the reduction in the inter-grain barrier reduces the resistivity [1]. Conversely, oxidizing gases, such as NO_2 cause an increase in the resistance of tin oxide. If a metal oxide is used that behaves as a p-type semiconductor, then reducing gases cause an increase in resistance, and oxidizing gases cause a decrease is resistance.

This sensing principle, however, does mean a lack of selectivity, as any reducing gas might cause the increase in conduction in tin oxide, making it difficult to realize a sensor sensitive to only one gas. However, some gases have greater effects than others, and changing the temperature also results in better selectivity for a particular gas. For example, tin oxide can be made more selective to carbon monoxide by doping to 0.5% palladium and 0.5% platinum. Better selectivity for ammonia is achieved by doping to 1% palladium [18].

Polymers

Organic materials have also been used for gas sensors. They have much better selectivity than metal oxides, and operate at much lower temperatures as compared to those required for metal oxides. Two main classes of materials have been studied: organic crystals, and polymer films[19]. The main disadvantage of organic materials is that they are not stable: they degrade relatively quickly, and are more prone to poisoning.

Carbon Nanotubes:

Carbon Nanotubes are an exciting new material for gas sensing and several groups have reported sensitivity of CNTs to gases [20][21]. Carbon Nanotubes (CNTs) can be thought of as a graphene sheet rolled up into a tube shape, and can be single-walled or multi-walled. CNTs can be either metallic or semi-conducting in nature depending on which angle the sheet has been rolled. It is the semi-conducting CNTs that are of more interest for gas sensing. CNTs are particularly attractive because their large surface to volume ratio means that they need a relatively small area for gas detection, which reduces the size of the gas sensor.

Selectivity and Drift

Gas sensors in general suffer from poor selectivity and drift. Gas sensors are often sensitive to other gases as well as the target gas for which they were designed.

Different techniques can be used to improve the selectivity of gas sensors. One method involves modulating temperatures to distinguish between two different gases [22]. The temperature is varied sinuosidally, and the resulting response from the gas sensor is analysed by extracting Fourier coefficients, and applying pattern matching techniques. This has been used to show that a single gas sensor can be used by this method to identify and distinguish between Carbon Monoxide (CO) and Nitrous oxide (NO_2).

Another method is the use of sensor arrays, which can result in better selectivity. Different materials have different responses to different gases. If an array of sensors, with different sensing materials are used, and the responses are analysed by appropriate pattern matching techniques, then good selectivity for a particular gas is possible [1].

Gas sensors also tend to drift with time, that is, their response changes over a period of time. For example, a gas which has been absorbed by the sensing material might not fully desorb, even after the gas is no longer present in the surrounding area. One way to overcome this is to use two sensors on the same chip. One is an active sensor, exposed to the air, while other is a passive one, which has been covered by a passivation layer. The difference between the two is used to determine the gas concentration. In this way any effects of drift are minimized. This technique also reduces common modes of sensitivity, e.g. humidity.

Membrane Power Devices

Power electronic circuits are required to process and control the electric power to a load, in an optimal form (the desired voltage/current). Power devices form the main components of power electronic circuits, and the performance of the power device to a large extent determines the circuit performance.

Most of the first semiconductor power devices fabricated were vertical devices, that is having an electrode connected to the base of the substrate, while the other connected at the top. The reason for this is that power devices need to support very high voltages (varying from 100V to upto 10KV depending on application) across them, and a large distance between the electrodes increases the voltage blocking capability. Thyristors, Power BJTs (Bipolar Junction Transistors), power MOSFETs and IGBTs (insulated Gate Bipolar Transistor) come into this category.

However, vertical devices cannot have circuitry readily integrated with the device in the same chip. This is because it is not easy to connect the device electrode at the base of the chip to the control circuitry. Therefore, for smart power ICs (device and circuitry integrated on the same chip), the devices must be quasi-vertical or lateral, with both the electrodes at the top surface of the chip. Many various designs of such devices can be found in literature, using SOI, as well as bulk technology.

Recently, Udrea et al. [7] have shown that fabricating lateral SOI power devices on membrane structures greatly improves the power device performance. Removing the substrate from underneath spreads the potential lines more evenly across the drift region

in the off state mode (when the device is not conducting). This greatly increases the breakdown voltage of the device (by as much as 20 times). Additionally, the switching speed of the device also increases. This is because the substrate is one of the sources of parasitic capacitance in the device. Removing the source greatly reduces the parasitic capacitance, lowering the switching time (achieving a turn off time of 40ns). Finally, the use of SOI technology results in excellent isolation of the power devices from the control circuitry on the chip, making the integration of such circuitry much easier.

However, this improvement in performance comes at a price. The presence of the membrane isolates much of the devices from the bulk substrate and hence restricts the heat flow from the device. The heat flow path is along the membrane which is thin, and has low thermal conductivity. This means that the device now operates at a higher temperature. This is an undesirable effect, as high temperatures reduce the long term reliability of the device (above 50°C, the failure rate for a device doubles for every 10-15°C rise [13]). Therefore, it is important to study the thermal effect in these membrane devices to create improved designs so as to reduce the device operating temperature.

Summary

Membranes are finding applications in many different devices. Integrating these devices with interface electronics on the same chip to form a smart device offers great advantages by lowering cost, as well as the size of the final system. Such integration however, can be challenging as care must be taken that the device fabrication is compatible with standard processes used for circuit fabrication. Care must also be taken to ensure that during operation, the device is well isolated from the circuitry. For example, it should not cause over heating in the circuits.

Two of these devices are micro gas sensors, and power devices. Micro-gas sensors need a heater to heat the sensing material to a high temperature to improve the sensitivity. A membrane greatly enhances the thermal isolation of the heater, and so reduces the power consumption. Using SOI technology gives more flexibility in the design, and the buried oxide acts as a natural etch stop during the bulk etching process. The circuitry on

SOI can also work at higher temperatures (as high at 225°C), allowing the use of the smart sensor in high temperature environments.

Using a membrane for SOI LIGBTs greatly increases the breakdown voltage, and improves the switching time of the device. The use of SOI allows better isolation between the power device and the on-chip control circuitry. However, the membrane reduces the heat flow path from the power device, which can result in higher operating temperatures. Additionally, the membrane is fragile, and can be broken at high mechanically stresses, such as those encountered during packaging.

Thesis Outline

This thesis analyses the thermal and mechanical aspects of both the gas sensors, as well as the power devices. In chapter 2, a brief overview of micro-hotplate designs found in literature is given, and a novel tungsten based SOI micro-hotplate is proposed. A thorough thermal analysis of micro-hotplates for gas sensors is presented, including simulations as well mathematical modeling. Power consumption, transient time and temperature uniformity are taken into account

Chapter 3 details the final design and fabrication of the micro-hotplates. Electrothermal results of the measurement are presented showing extremely low power consumption (14mW at 600°C) and fast transient times (2ms to 600°C). The simulations are then matched to the measured results by properly determining the material properties. Finally, mechanical profile measurements are also presented.

Chapter 4 presents an analysis of the membrane power devices. A quick overview of the device structure and working is given, followed by 2D and 3D electrothermal simulation and mathematical analysis. Thermo-mechanical simulations regarding the stresses encountered during packaging are also presented.

Chapter 5 gives the final conclusions and the scope for further work for improvement in both the micro-hotplates, and the membrane power devices.

Chapter 2

Gas Sensors – Initial Design and Analysis

Micro-hotplates in Literature

Micro-hotplates are needed in silicon based gas sensors to raise the temperature of the sensing material (up to 600°C depending on the material and target gas). Micro-hotplates consist of a micro-heater fabricated on a membrane formed by bulk etching. The membrane thermally separates the heater from the rest of the chip resulting in lower power consumption and good thermal isolation. For resistive gas sensing, electrodes (usually interdigitated) are fabricated on top of the heater area. The gas sensing layer is deposited on top of the electrodes, and the electrodes are used to measure its resistance. For calorimetric gas sensing, sensing electrodes are not needed, but a catalyst (such as palladium) is deposited within the heater area.

A micro-hotplate should ideally have:

1. Low power consumption: This allows micro-hotplate use in portable and wireless applications.
2. Small Size: This is important for portability, and also greatly reduces the cost, as less chip area is used.
3. CMOS Compatibility: This reduces the overall fabrication cost, and allows easy integration of interface circuitry

4. Fast heat up and cool down times: This can allow operation in pulsed mode, to further reduce power consumption. It also allows modulation of temperatures for better selectivity.
5. Uniform temperature in the heater area: This gives good accuracy, as all of the sensing material should be at the same temperature.

Micro-hotplates can be based on conventional closed membrane structures, as well as on suspended membranes [6]. Both approaches are abundantly found in literature. Dibbern [23] for example fabricated closed membrane microhotplates by first depositing a layer of oxynitride onto a silicon chip. This was followed by the deposition and patterning of a NiFe film to form the heater. Following passivation and the deposition of sensor electrodes, the membrane was released by bulk etching with KOH up to the oxynitride layer to form the micro-hotplate. A similar approach, using platinum as a heater material has also been employed by several groups [24,25,26,27]. Platinum has the advantage of being able to withstand high temperatures.

Micro-hotplates based on suspended membranes have also been reported by various groups for different designs. Fung et al. [28] for example, fabricated micro-hotplates by P+ doping of a silicon substrate to form a silicon P+ heater. This was followed by the deposition and patterning of layers of dielectric silicon oxide and aluminum contacts. Openings in the dielectric were made to expose the bulk silicon. The bulk silicon underneath was then etched away using EDP to release the membrane with four supporting beams. Tsamis et al. [29] used a design of a platinum heater on a membrane made of porous silicon using plasma etching. Furjis et al. [30] have designed micro-hotplates using platinum heaters embedded within suspended membranes made of silicon nitride, however theirs is a bridge structure supported by only 2 beams.

Micro-hotplates based on suspended membranes can have very low power consumption because of their reduced conduction path to the silicon substrate. Indeed, Elmi et al. [31] have reported micro-hotplates based on micro-bridges with power consumption as low as 8.5mW at 400°C (the results were for membranes without passivation). However, because they are supported by only 2 or 4 beams, they tend to be

less mechanically stable. The high deflection of these membranes when heated up can create reliability problems.

In general the micro-hotplates reported in literature have power consumptions at 300°C in the range 6.5mW – 150mW, with most micro-hotplates being within the range 70-100mW. The thermal transient times are very low, typically 10ms, which is to be expected as the size is very small.

These designs however, are not CMOS compatible, and there are very few CMOS designs found in literature. CMOS compatibility allows the fabrication of the sensors using standard microelectronics fabrication technology. This greatly reduces the manufacturing cost, and also allows interface circuitry to be integrated on the sensor chip [32]. However, making CMOS compatible devices places constraints on the design. CMOS processes usually have a very small number of available materials, and the thicknesses of various layers are fixed. For example, platinum, a popular choice for the heater in micro-hotplates, is not available in CMOS processes. Therefore micro-hotplates have to be designed with the constraints of the particular CMOS process used.

A few groups have fabricated micro-hotplates using commercial CMOS processes, such as Suhele et al. [33], Udrea et al. [34], and Graf et al. [35].

Suhele et al fabricated micro-hotplates with suspended membranes using polysilicon heaters. They used a standard CMOS process to fabricate a polysilicon heater, an aluminum temperature sensor and sensing electrodes using the top aluminum layer. The same process also allows them to leave exposed areas of silicon on the chip – allowing a maskless front etch using EDP to release a suspended membrane. At 300°C the heaters consume 40mW of power. The use of aluminum in these heaters limits the maximum operating temperature of the micro-hotplates, as aluminum has a low melting point (660°C) and suffers from electro-migration at high temperatures. In addition, polysilicon also has poor long term stability [36]. A later design by the same group [37] uses gold electrodes formed by post processing instead of aluminum and integrates some interface circuitry, showing the advantage of using CMOS processes.

Udrea et al. fabricated novel micro-hotplates based on MOSFET heaters using SOI technology. MOSFETS allow easy control of the temperature via the gate by restricting the current flow. SOI technology gives the flexibility to be able to isolate a MOSFET on

a membrane easily as the buried oxide acts as a natural etch stop. MOSFETs fabricated in SOI technology can operate at higher temperatures compared to those fabricated on bulk silicon. The hotplates consume about 70mW at 200°C (This scales to approximately 110mW at 300°C). Nevertheless, they do not operate very reliably above 400°C. This is because the high temperature triggers the parasitic bipolar in the MOSFET, causing it to lose gate control.

Graf et al. have fabricated micro-hotplates using polysilicon heaters. Instead of using aluminum for the gas sensing resistive electrodes, they have used a post-CMOS deposition of platinum to form the resistive electrodes, as well as a temperature sensor. This allows the micro-hotplate to operate at higher temperatures than possible with aluminum. This is followed by the deposition of a low stress silicon nitride layer to passivate the platinum tracks, as well as reduce stresses in the membrane. In addition, the silicon just below the heater region is doped heavily, and this region is not etched during the bulk etch of the silicon. This results in the formation of a silicon heat spreading plate for better temperature uniformity. The micro-hotplates consume about 70mW at 300°C. However, again the use of polysilicon can reduce the long-term stability of the micro-hotplates.

Proposed structure for Micro-hotplates

Results reported in literature show that micro-hotplates can be used for gas sensing at lower power consumption. These can also be fabricated on CMOS technology along with integrated circuitry. However, CMOS micro-hotplates reported in literature are based on either polysilicon or MOSFET heaters, neither of which operate reliably at high temperatures [34,36].

This can be overcome by the use of tungsten resistive heaters [38]. Tungsten is used as a high temperature interconnect metal in some SOI-CMOS processes, and as a material is ideally suited for micro-hotplates. Unlike aluminum, it does not suffer from electro-migration, has a very high melting point, and has good mechanical strength (which can help strengthen the membrane of a micro-hotplate).

The use of SOI technology allows greater flexibility in the design of micro-hotplates. For example, a thin silicon spreading plate can be designed, or diode temperature sensors can be easily incorporated within the structure. In addition, the interface circuitry fabricated on SOI technology can operate at much higher temperatures as compared to those fabricated on bulk CMOS. This allows the gas sensor to be used in high temperature environments.

The proposed structure is shown in Figure 7. During the fabrication of the interface circuitry, the tungsten metal layers (used as interconnect in CMOS circuitry) are used to form the heater, a heat spreading plate, and the tungsten resistive electrodes. Back etching using Deep Reactive Ion Etching (DRIE) is then used to release the membrane followed by the deposition of the gas sensing layer.

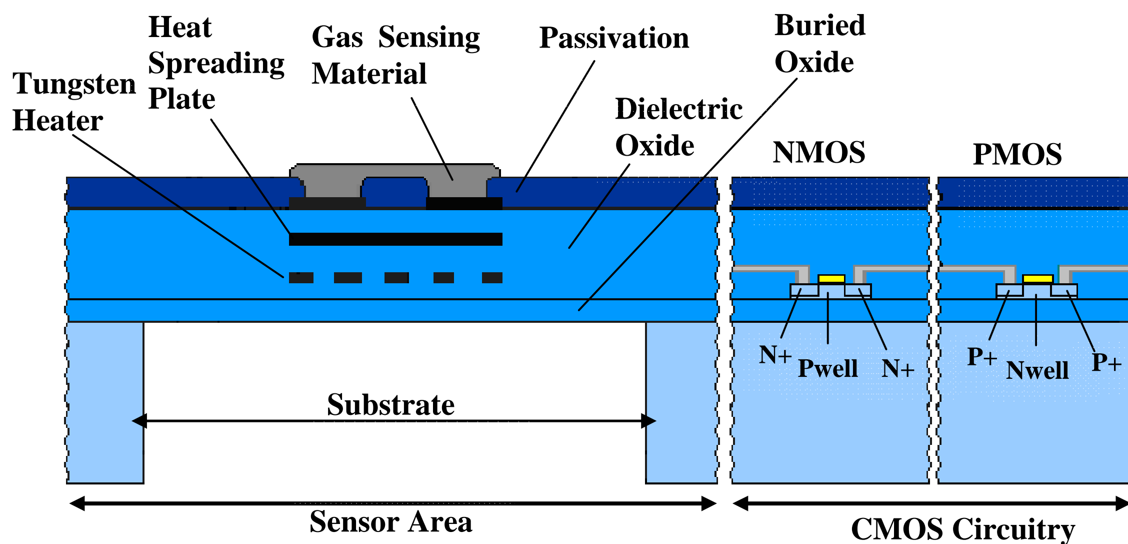


Figure 7: Proposed structure: Gas sensor and integrated CMOS circuitry

To design the micro-hotplates, various aspects of micro-hotplates were first studied. Some preliminary 3D electro-thermal simulations were performed in ANSYS to determine the feasibility of the design. This was followed by extensive simulations and analysis, using actual fabrication constraints, to determine the effect of shape and size to various characteristics of the heater, such as power consumption and temperature uniformity.

Finally, using the results obtained, micro-hotplates were designed and simulated. The layout for the designs was done using Cadence (icfb version 5.0.0), and the devices were fabricated at a CMOS foundry, followed by DRIE at a MEMS foundry. The micro-hotplates were then characterized and the results were matched with simulations.

Aspects of Micro-hotplate Design

Power Consumption

Power consumption is one of the most important aspects of micro-hotplate design. It is, in fact, the reason that heaters are fabricated on a membrane. The membrane thermally isolates the heater – considerably reducing the power consumption. Here the various sources of heat loss in a micro-hotplate are analyzed as well as their dependence of various design parameters.

There are 3 sources of heat loss in a micro-hotplate:

1. Conduction
2. Convection
3. Radiation

Conduction:

In micro-hotplates, conduction losses are losses due to the flow of heat through the membrane layers to the base of the chip. Packaging of many micro-electronic chips (especially those for gas sensors) is by fixing the base of the chip to a package housing using a die-attach material (mostly epoxy).

During operation, therefore, the path of heat flow is to the base of the chip, via the die-attach, into the package. The heat then flows out either through the package pins, or to the surrounding air by convection (since the area of the package is much larger than the chip, the heat flow to air is mostly through the package rather than directly from the

chip). In micro-hotplates, because the power generated is very small, it can usually be assumed that base of the chip is at room temperature.

Electrothermal simulations of the micro-hotplates in ANSYS were used to analyse the conduction losses. The micro-hotplate structure initially analysed is shown in Figure 8. The structure consists of a meander-shaped tungsten heater on top of a silicon dioxide membrane, which is supported by a silicon structure. When a potential difference is applied across the heater, heat is generated through Joule heating, resulting in a temperature rise in the micro-hotplate.

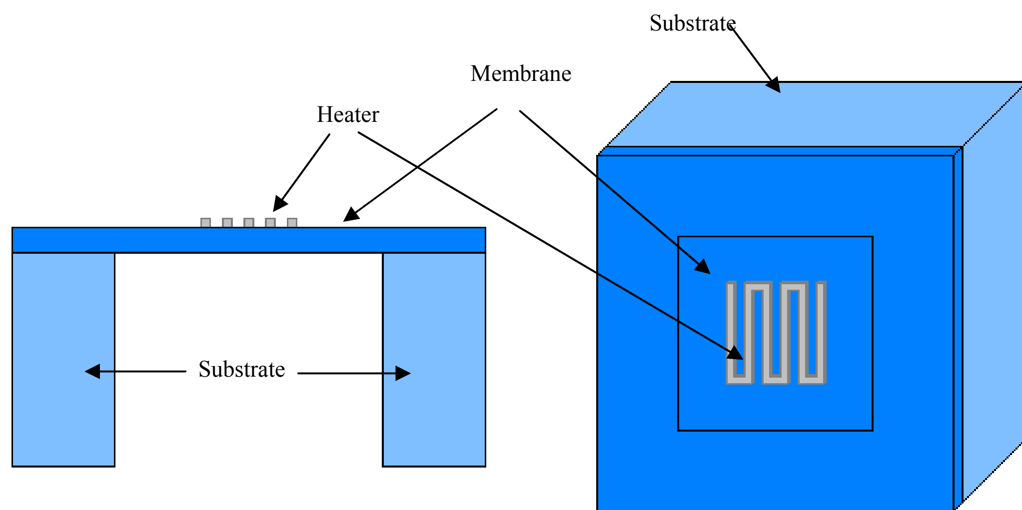


Figure 8: Micro-hotplate Structure

The structure is rectangular, with a membrane area of 500 X 500 µm, and a heater area of 300 X 300 µm. The meander heater consists of 6 vertical lines, with a width of 3µm, and a gap of 51µm between lines. Such a configuration for the heater ensures that the 300 X 300µm heater area is covered, and that the voltage required is near 5 V (to make it suitable for interface with CMOS circuitry). Additionally, an even number of lines ensures that the contacts are on the same side.

The substrate is 400µm thick, the oxide thickness is 3µm, and that of tungsten is 0.3µm. The layers used in this initial simulation are not the same as those available in the commercial process. However, they are easy to simulate, and adequate for preliminary simulations. In the initial stages of the simulations, the actual process layers were not

available, as they are confidential to the foundry. Since the other dimensions (heater and membrane width etc) are similar to the eventual design that is to be fabricated, this structure gives some idea of the feasibility of using tungsten based SOI micro-hotplates.

Unlike wet anisotropic etching, deep reactive ion etching allows easy formation of circular membranes. This is because DRIE is not dependent on crystal orientation, which are flat, and do not allow rounded structures with KOH or EDP. Circular micro-hotplates therefore, are also an option, as they result in better mechanical stability because there are no sharp corners where the stress is concentrated. Therefore a circular structure was also analysed. To keep the heater and membrane areas the same as that of the square structure, radii of 170µm and 280µm respectively were used. The meander shape of the heater was changed so as to fit inside the circle (Figure 9).

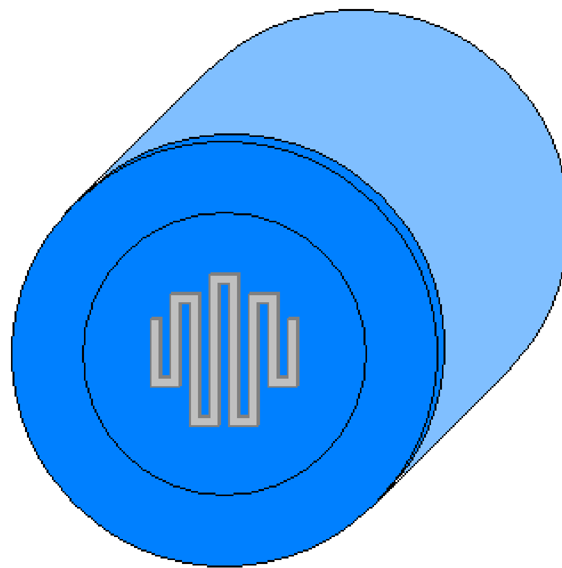


Figure 9: Circular Heater Structure

Two small structures were also simulated. The first is a square structure, with a heater area of 20x 20µm, and the membrane area of 50 x 50µm. Again a meander heater is used, with 10 lines, and widths and gaps of 1µm. The second was a circular structure with a heater radius of 11.2 µm (Corresponding to a rectangular area of 20 x 20µm), and a membrane radius of 26.2µm. The heater was again a meander shape, fitted to a circle. In both the smaller structures, the substrate thickness of 100µm was used.

Simulations

The simulations were performed in ANSYS 8.0. ANSYS is an FEM (Finite Element Method) software, allowing coupled field analyses of electrical, thermal, mechanical and magnetic domains, as well as fluid analysis. Both static, as well as transient analysis can be performed.

The properties of the materials used are shown in Table 1 (only the thermal conductivity of the materials was used in the static simulations. Density and specific heat capacity are only needed for transient simulation, which were performed later):

Material	**Thermal Conductivity (W/mK)**	**Density (kg m^{-3})**	**Specific Heat Capacity (J kg^{-1} K^{-1})**
Tungsten	177	19300	140
Silicon Oxide	1.4	2270	730
Silicon (Properties vary with temperature[1])	150 (at room temp)	2330	705-860

Table 1: Thermal properties of materials used in simlations (Taken from [39], [6], [40])

The initial analysis takes into account heat losses due to conduction only. The base of the heater is assumed to be at room temperature, and is fixed at 25°C. A potential difference of 4.5V was applied at the ends of the heater. The simulation takes only about 5minutes on a PC, and the result is shown in Figure 10.

As can be seen, the heater area heats up to a temperature of about 700°C. Interestingly, the chip area outside the membrane barely heats up. This is because silicon has a much higher thermal conductivity than silicon oxide (about 100 times more). Therefore, since the same amount of thermal energy is flowing through both, the temperature gradient within the membrane is much, much greater than the temperature

---

[1] The thermal properties tungsten and silicon oxide do not vary significantly with temperature, and so were assumed as constant. In silicon, however, the properties vary significantly with temperature so this dependence was taken into account.

drop in the substrate. This means that any interface circuitry fabricated outside the membrane will function as normal, and will not be affected by the high temperature of the micro-hotplate.

The current density through the heater can also be determined from ANSYS. Since it is uniform at the centre of the lines, rather than the corners, the current density at the centre of the lines was taken, and multiplied by the cross-section area of the tracks to determine the current flowing. This is multiplied by the voltage (4.5V in this case), to determine the power consumption, which comes out to 48.2mW. Thus a temperature in excess of 700^{0}C was obtained with a power of only around 50mW.

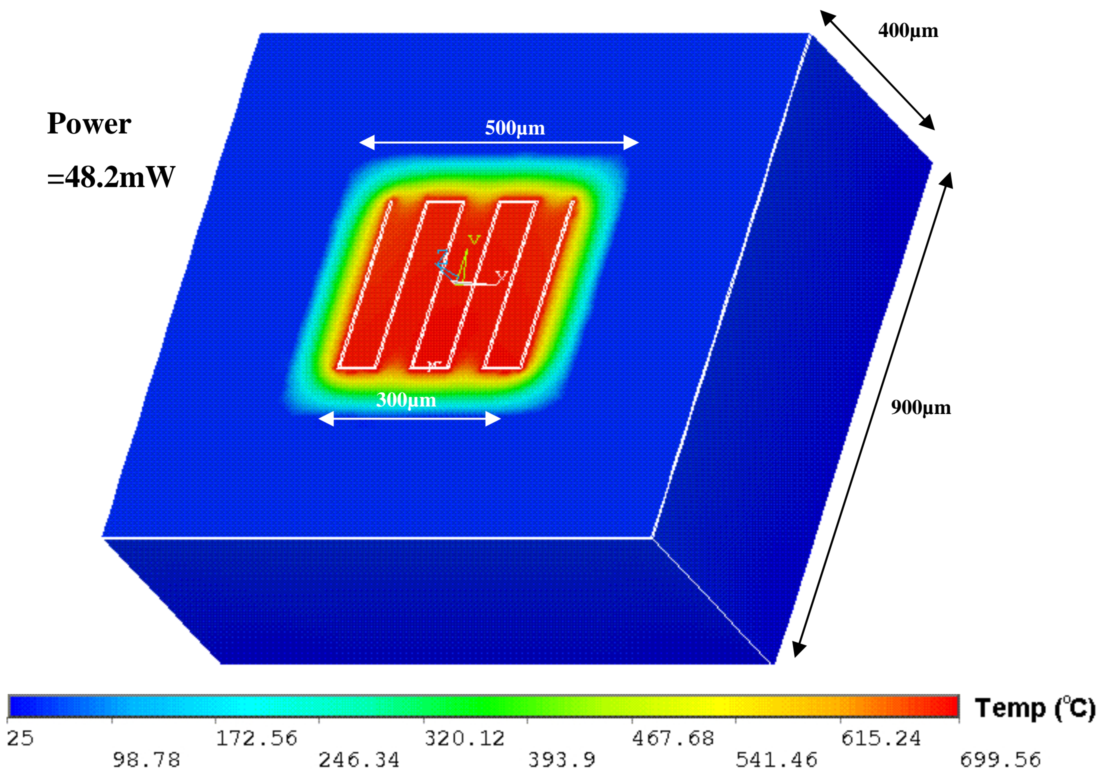


Figure 10: Temperature profile for Large Square Structure

Different potential differences from 1 to 5V were applied to the heater, and the resulting power vs maximum temperature graph is plotted in Figure 11. This is a straight line: the power consumption being proportional to the temperature rise.

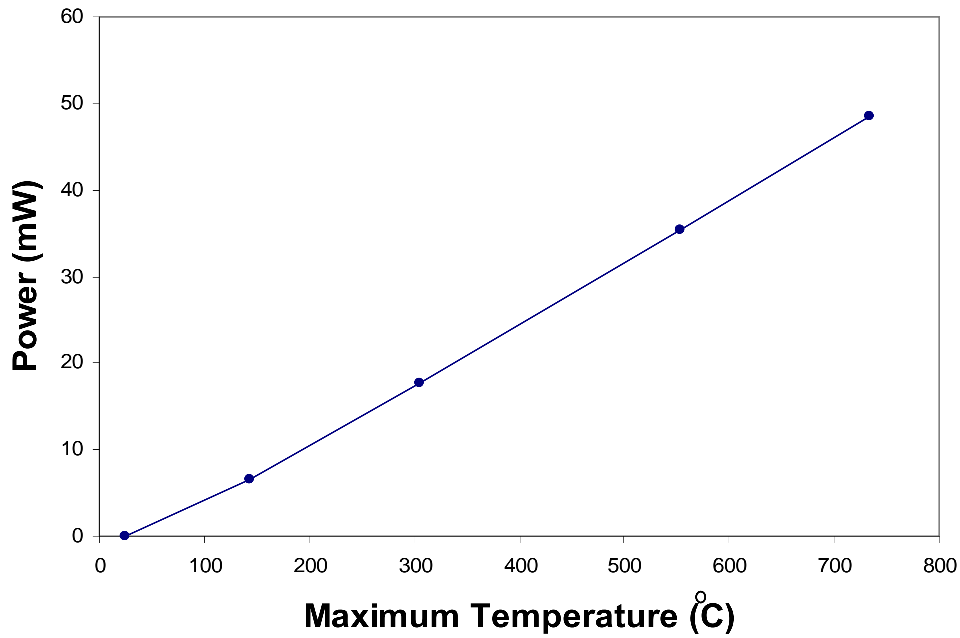


Figure 11: Power vs Maximum Temperature Graph for Large Square Heater

Simulations were also performed on the other structures. Results are shown in Figure 12-Figure 14. The power vs maximum temperature graphs for all four structures are shown in Figure 15.

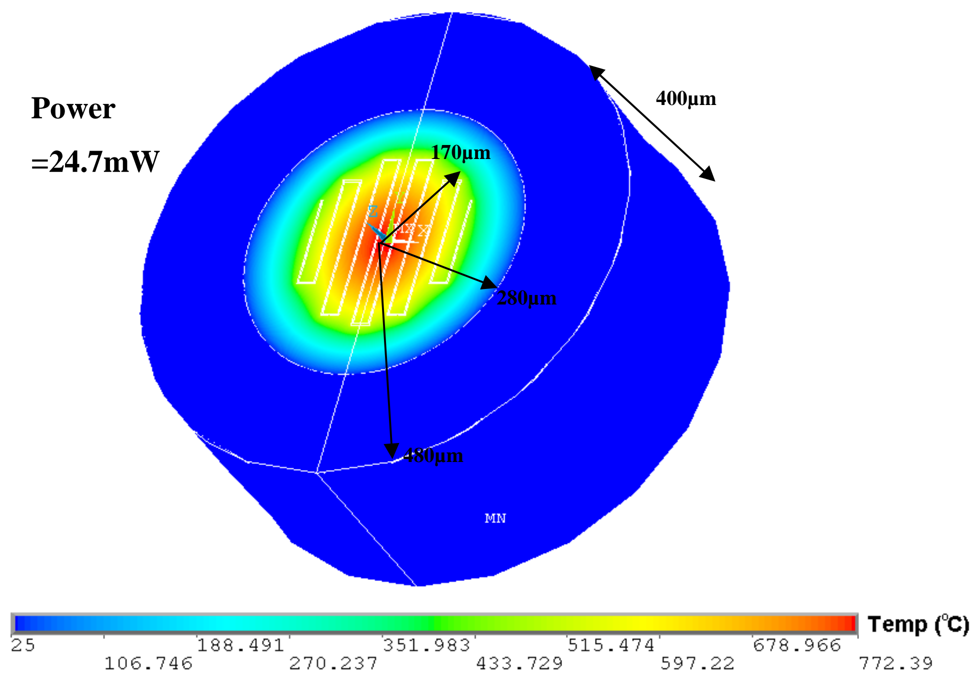


Figure 12: Large Circular Structure

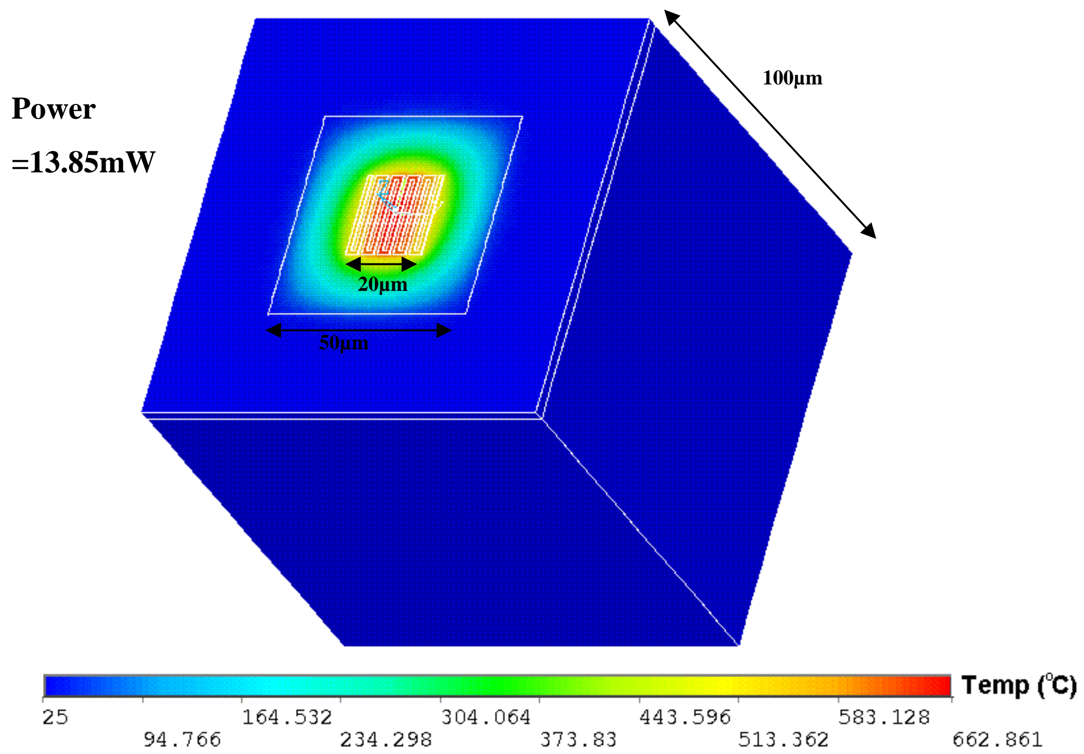


Figure 13: Small Square Structure

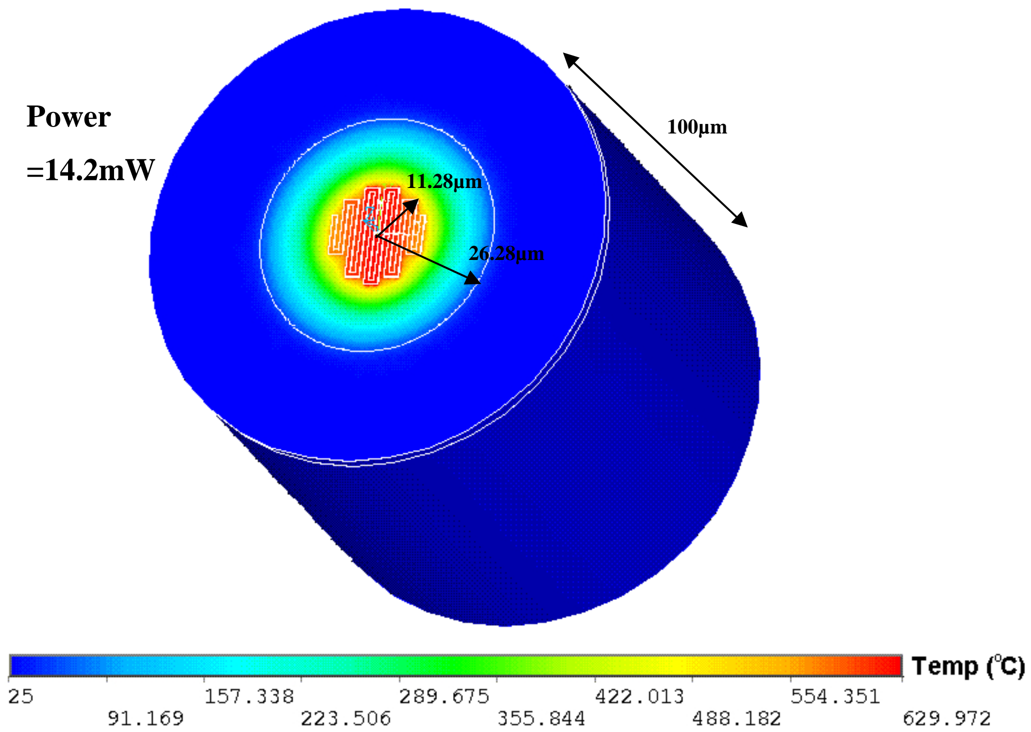


Figure 14: Small Circular Structure

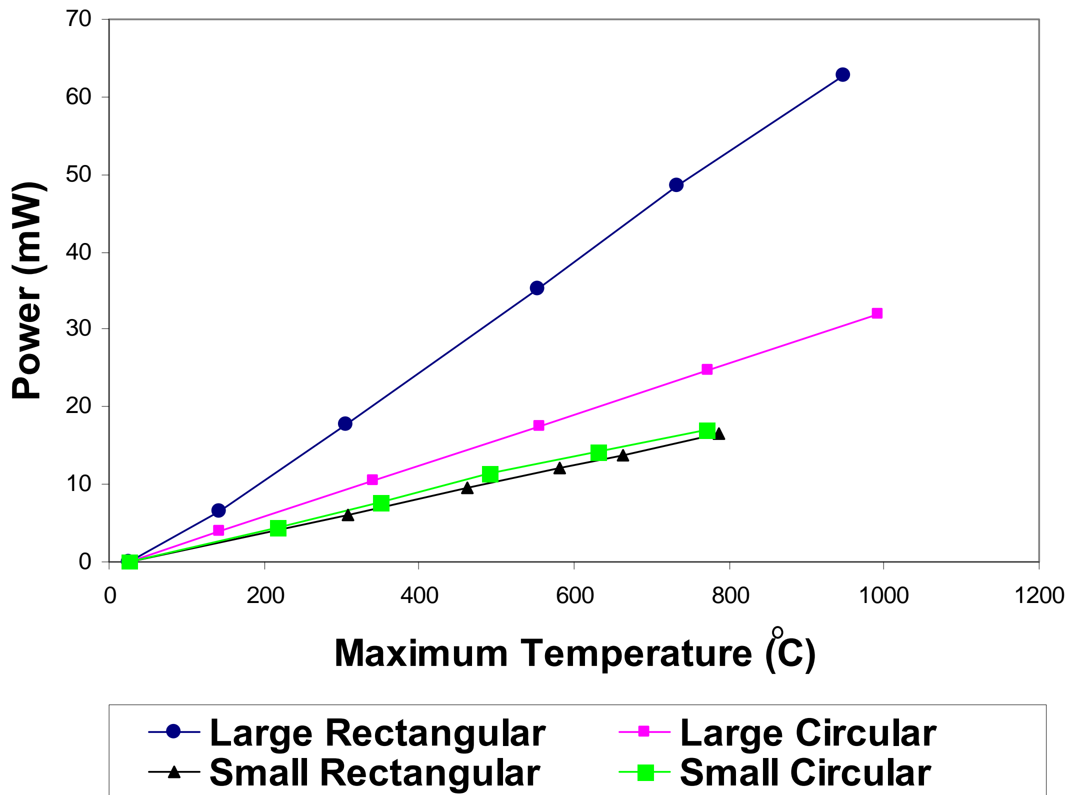


Figure 15: Power Consumed vs Max Temperature

These initial simulations show that tungsten based SOI micro-hotplates can be used for micro gas sensors, as they have low conductive heat loss less than (50mW at 600°C, and only 10mW for the smaller dimensions). Although convection has not yet been taken into account, the power consumption is low (especially for the smaller heaters).

Mathematical Analysis:

Mathematical analysis of thermal conduction was performed on the circular structure to verify the results of simulation as well as to gain a better understanding of the heat conduction process, to aid in better heater design.

The equation for steady-state heat conduction is:

$$W = kA\frac{dT}{dL} \tag{1}$$

where:
W is the power conducted
k is the thermal conductivity
A is the area
T is the temperature
L is the length

However, another method often used is to treat thermal conduction in a similar manner to electrical conductivity [41]. Consider eq(1) for a cuboidal slab of material. Since k and A are constant along the length of the slab, the equation reduces to:

$$WL = kAT$$

$$T = W\frac{L}{kA}$$

Compare this with the equation of electrical conductivity:

$$V = IR$$

$$V = I\frac{\rho L}{A}$$

$$V = I\frac{L}{\sigma A}$$

where:
V is potential difference
I is current
R is resistance
L is length
A is area
ρ is electrical resistivity
σ is electrical conductivity

The basic forms of the electrical and thermal equations are similar. This means that thermal conductivity can be treated in a manner analogous to electrical conduction.

Therefore, temperature can be treated as a 'voltage', while power dissipated can be treated as a 'current' [2,41]. The term L/kA can be treated as a thermal resistance.

Now consider the circular micro-hotplate structure. The heat flows from the heater (radius r_1) to the edge of the membrane (radius r_2), and then through the silicon substrate to the base. The thermal resistance of the silicon substrate is much lower than that of the membrane. The simulations have also shown that most of the temperature drop is within the membrane. Therefore, the thermal resistance of the silicon substrate may be assumed negligible.

Therefore, only the conductivity within the membrane needs to be considered between the radii r_1 and r_2. The thermal resistances of square membranes are often approximated by treating them as circular membranes, and [6] shows how to calculate the thermal resistance of a circular membrane. This is done by beginning with a ring within this area of small width (dr). The thermal resistance of this ring is:

$$dR = 1/(2\pi rkt)dr$$

where t is the thickness of the membrane.

Integrating from r_1 to r_2

$$R = \int_{r1}^{r2} 1/(2\pi r\alpha t)dr$$

$$R = \frac{1}{2\pi\alpha \cdot t}\ln\left(\frac{r2}{r1}\right) \qquad (2)$$

Since the thermal resistance of the silicon substrate is negligible, the temperature at the edge of the membrane (r_2) can be assumed to be 25°C, the same as the temperature at the base of the silicon substrate. Therefore if the temperature at the edge of the heater region (at r_1) is T_h, and the total power dissipated is P, then:

$$T_h - 25 = \frac{1}{2\pi\alpha \cdot t}\ln\left(\frac{r2}{r1}\right) \cdot P$$

$$P = \frac{2\pi kt(T_h - 25)}{\ln \frac{r_2}{r_1}} \quad (3)$$

The resistance of the small circular structure is calculated using this formula, and comes out to be 32 x10^3 K/W. The power generated by the heater was 14.2mW. Therefore the temperature difference in the membrane area should be around 455°C. In the simulation, the temperature at the edge of the heater (which is different from the maximum temperature) was approximately 500°C, meaning a difference of about 475°C, which is close to the calculated value. Similarly for the large circular structure, the thermal resistance is 17614 K/W, and for 24.7mW of power, the temperature at edge of heater should be 460^{0}C, which is the case for the simulations.

Equation 3 also shows that as far as thermal conduction is concerned, the power loss depends only upon the ratios of the heater and the membrane radii. Looking at Figure 15, one might possibly reach the mistaken conclusion that conductive heat losses depend on the membrane size. However, equation 3 shows that this is not so, and only the ratios of r_1 and r_2 matter. In Figure 15, the larger heaters have a lower r_2/r_1 ratio, thus resulting in higher power consumption.

Therefore if the r_2/r_1 ratio is small, the power loss is higher, while if it is large, the power loss is lower. This means that r_1 (and thus the heater area) should be as small as possible, and that r_2 (and thus the membrane area) should be as large as possible

The radius r_1 cannot be reduced indefinitely. The gas sensitive material is deposited over the heater area. If the heater area is very small, then the amount of material deposited is small, and the surface area in contact with the air is small. So the sensitivity is reduced. Therefore a smaller heater area means less sensitivity, and a larger heater area means greater power loss. Hence a compromise is needed between the two.

Similarly, the membrane area cannot be increased indefinitely either. A larger membrane is less mechanically stable, and more likely to rupture, either during fabrication, or due to stresses caused by heating. Additionally, a larger membrane area means that a larger chip space is occupied. Thus either the space for additional circuitry is

reduced, or a larger chip size is used, resulting in a higher cost per chip, and lower manufacturing yield (functional chips/total chips per wafer).

Consider the graph of $y=1/(\ln(r_2/r_1))$ vs the ratio r_2/r_1:

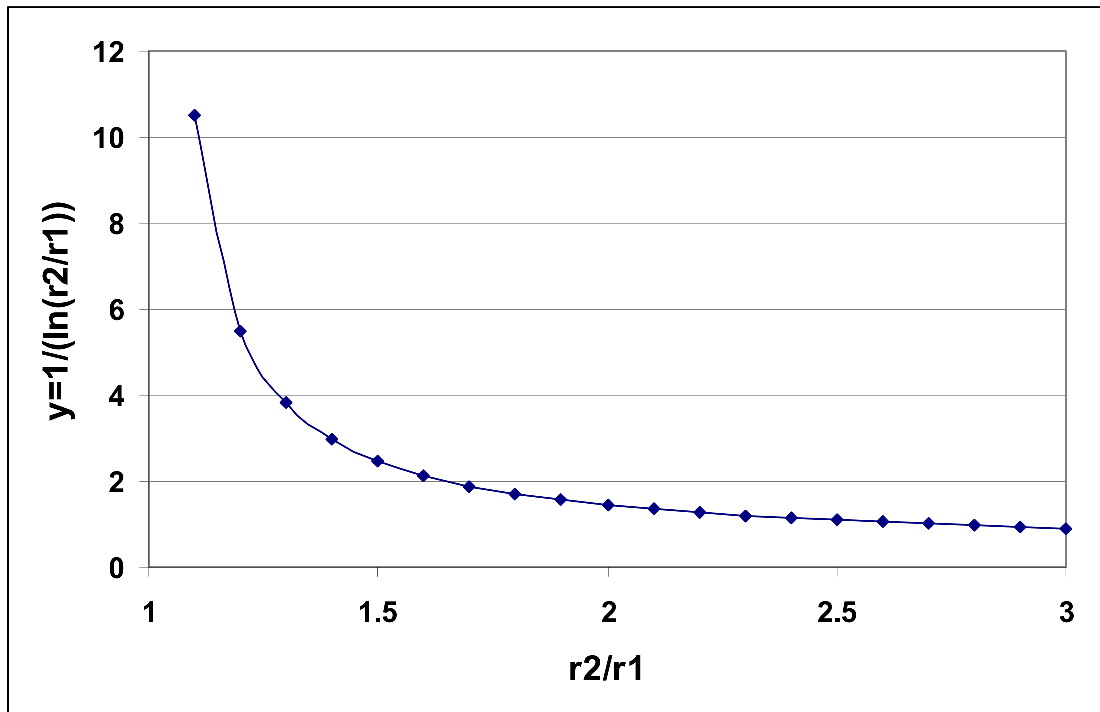


Figure 16: Plot of $y=1/(\ln(r_2/r_1))$ vs r_2/r_1

The graph shows that as the ratio r2/r1 increase, initially y drops quickly, but afterwards, an increase in the ratio does not have much effect on y. Since this function is similar to the power required in equation 3, the result for power in a micro-heater will be similar. Therefore, there best ratio to use is one after which there is no significant drop in power.

First suppose r2 is fixed. Then, what is the optimum value for r1? As r1 increases, the power consumed increase. However, the area heated also increases. So is there an optimum value for power/heated area?

From equation 3, the power is given by:

$$P = \frac{2\pi kt(T_h - 25)}{\ln\frac{r_2}{r_1}}$$

The heated area is $\pi(r_1)^2$. So the power per area is:

$$p = \frac{T - 25}{\pi \cdot \mathbf{r}^2 \cdot K \ln\left(\frac{r_2}{\mathbf{r}}\right)}$$

where, p is power per heated area, and $K = \frac{1}{2\pi k \cdot t}$, while **r** is used instead of r_1 to denote it as the variable of interest.

Therefore for a minimum value of power per area:

$$\frac{dp}{d\mathbf{r}} = \frac{T}{K\pi}(-1)\left(\mathbf{r}^2 \ln\left(\frac{r_2}{\mathbf{r}}\right)\right)^{-2}\left(2\mathbf{r}\ln\left(\frac{r_2}{\mathbf{r}}\right) - \mathbf{r}\right) = 0$$

This simplifies to:

$$\mathbf{r} = \frac{r_2}{e^{0.5}} \tag{4}$$

This then is the optimum value for r_1 for a given r_2.

Now, suppose r_1 is fixed. Increasing r_2 reduces the power loss, but increases the area occupied. Therefore a minimum value of power x area is needed. This is given by:

$$p = \frac{\pi \cdot \mathbf{r}^2 (T - 25)}{K \ln\left(\frac{\mathbf{r}}{r_1}\right)}$$

The minimum for this is:

$$\frac{dp}{d\mathbf{r}} = \frac{\pi(T-25).r}{K}\left(\ln\left(\frac{\mathbf{r}}{r_1}\right)\right)^{-2}\left(2\ln\left(\frac{\mathbf{r}}{r_1}\right)-1\right) = 0$$

$$\mathbf{r} = r_1 \cdot e^{0.5} \tag{5}$$

This suggests that the ratio $r_2/r_1=e^{0.5}$ is the optimum to use. However, this can vary according to the requirements of the specific application, depending on the emphasis on the cost/sensitivity/power consumption required.

Simulation with actual device layers

Having achieved good results with the preliminary simulations, the two circular micro-hotplates were simulated again using the actual layers of the SOI CMOS process. The cross section of the structures simulated is shown in Figure 17. It is similar to the initial structures simulated, except that the tungsten heater is now embedded within the oxide layer, rather than being placed on top of it. In addition there is a layer of silicon nitride on top of the structure which acts as a passivation.

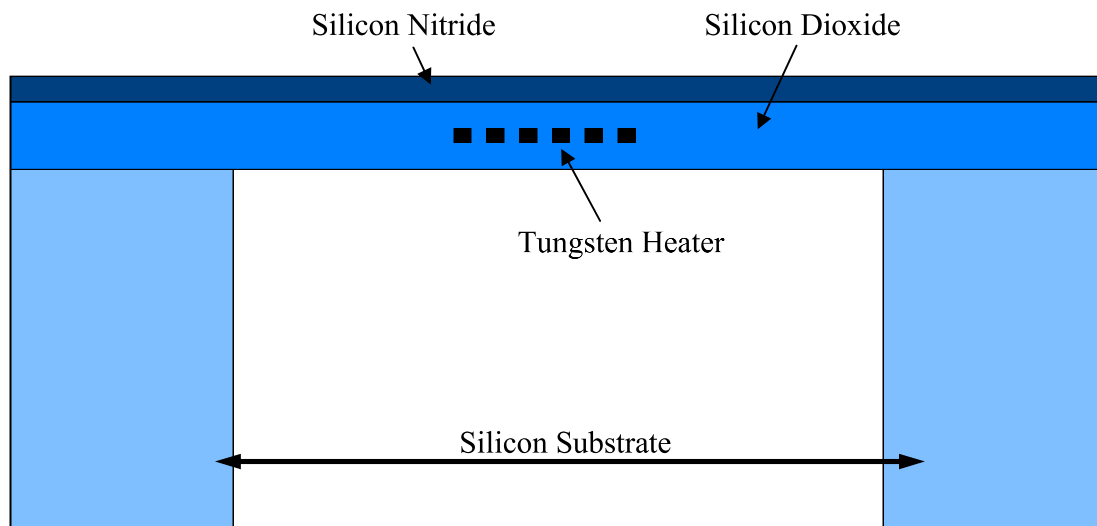


Figure 17: Cross-Section of actual device layers

The properties of Silicon Nitride used are:

Thermal Conductivity: 20W/mK

Density: 3440 kg/m^3

Specific Heat Capacity: 750 J/kg K

These values have been taken from various papers on micro-hotplates[6] [34] and used initially in our simulations

The simulated power consumption is shown in Figure 18.

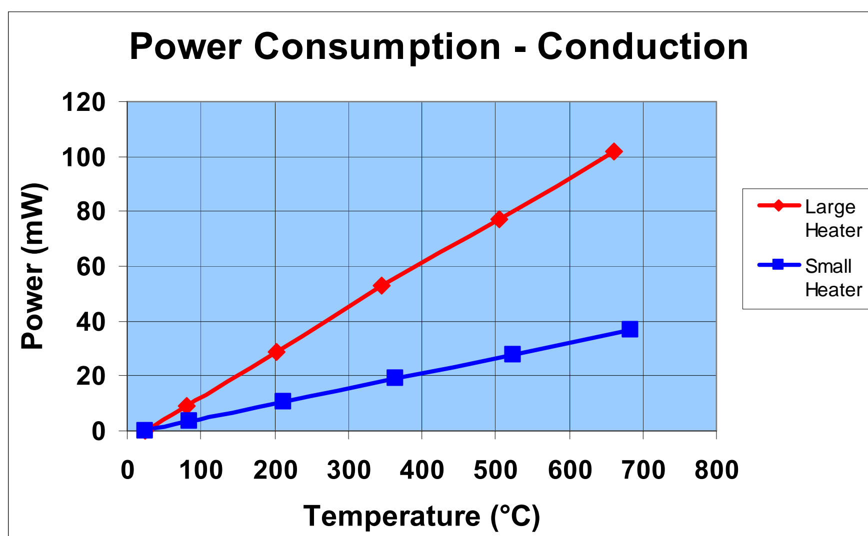


Figure 18: Power Consumption for the micro-hotplates simulated with actual fabrication layers.

The power consumption is much higher for these structures compared to those that were initially simulated. This is because of the presence of the silicon nitride layer, which has a much higher thermal conductivity than the silicon oxide. However, the power consumption is still low enough to be feasible, and a more optimized design (perhaps with a smaller heater area) can achieve lower power consumption.

Convection

Losses due to convection can form a significant part of the heat losses in a micro-heater. Therefore, they must be taken into account for a complete micro-hotplate design.

The heated membrane conducts heat to the surrounding air. This conduction is similar to the conduction in any solid, and is given by equation 1:

$$W = kA\frac{dT}{dx}$$

where:
W is the power loss
k is the thermal conductivity
A is the area
dT/dx is the temperature gradient.
x is the length

This conduction takes place at the solid-liquid interface. Once conducted to the air, however, the heat is primarily dissipated due to convection. That is, the air warmed by the membrane expands, and having a lower density rises.

This in turn increases the temperature gradient at the solid-air interface, resulting in a power loss much larger than due to simple solid to air conduction. These losses, in micro-hotplates are usually termed as convection losses.

Convection can be of two types, natural or forced.

Natural Convection is when there is no external flow of fluid. The primary force for fluid motion is due to the change in density caused by the difference in temperature.
Forced Convection is when there is an external flow of fluid (such as wind, or forced cooling systems).

This study only looks at natural convection. Forced convection is a result of the operating environment of the heater and would vary considerably in different

environments even for the same heater. Therefore a study of the forced convection is more suited when applying the sensors to a particular application.

Natural convection is usually given by Newton's law of cooling [42]:

$$P=hA(T-T_{amb}) \qquad (6)$$

Where:

P is the power loss

h is known as the convection coefficient

A is the area

T is the temperature of the surface

T_{amb} is the ambient temperature.

Determining h for micro-hotplates is not easy. At such small dimensions, surface and fringing effects come into play. h depends on the area of the micro-hotplate, as well as the geometry. ANSYS however, allows the simulation of fluid motion. Therefore, the motion of air above and below the membrane can be modeled. Using this, ANSYS automatically computes the convection coefficients, so there is no need to estimate them.

For simulation, two air regions were taken. One is the region below the membrane, to simulate the trapped air within. The other is a cubical region of air above the membrane of dimensions 2000 μm x 2000 μm x 2000 μm. Temperature and velocity boundary conditions were applied. In the air below the membrane the heat loss is not strictly due to convection, as the warm air cannot rise, rather the mechanism is conduction. Nevertheless, it is treated here as such since air in involved.

At all fluid boundaries of the air region below the membrane, no-penetration, no-slip conditions were applied [43], since this region of air is in contact with a solid throughout. No-penetration means that the fluid does not flow into the solid, so the perpendicular fluid velocity is zero. No-slip conditions mean that at the fluid-solid interface, there is no tangential motion, and so tangential velocity is zero. These conditions were also applied on the region of air above the membrane. Although this region is not enclosed in a solid, these conditions are necessary to avoid effects of forced convection. If the air region

simulated is large enough, then such conditions are valid, since the fluid flow due to natural convection affects only the air region close to the heater.

For the air region above the membrane, all boundaries (except those in contact with the membrane) were fixed at a temperature of 298K. This was not necessary for the region below the membrane, as the transfer conditions from the solid walls provided these conditions automatically. Gravity was assumed to be 9.81m/s^2 (this is needed for ANSYS to determine the rate at which the air rises). The temperature dependency of the thermal conductivity of air was also taken into account, as this varies considerably, from 0.026W/mK at 300K, to 0.063W/mK at 900K. When using simulation of fluids in ANSYS, the simulations are easier to do if Kelvin is used as the temperature unit, since most of the air properties in ANSYS have been tailored for a Kelvin temperature. Therefore, the simulations were done with temperature unit in Kelvin.

ANSYS does not allow direct coupling of electro-thermal analysis with fluid analysis. Therefore, the method used is to first simulate the electro-thermal analysis, then to transfer the temperatures to the air and run the fluid analysis, and then again to transfer the convection coefficients obtained to the electro-thermal analysis, and repeat the procedure until the solution converges. Because of symmetry, only half of the membrane structure was simulated. This saves time, but also improves the accuracy since a finer mesh can be used. There is a limit on the number of elements that can be used in ANSYS so for the full structure the mesh is too coarse. It takes about 15 minutes on a PC to run a simulation including conduction and convection for a single data point.

To ensure that a sufficiently large volume of the air above the membrane had been modeled, the simulations were repeated with an even larger volume. The results of both were similar, showing that the volume of air taken was large enough.

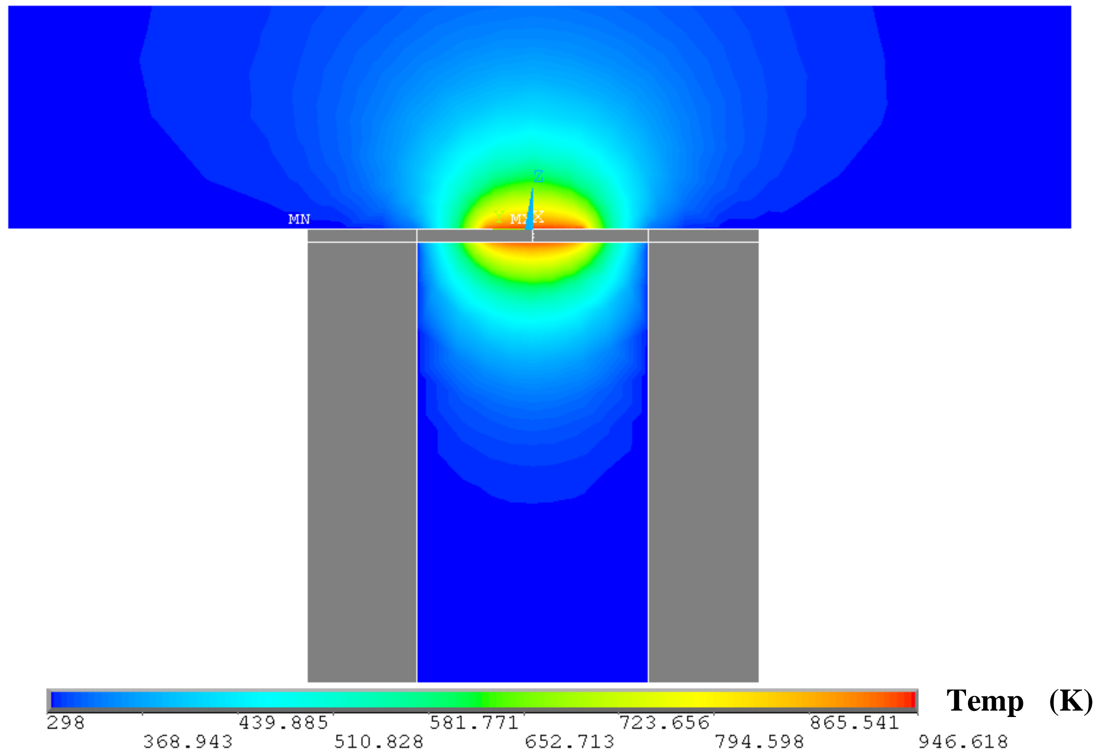


Figure 19: Temperature distribution in the surrounding air due to convection (For clarity, the whole of the simulated air above the membrane is not shown)

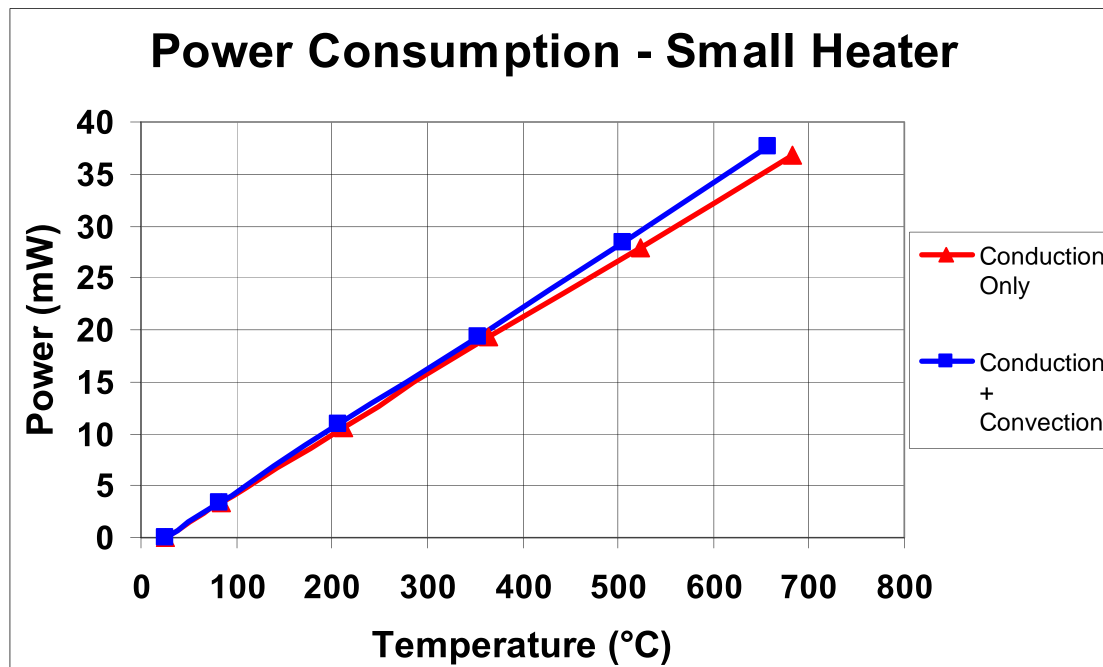


Figure 20: Convection power losses for small circular structure

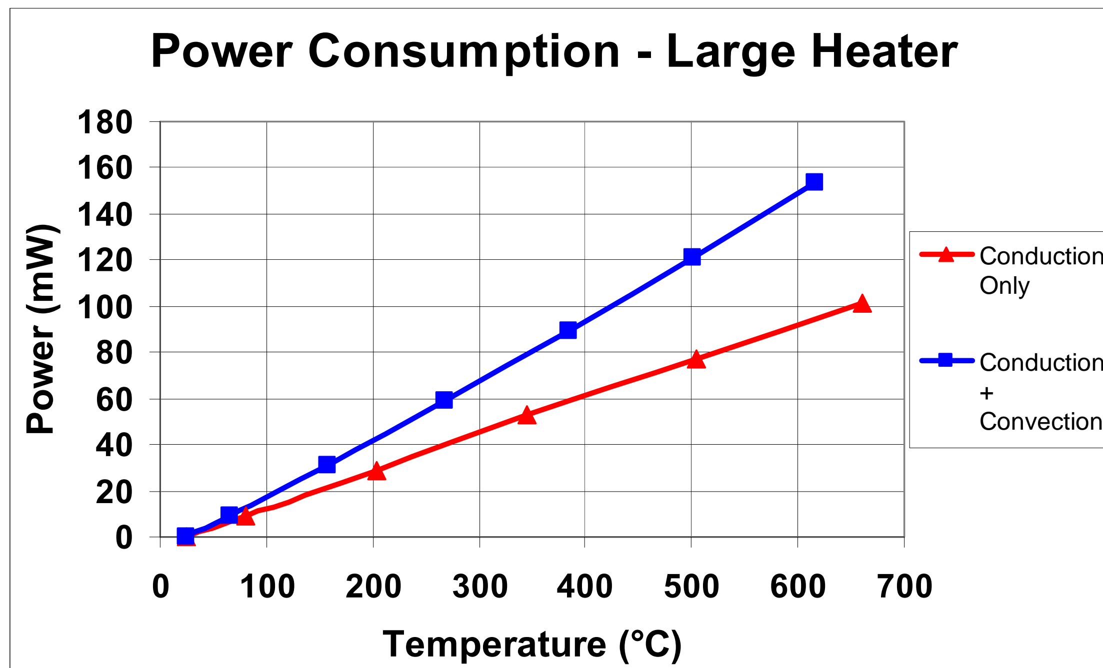


Figure 21: Convection losses for Large Circular Heater

Figure 19 shows the temperature distribution in the air surrounding the membrane. Figure 20 and Figure 21 show the effect of convection on the total power consumption. Convection losses in the small heater are very small compared to the conduction (2mW at 600°C due to convection compared to 32mW due to conduction). However, for the large heater, they are much more significant as the heater area is much bigger.

It is interesting to see how much of the convection losses are to the air above the membrane, and to the air below. If these are small enough, then they can be ignored in further simulations. Therefore, simulations were carried out on the structure, with only the losses due to the air below the membrane taken into account. The graph showing this power loss compared to the previous simulation is shown in Figure 22. It is interesting to note, that the power loss below the membrane is almost the same as above the membrane!

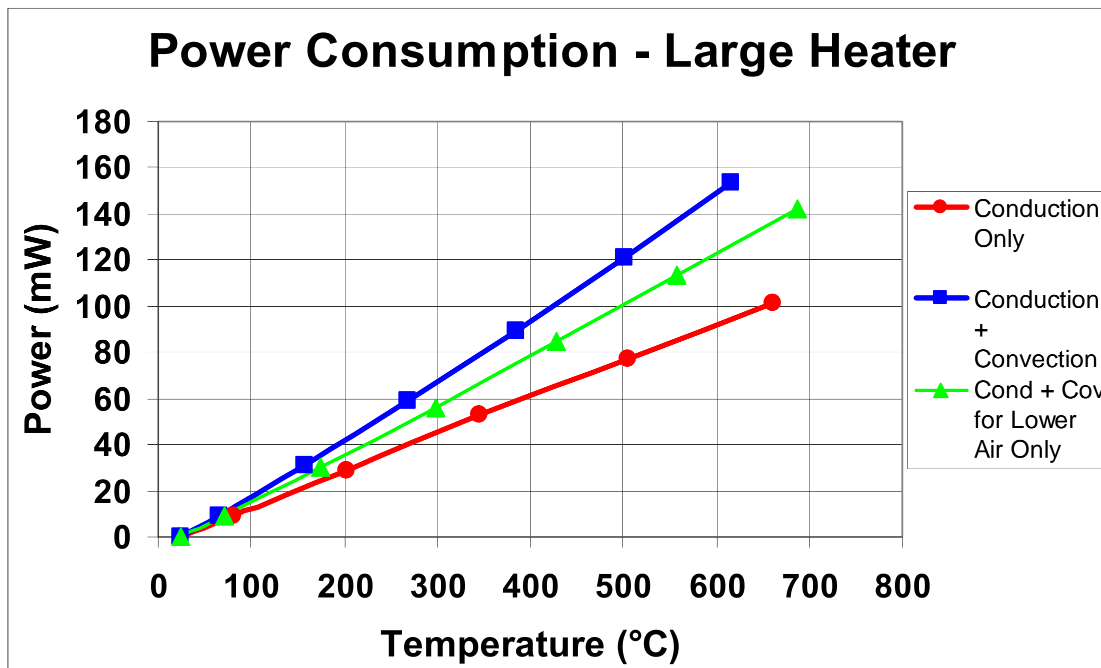


Figure 22: Power consumption for convection losses below the membrane, compared to total convection losses

This is not an expected result. Above the membrane, the heater air can rise, and thus can take the heat away more quickly. However, there is no such mechanism possible below the membrane. This can however, be explained by the fact that below the membrane, the heat is dissipated by conduction to the vertical sidewalls of the silicon substrate. Although the thermal conductivity of air is very low, the area of the heater, as well as the vertical sidewalls is very large, and can result in significant power loss. To verify this, another simulation was performed in which the power loss in the air below the membrane was treated as a conduction loss. The results compared to that due to convection are shown in Figure 23. The graphs are almost similar, and show this explanation to be correct.

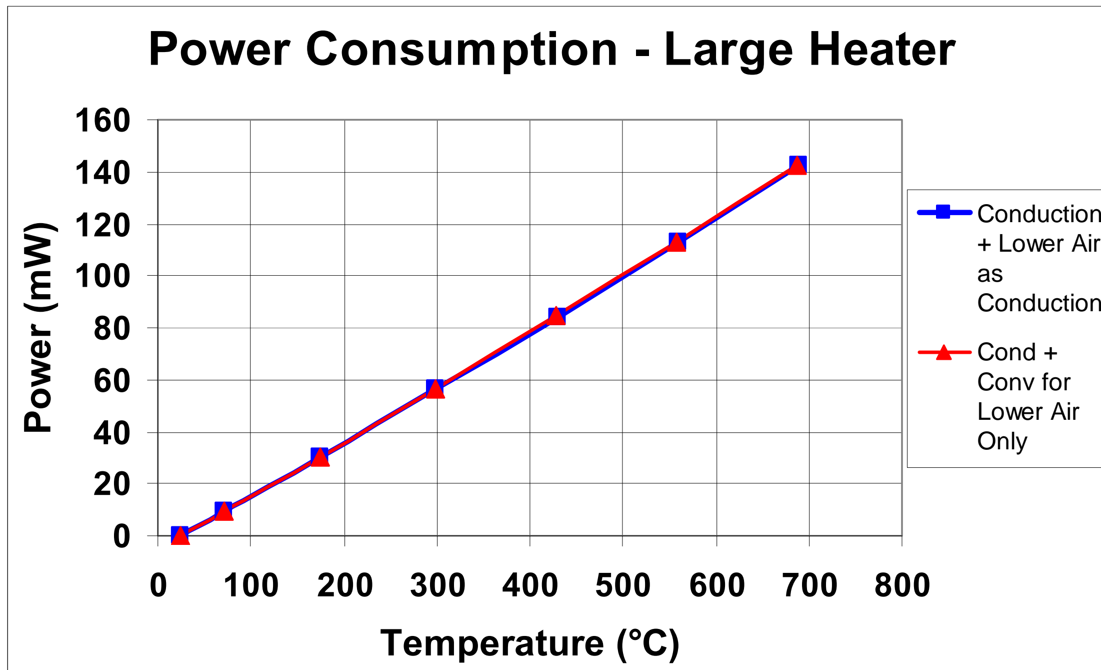


Figure 23: Power vs Temperature for taking into account losses in solid and air below membrane only (i) Losses below membrane treated as convection; (ii) Losses below membrane treated as conduction through air

This means that there is significant heat loss to the air below the membrane. The heat flows within the air from the heater to the side walls of the trench. In membranes formed by DRIE, the trench walls are vertical, compared to that due to KOH, which are at an angle of 45°. Therefore in KOH, heat has a greater distance to travel, and therefore, using KOH might result in lower heat losses. To check this, a simulation was performed on a structure with angled side walls, as would be in a trench formed by KOH etching (Figure 24). The result of the simulation (air above the membrane is not considered) compared to the results with DRIE are shown in Figure 25.

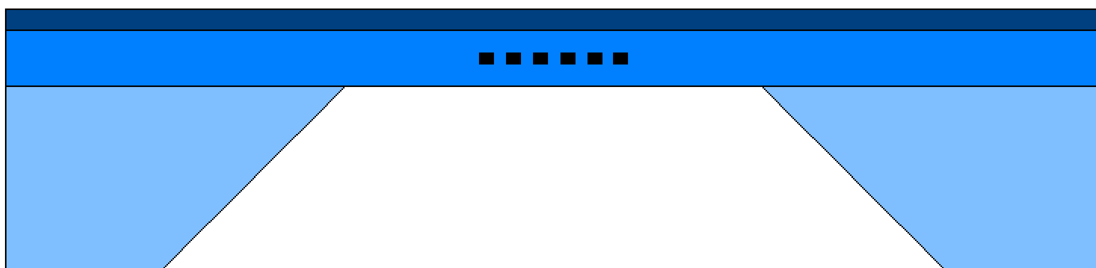


Figure 24: Structure with KOH Etching

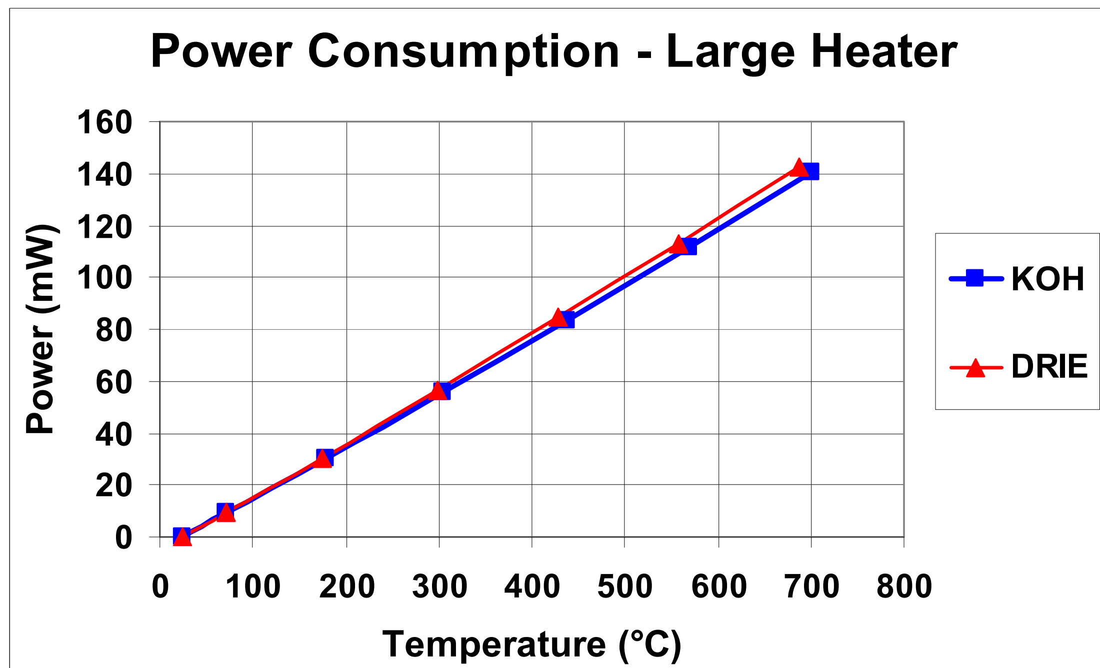


Figure 25: Power consumption with structures etched with (i) KOH, (ii) DRIE. (Includes conduction losses within membrane, and conduction losses to air below membrane)

The figure shows that the power consumption difference although present is insignificant. This is because for the structure formed by KOH, the surface area of the trench walls is much larger, which, to a large extent compensates for the extra distance that the heat has to travel. This effect might not scale for other membrane sizes or substrate thicknesses. However, for most typical micro-hotplate sizes, such as the size used here, the difference between KOH and DRIE structures in terms of power loss should be minimal.

The mechanism of convection above the membrane was also studied. Figure 26 shows the convection coefficients calculated by ANSYS above the membrane. The dotted lines mark the outer edges of the heater and the membrane.

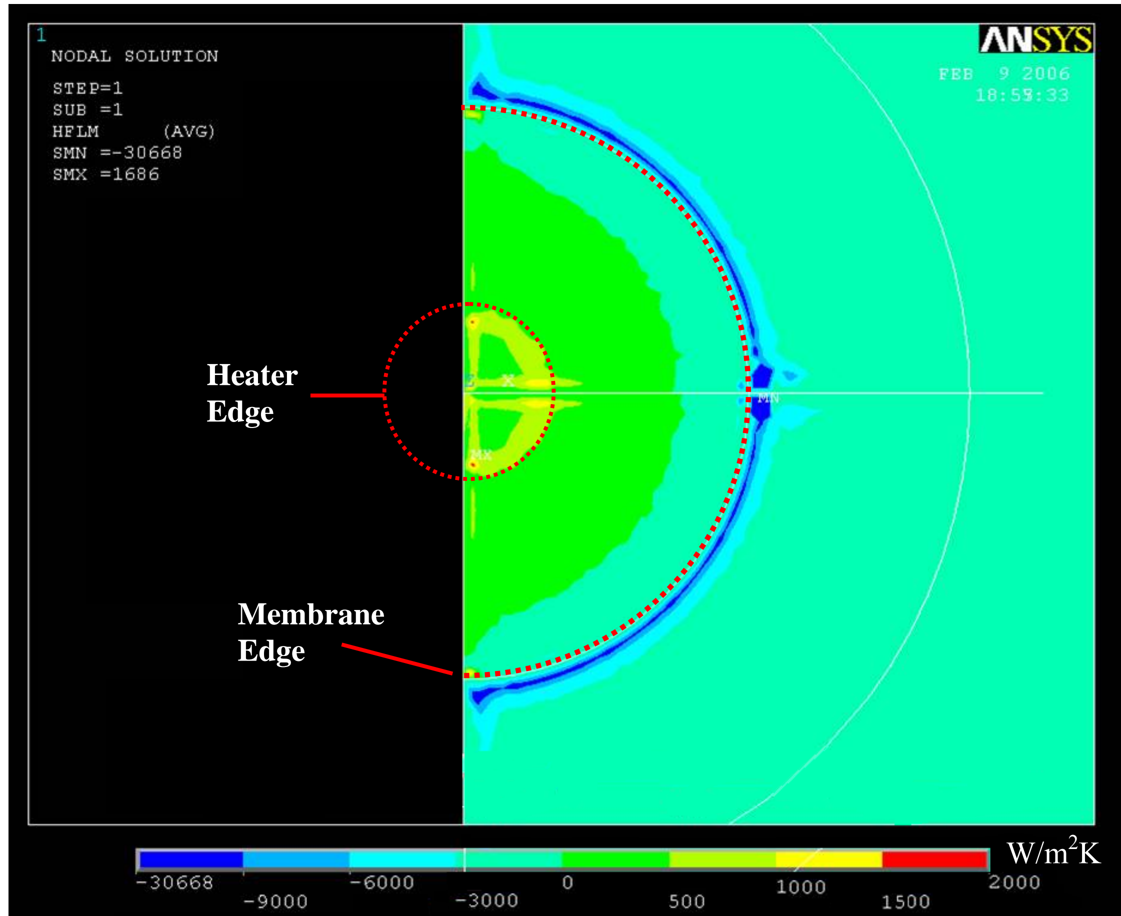


Figure 26: Convection Coefficients above the membrane (only half the structure is shown)

A positive coefficient means that heat escapes from the solid to the air, while a negative coefficient means that the heat flows from the air into the surface. The figure above shows that the heat flows from the heater to the air above it – which is to be expected since the heater region is so much hotter. But the interesting point to note is that just outside the edge of the membrane, the heat actually flows back into the solid! This means, that heat that goes to the air does not rise above into the ambient air, but rather, it conducts back to the cooler part of the chip outside the membrane. Once the simulation results are considered, this makes sense, since it is a much shorter distance to conduct back into the chip, rather than convection to the ambient air.

This means that the primary mode of heat transfer above the membrane is actually conduction via the air to the cooler parts of the chip. To check this, another simulation was run. This time, no air flow or convection was taken into account. It was simply assumed that the air is a conductive medium, with the conduction properties of air. The results (shown in Figure 27) show that there is very little difference caused by taking the effects of air flow into account, and that the heat transfer above the membrane can indeed be treated as conductive heat loss. A further investigation in the literature showed that similar results have also been reported earlier by another group [44], where the effect of air flow is shown to be negligible.

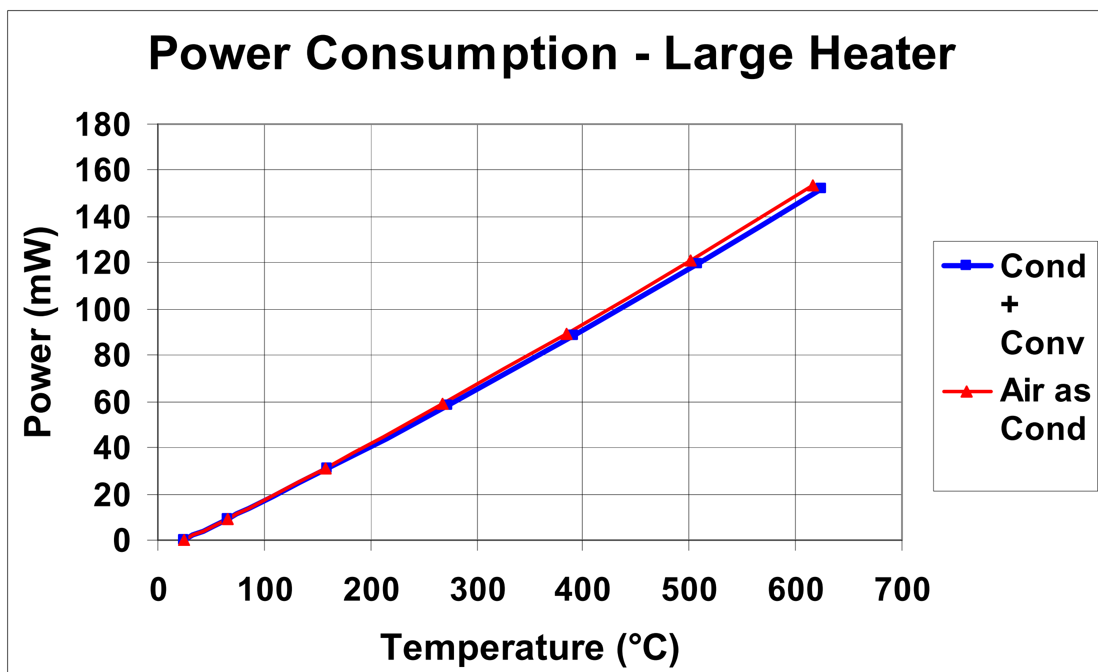


Figure 27: Simulation results for large heater (i) Treating heat loss above and below membrane as convection (ii) Treating heater loss above and below membrane as conduction via air

Radiation:

Radiation is the third possible source of heat loss. For micro-hotplate surfaces, radiation can be calculated by [42]:

$$q=\varepsilon\sigma A(T^4-T_o^4) \quad (7)$$

where:

q = Radiated power loss

ε = emissivity of the radiating surface

σ = Stefan-Boltzmann constant (5.669×10^{-8} $Wm^{-2}K^{-4}$)

A = area

T = surface temperature (in Kelvin)

T_o = Ambient temperature (in Kelvin)

The challenge in radiation calculations is the determination of the thermal emissivity. The thermal emissivity depends not only on the material, but also varies for thin films, and whether the film is stand alone or backed by a substrate [45]. Thermal emissivity measurements for a membrane consisting of a thin film sandwich system of silicon oxide and silicon nitride have been reported by Volklein [46]. This is a very close representation of our micro-hotplates, and can be used for our analysis. The reported value of emissivity varies slightly with temperature, with 0.2 as an average value.

It is not very easy to simulate radiation effects in ANSYS. However, a simple calculation can be made to estimate the power loss due to radiation.

Consider a heater temperature of 600°C. While the area as well as the emissivity is known, the temperature is not constant, and will vary over the membrane. First just consider the heater area which is simpler. For the heater area, the temperature will not vary too much, and can be considered uniform to calculate the radiation loss given by:

$$q=\varepsilon\sigma(T^4-T_o^4)\pi r_1^2 \quad (8)$$

(where T = 873K, T_o=298K).

For the rest of the membrane, the temperature will vary from room temperature (25°C) to the heater temperature (600°C). So as an approximation the average temperature can be used. However, as the radiation power is proportional to T^4, the

average of T^4 of the two temperatures is used. So an approximate power loss for this part of the membrane is given by:

$$q=\varepsilon\sigma \, (\pi \, (r_2^2-r_1^2) \,) \, (\, (T^4-T_o^4)/2 - T_o^4) \tag{9}$$

The sum of these two expressions gives the estimated total radiation power loss above the membrane, and multiplying by 2 gives the total radiation loss for the membrane (Since the radiation loss is from the bottom surface of the membrane as well as the top surface). Using the expressions, for the large and small membranes at a temperature of 600°C, the radiation power loss is 2.1mW for the large heater, and 0.02mW for the small heater. This is a relatively low power loss compared to the power losses due to conduction and convection (less than 2%). Additionally, the formulas used are only an estimate, and actually predict a higher value for the heat loss. So the actual radiation heat loss will be even lower. Therefore, the power losses due to radiation can be mostly ignored for the analysis of micro-hotplates.

Transient Time

The response time of a micro-hotplate (the time required to heat up), is an important parameter. If the response time is small enough, then the sensor can be used in pulsed mode to reduce the average power consumed. For example, if the power is applied for only 0.1 second, and not for the rest of the 0.9 second, then the gas sensing readings can be taken during that 0.1 second. This would reduce the average power consumed to a tenth of the DC power, while still giving a reading every second. This however, is only possible if the micro-hotplate heats up to the required temperature within the 0.1 second. If the response time is higher then this is not possible.

It is also not preferable to use low frequency cycles, and in some applications low frequency cycles may not be possible. For example, if a micro-hotplate has a response time of 2 seconds, then if a 20 second cycle is used, with power applied for only 2 seconds, then there will be a gap of 20 seconds within each reading. This could be problematic in control applications, and possibly not allowed for safety applications (such as smoke alarms etc).

In addition to lower average power, a fast transient time also allows the possibility of temperature modulation for improved gas sensing [22].

Transient simulations were done to determine the time required to heat up the micro-hotplates. These simulations were done in the initial stages of our analysis of the micro-hotplates, and so the structures used were the preliminary structures of tungsten heaters on an oxide membrane. The results of this are shown in the form of a temperature vs time graph in Figure 28, Figure 29. Two facts are obvious:

1. The larger heater structures have a larger response time than the smaller ones. This is due to the larger volume (and hence mass) that needs to be heated.
2. The response time is very low: less than 15ms for the large heaters, and less than 1 ms for the small heaters. This means that the micro-hotplates can be operated in pulsed mode, to greatly reduce the average required power.

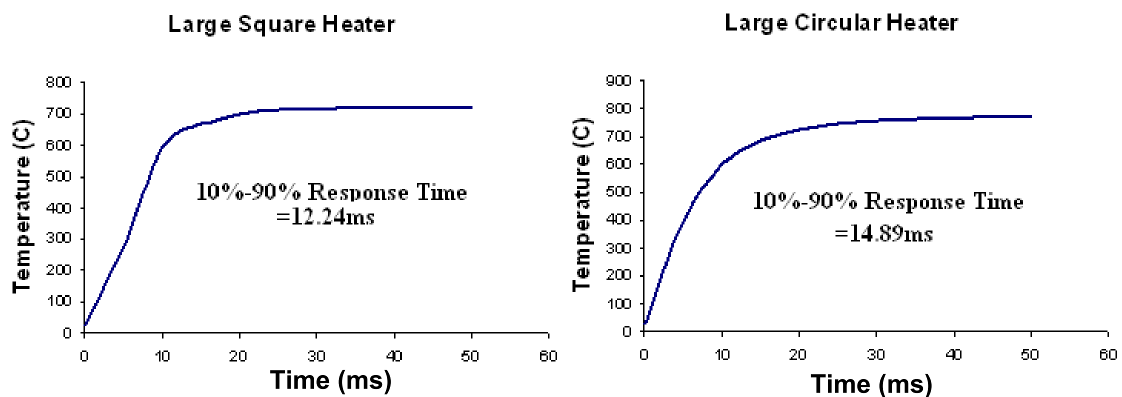


Figure 28: Transient analysis of Large Heaters

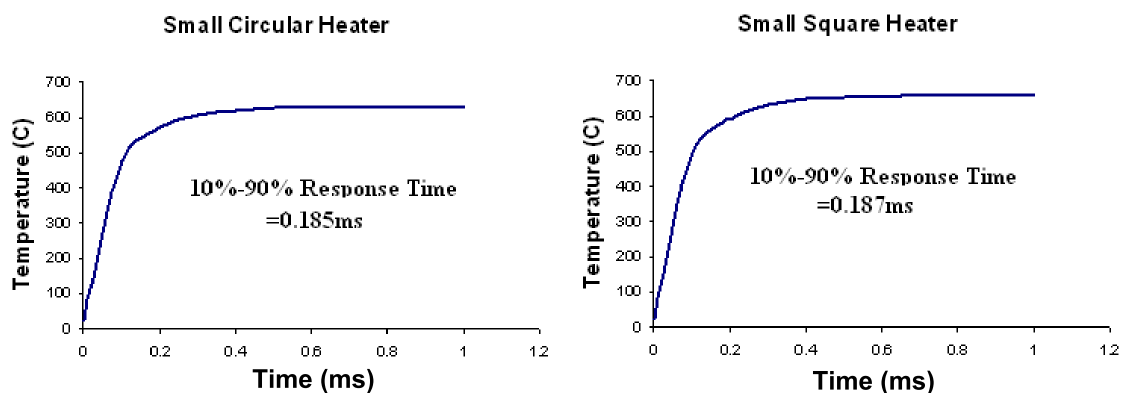


Figure 29: Transient analysis of Small Heaters

Temperature Uniformity

Temperature uniformity within the heater area is essential for accurate gas sensing. Good temperature uniformity ensures that the entire sensing material is at the same temperature, and so is equally sensitive to the target gas. Different methods have been tried to improve temperature uniformity. Lee et al. [47] compared different heater shapes, while Briand et al. [48] used a silicon island in the heater area. However, no systematic approach to design micro-hotplates for good temperature uniformity has been reported. Therefore, first a simple analysis of temperature distribution of different designs was done, and then heaters with good temperature uniformity were methodically designed.

First consider the case where the source of heat loss is only conduction. Figure 30 shows the heater region of the small circular structure (when simulated for only conduction losses). The temperature is high in the centre, but lower at the edges. The total temperature difference within the heater is about 200°C, which is unacceptable. In addition, the temperature seems to be higher at the heater lines, and lower at the gaps. So if there is a way to ‘fill’ the gaps, it would increase the uniformity.

One possible way, is to have a second heater embedded within the silicon oxide as shown in Figure 31. The heater is arranged so that the heater lines of one heater, overlap the gaps in the other. The simulation results of this are shown in Figure 32, using a scale from 480°C to 680°C. This scale is used so as to keep the difference at 200°C, so as to better compare with Figure 30. The temperature is slightly more uniform in this case.

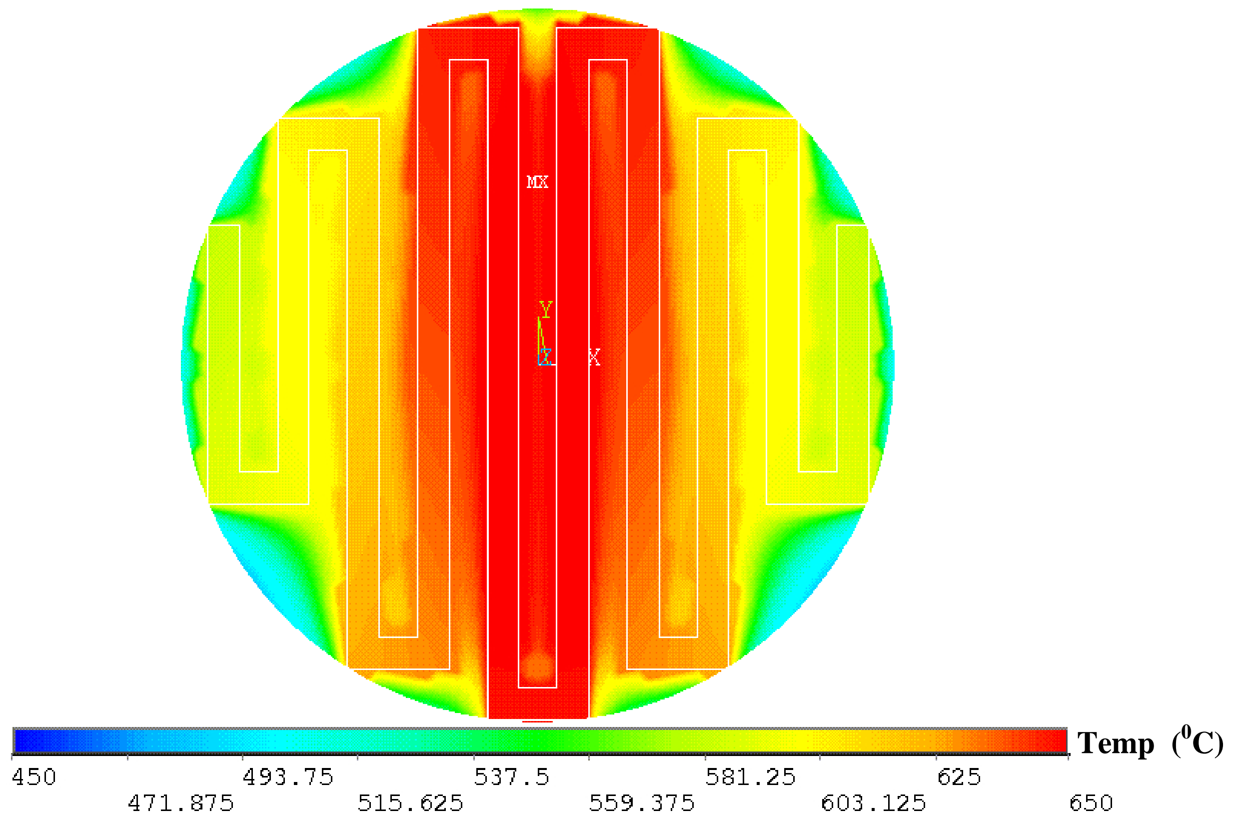


Figure 30: Temperature distribution in the heater area

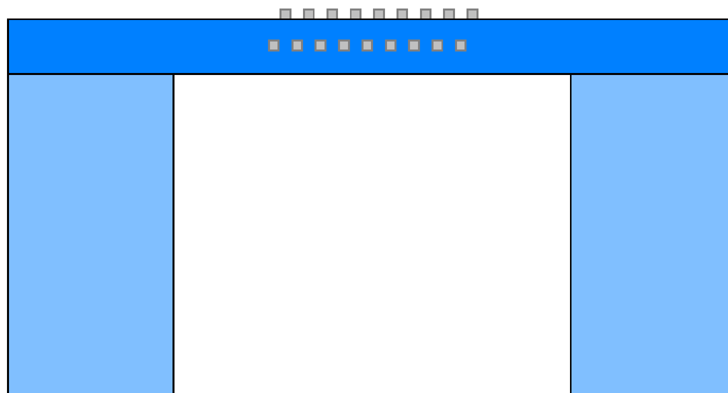


Figure 31: A Two Heater Structure

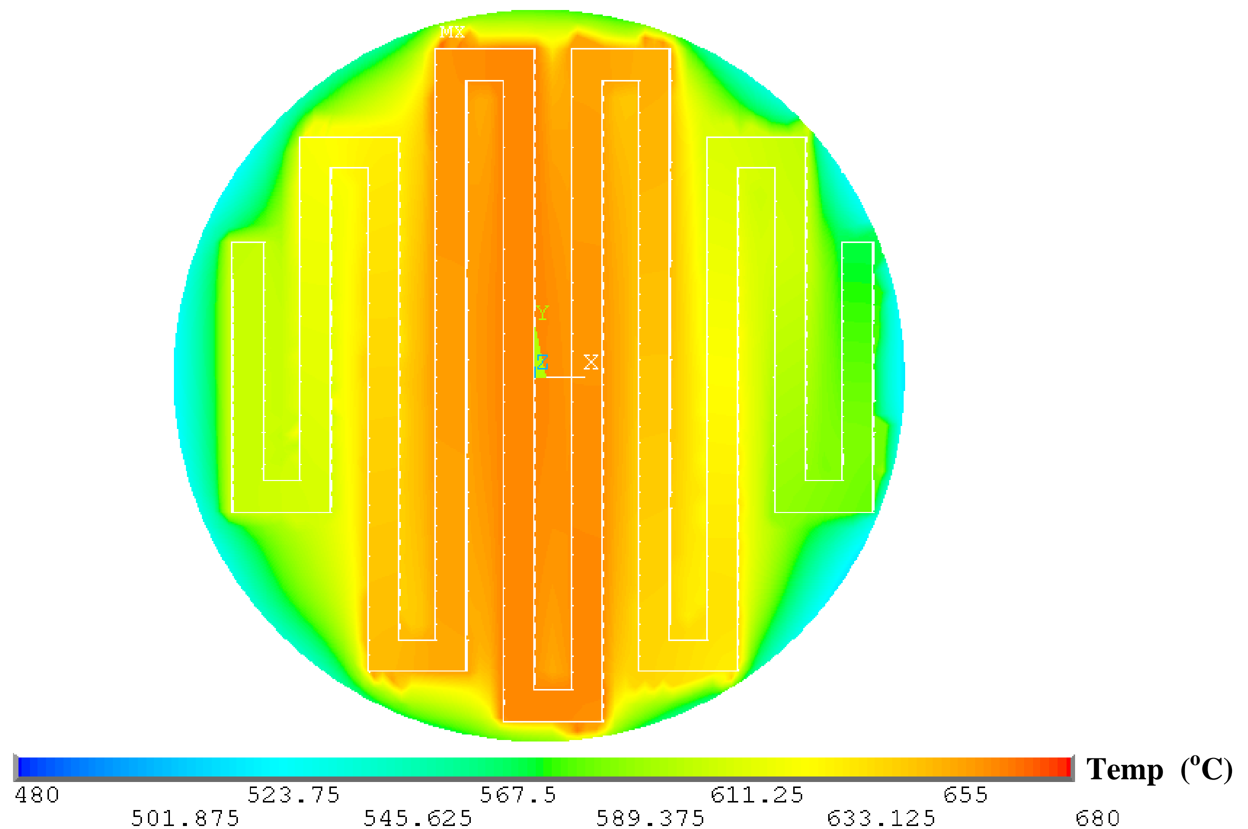


Figure 32: Temperature distribution for a 2 heater structure

Another method is to use a circular silicon plate embedded within the oxide, underneath the heater. Briand et al. [48] used a thick silicon island below the heater to achieve much better temperature uniformity. Silicon has a much higher thermal conductivity than silicon oxide, and therefore would spread the temperature more evenly. The thickness of the silicon available in the SOI layer is much smaller, but it can still have a significant effect. The results for this are shown in Figure 33. As expected, the results are much more uniform, with a difference of only about 100°C within the heater region.

A tungsten plate can also be used instead of Silicon. Tungsten has a slightly higher thermal conductivity than silicon, and so should result in even better uniformity. The simulation results (Figure 34) show this to be the case.

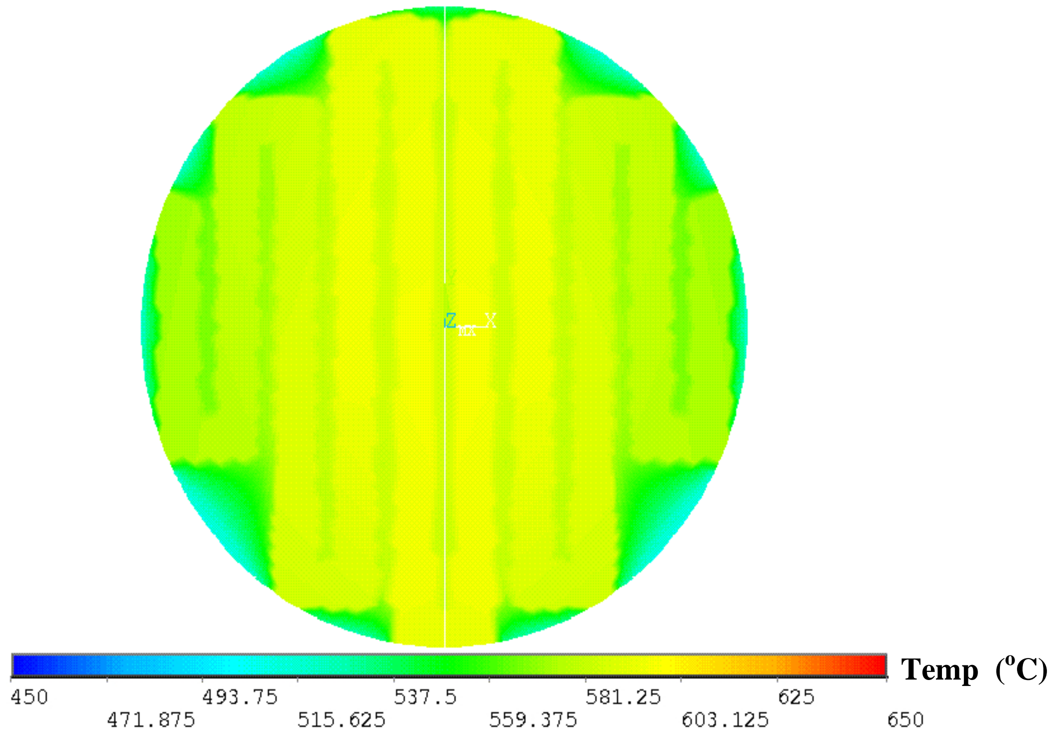


Figure 33: Temperature distribution for structure with Silicon plate

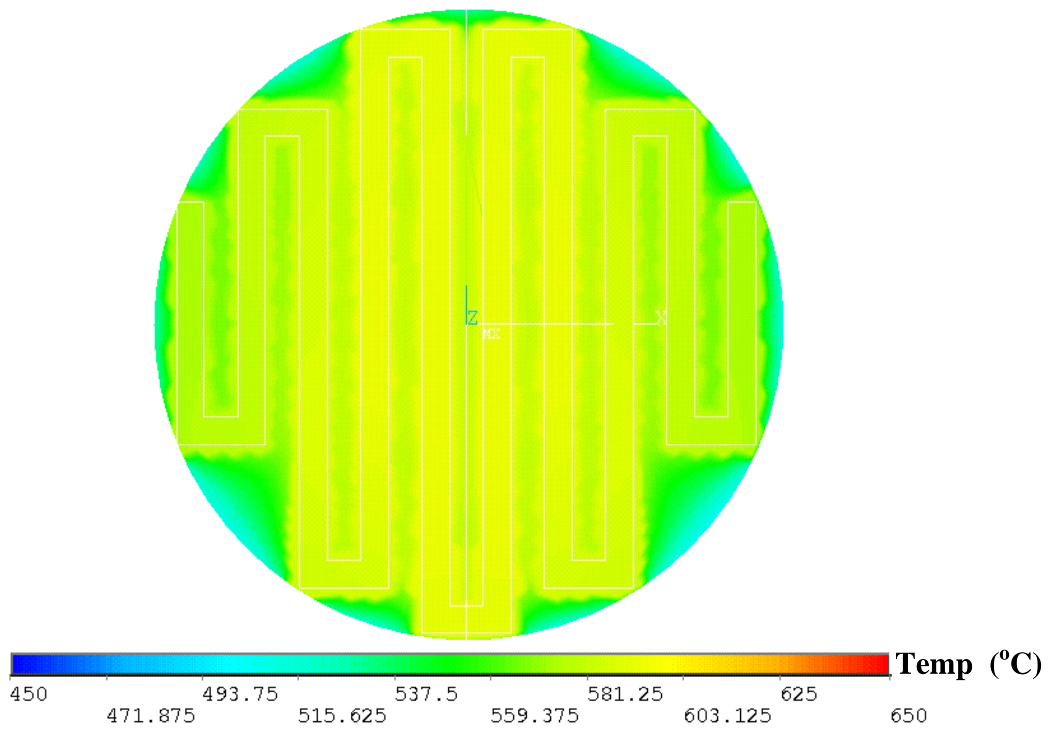


Figure 34: Temperature distribution for structure with Tungsten plate

Three different heater shapes were also tried. The heater in Figure 30 is essentially a rectangular shaped heater, fitted to a circular shape. A more circular heater design might give better results. For this, a spiral heater was tried. Figure 35 shows the results of the simulation. The temperature is not very uniform, the difference within the heater region being more than 270^{0}C. A double spiral heater (Figure 36) was also tried, but did not result in a very uniform distribution either. However, as compared to Figure 30, the temperature in these simulations varies radially only. Another heater shape used was a multi-ringed heater shape, shown in Figure 37. This shows a better temperature distribution. There is a temperature difference of 100°C within the heater region which is still high, but much better than the other shapes. Adding a silicon and/or tungsten plate can further improve the temperature uniformity.

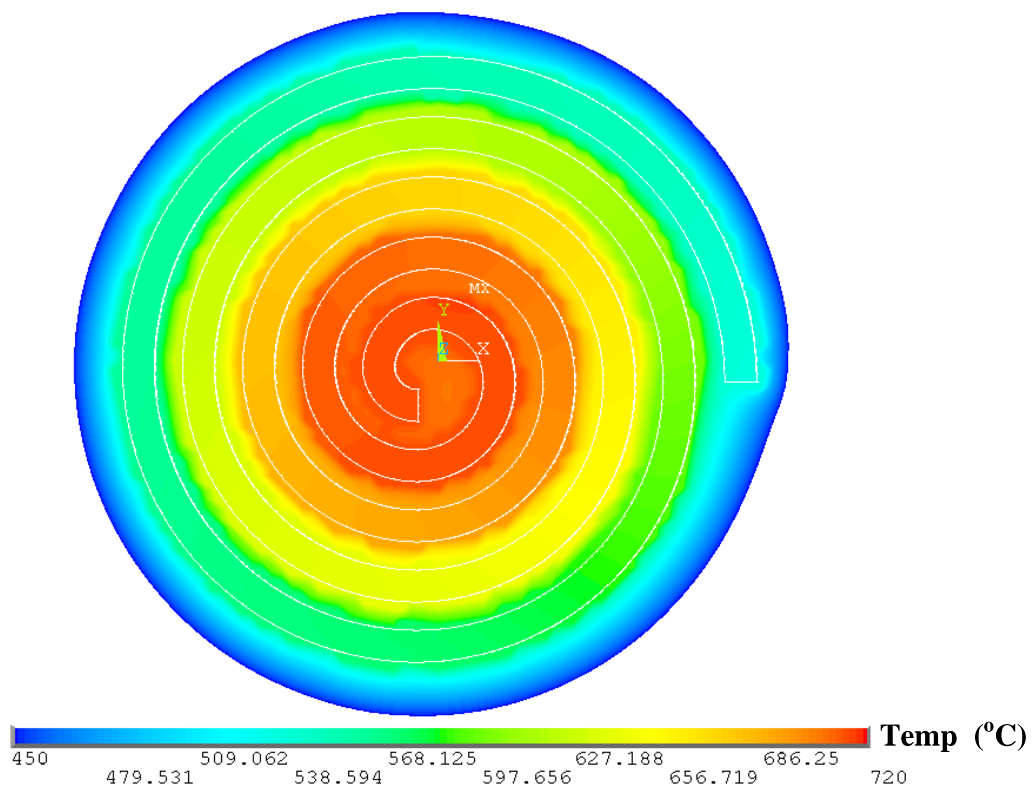


Figure 35: Temperature Distribution for a spiral heater

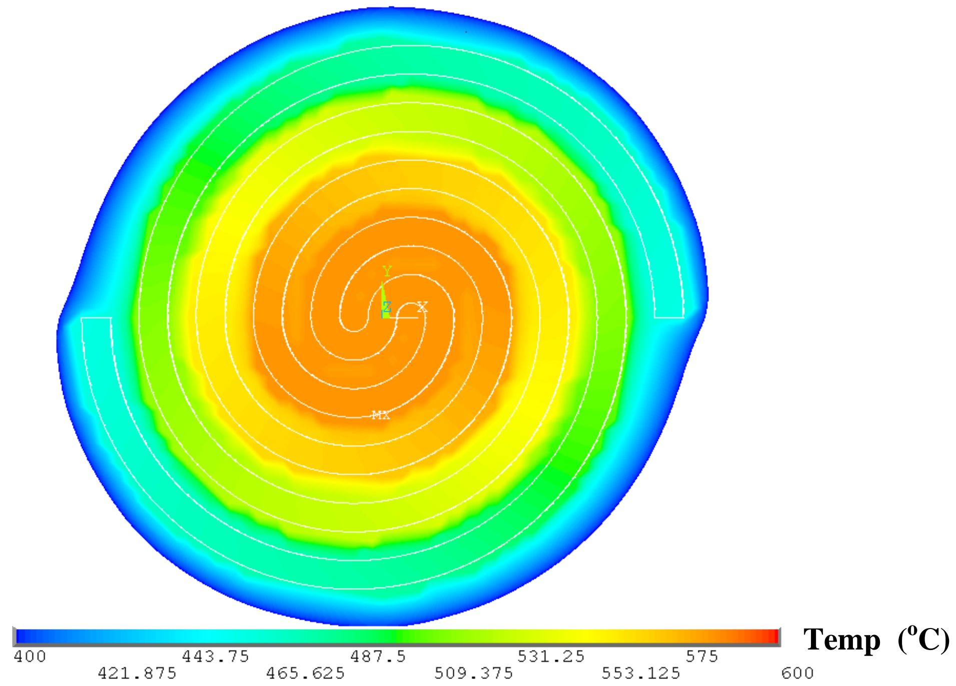


Figure 36: Temperature Distribution for a double spiral heater

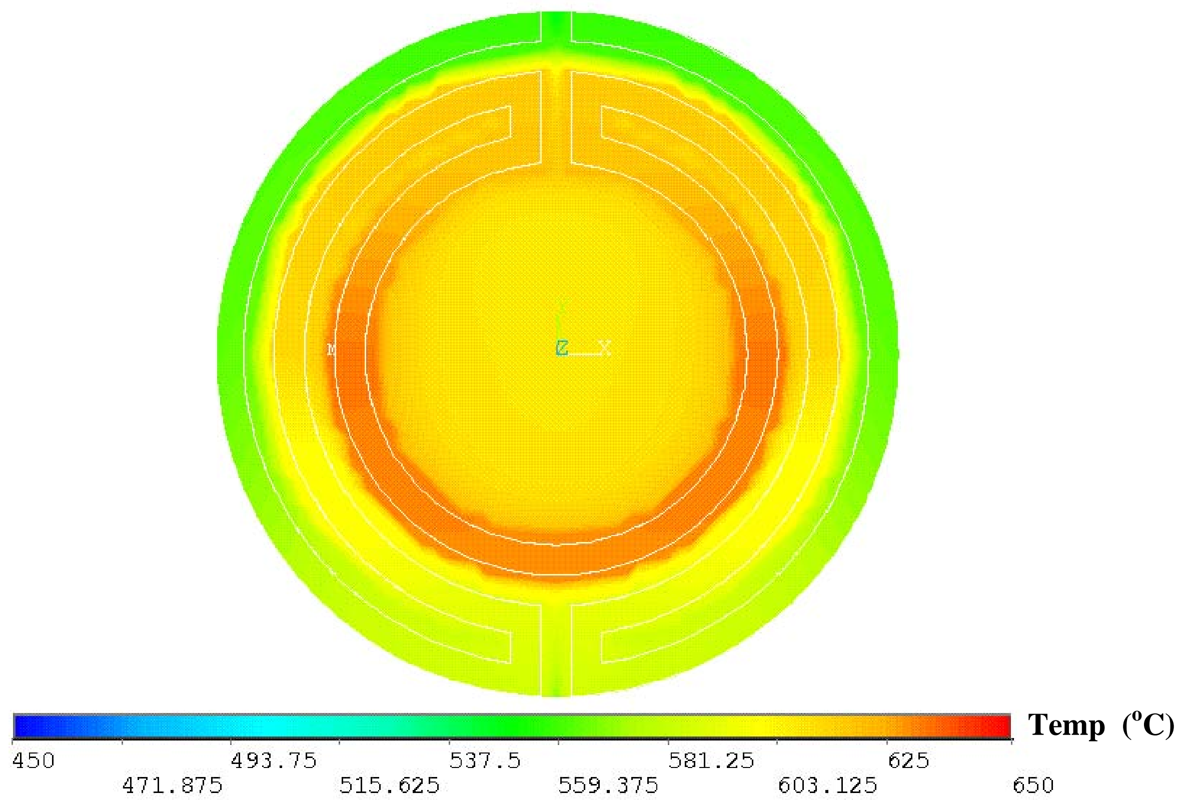


Figure 37: Temperature distribution for the Multi-ring Heater

These results show that the multi-ringed heater shape results in the most uniform temperature distribution. The use of a tungsten plate within the membrane will further increase the temperature uniformity.

Temperature Uniformity Analyzed:

So far, only a trial and error method has been used to obtain a good temperature profile. A more analytical method can be used instead as this gives a better insight into heater design.

A careful look at Figure 37, shows that the area within the innermost ring of the heater has an almost uniform temperature. Since the simulation only takes conduction losses into account, the ring seems to 'trap' the heat within it. This suggests that where the source of heat loss is only conduction, a simple ring heater will give an almost uniform temperature profile. Li et al. have indeed shown this to be the case [49].

A simple mathematical analysis also shows this to be so:

The Cylindrical Heat Equation is given by:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T}{\partial r}\right)+\frac{1}{r^2}\frac{\partial^2 T}{\partial \theta^2}+\frac{\partial^2 T}{\partial z^2}+\frac{g(r,\theta,z,t)}{k}=\frac{1}{\alpha}\frac{\partial T}{\partial t} \tag{10}$$

Where:

T: Temperature

k: Thermal Conductivity

g: Heat generation

α: constant

t: time

r, θ, z are the variables of the polar coordinates.

To model a Membrane:

Consider a 2D model, assuming conduction as the only source of heat loss. Suppose R2 is the edge of the membrane, and lets assume that all the heat flowing from the heater is absorbed at the edge (at R2) (this is close to the real case as the heat would flow

quickly through the silicon). And that the temperature outside the membrane is constant (for r>R2, dt/dr=0)

Now also suppose that the heater is a perfect ring, of radius R1, and has a small thickness.

To determine the temperature distribution, the heat equation has to be solved. Since the model is 2D, $d^2T/dz^2=0$. Also since the whole model has a circular symmetry, it is reasonable to suppose that $d^2T/d\theta^2=0$. And for a static solution, dT/dt=0.

The equation is now:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T}{\partial r}\right)=-\frac{g(r)}{k}$$

There are two sources of heat 'generation':

1. The heater edge
2. The membrane edge which absorbs the heat ('generates' negative heat)

Suppose the heat generated per length of the heater is *m*.

The total heat generated = m2πR1

The total heat absorbed at the membrane edge is equal to the total heat generated by the heater.

Therefore, heat absorbed per unit length of membrane edge = m. 2 πR1/(2 πR2)=mR1/R2

Therefore the heat generated is:

$$g=m\delta(r-R1)-\frac{mR1}{R2}\delta(r-R2)$$

The second term is negative since heat is absorbed. The δ is the impulse function, or Dirac-delta function, which shows that the heat is produced/absorbed at an infinitesimal small thickness.

The equation now becomes:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T}{\partial r}\right) = -\frac{m}{k}\delta(r-R1) + \frac{mR1}{kR2}\delta(r-R2)$$

Solving:

$$\frac{\partial}{\partial r}\left(r\frac{\partial T}{\partial r}\right) = -\frac{mr}{k}\delta(r-R1) + \frac{mR1\cdot r}{kR2}\delta(r-R2)$$

$$r\frac{dT}{dr} = -\frac{mR1}{k}U(r-R1) + \frac{mR1\cdot R2}{kR2}U(r-R2) + C$$

$$r\frac{dT}{dr} = -\frac{mR1}{k}U(r-R1) + \frac{mR1}{k}U(r-R2) + C$$

$$\frac{dT}{dr} = \frac{mR1}{kr}\left[U(r-R2) - U(r-R1)\right] + \frac{C}{r}$$

(The impulse function integrates to give the Unit Step Function)

C is a constant. To determine its value:

Applying the condition:

For r>R2, dT/dr=0

(since the temperature is uniform outside the membrane)

Therefore,

C=0,

Since

U(r-R2)-U(r-R1) = 0 for r>R2,

The equation now becomes:

$$\frac{dT}{dr} = \frac{mR1}{kr}\left[U(r-R2) - U(r-R1)\right] \tag{11}$$

Therefore, since U(r-R2)-U(r-R1)=0 for r<R1,

It implies that for r<R1, dt/dr=0,

That is, the temperature is completely uniform within the heater region!

Therefore, in a purely conducting environment (such as a vacuum), a ring heat gives a completely uniform temperature distribution inside the ring. This can then be checked by simulation of a simple ring heater. For this, a large ring heater, of radius 170µm on a membrane of 280 µm radius was simulated. Only conduction losses were considered. The temperature profile obtained is shown in Figure 38.

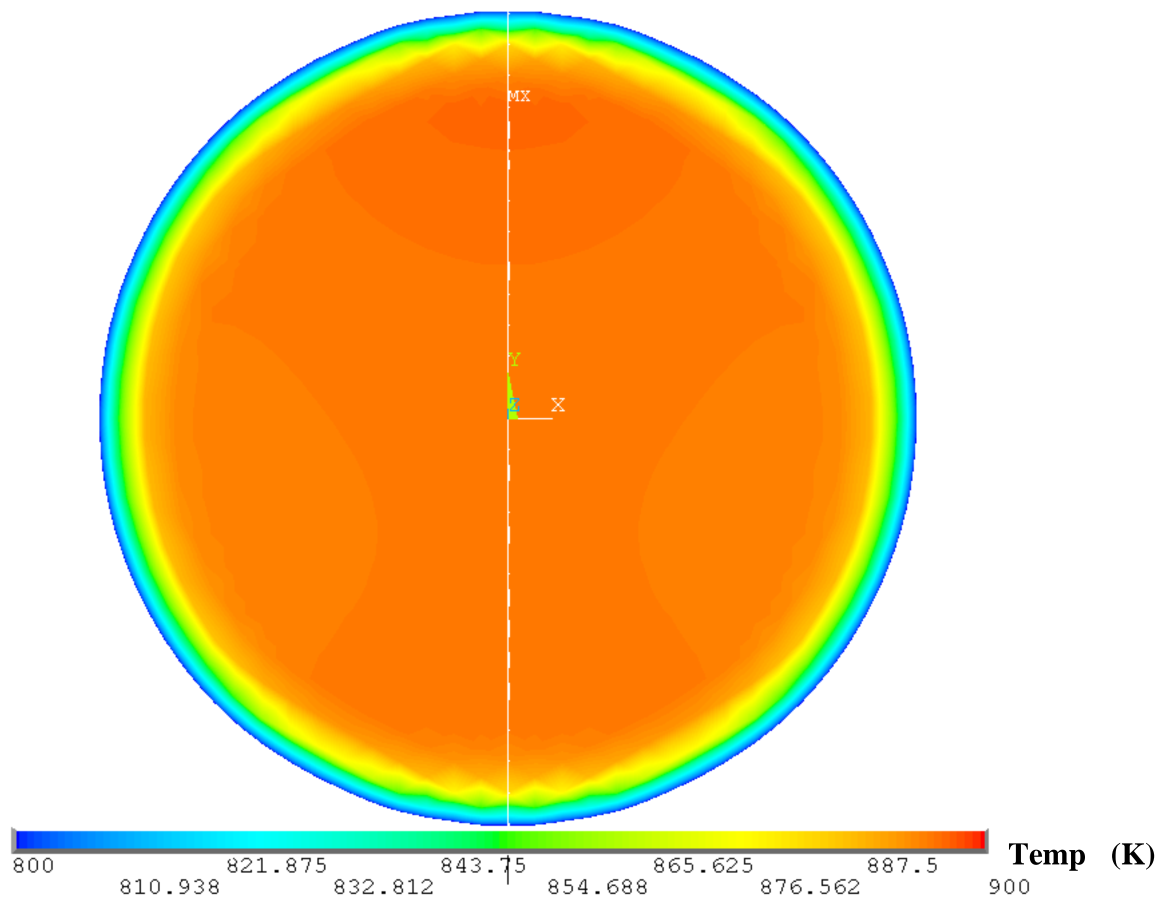


Figure 38: Temperature profile for a large ring heater

As the figure shows, the heater has an almost uniform temperature profile.

So what effect do convection[2] losses have on the temperature uniformity? This was checked by simulating the convection losses as well for the same heater, and the temperature profile obtained is shown in Figure 39.

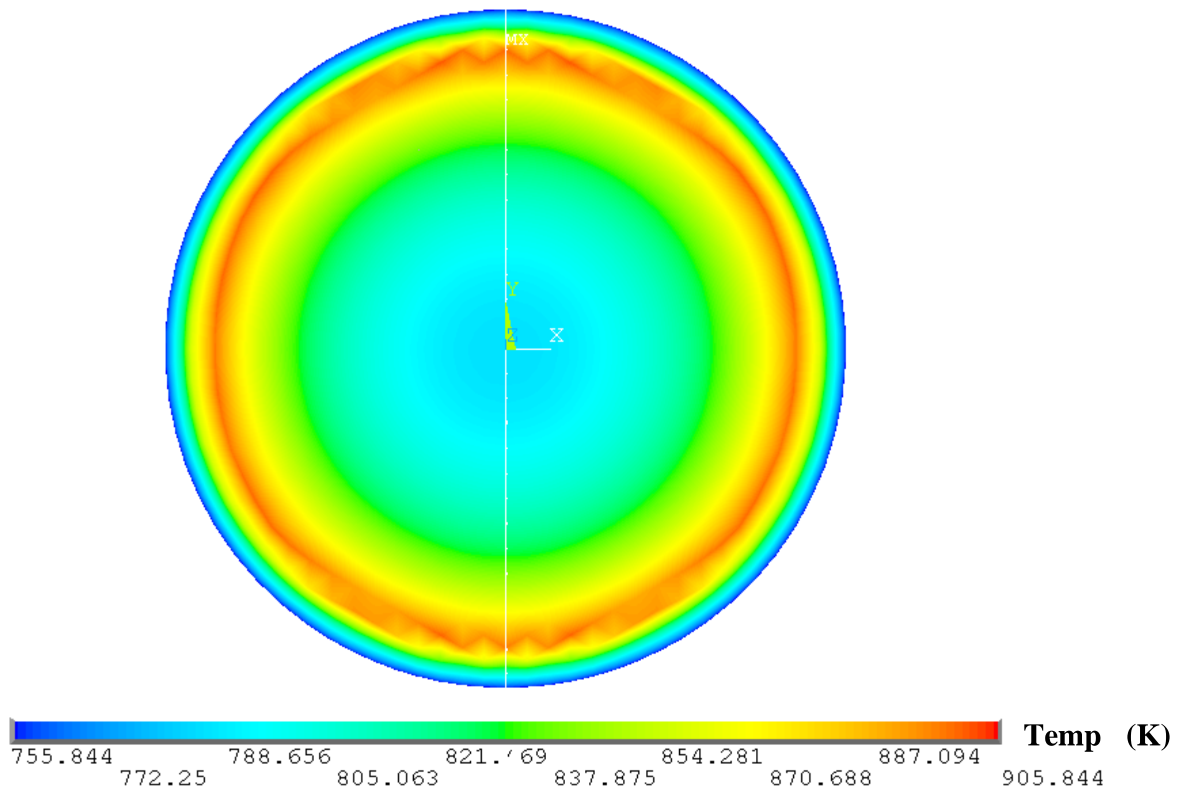


Figure 39: Temperature Profile for Ring Heater for conduction & convection losses

This time the temperature profile is much worse. The inner part of the heater is much cooler than the outer region. To improve this a floating metal plate was added in the empty space inside the ring to act as a spreading plate, but there was still a significant difference in the inner and outer temperature (Figure 40). This can be explained as follows.

---

[2] As shown before, the primary mechanism of heat loss to air is conduction, not convection. However, here these losses are treated as convection to make the estimation of heat losses in different parts of the membrane simpler.

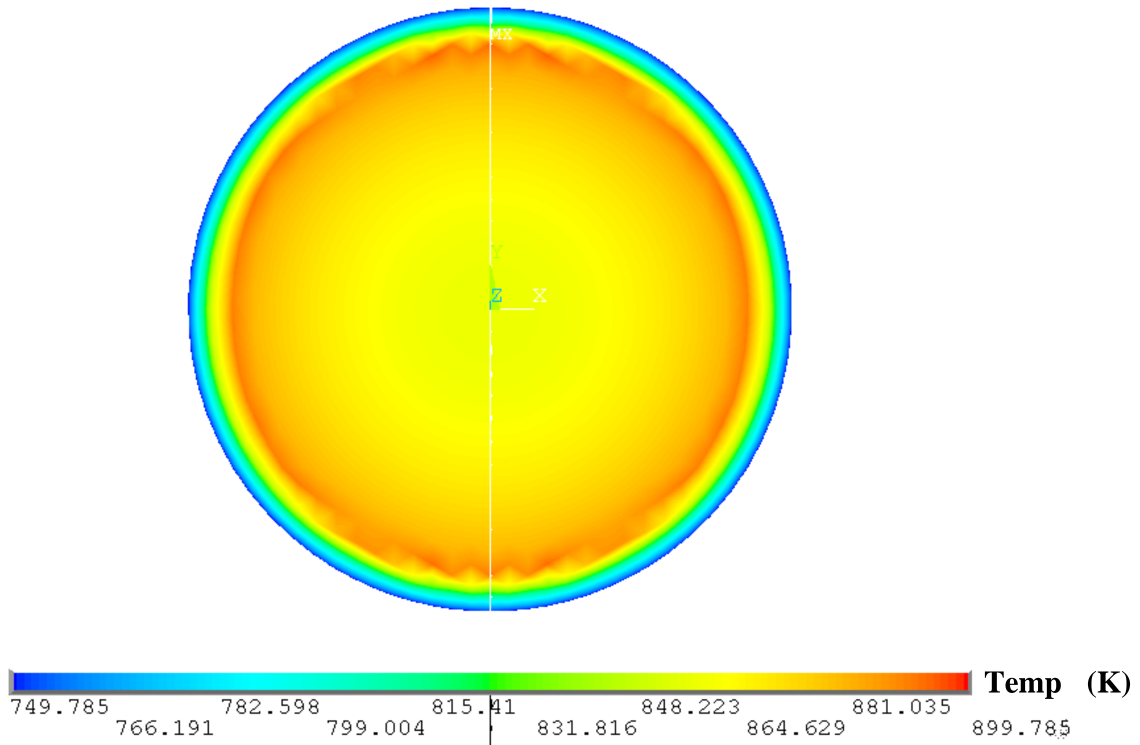


Figure 40: Temperature profile for a ring heater with a heat spreading plate at the centre

Consider Figure 41. For the ring heater in a conductive medium only, the heat flows outwards from the heater. There is no heat flow inside the heater, which results in a uniform temperature.

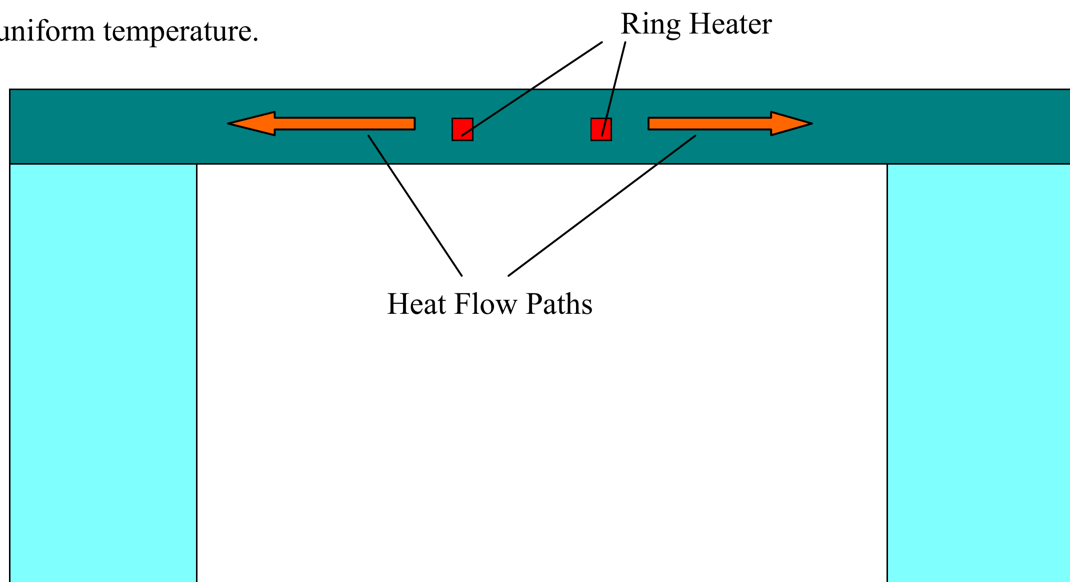


Figure 41: Heat flow path, if heat loss is only conduction

If losses to air are taken into account, however, more paths for heat flow are added (Figure 42).

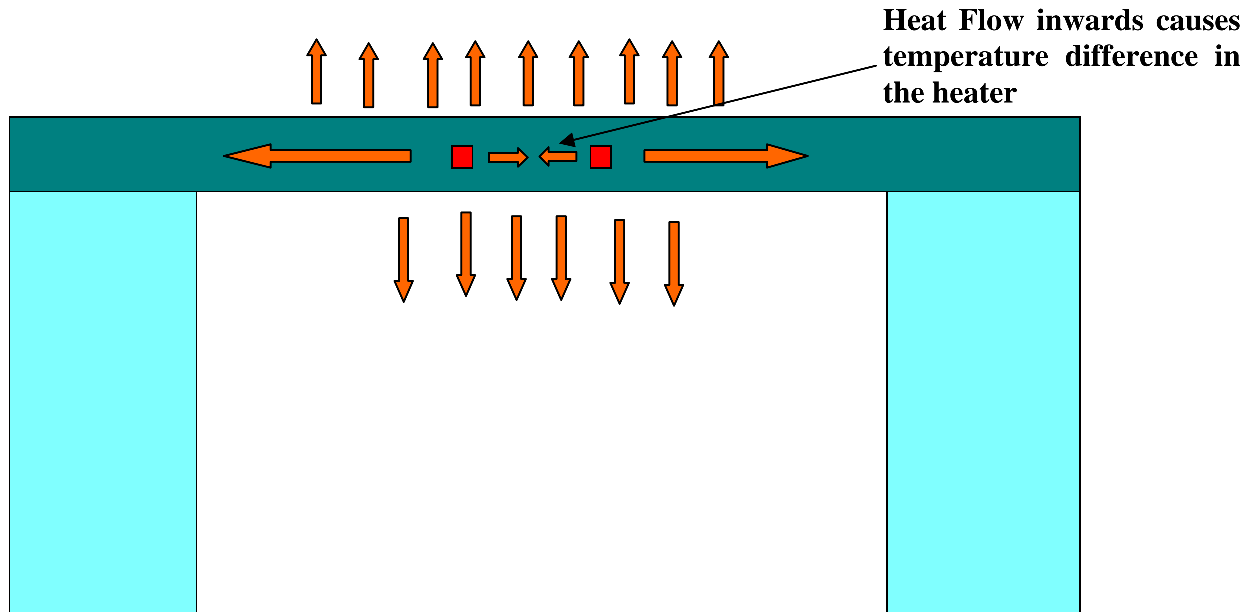


Figure 42: Heat flow paths for conduction and convection

Now heat is lost due to air from the surface of the membrane as well. Part of this heat is lost from the surface within the heater area, part of it is lost outside the heater area. Consider for example the centre of the ring heater. Heat is lost from the surface due to convection, however, no heat is generated at the centre. Therefore, to compensate for this heat loss, heat has to flow from the outer ring to the centre of the heater. This flow of heat, therefore, results in a temperature gradient, which makes the temperature profile non-uniform.

This suggests that for good temperature uniformity, there should be a heating element within the ring as well to compensate for the heat loss due to convection within the heater. But how much power should be generated by the inner heater?

Heat is lost from:

1. Conduction
2. Convection within the heater region
3. Convection from the membrane, but outside the heater region

The ratios for the power generated by the inner part of the heater, and the outer ring should be such that the outer ring accounts for heat losses 1 & 3, while the inner part accounts for the heat loss due to convection within the heater region (2). If the inner part generates more heat, then heat will flow from the centre to the outer part of the heater, making the centre hotter than the rest of the heater. If the inner part generates less heat, then the heat will flow from the outer ring to the centre, making the centre cooler than the outer part of the heater.

In this way it is possible to calculate and design a heater for good temperature uniformity.

The power loss due to conduction, and that due to convection can be easily determined by simulation results. However, it is harder to determine how much of the convection losses are from within the heater area, and how much from the rest of the membrane.

A simple method to calculate this is to assume that the convection coefficient is uniform all over the membrane (This is not quite correct, but gives a reasonable estimate for calculation). The temperature will also vary over the membrane, so the amount of heat loss due to convection will be different at each point, and this has to be taken into account.

Suppose first that the only source of heat loss is conduction. Given a uniform heater temperature of T_1, and an ambient temperature of T_0, the temperature at any radius r between r_1 and r_2 (using a simple potential divider rule between thermal resistances) is given by:

$$T(r)=\frac{\frac{1}{2\pi\alpha t}\ln\left(\frac{r_2}{r}\right)}{\frac{1}{2\pi\alpha t}\ln\left(\frac{r_2}{r_1}\right)}\cdot(T_1-T_0)+T_0=\frac{\ln\left(\frac{r_2}{r}\right)}{\ln\left(\frac{r_2}{r_1}\right)}\cdot(T_1-T_0)+T \tag{12}$$

This gives a good estimate of the temperature at each point on the membrane. This equation is fairly accurate even if convection is present. This can be shown by comparing the distribution predicted by this equation, to that obtained from simulations which take convection into account. Figure 43 shows this comparison, where the temperature

distribution across the membrane is shown. The simulation includes both conduction and convection. The calculation is done using the above equation, with T_1=500°C, which is the temperature at the edge of the heater in the simulation. The excellent matching shows that it is a sufficiently good approximation. Since convection effects have not been taken into account for the equation, the curve could vary slightly for different dimensions, however, the changes are unlikely to be significant for the case of our calculation.

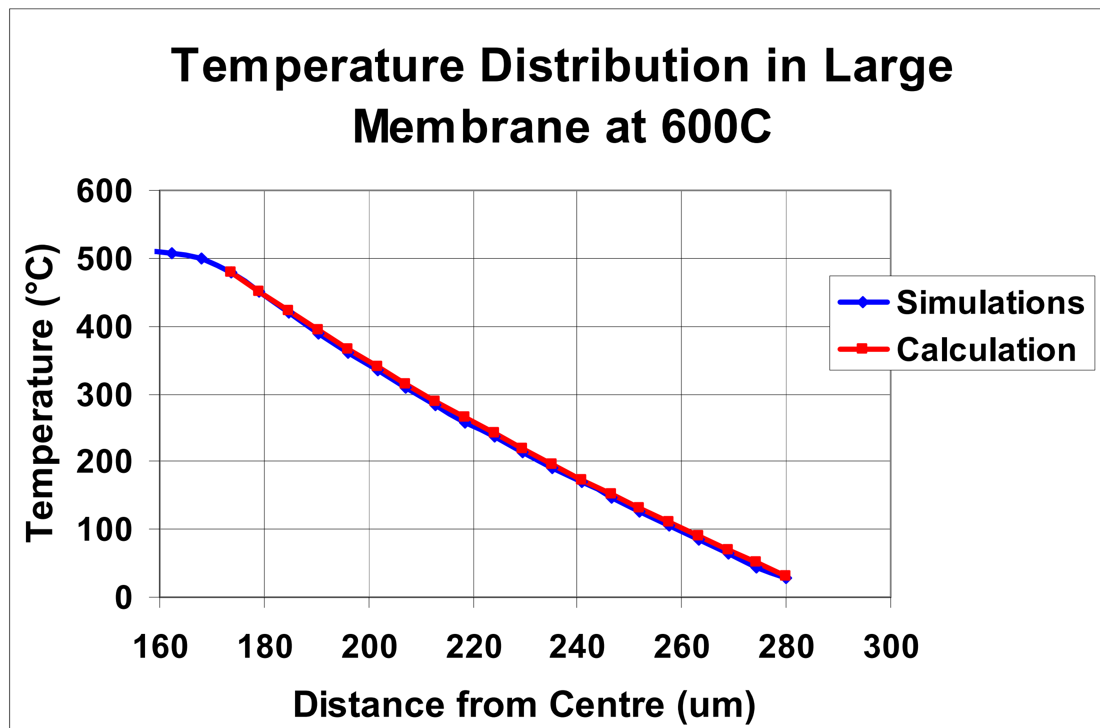


Figure 43: Temperature distribution within the membrane outside the heater area. The graph shows a comparison of the simulations, and the profile predicted by a simple calculation.

Using this, and assuming that the convection coefficient is constant all over the membrane, an equation for the convection power loss as a function of the heater temperature (T_1) and the convection coefficient (h) can be determined. This is done by dividing the membrane into 2 regions. The first region is the heater area, where the temperature can be assumed to be constant. The second region is the rest of the membrane. A ring within this region of infinitesimal width would have a uniform

temperature. This can be integrated from r_1 (Heater radius) to r_2 (membrane radius) to get the total convection loss in the second region. The equation is:

$$P_{conv} = \pi \ r_1^2 h(T_1 - T_0) \ + \frac{2\pi h(T_1 - T_0)_1}{\ln\left(\frac{r_2}{r_1}\right)} \int_{r1}^{r2} \ln\left(\frac{r_2}{r}\right) r \cdot dr$$

$$h = \frac{2P_{conv} \ln\left(\frac{r_2}{r_1}\right)}{\pi(T_1 - T_0)(r_2^2 - r_1^2)} \tag{13}$$

where P_{conv} is the total power loss due to convection. Looking at the graph for the large heater, at 600°C, the total convection loss is about P_{conv}=55mW. Setting T_1=600°C, T_o=25°C, we can determine the value of h. This allows us to estimate how much of the convection losses occur within the heater region, and how much are from the membrane outside the heater region. Calculating we get:

Convection within the heater region = 32mW
Convection outside heater region = 23mW.

Adding the power loss due to conduction (92mW), we can determine the power loss within the heater region, and outside the heater region:

Power needed within heater region = $\pi r_1^2 h T_1$ = 32mW
Power needed outside heater region = 115mW

Therefore, the heater should be designed so that there is an outer ring supplying 115mW of power, while an inner set of rings supply 32mW of power. Since the rings are in series, the ratio of the resistance of the outer rings to the resistance of the inner rings should be 115:32. It also seems reasonable to suppose that the inner rings should cover as much area as possible (ie, rather than have thin rings with large gaps between them

(which would cause a heat flow between the rings – and so a temperature variation), the rings should be thick, so that heat flow is minimum between the rings).

Heater Design:

The heater will consist of one outer ring, and a few inner rings. The sheet resistance of the tungsten fabricated by the foundry is 0.4 Ω/□ at room temperature.

Let W = Width of the outer ring

The resistance of the outer ring =

$$R_{outer} = (2\ \pi\ r_1/W) * R_{sheet}$$

Where:

r_1=Heater radius

R_{sheet} = Sheet resistance of tungsten

If we use a width of 2µm, the resistance is 213.63Ω

Therefore the total resistance of the inner rings should be 60Ω

For the inner rings, assume that all the rings have the same width, and the same gap between them

Let:

w = width of ring

g = gap between rings

The inner rings occupy an area from a radius of 5µm to 168µm.

Therefore if the number of rings = n,

$$168\mu m - g - 5\mu m = n(w+g) \qquad (14)$$

Setting the gap as minimal, g = 2μm, the total resistance of the inner rings can be determined as follows:

Resistance of Ring 1 (inner most ring):

$$R_1 = \frac{R_{sheet} \cdot 2\pi[r_0 + (r_0 + w)]}{2w}$$

The resistance R_i of the ith ring is thus:

$$R_i = \frac{R_{sheet} \cdot 2\pi[(r_0 + i(w+g)) + (r_0 + w + i(w+g))]}{2w}$$

$$R_i = \frac{R_{sheet} \cdot \pi[2r_0 + 2i(w+g) + w]}{w} = \frac{R_{sheet}\pi}{w}[2r_o + w] + \frac{2R_{sheet}\pi \cdot i}{w}(w+g)$$

The total resistance of all the rings would be:

$$R_n = \frac{nR_{sheet}\pi}{w}[2r_o + w] + \frac{R_{sheet}\pi \cdot n(n+1)}{w}(w+g) = \frac{nR_{sheet}\pi}{w}[2r_o + w + (n+1)(w+g)]$$

Combining with equation 14 and after algebraic manipulation, we get:

$$w = \frac{R_{sheet}\pi[2r_o + (n+1)(R - r_o)]}{R_n - R_{sheet}\pi n}$$

With this, value of w for various values of n, and the corresponding values of g can be tabulated:

n	w	g
1	7.187707	150.8123
2	11.23584	67.76416
3	15.4649	37.20176
4	19.88731	19.61269
5	24.51664	7.083363
6	29.36774	-3.03441
7	34.45696	-11.88553
8	39.80226	-20.05226

For n> 5 the value of g becomes negative, so the number of inner rings must be less than 5. Among these, n=5 is the best choice, as this has the lowest value g (and hence the smallest gap between the rings). The heater with these ring sizes was simulated. The shape is shown in Figure 44.

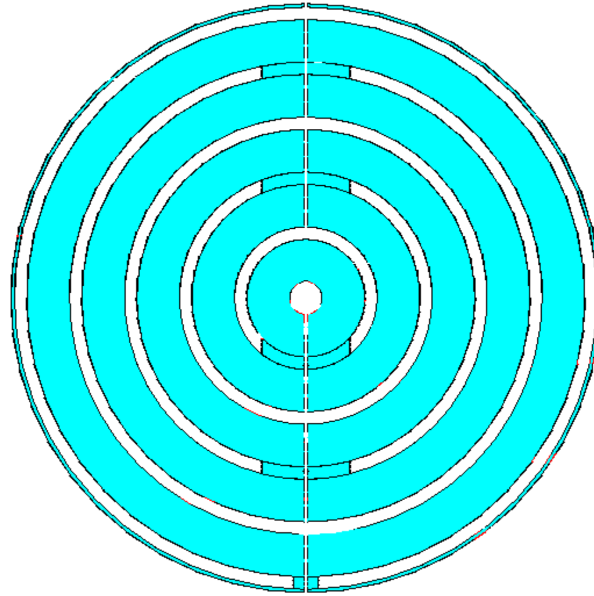


Figure 44: Shape of designed Multiring Heater

The temperature distribution within the heater is shown in Figure 45. Figure 46 shows a comparison of the temperature distribution for the ring, and multiring heaters. There is clearly a significant improvement for the multiring heater. The centre of the heater is slightly cooler than the outer ring (about 10°C at 600°C), but this difference is very small.

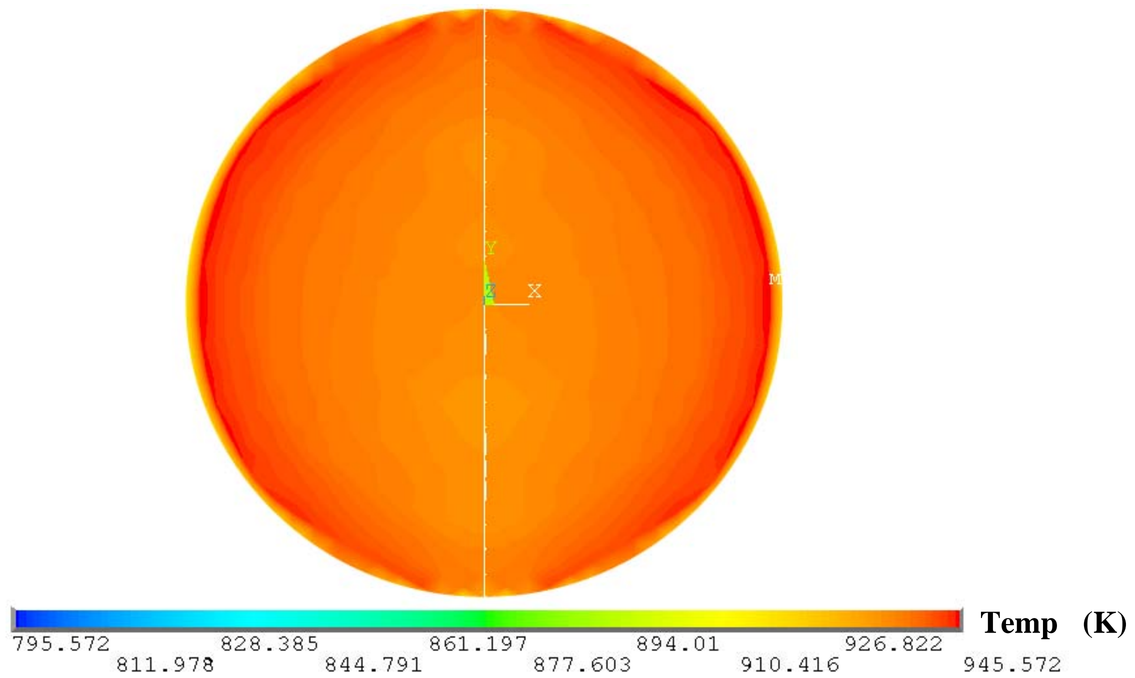


Figure 45: Temperature Distribution in Designed multiring Heater

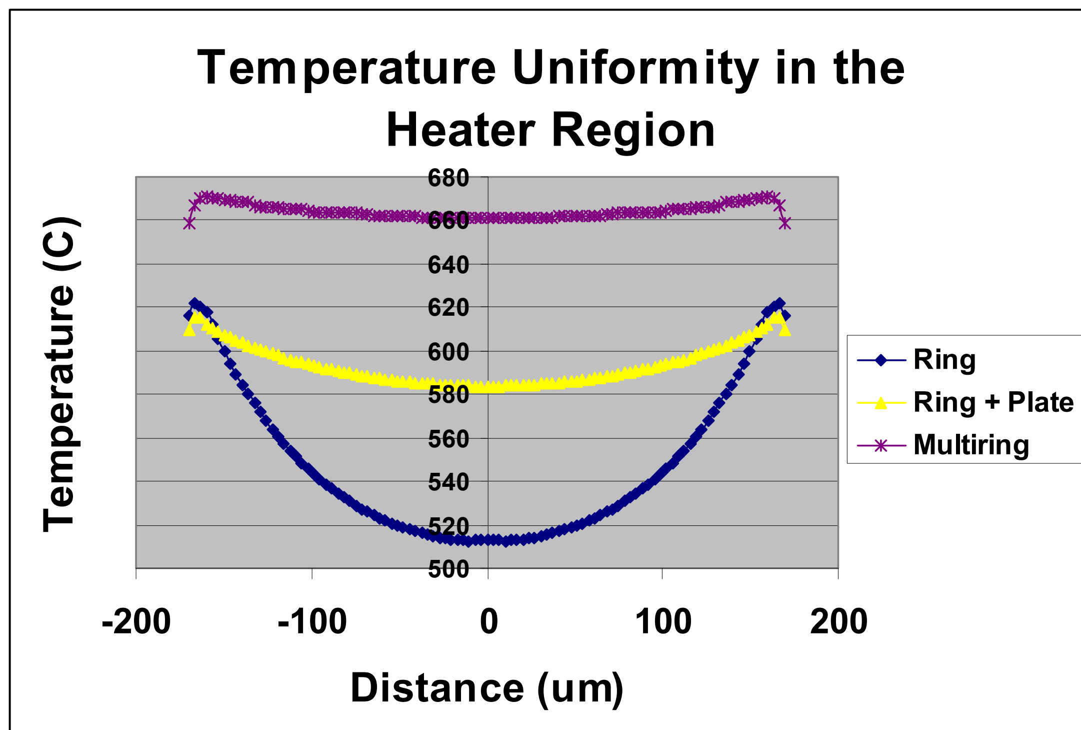


Figure 46: Comparison of Temperature Uniformity for: (i) Ring Heater, (ii) Ring heater + Spreading Plate, (iii) Designed Multiring Heater

Conclusions

Novel tungsten based SOI micro-hotplates have been proposed in this chapter. Tungsten can operate at high temperatures, and is CMOS compatible, allowing the possibility of circuit integration. The use of SOI gives more flexibility in design, and the interface circuitry is able to operate in high temperature environments.

A thorough thermal analysis of micro-hotplates has been presented. It has been shown that the power losses are mainly due to conduction through the membrane, and to the air. Radiation losses are negligible. The power consumption due to conduction through the membrane depends on the ratio of the membrane radius and heater radius, the larger the ratio, the lower the power consumption. Therefore for low power consumption the heater radius should be as small as possible, while the membrane radius should be as large as possible. However, this has to be balanced with the need for good sensitivity and smaller chip area depending on the application. The losses to air are mainly by conduction through air to the cooler parts of the chip, and effects of fluid flow are negligible. The losses to air above and below the membrane are almost equal. The micro-hotplates also have fast transient times (less than 10ms).

The temperature uniformity within the heater was also analysed. If air losses are not taken into account (for example in a vacuum), then it was shown that a ring heater provides a perfectly uniform temperature profile. However in air, the ring heater gives a very non-uniform profile, as heat escapes from the center of the heater, making it cooler than the outside. This can then be adjusted by carefully determining the heat loss to air from within the heater region, and designing inner heater rings that generate the exact amount of heat lost to the air from the heater region.

Chapter 3

Gas Sensors – Fabrication and Measurement

Standard Micro-hotplate Design

Micro-hotplates of two different sizes were designed:

Large Micro-hotplate: Heater Radius = 75µm, Membrane Radius =282µm

Small Micro-hotplate: Heater Radius = 12µm, Membrane Radius =150µm

Two different membrane sizes were chosen to determine the effect of membrane size on the heater characteristics, and also investigate other performance trade-offs due to size variations.

A large heater allows greater area for the sensing material – making deposition easier, as well as improving the sensitivity of the sensor. The heater is also much larger than the minimum metal width allowed in the fabrication process. This allows greater flexibility in the design of the heater shape as the width and the gap between the heater lines can be varied easily.

The small micro-hotplate was designed with the view of low area consumption and low power losses. As earlier analyses have shown, the power consumption of the heaters reduces as the heater area is reduced. However, for a very small heater radius, the resistance of the heater becomes very low. This results in the heater having a resistance which is much lower than that of the tracks – resulting in a lot of power being lost in the tracks. A 12 micron radius was chosen as it is a very small size, but still allows a relatively high resistance (55Ω) compared to tracks.

To choose the size of the small membrane, the heat loss due to conduction at 300°C was calculated for various different membrane sizes (Figure 47). The small heater area means that the convection and radiation losses are very low. Therefore just taking conduction into account is sufficient for an initial estimate. As expected, the figure shows that the power consumption reduces greatly as the membrane radius increases. After 150µm, however, further increase in membrane size results in only a marginal reduction in power consumption. Therefore 150µm was chosen as the membrane size.

In the earlier calculations, it had been determined that the ratio $r_2/r_1=e^{0.5}$ was the most optimum one to use. However, in that case, the membrane radius for the small heater would have to be 20µm, and a power consumption of about 50mW at 300°C. It was decided that it was more important to have lower power consumption, even if it meant a much larger membrane area. So a membrane radius of 150µm was used to reduce the power consumption by 5 times, even though that required an increase of area by 56 times. This also suggests that perhaps the formula for the optimum radius needs to be reviewed by added a scaling factor to give more importance to either power consumption or membrane area depending on the application and certainly manufacturing cost.

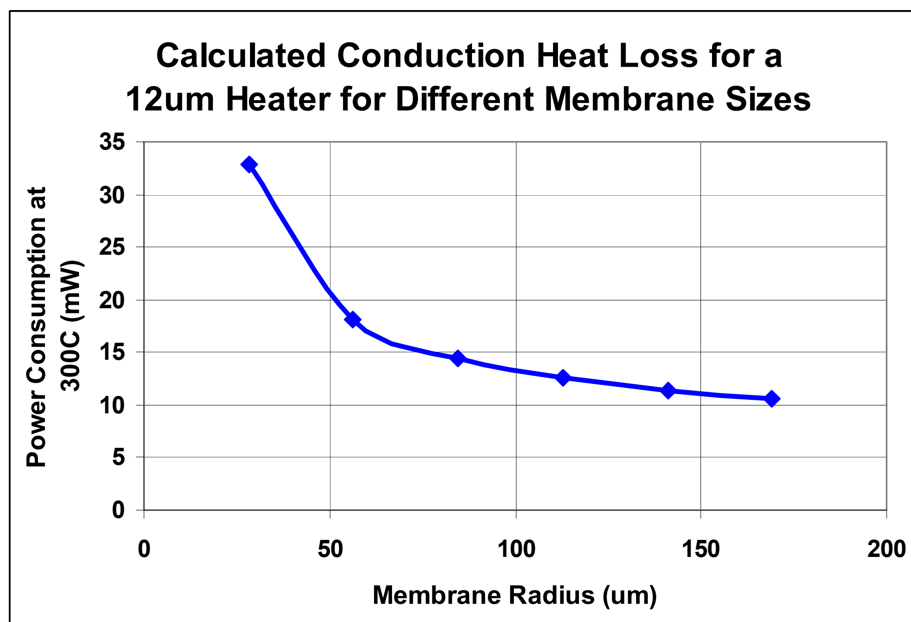
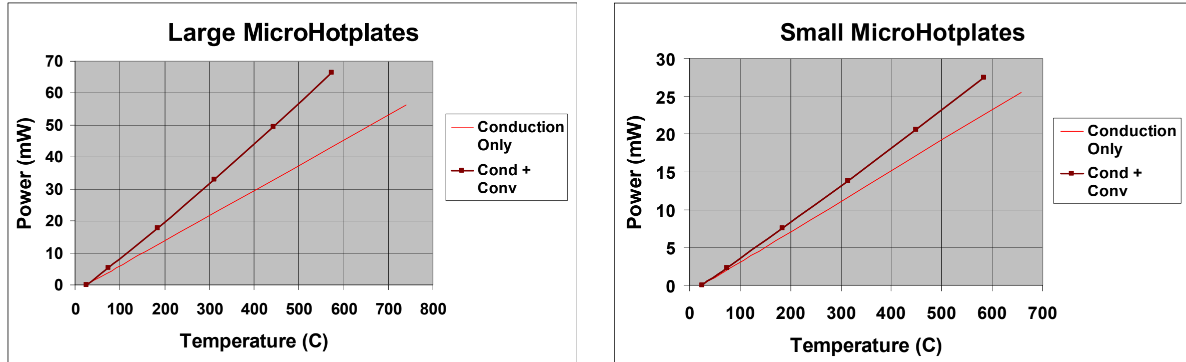


Figure 47: Effect of membrane radius of small heater on the conduction heat losses at 300°C

Both the heaters were simulated in Ansys. The power vs temperature graphs are shown in Figure 48. For these heaters, the power consumption is quite low, only 32mW at 300°C for the large heater, and 14mW at 300°C for the small heater.



(a): Power vs Temperature for large heater with/without effects of convection

(b): Power vs Temperature for small heater with/without effects of convection

Figure 48

Heater Design:

Large Heater:

Temperature uniformity is an important aspect of heater design, but there are other constraints in designing the heater too.

Resistance: The heater resistance should not be too high, otherwise the voltage needed would be much higher than that which can be supplied by CMOS circuitry. Typically, the required voltage should be less than 5V.

At 600°C, the power consumption is 70mW as shown in Figure 48a.

$$P(Power) = \frac{V^2}{R}$$

$$R = \frac{V^2}{P}$$

At 5V, P=70mW,

R = 357Ω

This is the maximum possible resistance the heater should have at 600°C. The maximum resistance at room temperature would be much lower:

The temperature coefficients of resistance for tungsten given by the CMOS foundry are:
TCR1: 2.05e-3 K^{-1}
TCR2: 0.3e-6 K^{-2}
Since

$$R = R_0[1 + TCR1(T - T_0) + TCR2(T - T_0)^2]$$

Where:
R – Resistance at Temperature T
R_o – Resistance at Temperature T_o
TCR1 – 1st Coefficient of resistance
TCR2 – 2nd Coefficient of resistance

R_o=157Ω at room temperature. (for a resistance of 375Ω at 600°C)

Therefore at room temperature, the maximum resistance should be 157Ω. However, this is an estimate, since the actual power required by the heater might be different from that given by the simulations, or the TCRs might be slightly different due to process variations. Therefore, it was decided to leave some margin and design a heater with a resistance of 100Ω.

Current Density:

Current density in microelectronics is also important, as a very high current density in metals can cause reliability problems. Aluminum, for example can degrade significantly due to electro-migration at high current densities, especially if the temperature is high. While tungsten does not suffer from electro-migration, the foundry recommends a maximum limit of 5mA/µm of width for reliability. 70mW of power, at 5V, means that the current through the heater could be as high as 16mW. Therefore the heater rings should be at least 4µm thick (leaving some margin for differences).

Temperature Uniformity:

Finally the heater should be designed such that the temperature is uniform throughout the heater region. It was decided to optimize the temperature uniformity for a temperature of 300°C. To calculate this, the power consumption values are taken from Figure 48:

Conduction power loss at 300°C : 22mW
Convection power loss at 300°C : 9mW

Using Equation 13, we find that the convection coefficient is 373.397W/m^2K, resulting in the power loss due to convection from within the heater to be 1.815mW. This is very small because the heater size is so small compared to that of the membrane.

Therefore:
Power needed in the outer ring of heater = 29.185mW
Power needed within the heater rings = 1.815mW

Therefore the heater needs an outer ring of very large resistance. Let *w* be the width of the outer ring, and *r* be the radius (in this case 75µm).

Therefore, the resistance of the outer ring of the heater, $R_O = \frac{2\pi r}{w}.R_{sheet}$

Where R_{sheet} is the sheet resistance given as 0.4Ω/□ by the foundry and r is the radius of the outer ring which can be taken as 75µm.

To make sure that the total heater resistance is 100Ω,
$R_i + R_o = 100$
Where R_i is the resistance of the inner rings.

Also , $R_o/R_i = 29.185/1.815$,

$R_o(1.815/29.185 + 1)=100$

$R_o = 97.283\Omega$

Therefore, the width of the outer ring should be 1.94µm.

But due to constraints on current density, such a small width cannot be allowed, as the minimum width should be 4µm as determined earlier. However, the same effect can be achieved by using 2 outer rings in series with each other, each having a width of 4µm. So while the width is doubled, the length is also doubled, and the resistance remains the same.

For the inner part of the heater, it was decided to have just one ring, as the power needed within the heater is very small. This also makes it easier to design the heater having tracks at opposite ends (results in better mechanical stability). The heater was designed as shown in Figure 49:

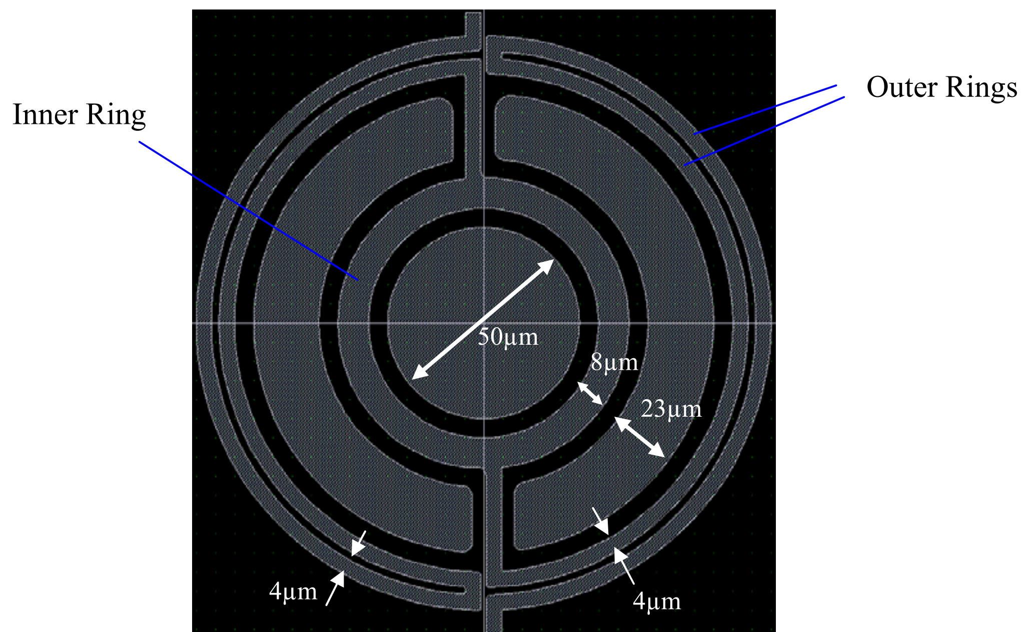


Figure 49: Design of Standard Large Heater

The inner ring is 8µm wide, and the inner and outer radii of the ring are 32µm and 40µm respectively. Since the two halves are parallel to each other, the resistance of the

inner ring is 2.25Ω, approximately the same as required by the calculations. Within the empty spaces within the heater region, floating metal plates were added to improve the temperature uniformity. All corners have been rounded to reduce current crowding, as well as to reduce concentration of mechanical stress.

Small Heater:

The small heater has a radius of only 12μm. Since the fabrication process is a 1micron process, there is not much flexibility in the design of the heater. Therefore a multi-ring heater was designed, so as to have as high a resistance as possible as compared to the heater tracks. The structure has a resistance of about 55Ω. This is still small (given that the tracks will have a high resistance, about 10-20 Ω). The multi-ring design is shown in Figure 50.

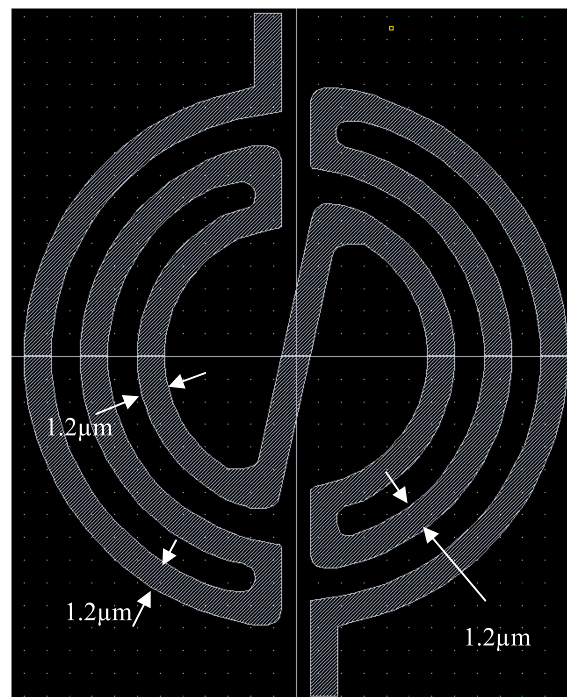
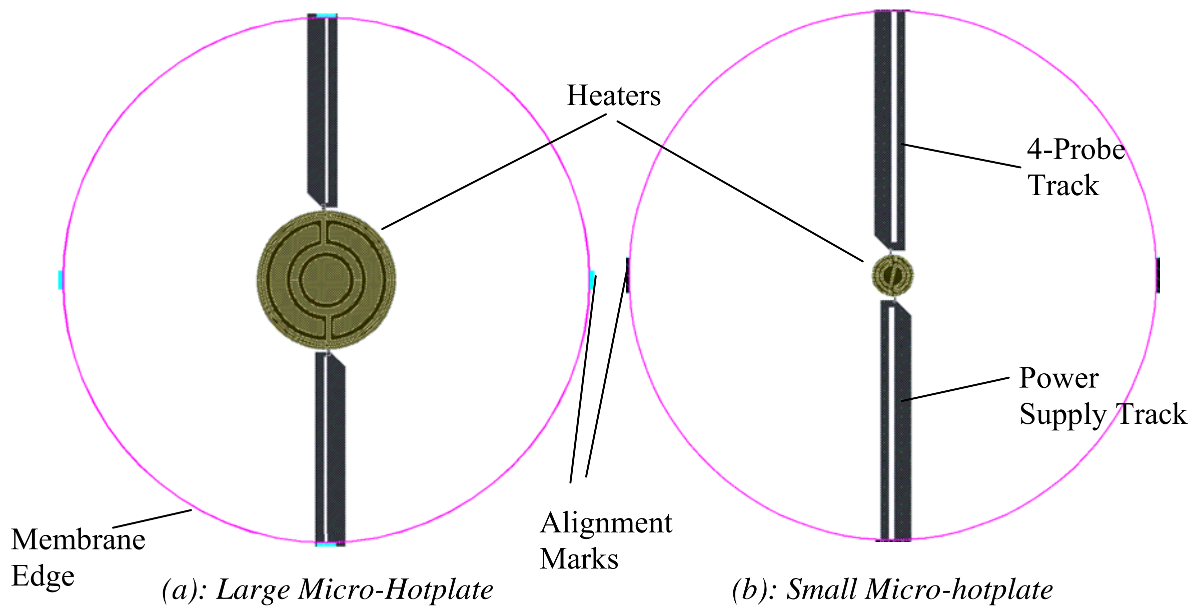


Figure 50: Design of Standard Small Heater

Standard Micro-hotplates:

The Micro-hotplates designed are shown in Figure 51. The layouts were done in Cadence (icfb version 5.0.0).



(a): Large Micro-Hotplate *(b): Small Micro-hotplate*

Figure 51

The heater tracks are at the opposite sides of the heater. This gives additional structural support to the membrane, as the tracks act as beams, providing strength to the membrane.

The tungsten heaters themselves are used as temperature sensors. To measure the resistance accurately, a four probe method is used [50]. The two thick tracks carry a constant current to the heater, while the voltage across the heater is measured using the two thinner tracks. Since negligible current flows in the thinner tracks, the resistance measured is more accurate.

There are also alignment marks at four sides of the membranes. They are made of metal 3. The alignments marks are used for accurate back to front alignment during the DRIE step. They also help to monitor how well the DRIE is aligned to the CMOS after the processing is completed.

A cross section of the heater is shown in Figure 52.

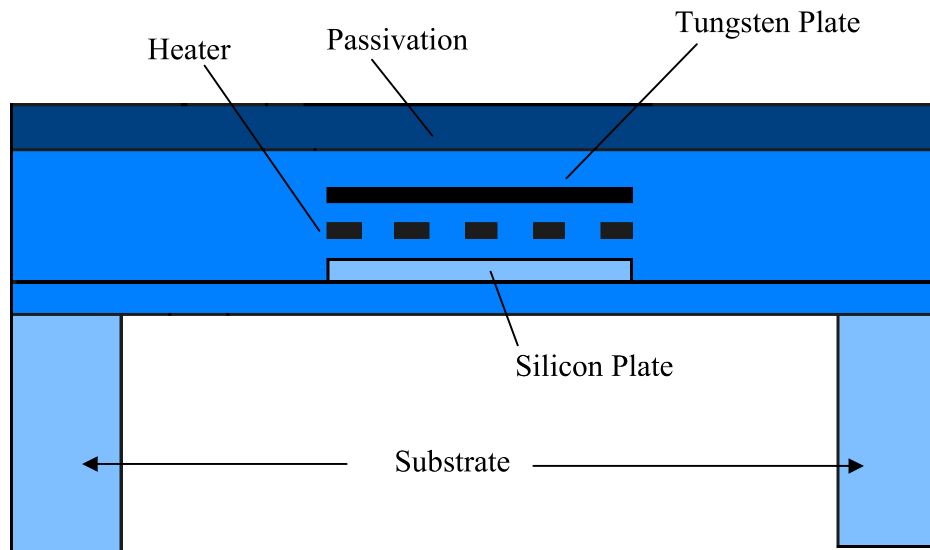


Figure 52: Cross-section of Micro-hotplate

For good temperature uniformity, a silicon plate below the heater, and a tungsten plate (formed of metal 2) above the heater were added.

The micro-hotplates described above can only be used as micro-calorimeters, since the resistance of the sensing material deposited on top cannot be measured. Therefore, some micro-hotplates for use as resistive gas sensors were also designed. They are similar to the micro-calorimeters, except that a pair of metal 3 electrodes were designed above the heater region. The passivation on to these electrodes can be etched away during the CMOS process, using the same process step which is used to form the bond pads on chips. These leaves the electrodes exposed, and gas sensing materials can then be deposited on to them. These are shown in Figure 53-Figure 55. Due to fabrication constraints, they were only designed for the large heaters.

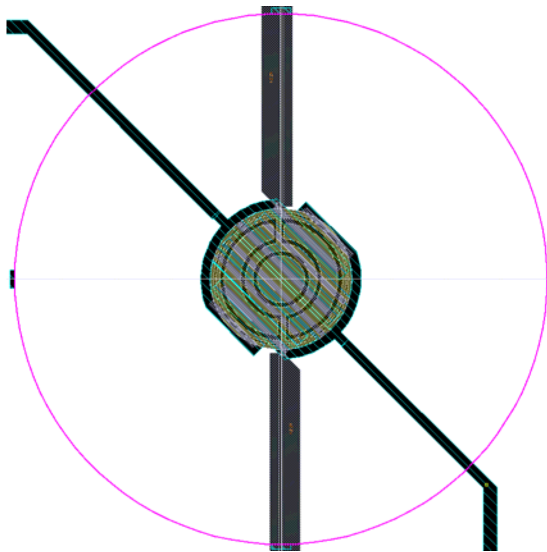


Figure 53: Resistive Micro-hotplate

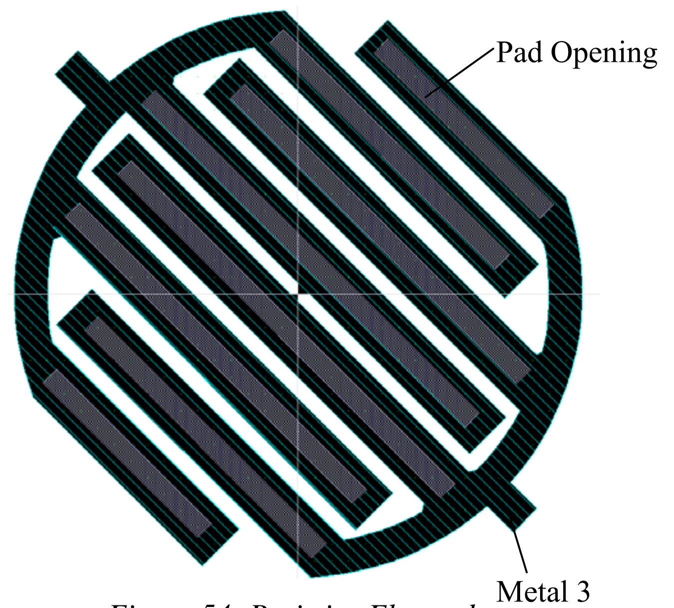


Figure 54: Resistive Electrodes

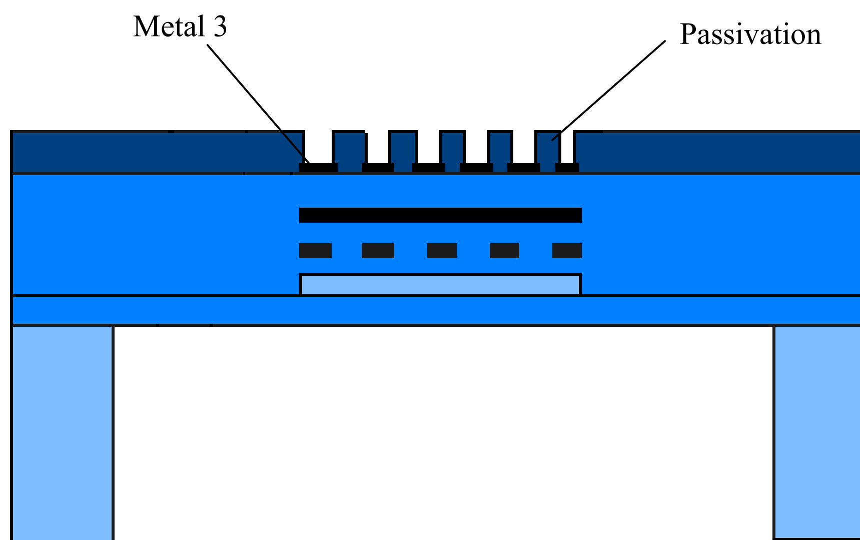


Figure 55: Cross-Secton of Resistive Micro-hotplate

Micro-hotplate Variations:

Besides these main structures, a number of other variations were also designed to get a better perspective of micro-hotplates performance and limits, and determine the best ways to design the micro-hotplates for future batches.

Membranes:

Because membranes are very thin, they can potentially break. So some variations were tried to make the membrane more mechanically stable, by using the silicon and metal 2 layers. These are shown in Figure 56. In Figure 56a, beams of silicon are used, while in Figure 56b beams of Metal 2 (Tungsten) were implemented. In Figure 56c, the whole membrane has a layer of silicon. While these improve the mechanical strength of the micro-hotplate, the power consumption will increase significantly.

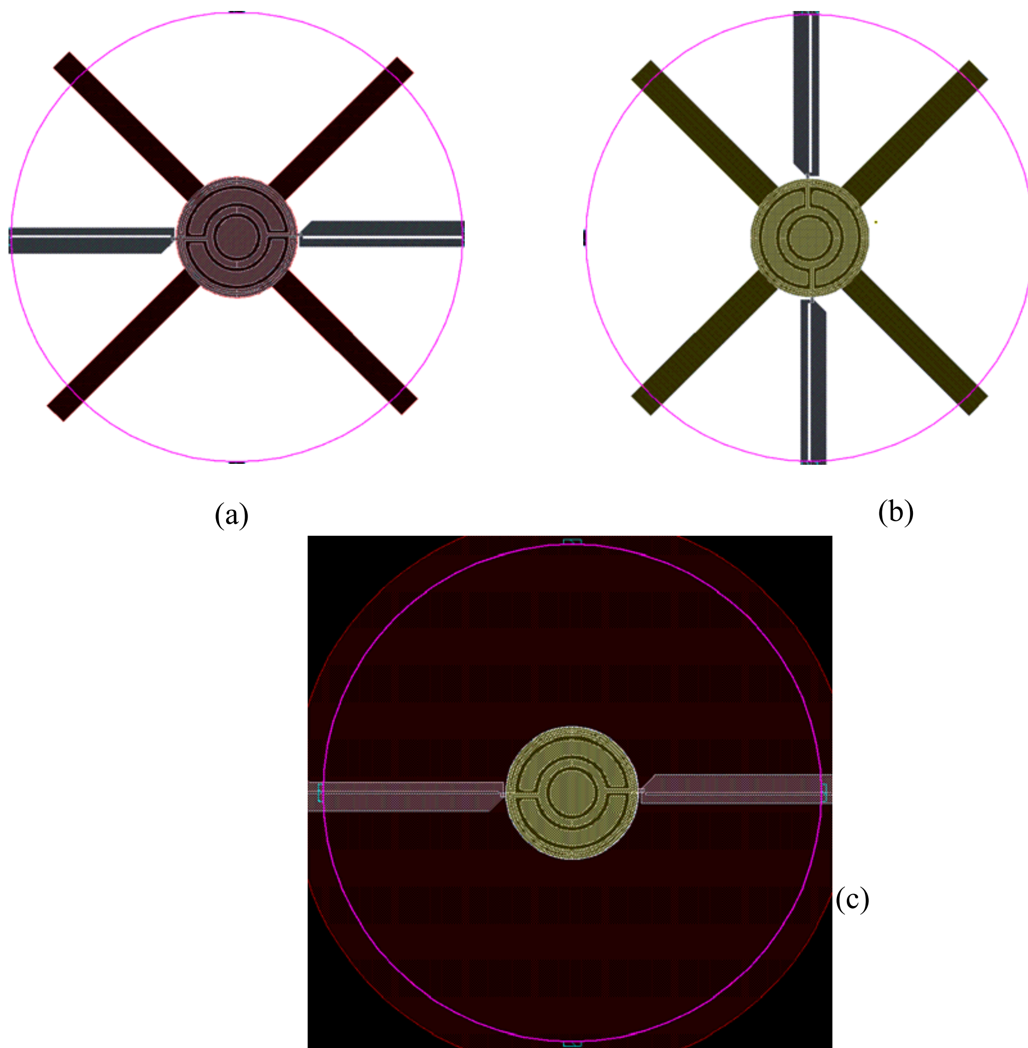


Figure 56: (a) A membrane reinforced by Silicon Beams, (b) membrane with Tungsten Beams (c) Membrane including a thin silicon layer (SOI layer)

Size:

Two different heater sizes (100µm and 50µm) were also designed for the large micro-hotplates, while two different sizes were designed for the small heater (9µm and 15µm). This was just done in order to assess how the heater size affects power consumption.

Temperature Sensors:

Besides using the tungsten heater as a temperature sensor, diodes and silicon resistors can also be used as temperature sensors. Like tungsten, the resistance of silicon increases with temperature, and this can be used to measure the temperature. In diodes, the forward bias voltage drop reduces with temperature, approximately by 0.2V per 100°C rise.

These are fabricated on the thin SOI layer (otherwise used as a heat spreading plate below the heaters) present in the SOI process. The diode and silicon resistor used are shown in Figure 57, Figure 58.

The diode is a P+/P-/N+ diode, incorporating a small p- resistive region. The silicon resistor is made of P+ doped silicon, as this has a higher temperature coefficient of resistance (TCR) than N+, and hence is more sensitive to temperature rise. The resistor is a thin rectangular strip of P+, surrounded by an N-well region. The thin strip is used to have a high resistance for the temperature sensor.

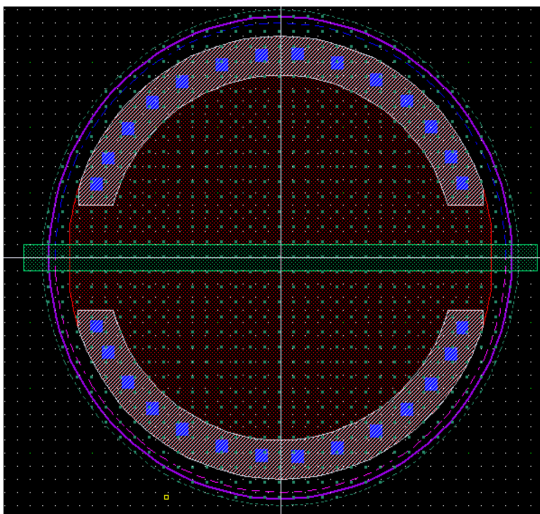


Figure 57: Diode Temperature Sensor

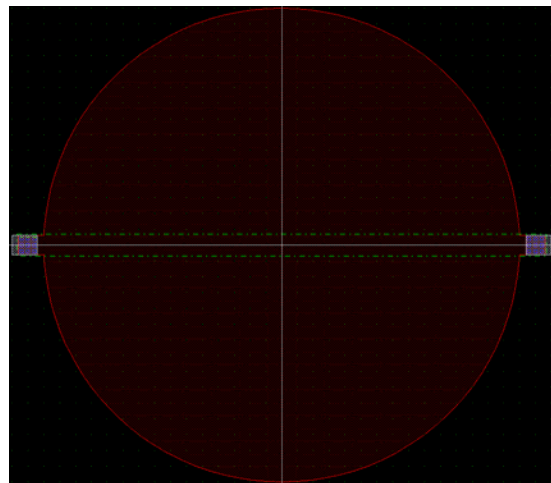


Figure 58: Silicon Resistive Temperature Sensor

Fabrication

The micro-hotplates were fabricated on 6” wafers by first using a commercial SOI-CMOS process. This is a 3 metal, 1µm process, and can employ either aluminum or tungsten metallization. This was followed by back etching to the buried oxide by DRIE at a commercial MEMS foundry, to from the membrane. Figure 59 shows the processing steps to form the micro-hotplates[3].

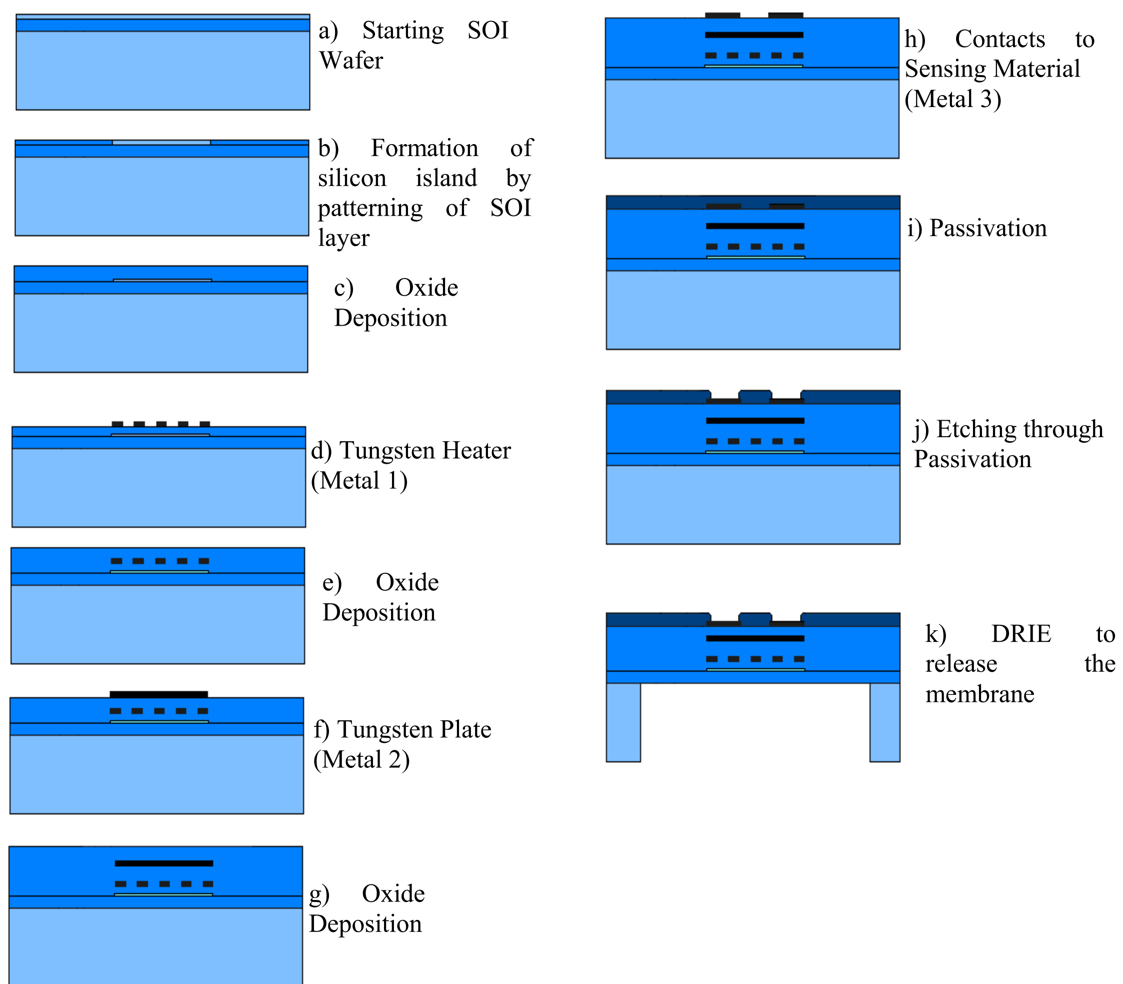


Figure 59: Fabrication process steps

---

[3] A total of 16 chips were designed at the University of Cambridge and the University of Warwick and were sent for fabrication. The first four chips were of Tungsten micro-hotplates and were designed here.

Steps a-j were performed using the standard processing steps for the SOI process offered by the CMOS foundry. (Some of the processing steps, such as polysilicon and ion implantation were used in the process for the electronic circuits, but not required directly for micro-hotplate fabrication.). DRIE (step k) was performed at a MEMS foundry to release the membrane.

Figure 60 shows the fabricated micro-hotplates. The membranes have very good alignment to the top CMOS layers, the membrane edges being right under the top metal alignment marks. The sensing electrodes are shown in Figure 61. 8 wafers were fabricated, out of which wafers 1,2 and 3 had aluminum metallization, while wafers 4,5,6,7 and 8 had tungsten metallization.

Some of these wafers were then diced at a packaging house. The standard dicing process consists of a sharp, diamond tipped blade sawing through the wafer, while at the same time being cooled by water at high pressure. This caused a particular problem, as the high pressure water caused the membranes to break. Therefore, the process was done without any cooling water being supplied to the cutting blade – making the process slower, but not damaging the membranes.

Most of the measurements were done on full wafers. This was because it was easier and quicker to measure the same design on many different parts of the wafer. However, some measurements, when needed, were performed on single chips.

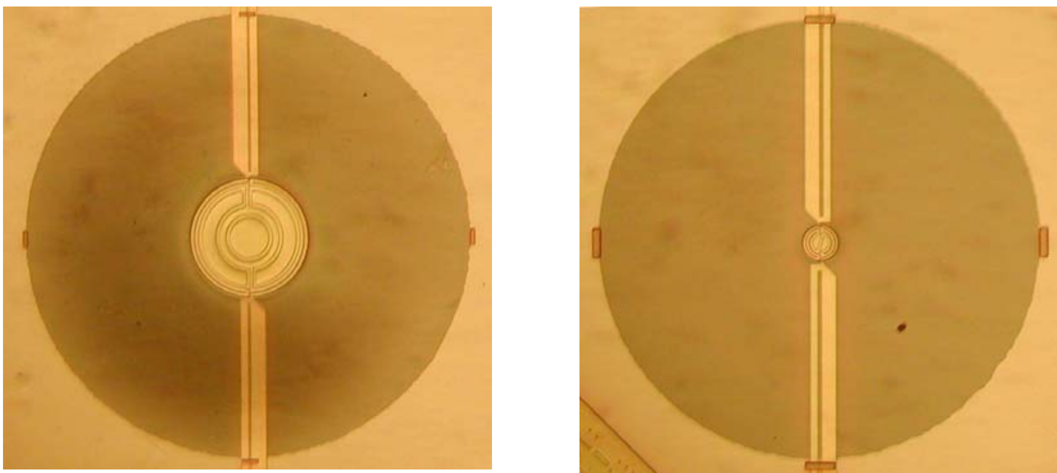


Figure 60: The fabricated Large and Small Micro-hotplates

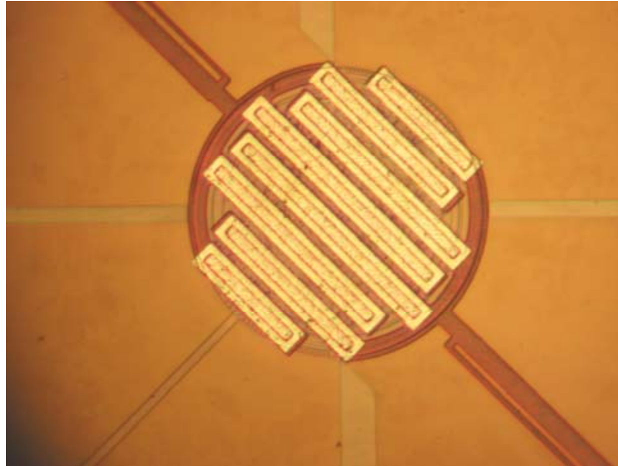


Figure 61: Gas Sensing Electrodes

Measurement and Analysis

Pre-Etch Measurements:

After the first CMOS step at XFab, the wafers were characterized before sending for DRIE. This was to check the uniformity and various characteristics of the devices.

Figure 62 shows the measurement of the resistance of the large tungsten heaters. The figure shows the resistance values for different chips across the wafer. The resistance was measured using both 2-probe, and 4-probe methods. The 2-probe method gave a significantly higher resistance, showing the track resistance is significant. The heater resistances are fairly uniform across the wafer, and approximately equal to 100Ω (average=103 Ω), which was the target design value. Figure 63 shows the measurement of the same device on a different wafer. The results are similar to the first wafer, showing good uniformity.

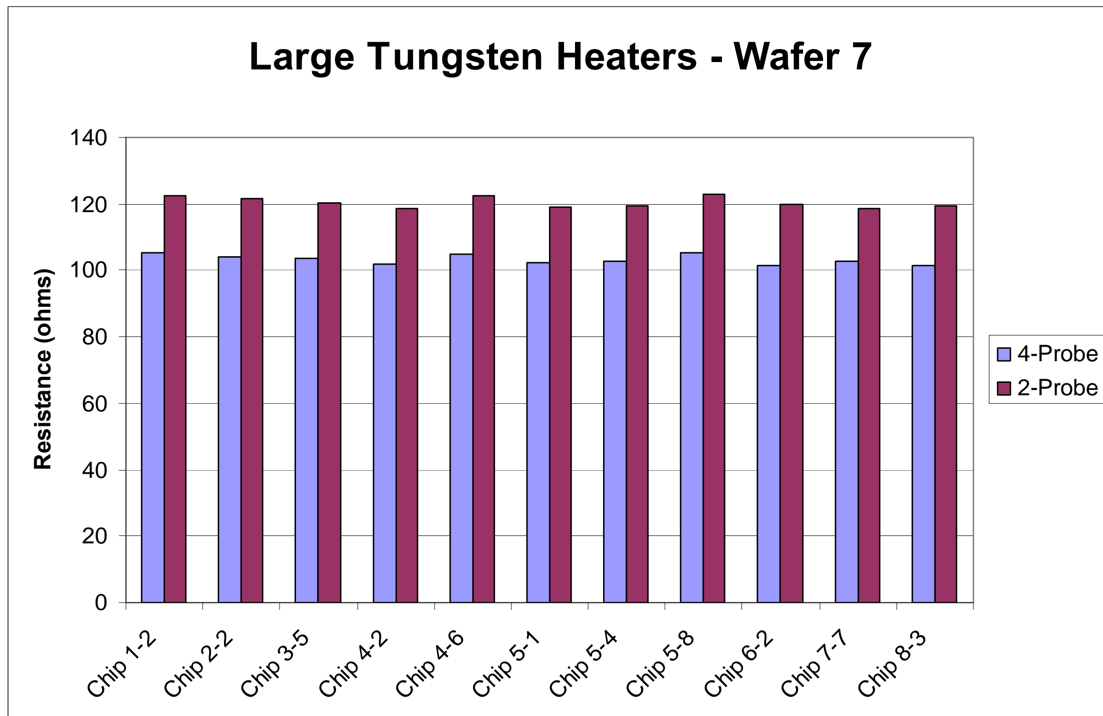


Figure 62: Resistance of Large Tungsten Heater on Wafer 7

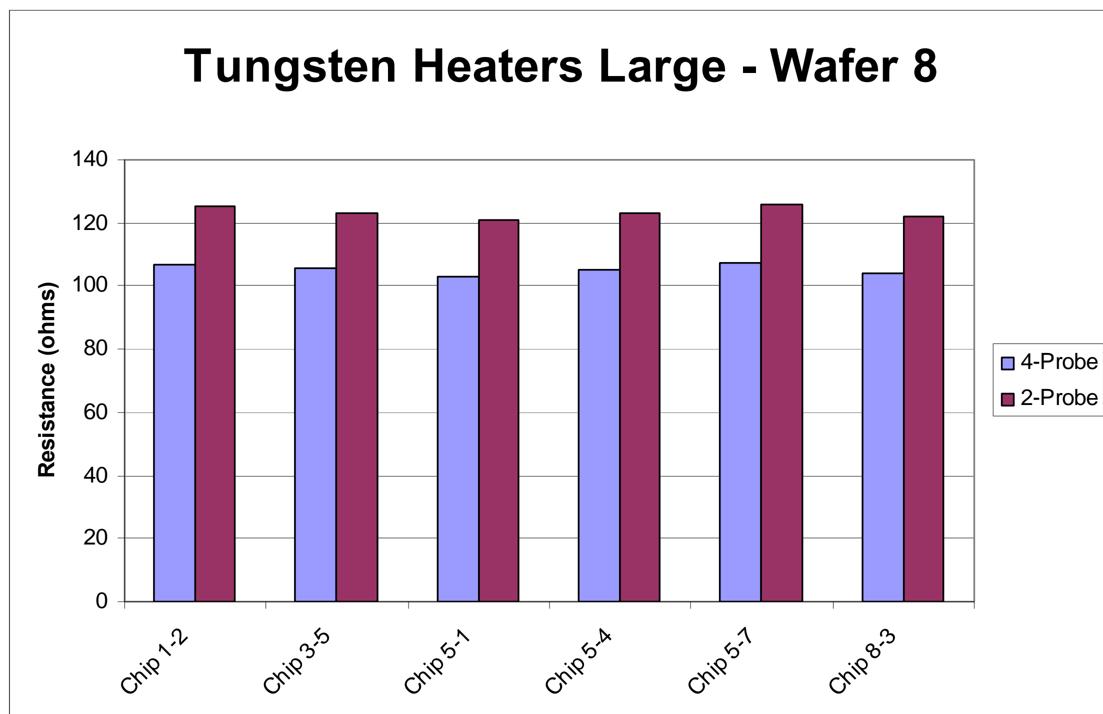


Figure 63: Resistance of large Tungsten heater on wafer 8

Figure 64 shows the resistance measurement on the small heater. Again the values are very uniform, however, the values are much higher than those calculated during the design phase. The measured resistance value is 78Ω, compared to the calculated design value of 55 Ω. This was attributed to the fact that the heater rings are very thin (1.1μm), which increases the resistance due to edge effects (a recheck of the process specification provided by the CMOS foundry indeed showed this to be the case). Interestingly this also improves the performance, because now, the heater resistance is relatively larger as compared to the tracks – which would result in slightly lower power losses in the tracks. Measurements on another wafer showed similar values (Figure 65). Diodes, as well as the Silicon resistive temperature sensors show good uniformity as well (Figure 66, Figure 67).

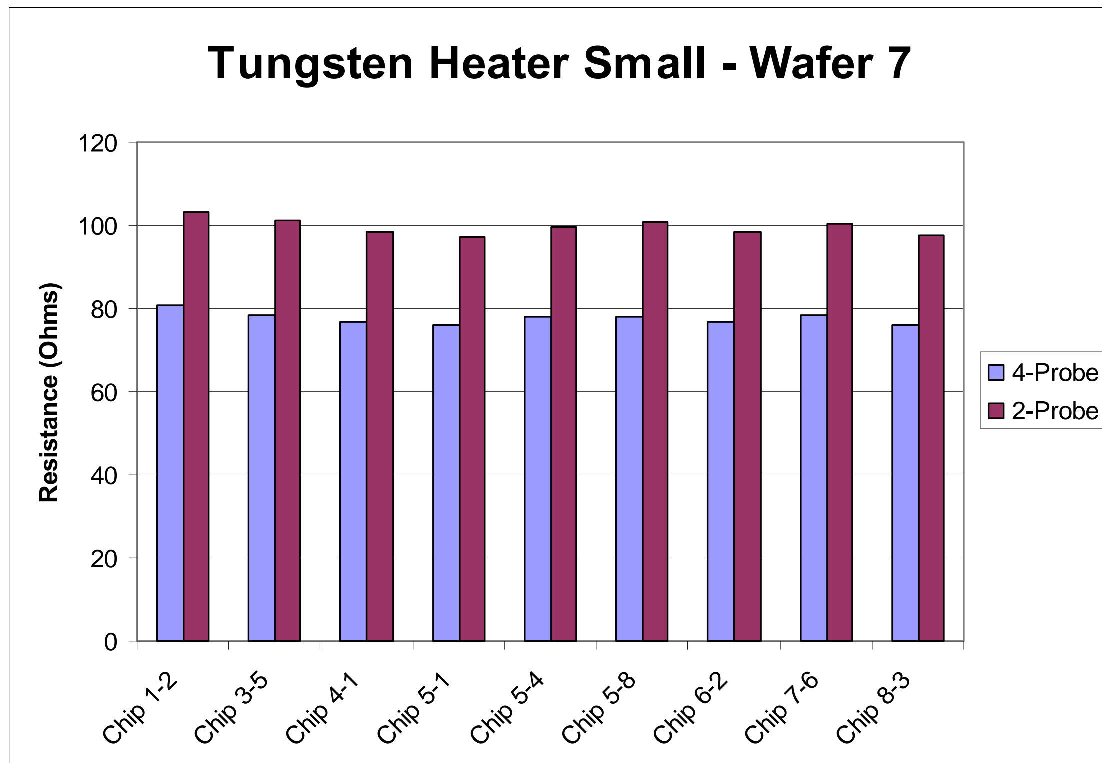


Figure 64: Resistance measurements for the small heater

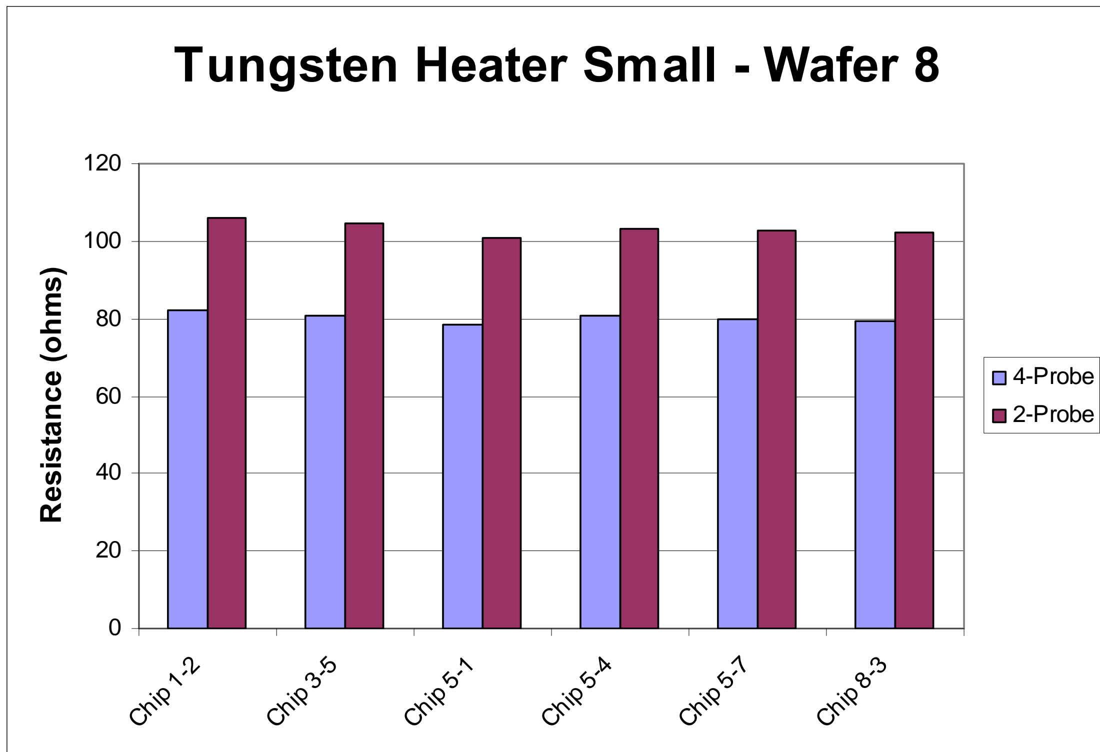


Figure 65: Resistance measurements for the small heater on a different wafer

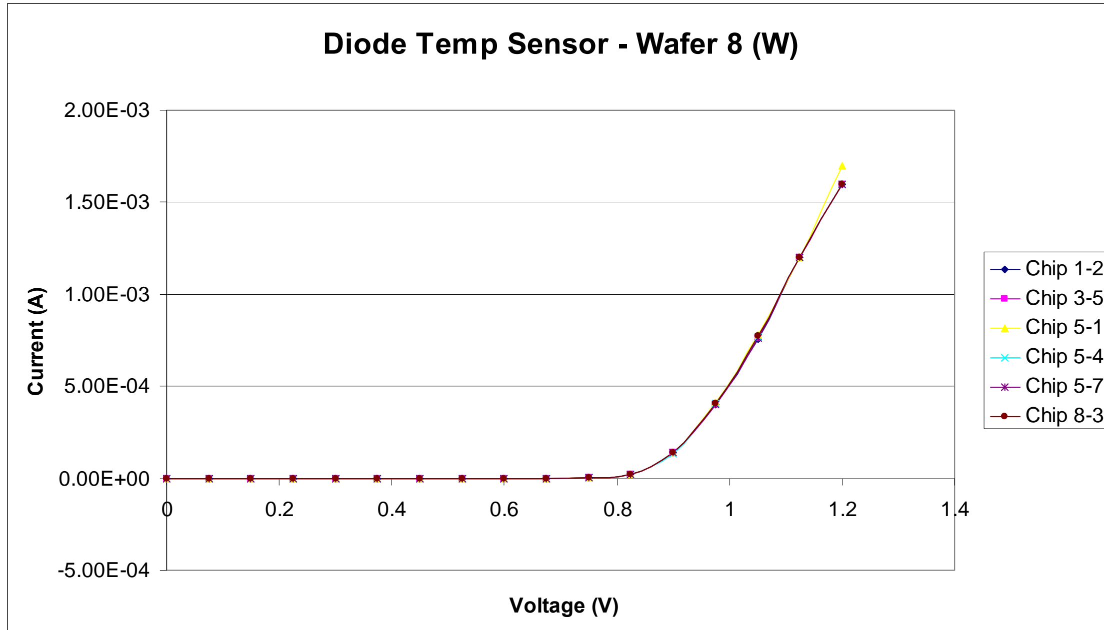


Figure 66: Diode Measurements

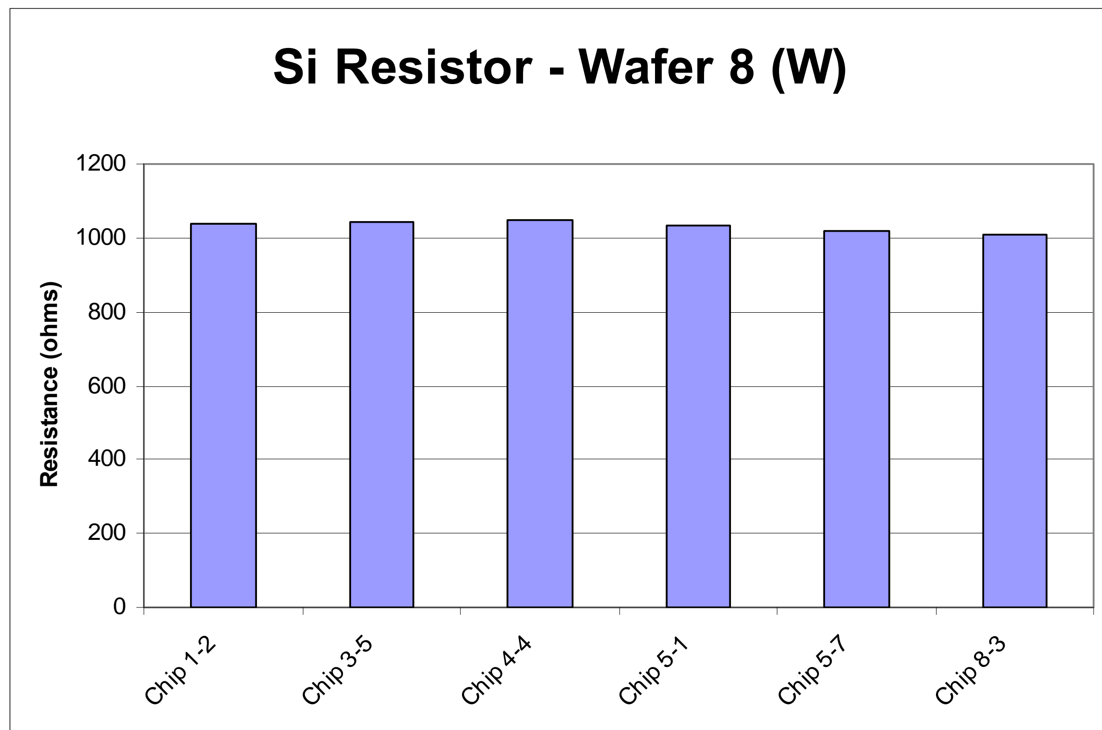


Figure 67: Resistance measurements of Silicon Resistive temperature sensor

An aluminum wafer was also tested, and the result is shown in Figure 68. The resistance of the large aluminum heater is much lower than the calculated value, (18 ohms, compared to 25 ohms calculated). The reason for this is that the aluminium process is usually used for electronic circuits, where the lower the resistance of the aluminum, the better. Therefore, the sheet resistance cited in the data sheets (0.1Ω/□) was a maximum, and the actual sheet resistance was much lower.

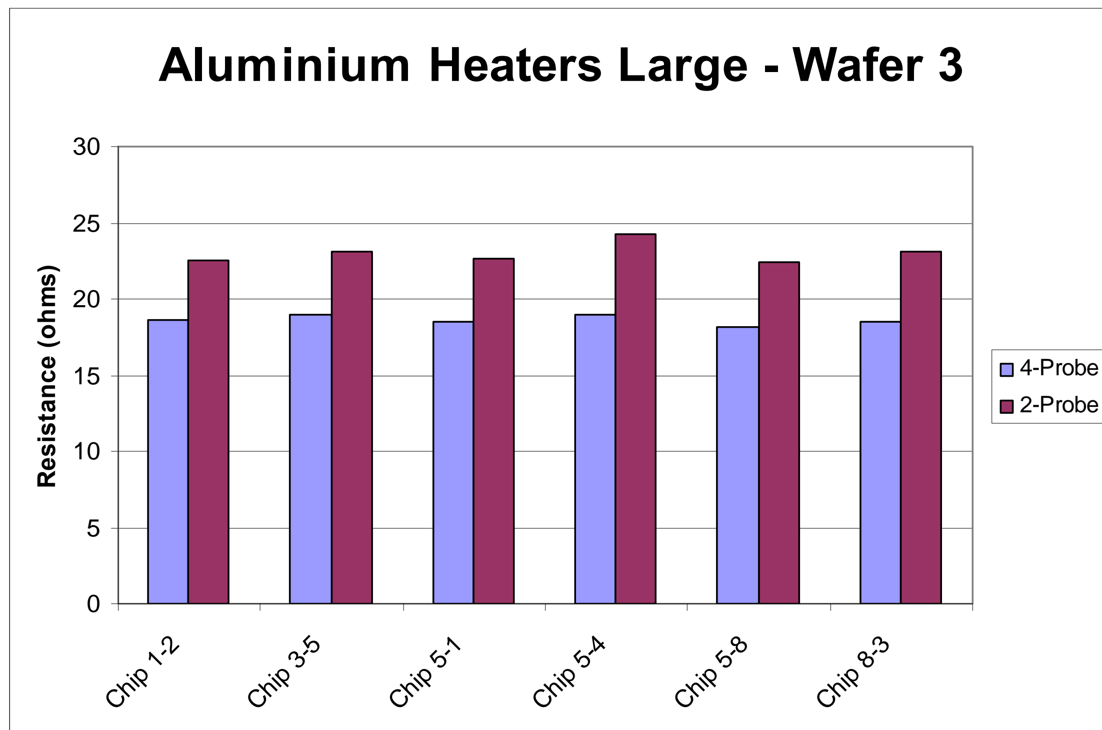


Figure 68: Resistance measurements of large Aluminum heaters

Thermal Characterization and Analysis

Calibration

All the temperature sensors used were first calibrated up to 300°C using a high temperature chuck (Signatone S-1060R-6TG), with an accuracy of 1°C. The calibrations were performed on unetched wafers. This was because the etched wafers suffered from bowing at high temperatures. At high temperatures, the wafers become stressed due to uneven expansion of various layers, which cause them to bend slightly. This was more prominent in the etched wafers, and made it hard to get good results.

The calibration curves for tungsten, aluminum, diodes, and silicon P+ are shown in Figure 69-Figure 73. The temperature coefficients of resistance were then extracted from these results by curve matching, and are summarized in Table 2. These values were very similar to those given by the CMOS foundry.

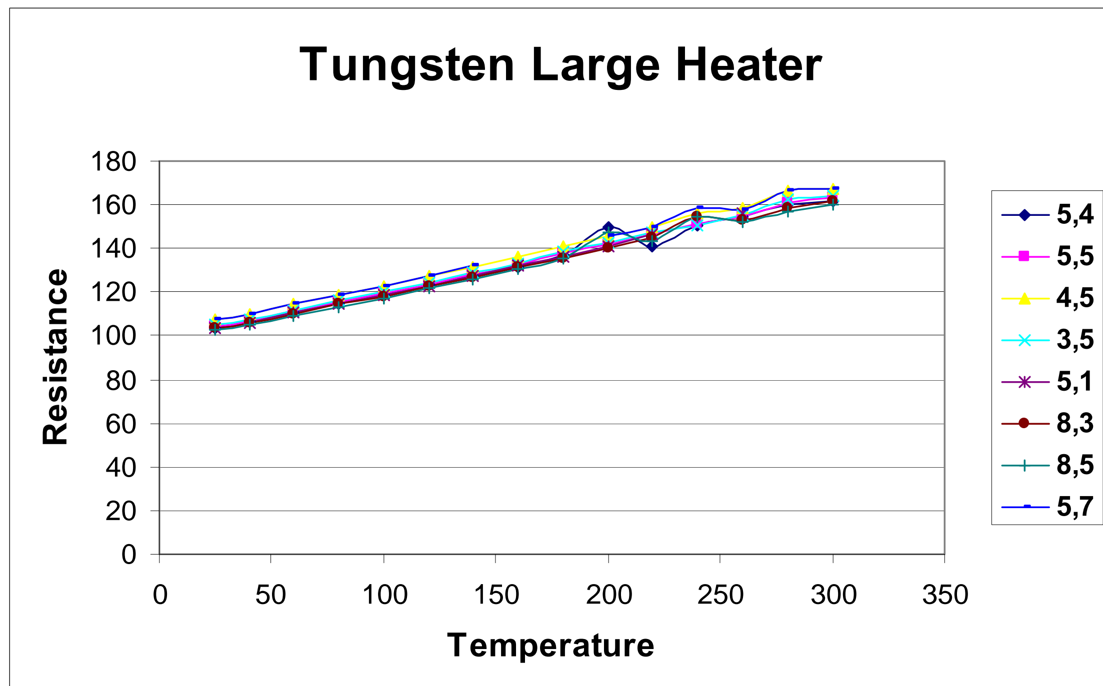


Figure 69: Calibration Curve for Tungsten

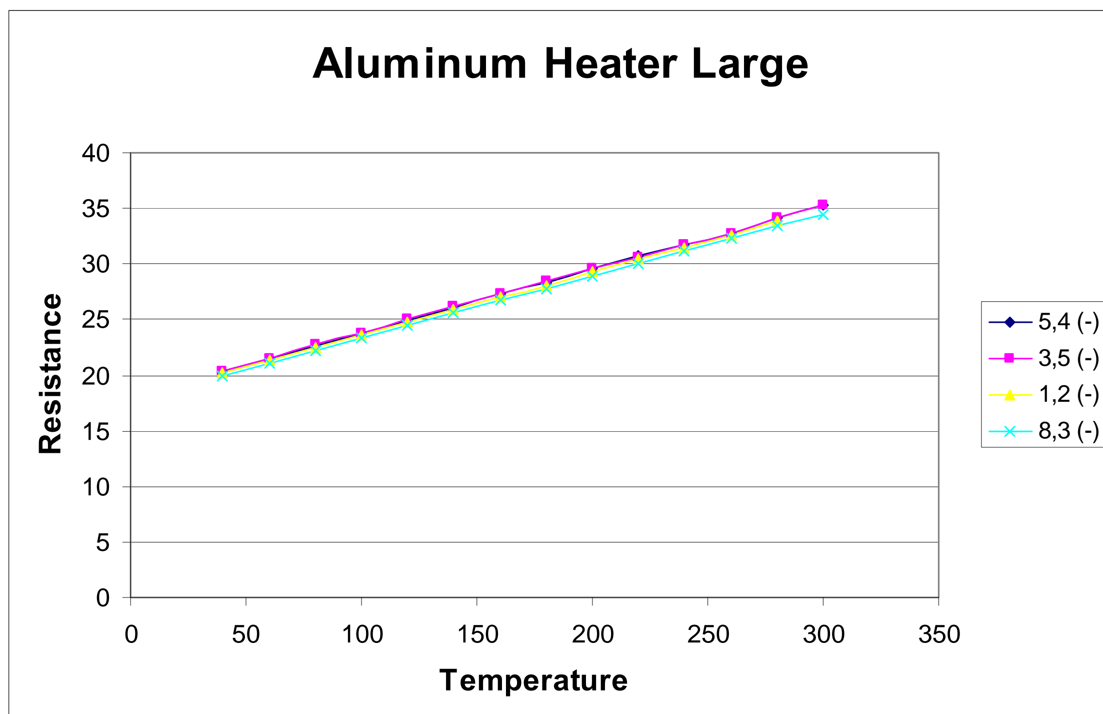


Figure 70: Calibration for Aluminum

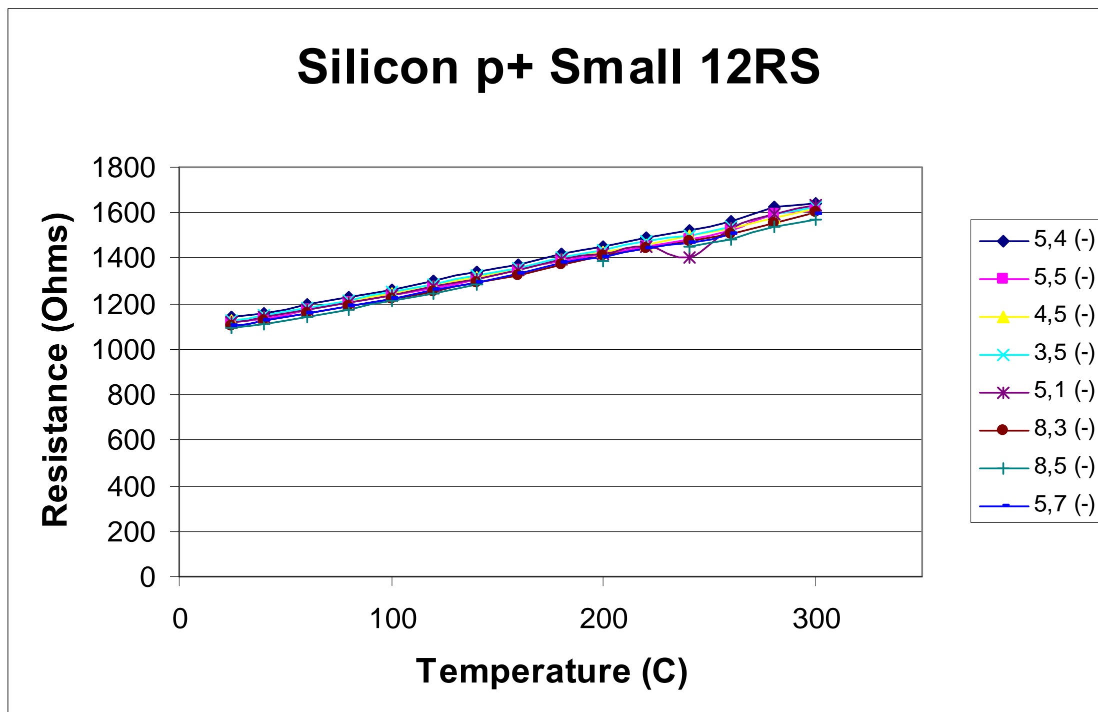


Figure 71: Calibration Curve for Silicon P+ Region

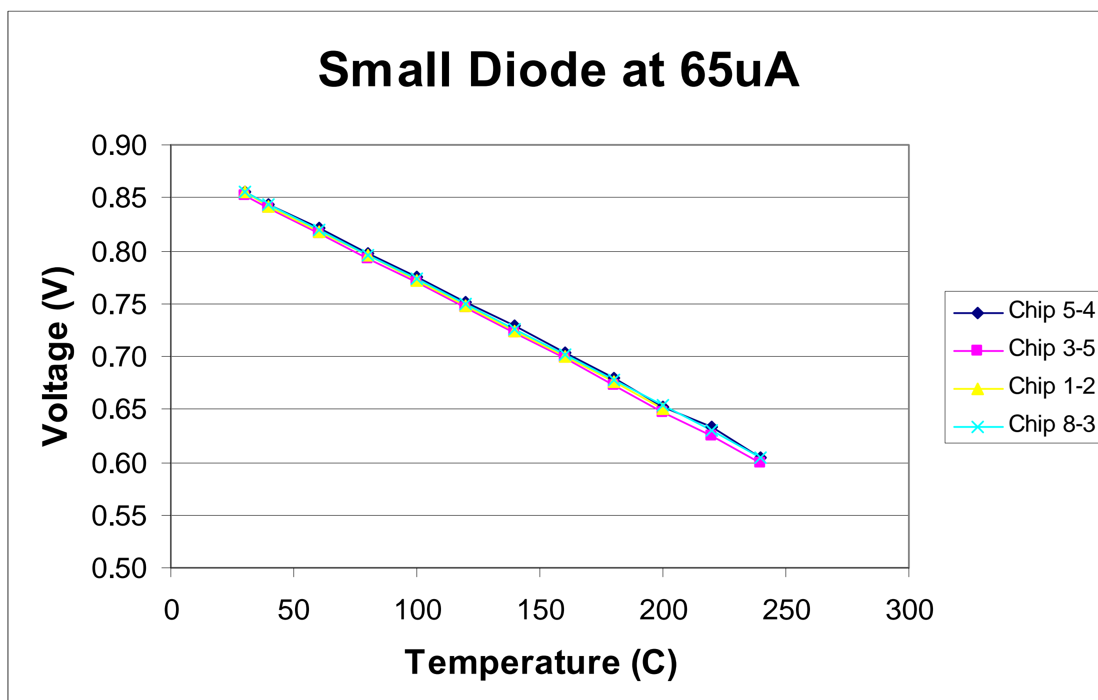


Figure 72: Calibration Curve for Diode for small heater

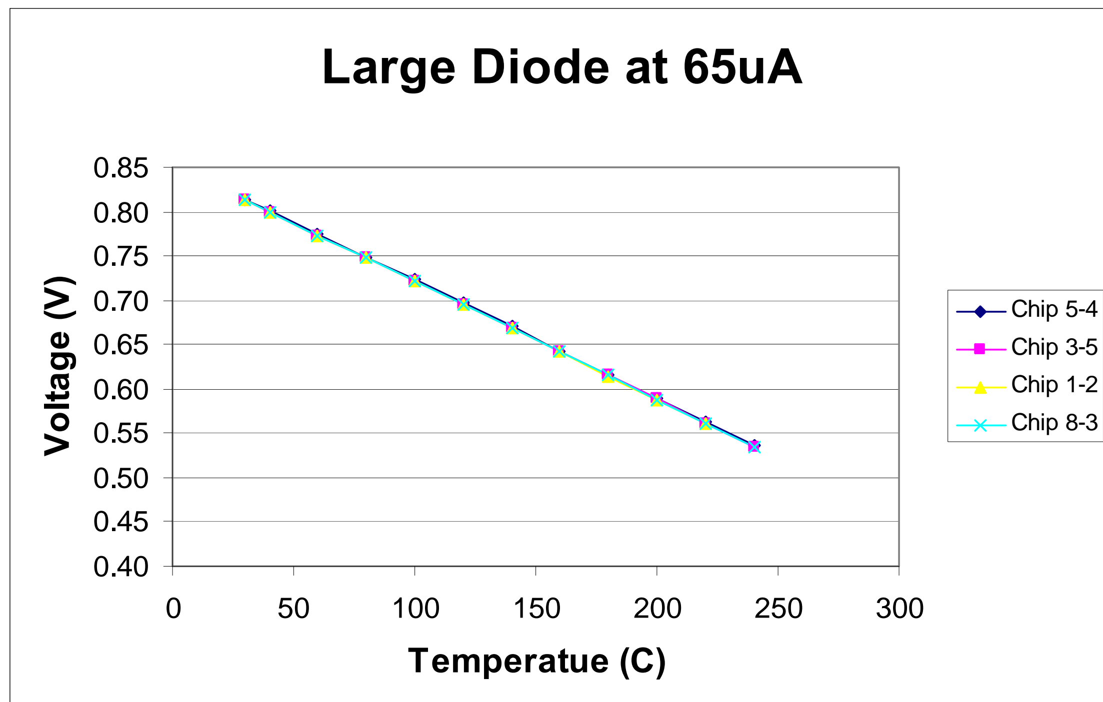


Figure 73: Calibration Curve for Diode for Large Heater.

Material Property	**Measured**	**Given by CMOS Foundry**
Tungsten TCE 1 (K^{-1})	2.086×10^{-3}	2.05×10^{-3}
Tungsten TCE 2 (K^{-2})	0.378×10^{-6}	0.3×10^{-6}
Aluminum TCE 1 (K^{-1})	3.19×10^{-3}	3×10^{-3}
Silicon N+ TCE 1 (K^{-1})	1.321×10^{-3}	1.35×10^{-3}
Silicon N+ TCE 2 (K^{-2})	0.299×10^{-6}	0.29×10^{-6}
Silicon P+ TCE 1 (K^{-1})	1.537×10^{-3}	1.51×10^{-3}

Table 2: Calibration results of the temperature coefficient of resistance alongside values quoted by CMOS foundry. (note: no values were given by the CMOS Foundry for TCE2 of Silicon P+ and Aluminum)

Power Consumption

The power consumption of the heaters was measured by applying a constant current, and measuring the voltage across the heater. The power source unit (HP4070, controlled by a computer) was used to apply the current for 2 seconds before measuring the voltage. This was necessary as the micro-hotplates need a finite time (in milliseconds) to heat up. To make sure that 2 seconds were enough to perform an accurate measurement, a few measurements were performed after applying power for higher amounts of time (up to 3 min). The results were same, so 2 seconds was considered to be sufficient.

Figure 74, Figure 75 show the power consumption vs temperature curves for the standard large and small micro-hotplates (the temperature is measured by using the tungsten heater itself as a temperature sensor). Because of the 4 point measurement, it was possible to determine both, the power consumed by the heater only (by 4-wire measurement), as well as the power consumed by both the heater and connecting tracks (using just 2-wire measurements). The 4-wire measurements represent the actual heat loss in the micro-hotplate (i.e. the actual useful power). The 2-wire measurements include the power losses in the tracks.

Figure 76 shows the power consumption for the large heater with resistive gas sensing electrodes. The power consumption is slightly higher, this is because of the additional power loss caused by the tracks to the sensing electrodes.

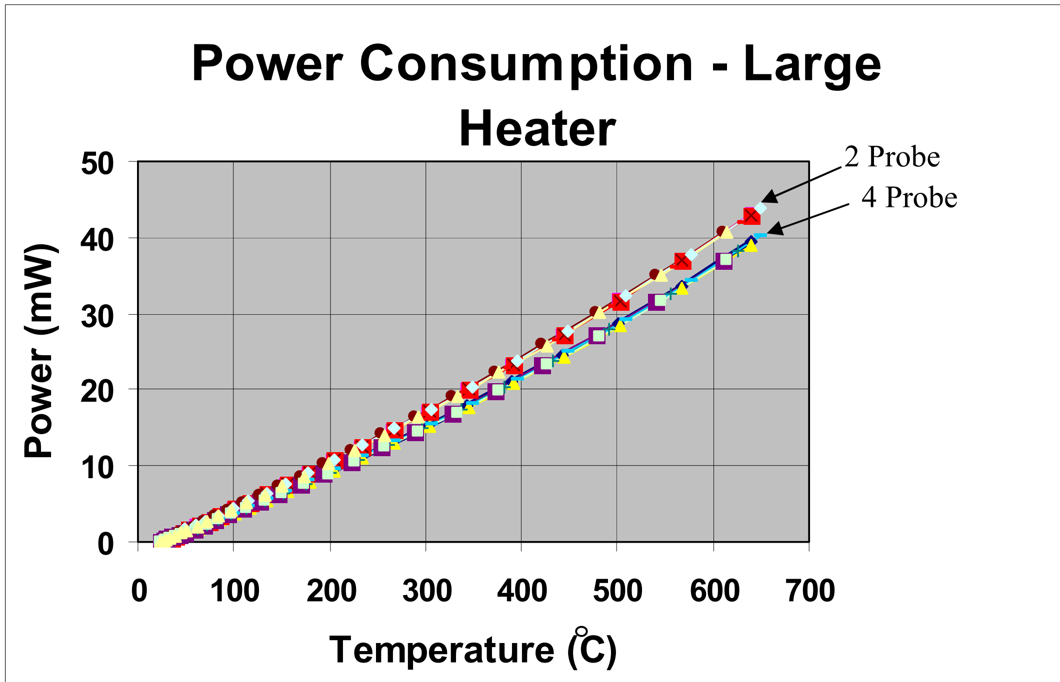


Figure 74: Power/Temperature Curve for Large Heater

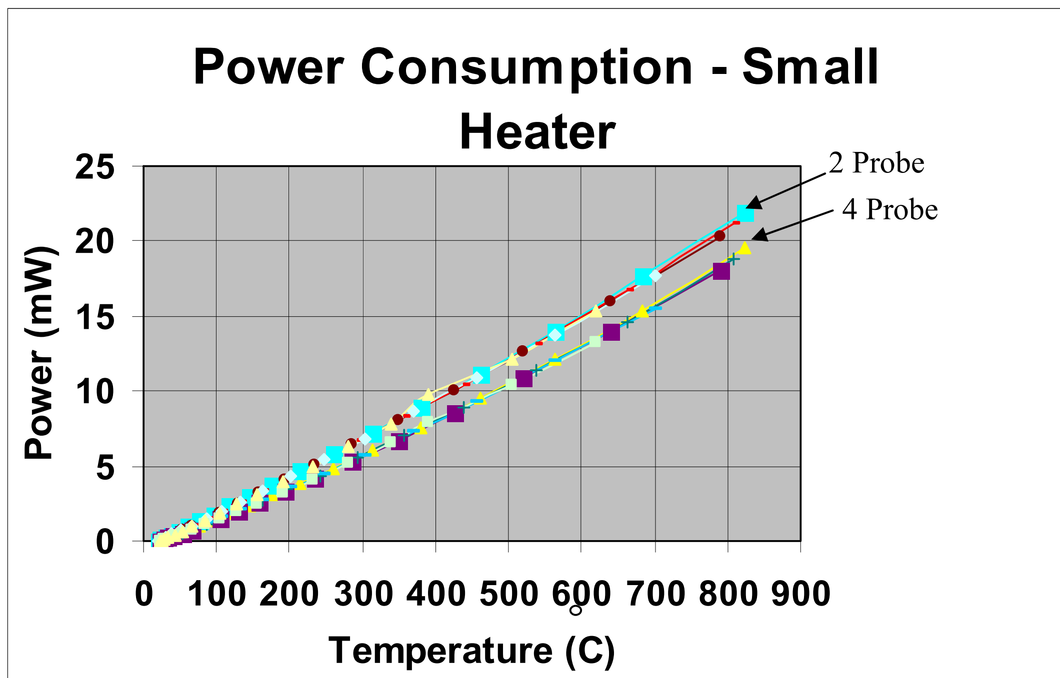


Figure 75: Power/Temperature Curve for Small Heater

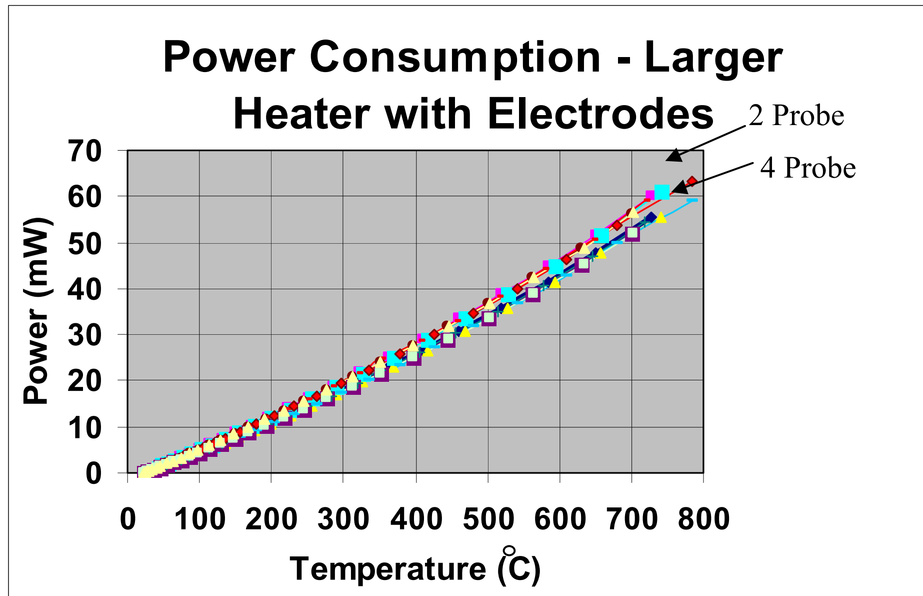


Figure 76: Power consumption for Large micro-hotplates with electrodes

The curves for both the large and small heater show very high reproducibility. Different devices across the wafer have the same characteristics. This was also checked for variations across wafers. Figure 77 shows the average power vs temperature curves for different wafers, showing extremely good uniformity from wafer to wafer.

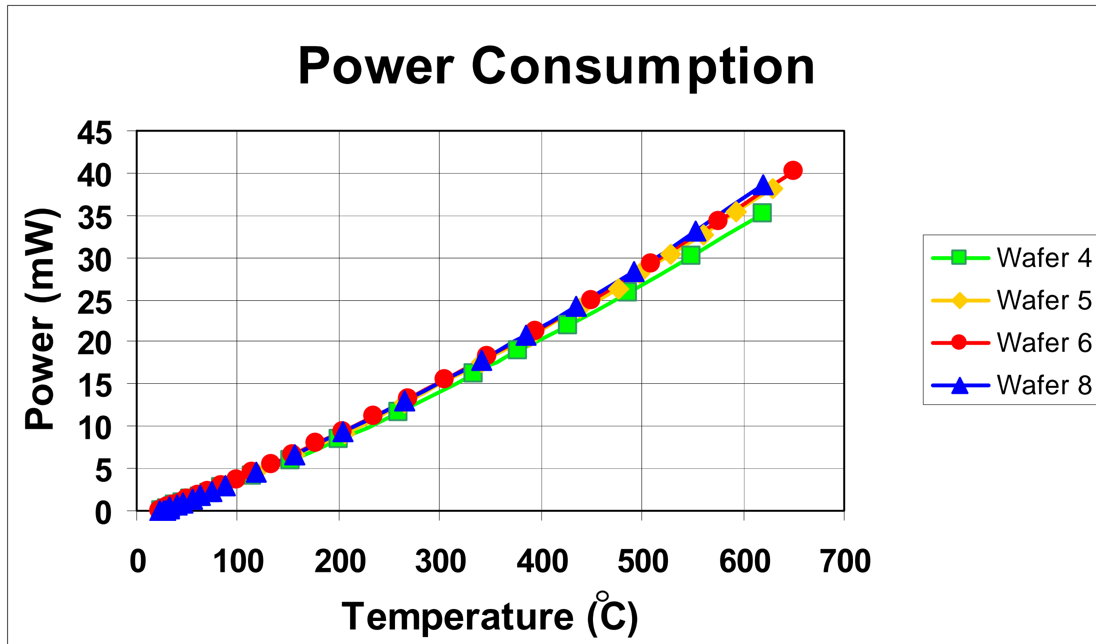


Figure 77: Typical power consumption curves for different tungsten wafers

Another striking feature is the extremely low power consumption. The large heater, for example, requires only 34 mW to obtain a temperature of 600°C, while the small heater only needs 14mW for 600°C. These are very low values, much lower than even those predicted by the simulation! Figure 78 and Figure 79 show the comparison of the simulated and measured results of the power consumption. As can be seen, the simulations predict almost double the actual power consumption.

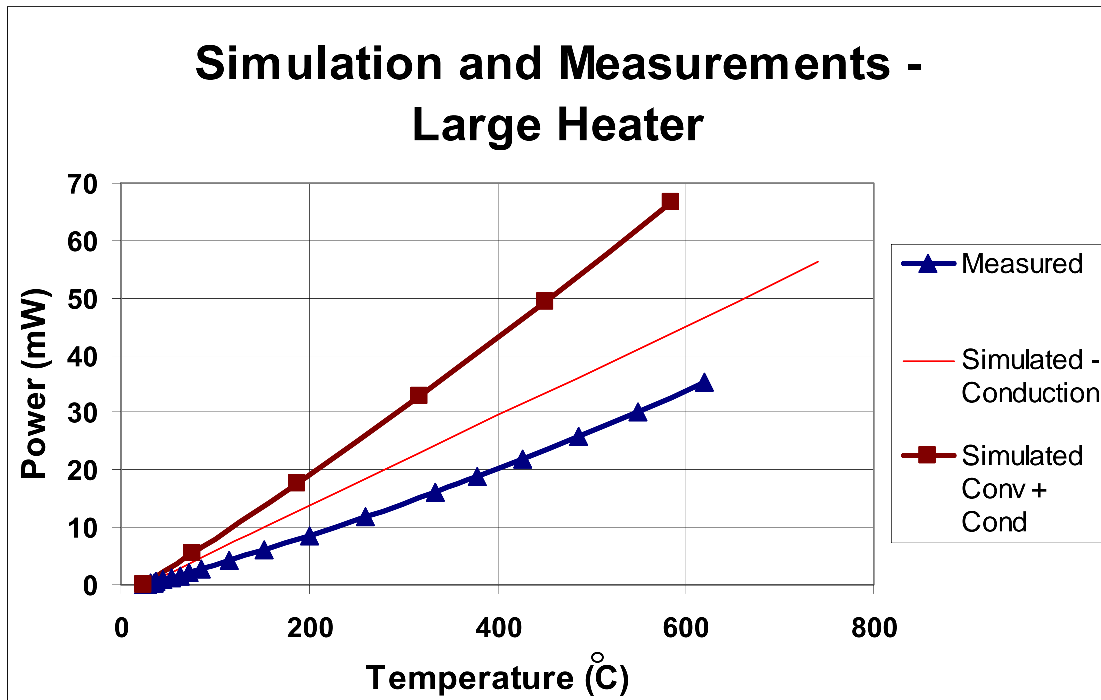


Figure 78: Comparison of simulation and Measurement for Large Heater

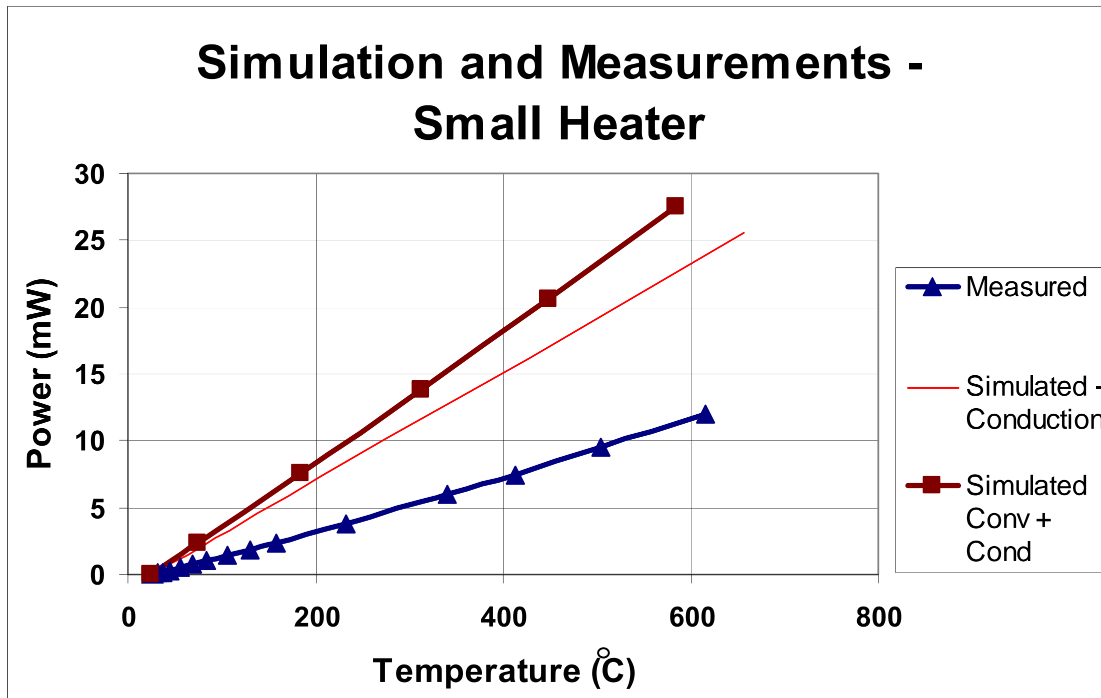


Figure 79: Comparison of Simulation and Measurement of Small Micro-Hotplates

To explain the discrepancy, different factors were looked at. The most obvious one was the thermal conductivity of the silicon nitride. The properties of silicon nitride vary greatly according to fabrication conditions. The value of thermal conductivity used in the simulations was 20 W/mK. This is similar to the values usually found in gas sensor literature[6,34]. However, this is the value for nitride deposited by LPCVD, in laboratories. In many commercial CMOS foundries, nitride is grown by PECVD (Plasma Enhanced Chemical Vapor Deposition), which has properties different to those of LPCVD nitride. Therefore, the first step was to determine, with an acceptable degree of accuracy, the thermal conductivity of the nitride used in our device.

The best way to determine the thermal conductivity of the nitride is to do measurements, with and without the nitride. All the chips have nitride passivation on them, so the passivation has to be removed to determine the difference.

For this a single chip was first characterized, for both the large, and small membranes. The nitride passivation was then etched away by Reactive Ion Etching using SF_6 for 4-5 minutes (40sccm of SF at 100mT and RF power of 100W).[4]
The membranes were then characterized again.

The comparison is shown below:

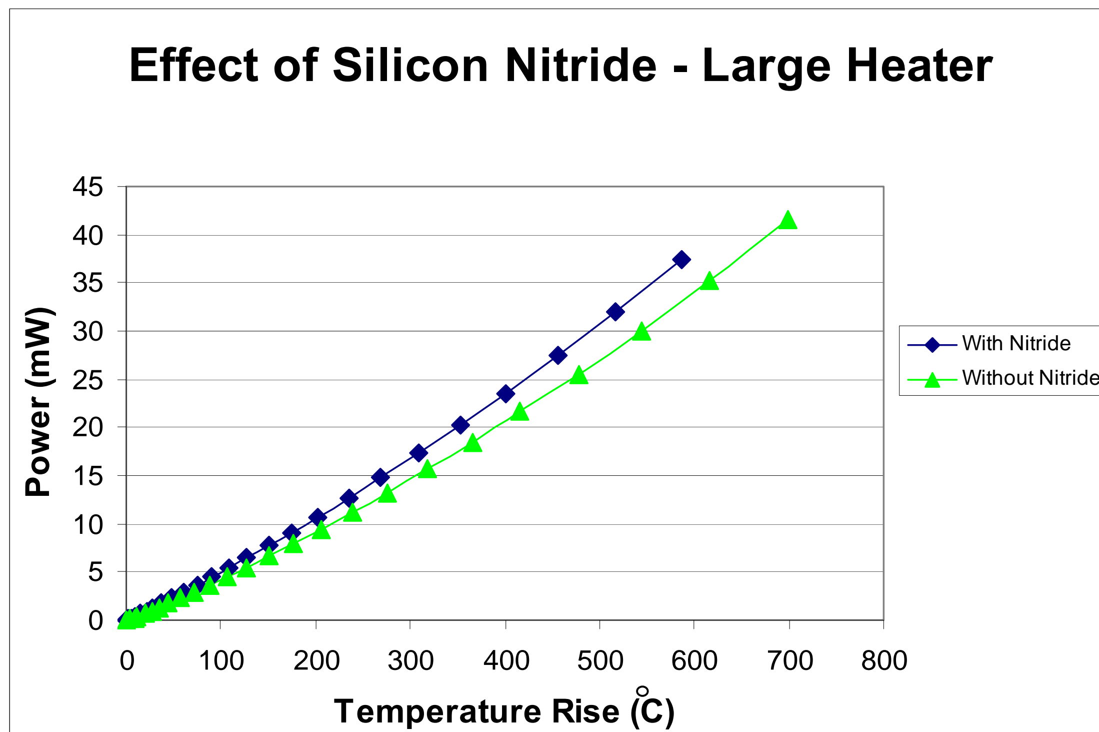


Figure 80: Power consumption of large micro-hotplate with/without silicon nitride

The curve can be used to calculate the thermal conductivity of the silicon nitride. For example, at 300°C, the difference in power required is 2mW. This means, that at 300°C, 2mW of power dissipated through the silicon nitride. Using equation (3) we can determine the thermal conductivity of the nitride:
Calculated Thermal Conductivity = 3 W $m^{-1}K^{-1}$

[4] Many thanks to Dr. Mohamed Boutchich who performed the etching of the silicon nitride

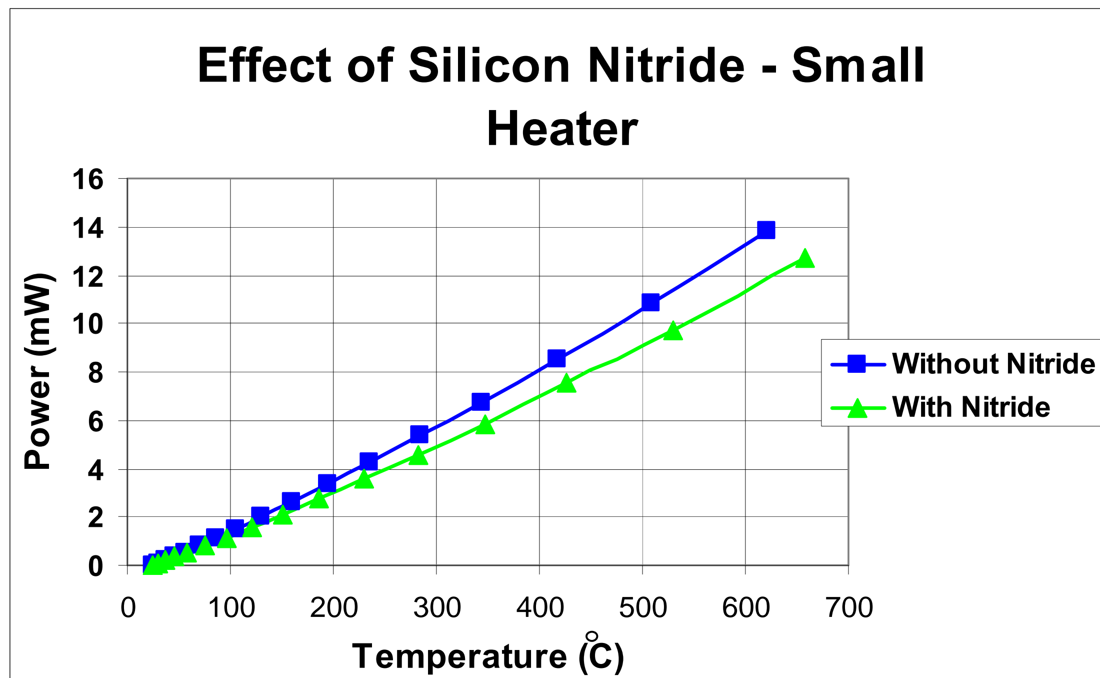


Figure 81: Power consumption of small micro-hotplate with/without silicon nitride

For the Small Heater, at 300°C, the difference in Power required is 0.8mW

Calculated Thermal Conductivity = 2.2 W $m^{-1}K^{-1}$. Table 3 tabulates the calculated values for different temperatures.

Large Heater			Small Heater		
Temperature (C)	**Power Difference (mW)**	**Calculated Thermal Conductivity (W/mK)**	**Temperature (C)**	**Power Difference (mW)**	**Calculated Thermal Conductivity (W/mK)**
125	0.75	**2.86**	125	0.275	**2.01**
225	1.4	**2.67**	225	0.575	**2.10**
325	2.1	**2.67**	325	0.9	**2.19**
425	2.85	**2.72**	425	1.2	**2.19**
525	3.75	**2.86**	525	1.55	**2.27**

Table 3: The difference in required power before and after etching the silicon nitride, along with the calculated thermal conductivity

The value calculated using the small heater is lower. This could be due to different sizes, and effects on the different designs. However, the value from the smaller membrane is expected to be a more accurate value. There are two reasons for this:

1. Convection effects are much smaller than those present in the large heater. So any interference caused by convection is greatly reduced in the small heater
2. The ratio between the heater radius, and membrane radius is much smaller for the small heater. So the heat flow is much more lateral (although any difference is quite small for both).

Just to confirm, this process was repeated with another chip – with a longer etching time (7 minutes) just to ensure that all the nitride had been etched away.

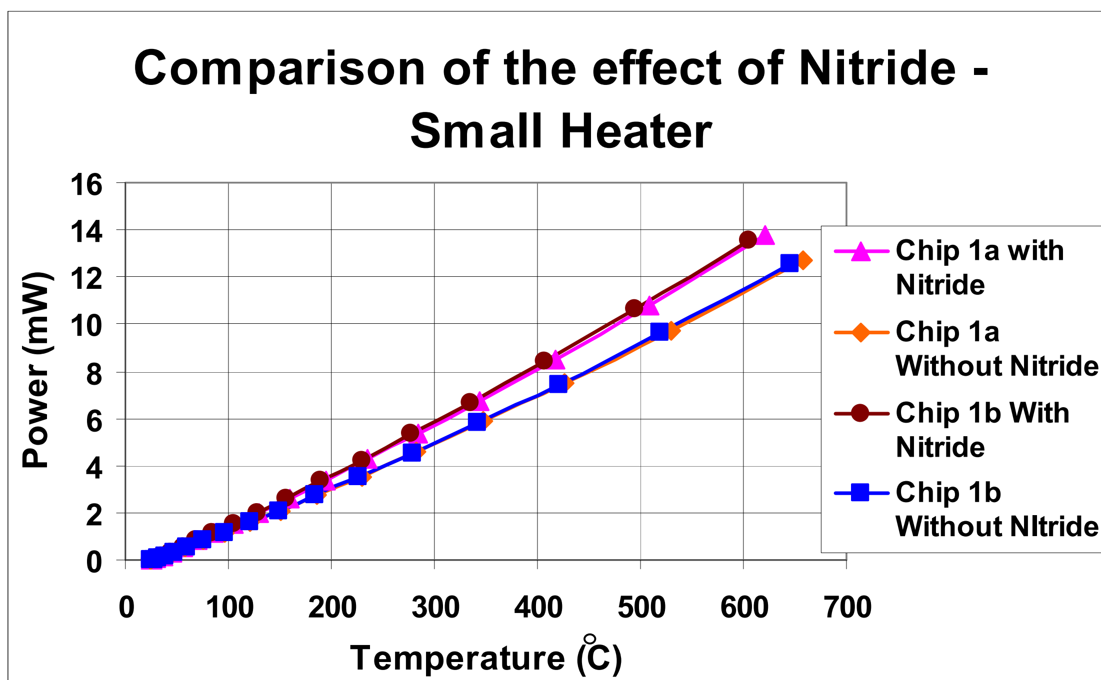


Figure 82: Power consumption before and after etching silicon nitride for 2 different chips

The graph in Figure 82 shows that the results are the same as before, which not only show that all the nitride had been etched away, but also that the values of thermal conductivity obtained are the same for both.

Thermal conductivities of some commercial nitrides have also been measured by Arx et al. [51], and report similar values. The value determined from the small heater, matches well with that given by Arx et al., and hence this value was used further in our modeling analysis.

Another material property that could cause the difference is the thermal conductivity of tungsten. Besides the rest of the membrane, the heat also escapes through the tungsten metal tracks of the heater. The thermal conductivity quoted for tungsten is its bulk value, however, properties for thin films can often be different that the bulk values.

To determine the thermal conductivity of the tungsten, measurements were done on the micro-hotplate design with tungsten beams (shown in Figure 56b). This is similar to the standard micro-hotplate, except that there are tungsten beams within the membrane. These beams provide an extra path for heat flow, so these micro-hotplates have larger power consumption. The measured difference in power consumption is the extra power dissipated through the tungsten beams. Since the dimensions of the beams are known, it is then possible to determine the thermal conductivity of tungsten.

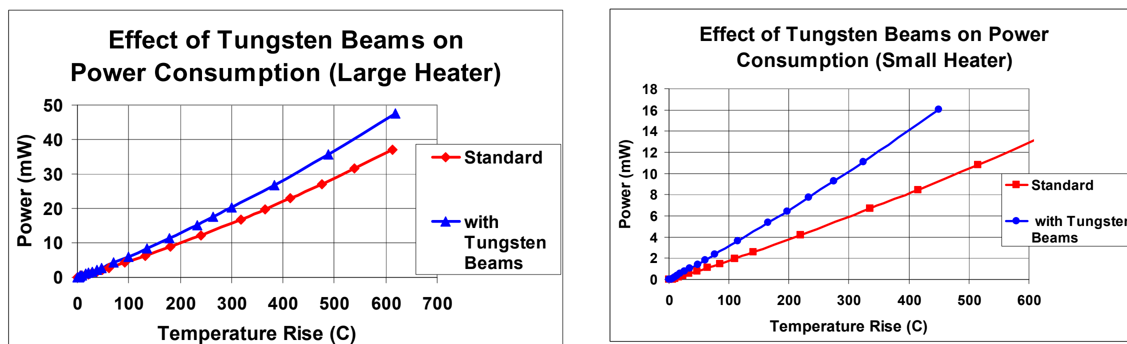


Figure 83: Graphs showing the increase in power consumption when tungsten beams are added to reinforce the membrane

Large Heater			**Small Heater**		
Temperature (^{o}C)	**Power Difference (mW)**	**Calculated Thermal Conductivity (W/mK)**	**Temperature (^{o}C)**	**Power Difference (mW)**	**Calculated Thermal Conductivity (W/mK)**
125	1.4	54	100	1.3	75
225	3	65	200	2.7	78
325	4.5	67	300	4.3	83
425	6.1	70	400	6	87
525	7.8	72			
625	9.9	77			

Table 4: The extra power need at different temperatures because of the tungsten beams. Thermal conductivity of tungsten is calculated at different temperatures.

Figure 83 shows the graphs for the micro-hotplates with and without the tungsten beams, and Table 4 shows the extra power needed at different temperatures, and the corresponding calculated thermal conductivity for both the large and small heaters. (The thermal conductivity was determined in the similar way to that used for the silicon nitride. However this time a formula for 4 rectangular blocks was used, rather than that for a circular shape). There is a significant difference in the determined thermal conductivity for the two devices, and at different temperatures. The difference at different temperatures could be due to the fact that the thermal conductivity changes with temperature. The difference for the different structures is caused by other effects such as convection or changes in the temperature distribution over the membrane because of the beams. But in all cases, the thermal conductivity is much lower than that usually given for the bulk material.

This is not a strictly accurate method of measuring the thermal conductivity of the tungsten, however it does provide an approximate value to use in the simulation of the micro-hotplates. In this case, as the thermal conductivity varies, it was decided to use an average value for the small heater (80W/mK in this case). As in the case of Silicon Nitride, the small micro-hotplate is expected to give a more accurate value of the tungsten thermal conductivity as there are fewer effects due to convection.

Using these values for the thermal conductivity of nitride and tungsten, the simulations were repeated, and are shown in Figure 84.

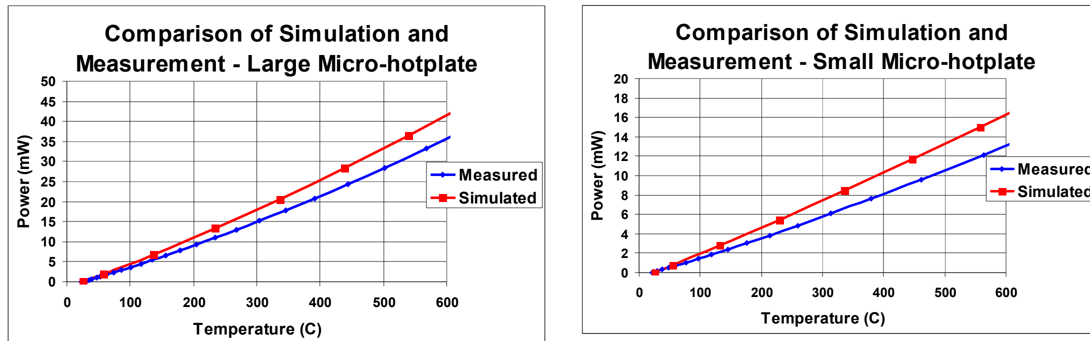


Figure 84: Comparison of Simulation and Measurements after adjusting the thermal conductivity of Silicon Nitride (at 2.2W/mK) and Tungsten (80W/mK) in the simulations

The simulations and measurements match much better now. However, there is still some difference. This can only be due to the thermal conductivity of the silicon oxide, as that is the only material that has not been checked. The thermal conductivity of the oxide used in the simulations is 1.4W/mK, but depending on the fabrication process, this can be lower [51].

It was not possible to measure the thermal conductivity of the silicon oxide from the available structures, as unlike the nitride case, the silicon oxide cannot be removed (as the heater is embedded within it). However, since it is the only large source of error left in the simulation, the thermal conductivity can be determined by comparing the simulations and the measurement results. To do this, the difference in power consumption at a certain temperature (for example 600°C) is determined for the large heater in the graph in Figure 84 (which is 5.6mW at 600°C). This is the extra power that the simulation predicts and is directly proportional to the 'extra' thermal conductivity that has been used for the oxide.

So using equation 3 with the thickness of the oxide, this 'extra' thermal conductivity can be determined, which comes to 0.55W/mK. So for an accurate simulation to match the measurements, the thermal conductivity of the oxide has to be reduced by 0.55W/mK, leading to a value of 0.85W/mK. The simulations were then repeated with this new value, and the graphs are shown in Figure 85. The simulations, as they now should, match almost perfectly with the measurements.

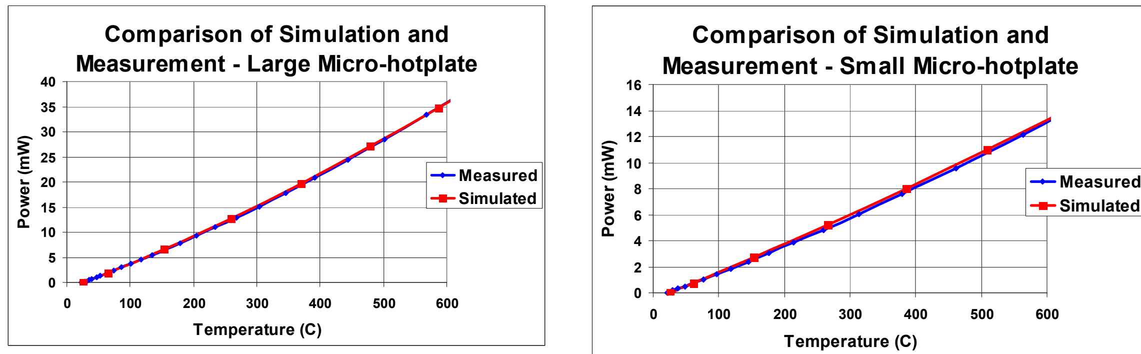


Figure 85: Comparison of measurement and simulation results after changing the values of thermal conductivity of silicon nitride, tungsten and silicon dioxide in the simulations

Transient Time

The time required for the micro-hotplates to heat up was also measured. This was done by applying a pulsed voltage source across the heater, and measuring the forward voltage drop on the temperature sensing diodes. The temperature-time curves for various temperatures are shown in Figure 86.

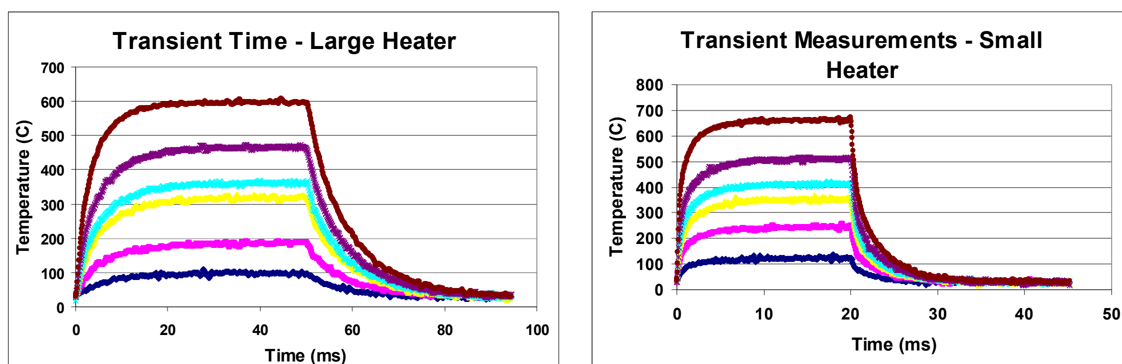


Figure 86: Transient measurement of the Micro-hotplates

The measurements show that the micro-hotplates have extremely fast transient times. The large heater has a 10-90% rise time of 10ms for 600°C, and fall time of 20ms. The small heater has a 10-90% rise time of only 2ms, and a fall time of only 6ms.

The cool down time is larger than the rise time for both cases. The reason is that during cooling, the cooling path is much longer for the heat to travel. During rise time, a

large portion of the heat stays within the heater region, or close to it, so it does not travel far from the heater. However, for cool down, the heat has to travel all across the membrane and down the substrate. This is a much longer path, with a lot more thermal resistance, and therefore takes longer to reach the steady-state.

Transient simulations were also carried out, and the results are also shown in Figure 87. The simulations were done for both the rise time, as well as the cool down time, and show an excellent match with the measurements. Because the thermal conductivities have been properly extracted during the static simulations, the transient simulations matched correctly.

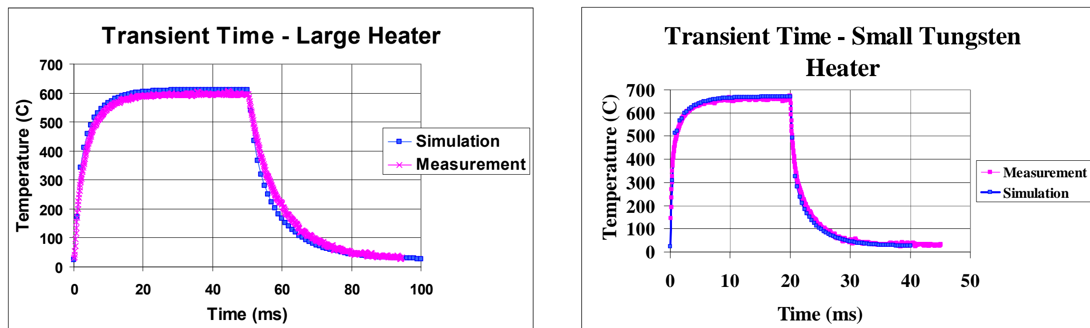


Figure 87: Comparison of transient simulations and measurements

Transient SPICE Model:

An analytical transient SPICE model was also developed to gain a better understanding of the transient aspects.

Micro-hotplates require a finite time to reach the steady state temperature. This time is required because the membrane needs to absorb heat energy to reach a high temperature. To model this behavior, the concept of thermal capacitances can be used, analogous to the way that electrical capacitances behave.

An electrical capacitor stores charge; the amount of charge stored is equal to:

$$Q=CV \qquad (14)$$

where Q is the charge stored, C is the electrical capacitance, and V is the potential difference across the capacitor.

Now consider a body of mass m, the temperature of which is raised from T_0 to T_1. The amount of extra heat energy stored within the mass is given by:

$$h=mc(T_1-T_0)$$

or:

$$h=\rho V_{OL}c(T_1-T_0) \quad (15)$$

where h is the heat absorbed, m is the mass, c is the specific heat capacity, ρ is the density and V_{OL} is the volume. Compare this equation with equation (6): (T_1-T_0) acts as a thermal 'voltage', while Q and h standing for charge absorbed and heat absorbed respectively are analogous to each other. Therefore, the thermal capacitance, C_{Th} can be given by [41]:

$$C_{Th}=\rho Vc \quad (16)$$

In electrical circuits, the transient time for a simple RC network is dependent upon the constant RC. The 10%-90% transition time is given by 2.2RC. However, such a simple method does not work in the case of micro-hotplates, as we cannot simply calculate the total thermal capacitance of the membrane and use the above formula. There are two reasons for this:

1. The 2.2RC formula is for a constant power supply, which is not the case for the micro-hotplate. As the membrane heats up, the resistance of the heater increases. If a voltage is applied in a square pulse to the heater, then initially the resistance will be low so the power supplied will be higher (as given by $P=V^2/R$), but as the resistance increases, the power supplied decreases. Therefore, an accurate model should take into account the varying power supply.
2. If the total thermal capacitance of the membrane is used, then we are lumping the whole membrane as one capacitor. When the capacitor charges, it effectively equates to the whole membrane rising to the same temperature. In actual fact this is not the case, as the centre of the membrane is at the highest temperature, and the temperature in the rest of the membrane reduces outwardly.

Therefore, system need to be modeled as a network of thermal resistors and capacitors as shown in Figure 88. The membrane can be split into several concentric rings, and the thermal resistance and capacitance of each ring can be determined and inserted into the network, with C_1 being the capacitance of the circular region in the centre of the membrane, and R_n and C_n being the values for the outermost ring. In steady state, C_1 would be at the highest voltage (being equivalent of the highest temperature), and the voltage would be lower across the other capacitors. In addition, the current source is a voltage controlled current source. This models the fact the power supplied by the heater depends upon its temperature.

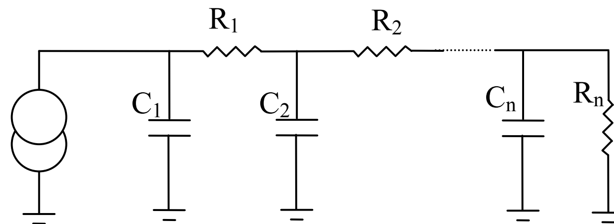


Figure 88: RC network to model the thermal transient time

Besides the membrane, heat loss also occurs through the air, and the air gets heated also, therefore, the thermal resistance and capacitance of the air also needs to be modeled. Since the heat flow through the air is relatively complicated, a simplified model is needed. Consider the heat distribution in air as shown by simulations in Figure 19. Most of the heat is distributed in a spherical region around the membrane. This suggests a simple approximation, where we assume the flow of heat through air is from a sphere of radius r1 to a concentric sphere of radius r2. (where r1 is the heater radius, and r2 is the membrane radius). This allows us to determine the thermal capacitance and resistance of spherical shells of air, which are added in parallel to the network shown in Figure 88 to come with a complete model.

The thermal capacitance of a spherical shell is simply the volume of the shell multiplied by the density and thermal heat capacity:

$$C_{th}=c\rho\,(4/3)\,\pi\,(r_2^3-r_1^3)$$

Where c is the thermal heat capacity of air, ρ is the density, and r_1 and r_2 are the inner and outer radii of the spherical shell.

For the thermal resistance, of a shell, first consider the thermal resistance of a shell of infinitesimal thickness, and radius r. The thermal resistance of this shell would be:

$$dR_{th} = \frac{dr}{\alpha 4\pi r^2}$$

where α is the thermal conductivity of the air. This integrates to:

$$R_{th} = \frac{1}{4\pi\alpha}\left(\frac{1}{r_1} - \frac{1}{r_2}\right)$$

Using these equations, the thermal resistance and capacitance of spherical shells of air above and below the membrane can be modeled, and added in parallel to the circuit blocks shown in Figure 88.

The accuracy of the model depends on how many nodes are used in the circuit model (the number of nodes depends on the number of parts the membrane has been divided into). The larger the number of nodes, the higher the accuracy. The model was analysed in PSPICE with various number of nodes and the results are shown in Figure 89 compared to the measurement of the large and small micro-hotplates. For just one node (a lumped model), the predicted time is (very) inaccurate. However, the accuracy greatly improves if the number of nodes is increased, with 20 nodes giving a sufficiently good approximation. It is also worth noting that the model works equally well for both the large and small micro-hotplates, proving that the model is fully scalable. This is because the model is physics based and does not rely on any empirical parameters.

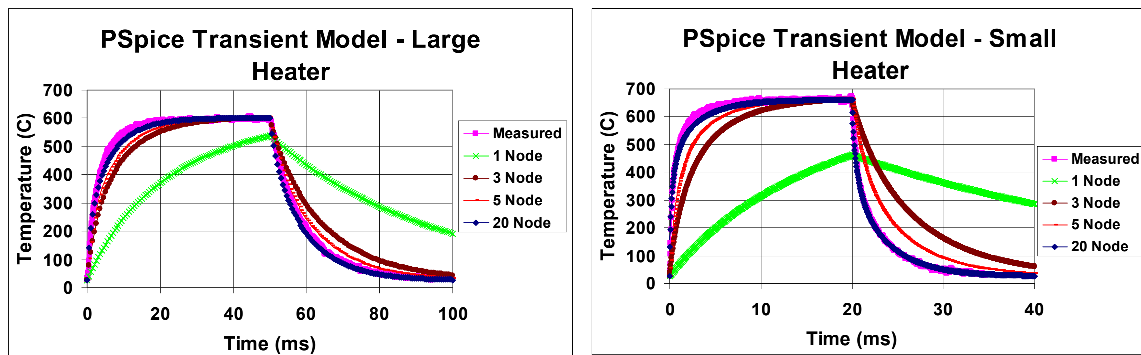


Figure 89: Results of the transient SPICE model compared to measurements

Effect of Membrane Types

Some of the designed membranes were reinforced with tungsten or silicon. While these are expected to make the membranes more mechanically stable, they do result in larger heat losses. These micro-hotplates were also characterized for comparison, and the results are shown in Figure 90, showing higher power consumption.

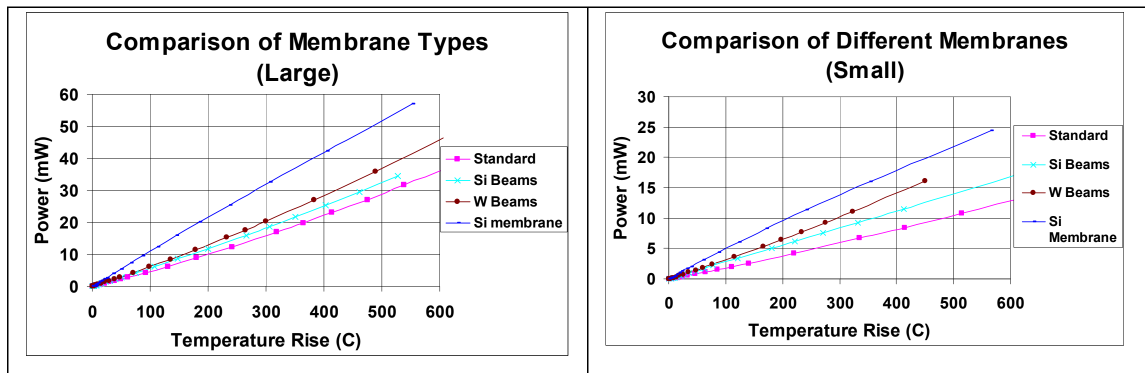


Figure 90: Effect of different membrane types on power consumption

There are two things to be noted:

Firstly the curve for a complete silicon membrane has a shape different to that of the other curves. The reason for this is that at high temperatures the thermal conductivity of silicon decreases significantly [40], therefore the amount of extra power needed is less. In the other curves, the main effect is that the thermal conductivity of air increases as the temperature increases, so the extra power needed is more for higher temperature. This causes the shapes of the curves to be different.

Secondly, the amount of power needed for the silicon membrane is only twice of that needed by the standard device. The thermal conductivity of silicon is about 100 times greater than that of silicon oxide at room temperature. Therefore the power consumption in the silicon membrane was expected to be a lot more than measured. Figure 91 shows the results predicted by simulations. The simulations predict much higher power consumption than those measured. The obvious reason for the discrepancy was the value of the thermal conductivity of silicon used in the simulations, as that was the only extra parameter to the set used in the previous simulations.

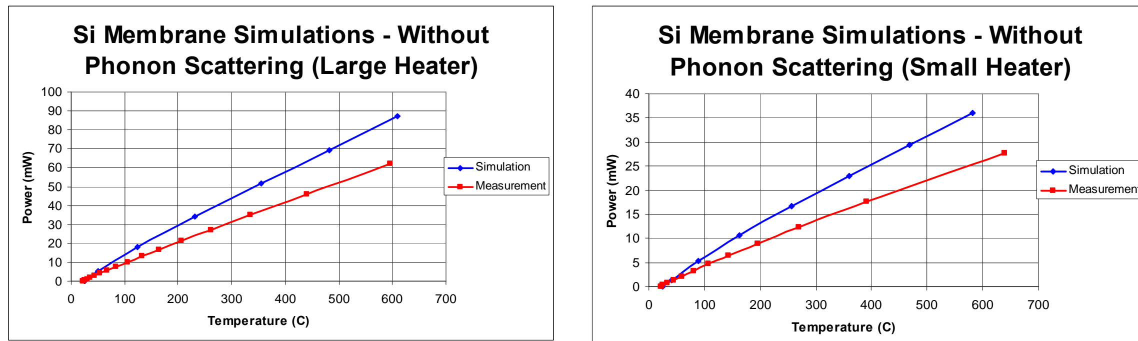


Figure 91: Simulations of Micro-hotplates with Silicon Membranes compared to measurements

The thermal conductivity of silicon was very carefully measured at various temperatures and reported by GlassBrenner and Slack in 1964 [40]. And this was the value used in the simulations.

However, the silicon layer in this case is only 0.25μm thick, while the values reported by GlassBrenner and Slack were for bulk silicon. At such a small thickness, phonon boundary scattering effect become important, and result in a much lower thermal conductivity of silicon [52].

Phonons are the quantized particle like entities equivalent of lattice waves (just as photons are the particle equivalent of electromagnetic waves) [53]. Phonons are the principle cause of heat conduction in insulators and semiconductors (conductors such as metals also have free electrons for heat conduction). For very thin layers, the thickness of the layer becomes close to the mean free path of the phonons. For example, the mean free path in silicon is 430nm, compared to the SOI thickness of 250nm. This causes scattering effects at the boundaries to be much more prominent, and result in an overall thermal conductivity which is significantly less than the bulk value.

Calculations were done to determine the effect of phonon boundary scattering on thermal conductivity.

A formula for the reduced thermal conductivity in thin Silicon due to phonon boundary scattering is given in [54]:

$$k_{\text{film}} = \frac{(1/3)Cv}{(1/3)Cv/k_{\text{bulk}} + 3/(8d)},$$

Where:

$$\frac{1}{3}Cv = 1.13 \times 10^{13} \frac{\exp(195/T)}{T^2(\exp(195/T) - 1)^2}$$

T – Absolute Temperature

d – Thickness of Silicon

C – Heat Capacity of phonons

v – Velocity of Phonons

k_{bulk} – The bulk thermal Conductivity

k_{film} – The conductivity of the thin Silicon in W/mK

Simple algebraic manipulation reduces the formula to:

$$k_{film} = \frac{1}{\frac{1}{k_{bulk}} + \frac{9}{8dCv}}$$

Since from [40]:

$$k_{bulk} = \frac{1}{a + bT + cT^2}$$

where:

a=0.03 cm K/W

b=1.56 x 10^{-3} cm/W

c=1.65 x 10^{-6} cm/ KW

Therefore:

$$k_{film} = \frac{1}{a + bT + cT^2 + \frac{9}{8dCv}} * 100$$

This formula can be used to determine the thermal conductivity of the thin silicon at different temperatures (Tabulated in Appendix B). These values were then used in simulation of the micro-hotplates.

Simulation results with this value are shown in Figure 92, showing a much better match. There is still a little difference. This is most probably because the formula used is an approximation (within 15%) and possibly gives a slightly higher value than the actual value of the thermal conductivity.

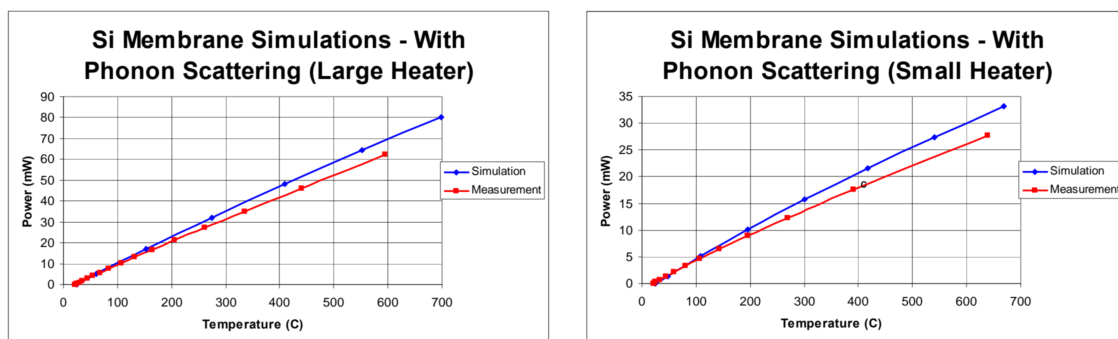


Figure 92: Simulations of silicon Micro-hotplates after phonon scattering effects have been taken into account

Aluminum:

Chips with Aluminum heaters were also characterized. The results are shown in *Figure 93*, *Figure 94*. The power consumption is slightly larger than that of the tungsten micro-hotplates. This is because the aluminium tracks used in the fabrication process are twice as thick as tungsten, and because the thermal conductivity of aluminium is larger than that of tungsten (the bulk value is 240W/mK, compared to 177W/mK for tungsten). This means that a lot more power is dissipated through the heater tracks, leading to higher power consumption.

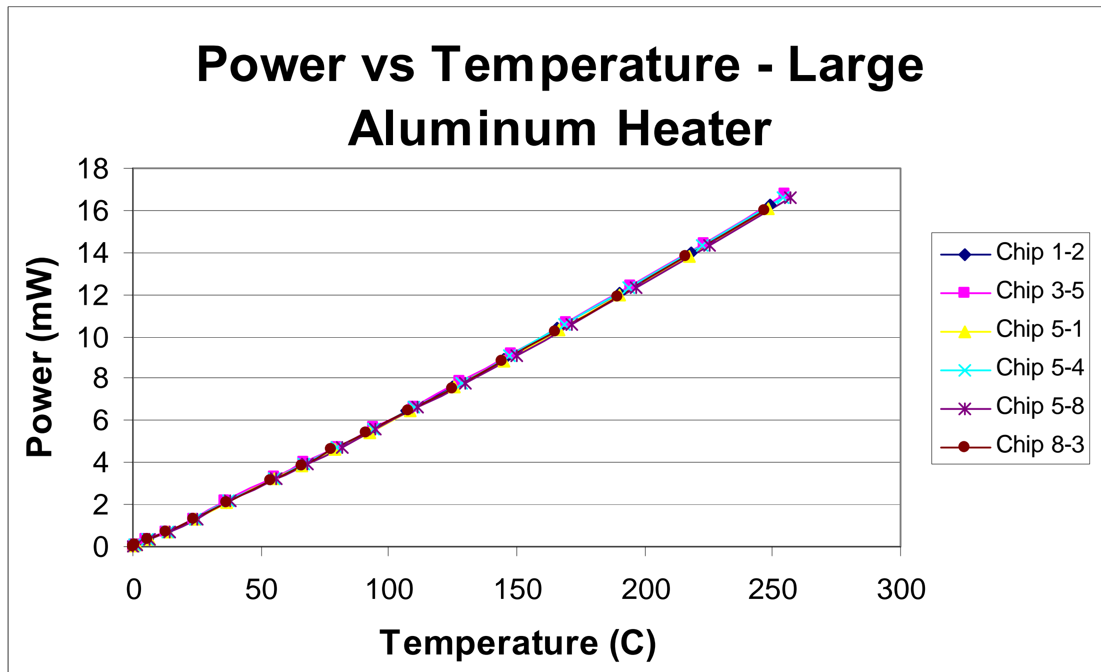


Figure 93: Power/Temperature curve for large aluminium heater

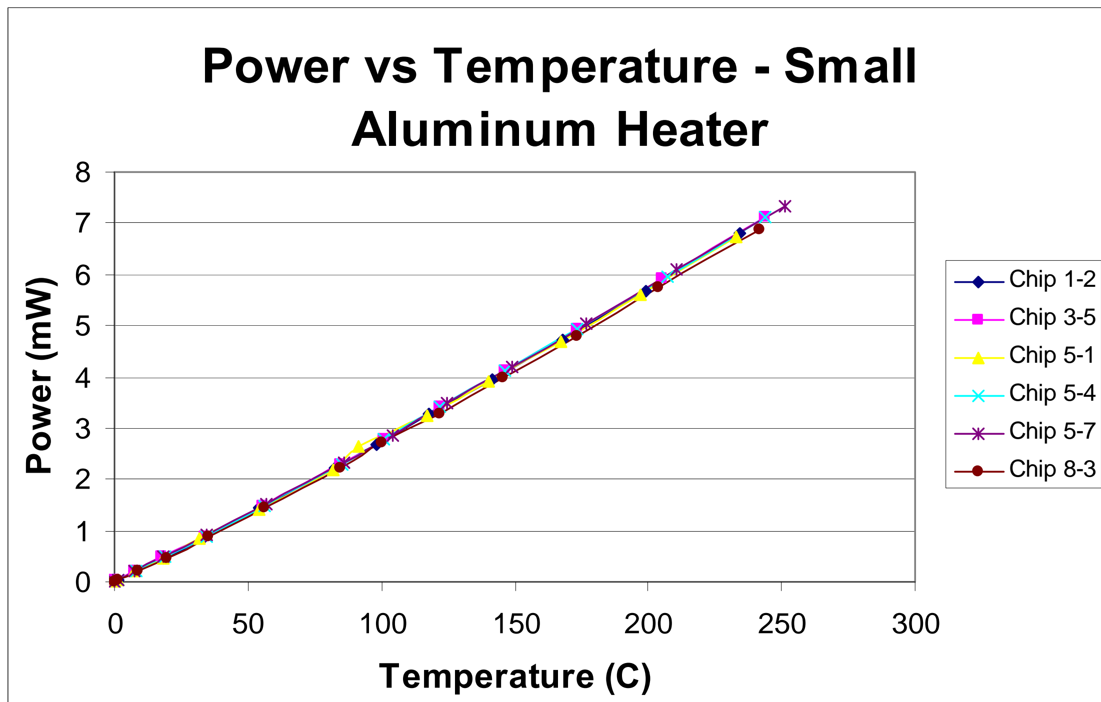


Figure 94: Power/Temperature curve for the small aluminium heater

Different Temperature Sensors:

Since there were different designs with tungsten, diode and silicon temperature sensors, the sensors were compared to each other. Figure 95 shows the power vs temperature curves measured by the three different sensors, for the large and small membranes.

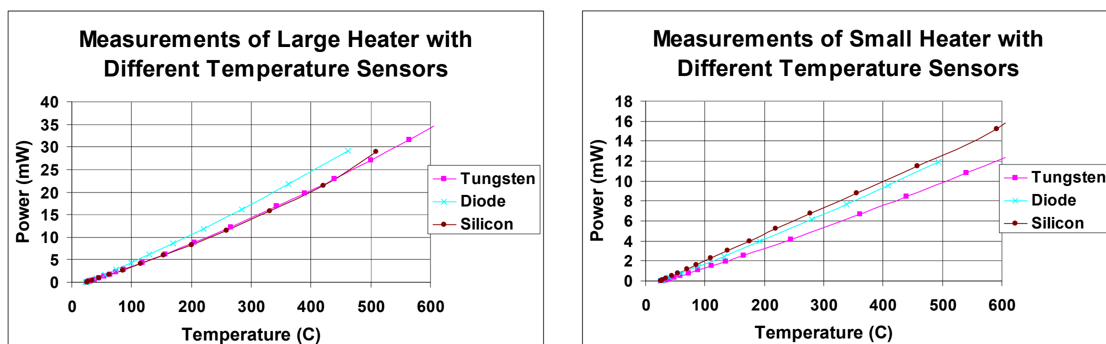


Figure 95: Power/Temperature Curves for different temperature sensors

In the large heater, the silicon and tungsten temperature sensors give similar results. However, for diode it is different. This is because the diode size is greater than the heater area, and as it has a greater thermal conductivity, it increases the power consumption of the micro-hotplate, giving a different result. For the small heater, the same argument applies for the diode difference. The difference in the silicon temperature sensor is because the resistance of the sensor is small compared to the resistance of the tracks, which does not allow the temperature to be measured very accurately. This design needs to be improved greatly, either by using a 4-probe measurement, or by having a higher resistance for the temperature sensor.

Heater Sizes:

Because heaters of different sizes were fabricated, the power losses of different heater sizes were also measured, and typical curves are shown in Figure 96. The larger the heater size, the greater the power consumption. For the small membrane, the effect of the heater size seems to be much smaller than for the large membrane. This can be explained by the ratios of the membrane and heater radii. From equation 3, the conduction power loss depends on ln(r2/r1) , where r2 is the membrane radius, and r1 is the heater radius.

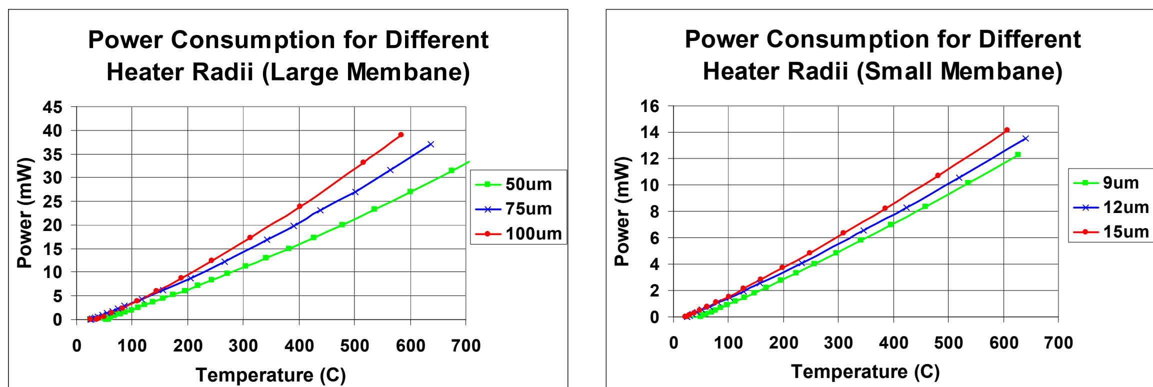


Figure 96: Effect of heater size on power consumption

For the large heater, the values of ln(282/50), ln(282/75), ln(282/100) are 1.73,1.32, 1.04. For the small heater the values of ln(150/9), ln(150/12), ln(150/15) are 2.81, 2.52, 2.30. So for the large heater, the percentage increase from 50µm to 100µm is 100x(1.73-1.04)/1.04=66% (the measured increase is a bit less as the effect of convection and loss due to tracks has not been taken into account). For the small heaters, the percentage increase from 9µm to 15µm is 100x(2.81-2.3)/2.3=22%. This increase is much lower compared to the large heater, and explains why the effect of the heater size is greater for the large micro-hotplate.

Mechanical Characterization

Membranes are fragile structures, and therefore need to be analysed for stresses. If stresses are too high the membrane can break.

Membrane surface profiling:

The surface profiles of the micro-hotplates were measured using an optical profilometer (Fogale Nanotech Zoomsurf 3D). The profiles of the large and small membranes are shown in Figure 97, Figure 98 (The deflection in the pictures is greatly magnified to show the deflection more clearly). These measurements were taken at room temperature, without supplying any power to the heater.

There is very little deflection in the membranes. The large membrane deflects upwards by only 8µm (2% of the membrane diameter), while the small membrane deflects upwards by only 2.5 µm (1% of membrane diameter). These deflection are extremely small, and show that the membranes have extremely small residual stresses.

The slight deflections are caused by the residual stresses in the membrane layers. There are two types of residual stresses: intrinsic stresses due to the growth mechanism, and thermal stresses, due to the thermal mismatch between different material layers [55]. The membrane materials (Silicon dioxide and Silicon Nitride) have a lower thermal coefficient of expansion (TCE) compared to the substrate (silicon). Since the materials are deposited at high temperatures, on cooling, the silicon contracts more than the oxide or nitride, which causes the membrane to deflect.

The deflection direction for membranes tends to be upwards, as is the case for the small heater. However, there is also the bimetallic effect between oxide and nitride, which tends to deflect the membrane downwards, plus any intrinsic stresses. This effect is greater in the large heater, as the membrane is larger, and causes the larger membrane to deflect downwards.

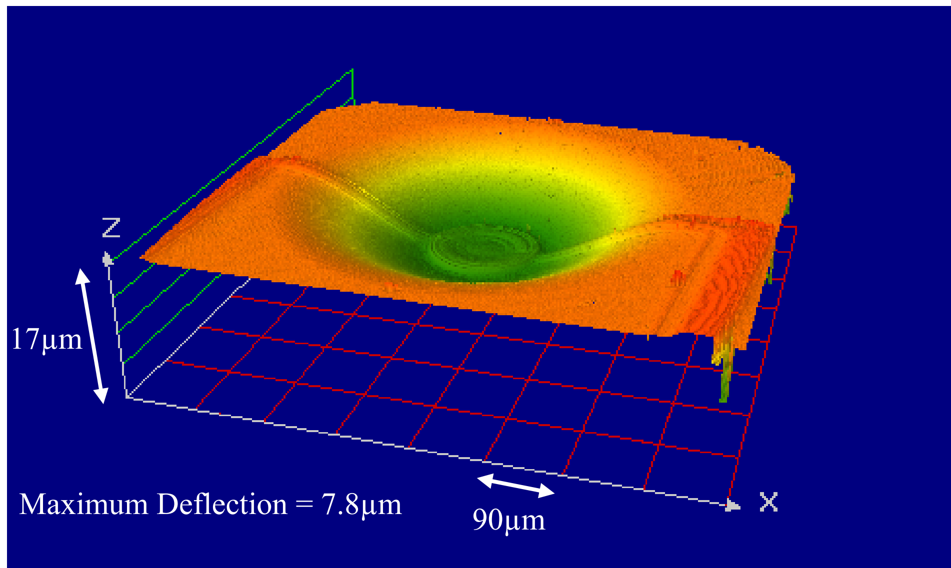


Figure 97: Surface profile of the large heater

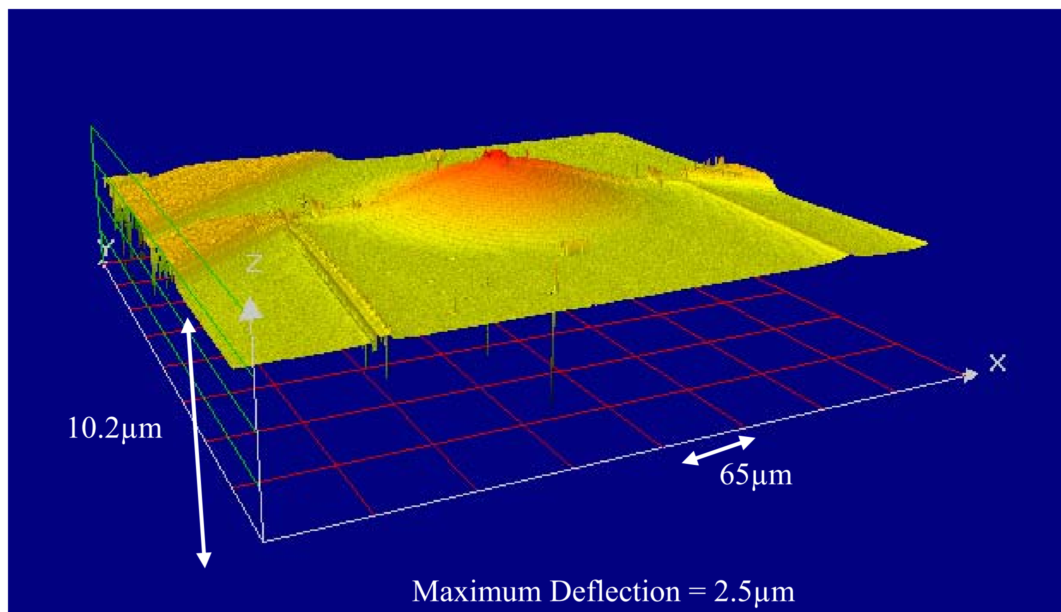


Figure 98: Surface profile of the small heater

As shown earlier, a few micro-hotplates were fabricated with membranes reinforced with silicon or tungsten, to improve the mechanical stability. Their profiles were also measured to determine if there was any improvement. Figure 99 shows the profiles for various reinforced membranes.

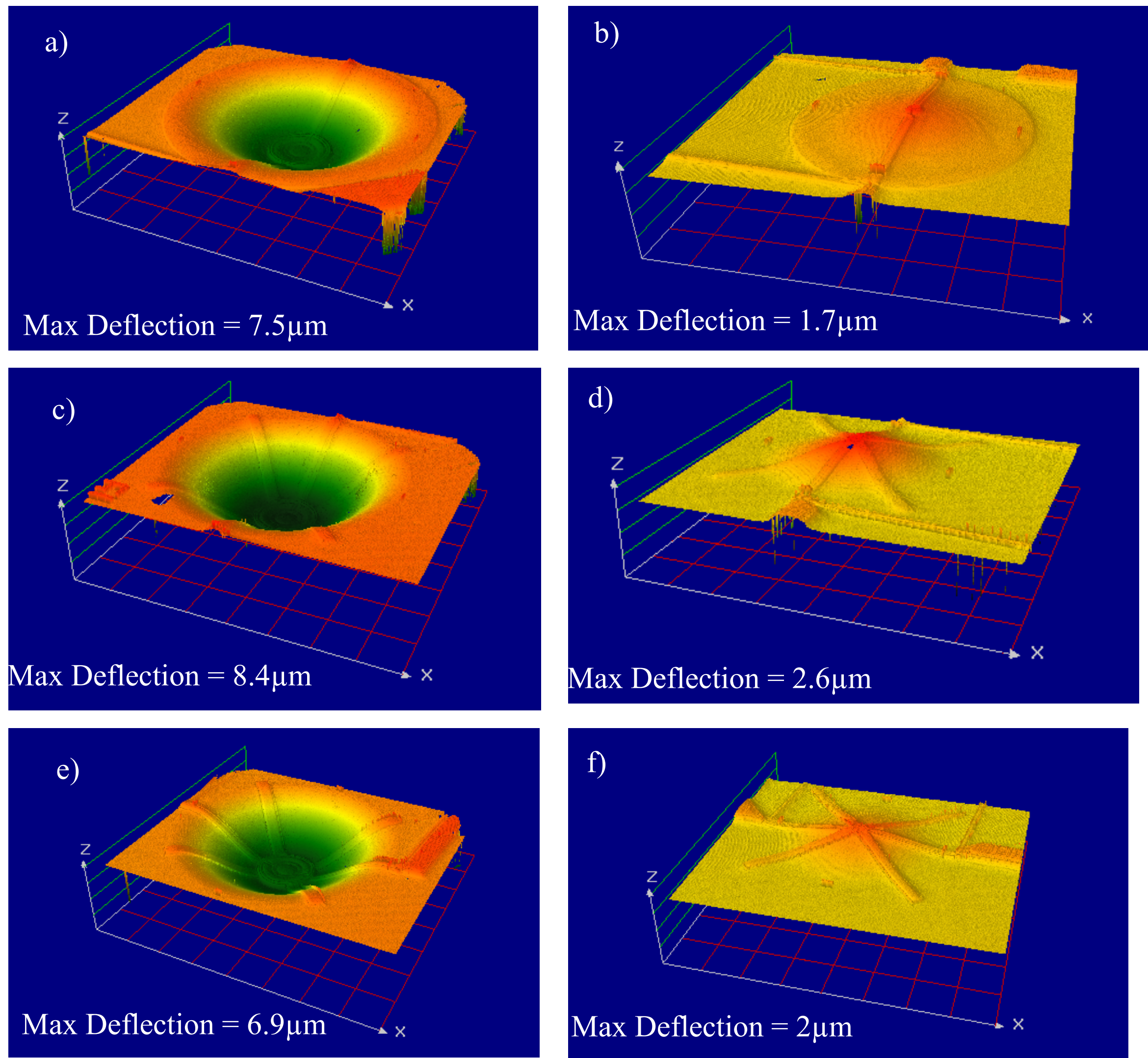


Figure 99: Profiles for reinforced Membranes, (a) Large heater on Si Membrane, (b) Small Heater on Si membrane, (c) Large membrane with Si beams, (d) small membrane with Si Beams, (e) Large membrane with tungsten beams, (f) Small membrane with tungsten beams

As the figures show, there is a little improvement in the deflection. But because the deflection is already so small, it is difficult to determine any noticeable improvement. Tungsten seems to have a slightly better effect, which is expected since it has a much higher Young's modulus than silicon. However, in all cases, the large membranes deflect downwards, while the small membranes deflect upwards.

Effect of heating the membrane.

During operation, the micro-hotplates get hot, and the high temperatures can induce additional stresses in the membrane due to the different thermal expansions of different materials. To investigate this, the small membrane was heated up to 400°C using its micro-heater, and the profile measured. The results are shown in Figure 100. As can be seen, heating to a high temperature does not significantly increase the deflection. The deflection due to internal stresses is much more, than any additional stress caused by the high temperatures of the micro-hotplate. This shows that the micro-hotplates can operate reliably at high temperatures.

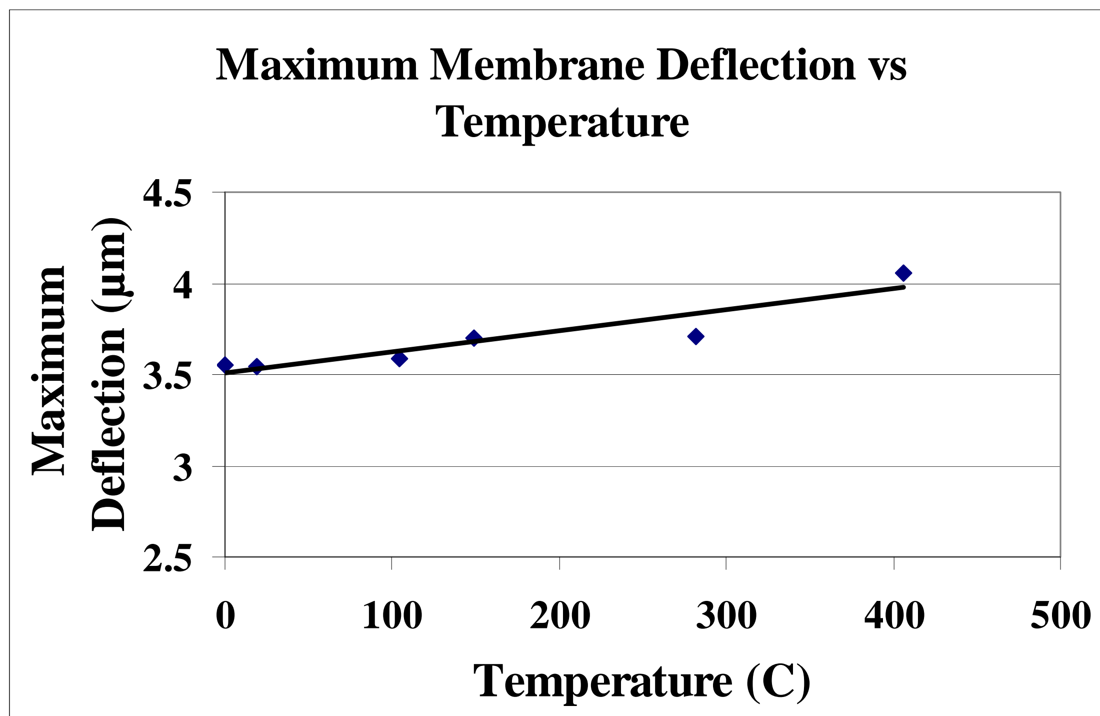


Figure 100: Deflection for a heated membrane

Long Term Reliability:

Long term reliability of devices is a very critical issue, as in the real world, the devices have to keep working continuously for long periods of time.

The reliability of the tungsten micro-hotplates was measured by maintaining them at high temperatures for 500 hours [5]. A constant current was applied to the heater to heat it to 350°C. At suitable intervals, the current was turned off, and the resistance was measured at room temperature. The current was then switched on again. This was done, until the micro-hotplate had been at 350°C for a total of 500 hours (not including the time taken for resistance measurement). This was then repeated for another device of the same design, for a temperature of 500°C. The measurements were then repeated by first annealing a device for 1 hour before the reliability measurements.

The results of the measurements are shown in Figure 101, Figure 102. At 350°C, the tungsten micro-hotplates are extremely stable, with very little drift even after operation for 500 hours. At a temperature of 500°C, there is some drift, and after 500 hours, the resistance increases by about 3.5%. However, this can be greatly reduced by annealing at 600°C for 1 hour, which reduced the drift to less than 1% over a 500 hour period.

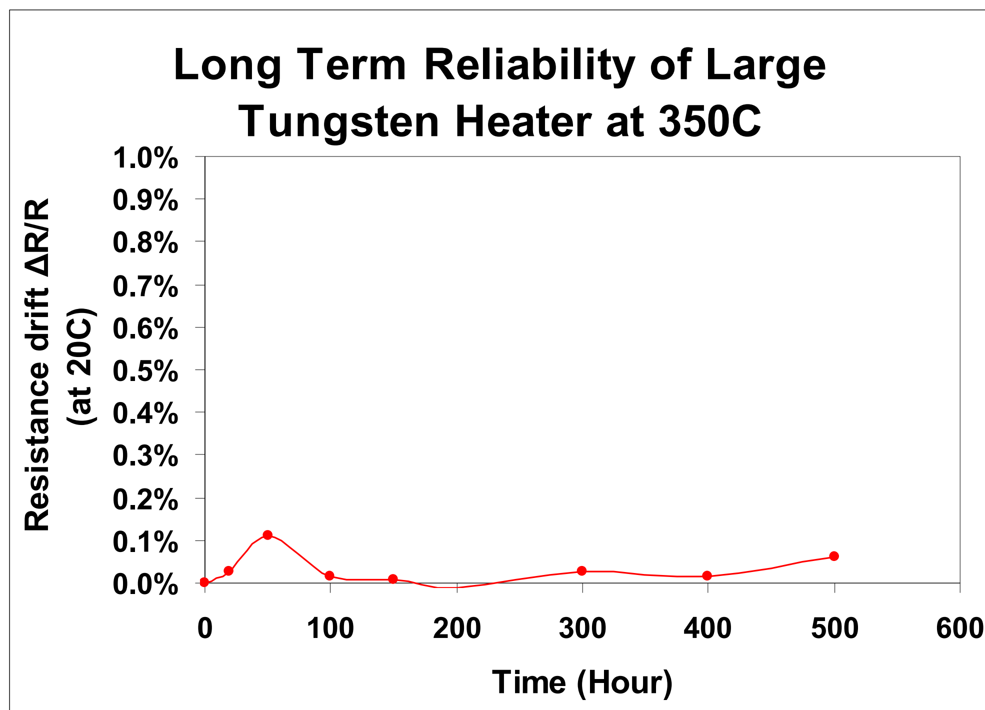


Figure 101: Measurement of long term resistance drift when the large tungsten heater is operated for 500 hours

[5] Many thanks to Mr Takao Iwaki from the University of Warwick who carried out all the long term reliability measurements of the tungsten micro-hotplates

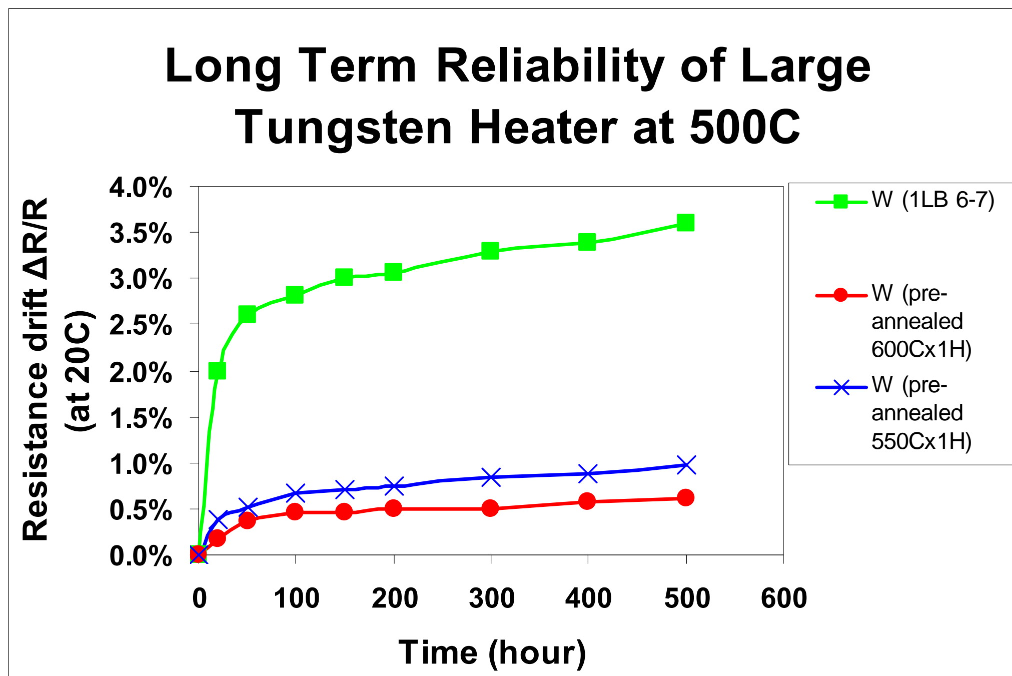


Figure 102: Measurement of long term resistance drift of large tungsten heater at 500°C with and without pre annealing

Conclusions

Tungsten based micro-hotplates were designed, fabricated and measured. Besides temperature uniformity, heater design also took into account the operating voltage so as to be suitable with CMOS circuitry, and current density to improve the device reliability. The devices were fabricated by a SOI CMOS process followed by DRIE. The devices were calibrated on unetched wafers using a hot chuck. Etched wafers have greater bowing at high temperature (above 150°C) and so are difficult to measure. Also the heaters had significant track resistance. This was determined as both 2-probe and 4-probe measurement methods were used. 4-probe measurement can significantly improve the accuracy of the measurements, and should be used wherever possible. Additionally the track resistance can become significant, so during design the tracks should be made as wide as possible to reduce the power losses due to heat generation in the tracks.

The measured micro-hotplates showed very good characteristics, with low power consumption (14mW at 600°C), fast transient times (2ms for 600°C) and good stability (were operated at high temperature for upto 500hours).

The simulations were then compared to the measurements, and there was a significant difference due to the values of thermal conductivity used in the simulations. The thermal conductivity of the materials depends greatly on the process used for fabrication. Therefore it is important to create test structure in batches to determine the properties of the different material layers. It was also found that for thin silicon, the thermal conductivity is much more reduced compared to bulk silicon because of phonon boundary scattering effects. This suggests that thin silicon can be used within the membrane to strengthen it, which otherwise would result in large power consumption as silicon has a very high thermal conductivity. Surface profile measurements were also performed, showing that the large membranes tended to deflect downwards, while the small membranes deflected upwards.

Chapter 5

Conclusions and Further Work

Conclusions

An elecro-thermo-mechanical analysis was carried out for two different devices: micro-hotplates for gas sensors, and membrane power devices. The common factor between these classes of devices is that both are based on membranes, have been fabricated using similar commercial SOI-CMOS processes, and both are suitable for integration with electronic circuitry to form a smart chip. A crucial difference is that in micro-hotplates, the aim is to reach a high temperature for low input power, while in membrane power devices high temperatures are to be avoided as they adversely affect device performance and reliability. Therefore while micro-hotplate membranes are designed with a circular shape to retain as much heat as possible, membranes for power devices are designed with a long rectangular shape to dissipate the heat quickly.

Novel tungsten based SOI micro-hotplates were presented, and extensive thermal analysis in the form of simulations and mathematical analysis were performed. It was shown that the main source of heat loss were conduction through the solid, and the losses to air both above and below the membrane. The conduction through the membrane increases as the heater radius to membrane radius ratio increase. Therefore the membrane radius should be as large as possible, while the heater radius should be as small as possible for low power consumption. However, this has to be balanced with the need for sensitivity and cost requirements of the given application.

The heat losses in air were shown to be primarily in the form of conduction, with air flow having very little effect. Also the losses below the membrane were as significant as

the losses above the membrane. Also, for the losses below the membrane, it was shown that the etching type (KOH or DRIE) did not have any significant effect. Additionally, for the first time, a systematic method to design heaters for good temperature uniformity was presented, and this was backed by extensive numerical simulations. It was shown that a ring heater gives perfect temperature uniformity in a vacuum, while in air, an inner heating element is also required to balance the power loss from within the heater region.

The devices were then fabricated, and the measurements have been presented. The tracks were found to have significant resistance, but the use of 4-probe measurement method gives good accuracy in temperature and power consumption measurements. The heaters have extremely low power consumption: 14mW at 600°C for the small micro-hotplates, and 34mW for 600°C for the large micro-hotplates. This is the lowest power consumption ever reported for CMOS micro-hotplates, and among the lowest for any type of micro-hotplate (either made in CMOS or non-CMOS processes). The thermal response time is also extremely small (2ms for the small heater, and 10ms for the large heater), which allows the use of the micro-hotplates in pulsed mode to further reduce the average power consumption.

The measurement results did not match with the initial simulations. This was because of the thermal conductivities of different materials which can vary for different processes. These were then measured, and the revised simulations then matched well with the measurements. Therefore it is important to fabricate test structures for each process. A SPICE transient model was also presented. This consists of a network of resistors and capacitors, and was shown to be much more accurate than a simple lumped model.

The micro-hotplates also have extremely good uniformity and reliability. Devices coming from different parts of a wafer have almost identical characteristics, as do the devices in different wafers. The membranes are mechanically stable, and have very little deflection both at room temperature, and when in operation. Finally the heaters are reliable, and have been shown to operate stably for 500 hours at high temperatures. These aspects are very important from a point of view of making a final gas sensor product, rather than just a simple laboratory demonstration. The micro-hotplates form an ideal platform for a smart gas sensor.

The two membrane devices studied here - the tungsten micro-hotplates, and the membrane power devices – are promising technologies for use in smart devices. An electro-thermo-mechanical analysis has been presented for both in this thesis. The better understanding gained by this study can help in improving and future design of these devices.

Further work:

As good as the micro-hotplates are, they have little value if the whole setup is not used as a gas sensor. Gas sensing materials need to be deposited and used for gas sensing. In this regard, Carbon Nanotubes (CNTs) have been grown on the micro-hotplates as a gas sensing material[6]. Preliminary gas testing has been performed and show good response to NO_2[7]. Other well known sensing material such as tin oxide can also be employed. As these are stable and already well known for gas sensing, it would be quicker to make a complete gas sensor with them. Sensing material deposition, and extensive gas testing is the logical next step to creating a smart gas sensor.

While the tungsten based micro-hotplates have shown excellent results, there is always room for improvement. A second generation of micro-hotplates has just recently been taped out to XFAB. These micro-hotplates have:

1. Smaller Membranes: Membranes with diameters 50µm and 100µm have been used, with heater sizes of 10µm & 12µm. This will increase the power consumption slightly. However since the power consumption was already very low in the first batch, the power consumption of these devices will still be very low in spite of the slight increase. The smaller membrane size will greatly increase the mechanical stability of the membranes, as well as greatly reducing the occupied chip area. These two advantages greatly outweigh the small increase in power consumption that results
2. Better gas sensing electrodes: 4-probe electrodes have been designed for more accurate measurement of the gas sensing layer. This method in particular will eliminate the effect of the contact resistance between the electrode and the sensing material which can be significant and greatly reduces the sensitivity and accuracy of the measurement.
3. Micro-hotplate arrays: Arrays of micro-hotplates (upto 4) have been designed to allow the simultaneous gas measurements by different sensing materials. This can be used in a system with appropriate pattern matching techniques achieve good

[6] CNTs were grown on the micro-hotplates by Samiul Haque (University of Cambridge)

[7] The gas testing measurements were performed by Dr. Jonghyurk Park (ETRI, Korea)

selectivity of a target gas, or to measure different gases at the same time for an electronic nose system.

List of Publications

List of publications related to the work presented in this thesis:

1. S.Z. Ali, W. Gonzalez, J.W. Gardner, F. Udrea, "Analysis of high temperature SOI micro-hotplates," Proceedings of the 2004 International Semidoncutor Conference, CAS 2004, Vol 2, pp 351-354

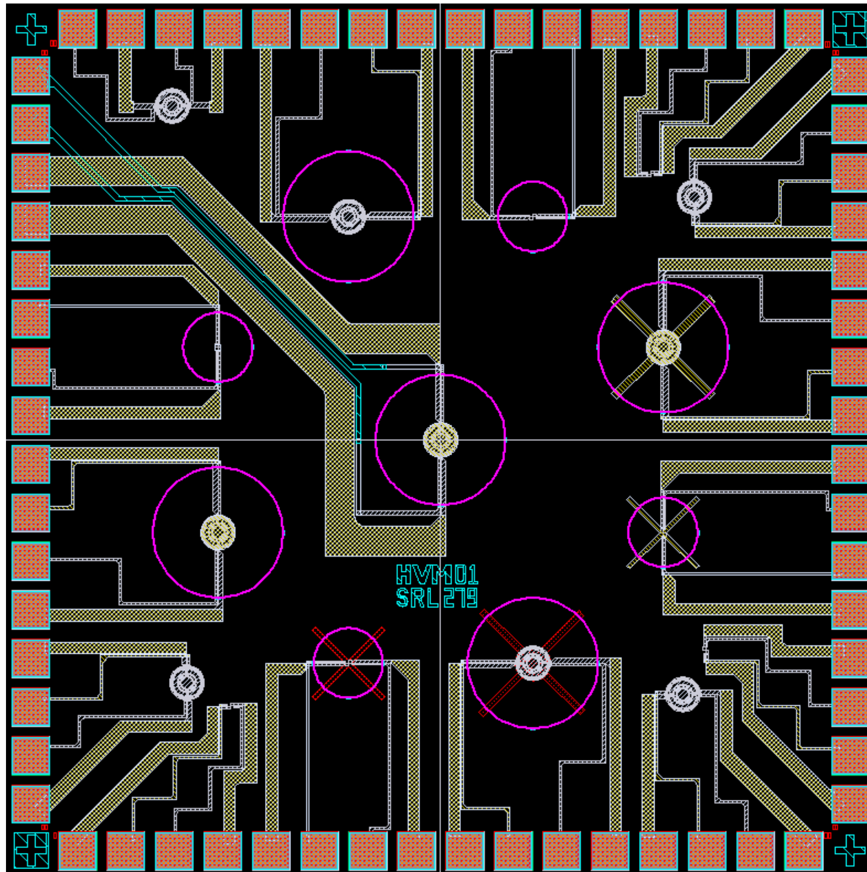
2. S.Z.Ali, P.K.Guha, C.C.C.Lee, F.Udrea, W.I.Milne, T.Iwaki, J.Covington, J.W.Gardner, J.Park, S.Maeng, "High temperature SOI CMOS Tungsten Micro-Heaters," IEEE Sensors 2006 p. 847 – 850

3. S.Z. Ali, F. Udrea, W.I. Milne, J.W. Gardner, J. Park, S. Maeng, "Tungsten Based SOI Micro-Hotplates for Smart Gas Sensors," – Submitted for publication in IEEE/ASME Journal of Microelectromechanical Systems

4. F. Udrea, J.W. Gardner, J. Park, M.S. Haque, S.Z. Ali, P.K. Guha, S.M.C. Vieira, H.Y. Kim, S.Y. Lee, S.H. Kim, Y. Choi, K.C. Kim, S.E. Moon, W.I. Milne, S. Maeng, "Three Technologies for a smart miniaturized gas-sensor: SOI CMOS, micromachining and CNTs – Challenges and Performance," accepted for presentation at IEDM 2007,10-12 December 2007, Washington DC, USA

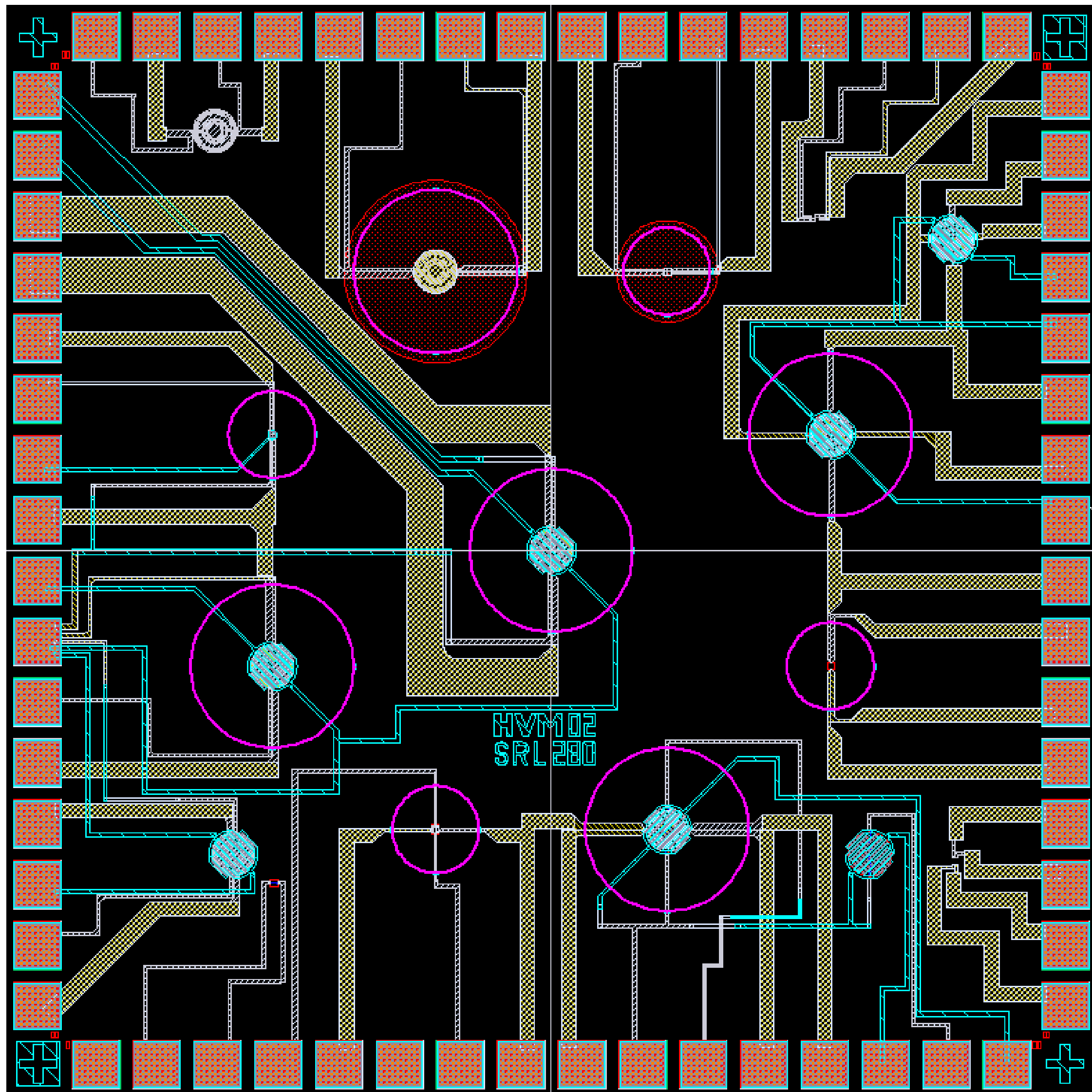
Appendix A: Fabricated Chips for Tungsten Micro-hotplates

Chip 1:



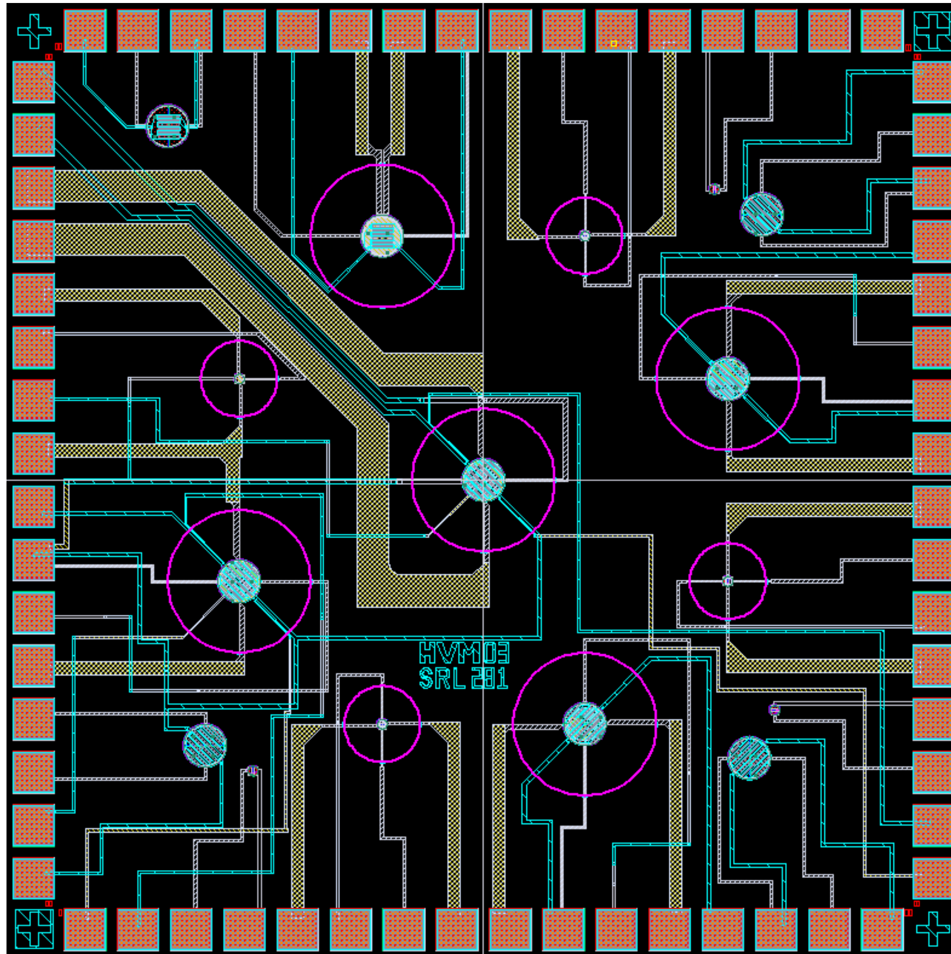
	Membrane		Heater		Temp Sensor		Layers			
Heater	Shape	Sensor	Type	Shape	Size	Type	Silicon	Met1	Met2	Met3
LB	Circular	Calorimeter	Tungsten	Loop Ringed	75	None	Plate	Loop Ringed	Plate	None
DB	Circular	Calorimeter	Tungsten	Loop Ringed	75	None	Plate + Beams	Loop Ringed	None	None
RB	Circular	Calorimeter	Tungsten	Loop Ringed	75	None	None	Loop Ringed	Plate + Beams	None
UB	Circular	Calorimeter	Tungsten	Loop Ringed	75	None	None	Loop Ringed	None	None
C	Circular	Calorimeter	Tungsten	Loop Ringed	75	None	Plate	Loop Ringed	Plate	None
LS	Circular	Calorimeter	Tungsten	Twisted Ring	12	None	Plate	Twisted Ring	Plate	None
LS	Circular	Calorimeter	Tungsten	Twisted Ring	12	None	Plate + Beams	Twisted Ring	None	None
RS	Circular	Calorimeter	Tungsten	Twisted Ring	12	None	None	Twisted Ring	Plate + Beams	None
US	Circular	Calorimeter	Tungsten	Twisted Ring	12	None	None	Twisted Ring	None	None

Chip 2



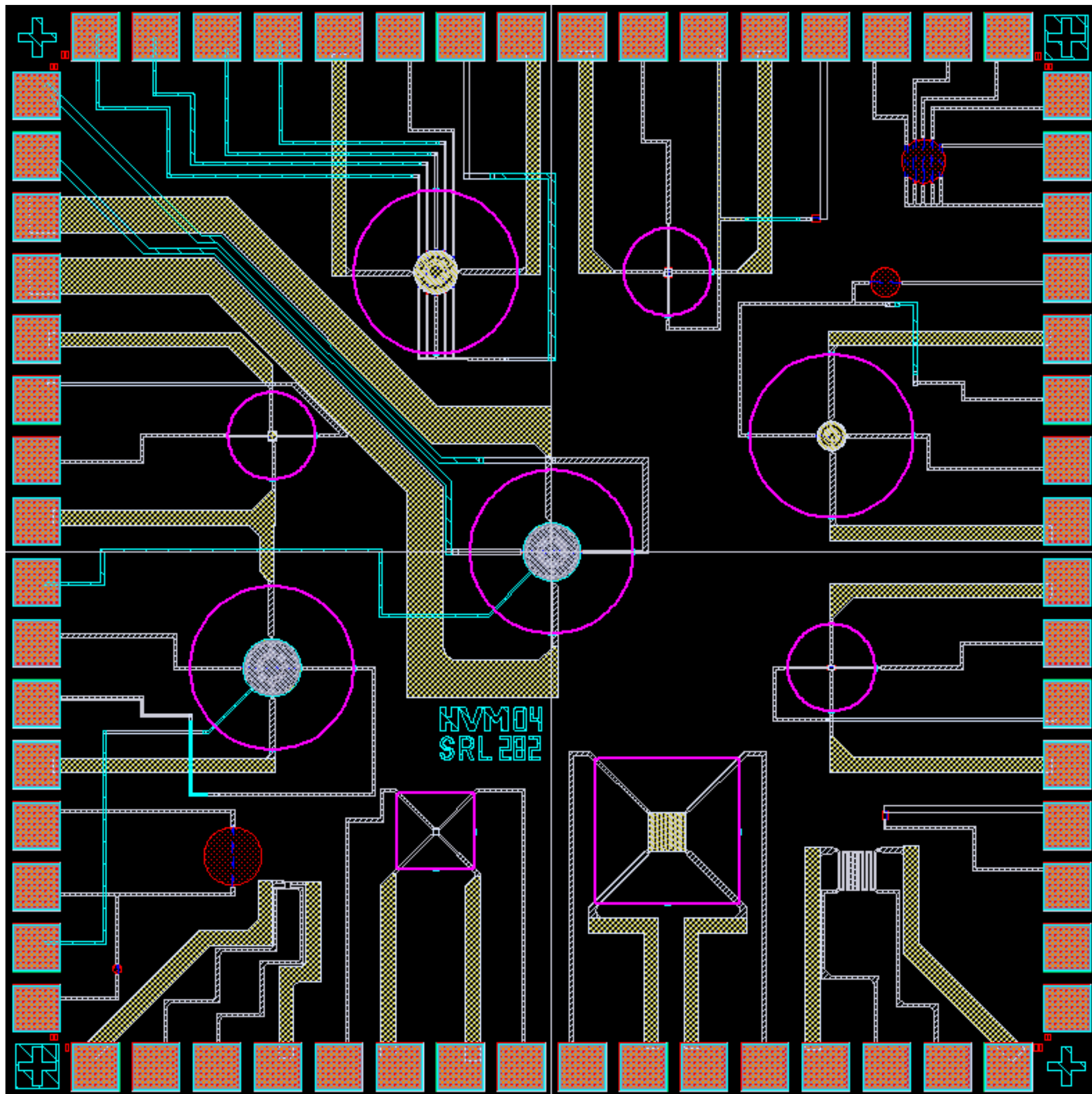
	Membrane		Heater		Temp Sensor		Layers			
Heater	Shape	Sensor	Type	Shape	Size	Type	Silicon	Met1	Met2	Met3
LB	Circular	Resistive	Tungsten	Loop Ringed	75	None	Plate	Loop Ringed	Plate	Resistive
DB	Circular	Resistive	Tungsten	Dual	75	Si Resistor	Plate/Res	Ring Heater	Heater	Resistive
RB	Circular	Resistive	Tungsten	Dual	75	Tungsten	Plate	Loop Ringed	Loop Ringed	Resistive
UB	Circular	Calorimeter	Tungsten	Loop Ringed	75	None	Membrane	Loop Ringed	Plate	None
C	Circular	Resistive	Tungsten	Loop Ringed	75	None	Plate	Loop Ringed	Plate	Resistive
LS	Circular	Calorimeter	Tungsten	Twisted Ring	12	None	Plate	Twisted Ring	Plate	Electroplate
DS	Circular	Calorimeter	Tungsten	Dual	12	Si Resistor	Plate/Res	Multiringed	Loop Ringed	None
RS	Circular	Calorimeter	Tungsten	Dual	12	Tungsten	Plate	Multiringed	Multiringed	None
US	Circular	Calorimeter	Tungsten	Twisted Ring	12	None	Membrane	Twisted Ring	Plate	None

Chip 3



	Membrane		Heater		Temp Sensor		Layers			
Heater	Shape	Sensor	Type	Shape	Size	Type	Silicon	Met1	Met2	Met3
LB	Circular	Resistive	Tungsten	Loop Ringed	75	Diode	Plate/diode	Loop Ringed	Refresh	Resistive
DB	Circular	Resistive	Tungsten	Spiral	75	Diode	Plate/diode	Spiral	Plate	Resistive
RB	Circular	Resistive	Tungsten	Meander	75	Diode	Plate/diode	Meander	Plate	Resistive
UB	Circular	Resistive	Tungsten	Multiring+Ring	75	Diode	Plate/diode	Multiring_Ring	Plate	Resistive
C	Circular	Resistive	Tungsten	Loop Ringed	75	Diode	Plate/diode	Loop Ringed	Refresh	Resistive
LS	Circular	Calorimeter	Tungsten	Twisted Ring	12	Diode	Plate/diode	Twisted Ring	Plate	None
DS	Circular	Calorimeter	Tungsten	Spiral	12	Diode	Plate/diode	Spiral	Plate	None
RS	Circular	Calorimeter	Tungsten	Meander	12	Diode	Plate/diode	Meander	Plate	None
US	Circular	Calorimeter	Tungsten	Loop Ringed	12	Diode	Plate/diode	Loop Ringed	Plate	None

Chip 4



Heater	Membrane		Heater		Temp Sensor		Layers			
Heater	Shape	Sensor	Type	Shape	Size	Type	Silicon	Met1	Met2	Met3
LB	Circular	Calorimeter	Tungsten	Loop Ringed	100	Si Resistor	Plate/Res	Loop Ringed	Plate	Electroplate
DB	Square	Calorimeter	Tungsten	Loop Ringed	75	None	Plate	Meander	Plate	None
RB	Circular	Calorimeter	Tungsten	Loop Ringed	50	Si Resistor	Plate/Res	Loop Ringed	Plate	None
UB	Circular	Calorimeter	Tungsten	Loop Ringed	75	Si Resistor	Plate/Res	Loop Ringed	Plate	None
C	Circular	Calorimeter	Tungsten	Loop Ringed	100	Si Resistor	Plate/Res	Loop Ringed	Plate	Electroplate
LS	Circular	Calorimeter	Tungsten	Twisted Ring	12	Si Resistor	Plate/Res	Twisted Ring	Plate	None
DS	Square	Calorimeter	Tungsten	Meander	12	None	Plate	Meander	Plate	None
RS	Circular	Calorimeter	Tungsten	Twisted Ring	9	Si Resistor	Plate/Res	Twisted Ring	Plate	None
US	Circular	Calorimeter	Tungsten	Twisted Ring	15	Si Resistor	Plate/Res	Twisted Ring	Plate	None

Appendix B – Thermal Conductivity of Thin Silicon

Calculated values of thermal conductivity of 0.25µm thin silicon are:

Temperature (K)	Thickness (µm)	1/3 CV (W/m^2K)	k (Bulk) (W/mK)	k (Film) (W/mK)
300	0.25	2.87E+08	154.679	85.52268
310	0.25	2.88E+08	148.773	83.76709
320	0.25	2.88E+08	143.2336	82.05257
330	0.25	2.89E+08	138.0291	80.37933
340	0.25	2.89E+08	133.131	78.74727
350	0.25	2.9E+08	128.5141	77.15608
360	0.25	2.9E+08	124.1557	75.60525
370	0.25	2.9E+08	120.0358	74.09418
380	0.25	2.91E+08	116.1359	72.62212
390	0.25	2.91E+08	112.4398	71.18829
400	0.25	2.91E+08	108.9325	69.79182
410	0.25	2.92E+08	105.6005	68.43182
420	0.25	2.92E+08	102.4317	67.10737
430	0.25	2.92E+08	99.41494	65.81755
440	0.25	2.92E+08	96.54001	64.56143
450	0.25	2.93E+08	93.79763	63.33805
460	0.25	2.93E+08	91.17931	62.14651
470	0.25	2.93E+08	88.67725	60.98588
480	0.25	2.93E+08	86.28425	59.85526
490	0.25	2.93E+08	83.99373	58.75377
500	0.25	2.93E+08	81.79959	57.68054
510	0.25	2.94E+08	79.6962	56.63473
520	0.25	2.94E+08	77.67835	55.61551
530	0.25	2.94E+08	75.74122	54.62208
540	0.25	2.94E+08	73.88034	53.65366
550	0.25	2.94E+08	72.09156	52.7095
600	0.25	2.95E+08	64.10256	48.3275
700	0.25	2.95E+08	51.80005	41.00832
800	0.25	2.96E+08	42.8449	35.19564
900	0.25	2.96E+08	36.09457	30.51353

References

[1] J.W Gardner, V.K Varadan, O.O Awadelkarim, “Microsensors MEMS and Smart Devices”, 2001, John Wiley & Sons Ltd, UK.

[2] C. Liu, “Foundations of MEMS,” 2006, Pearson Education Inc, New Jersey

[3] P.R. Scheeper, A.G.H. Donk, W. Olthuis, P. Bergveld, “A review of silicon microphones,” Sensors and Actuators A 44 (1994) p1-11

[4] J. Fraden, “Handbook of Modern Sensors”, Third Edition, 2004, Springer-Verlag, New York

[5] J.S. Ko, W. Liu, W. Zhu, “Substrate effects on the properties of the pyroelectric thin film IR detectors,” Sensors and Actuators A 93, 2001, p 117-122

[6] I. Simon, N. Barson, M. Bauer, U. Weimar, “Micromachined metal oxide gas sensors: Opportunities to improve sensor performance,” Sensors and Actuators B 73, 2001, p 1-26

[7] F. Udrea, T. Trajkovic, G. Amaratunga, “High Voltage Devices – A Milestone Concept in Power ICs,” IEDM Technical Digest 2004, p 451-454

[8] M.J. Madou, “Fundamentals of Microfabrication – The Science of Miniaturization,” Second Edition, CRC Press, Florida, USA, 2002

[9] N. Maluf, “An Introduction to Microelectromechanical Systems Engineering,” Artech House Publishers, Norwood, 2000

[10] M. Esashi, M. Takinami, Y. Wakabayashi, K. Minami, “High-rate directional deep dry etching for bulk silicon micromachining,” Journal of Micromechanics and Microengineering 5 (1995) pp. 5-10

[11] F. Laermer, A. Schilp, “Method for Anisotropic Plasma Etching of Substrates,” Robert Bosch GmbH: US Patent 5,498,312

[12] H.K Trieu, N. Kordas, W. Mokwa “Fully CMOS compatible capacitive differential pressure sensors with on-chip programmabilities and temperature compensation”, Sensors, 2002. Proceedings of IEEE , Volume: 2, Pages:1451 - 1455 , 12-14 June 2002

[13] N. Mohan, T. Undeland, W. Robbins, “Power Electronics Converters, Applications and Design,” Third Edition, John Wiley and Sons, Inc, 2003

[14] F. Udrea, D. Garner, K. Sheng, A. Popescu, H.T. Lim, W.I. Milne,(2000) “SOI Power Devices”, Electronics and Communication Engineering Journal 12 (1): 27-40 Feb 2000

[15]G.G. Shahidi, “SOI Technology for the GHz era,” IBM Journal of Research and Development, Vol 46 No 2/3 March/May 2002

[16] http://www.soitec.com/

[17] J.R. Schwank, V. Ferlet-Cavrois, M.R. Shaneyfelt, “Radiation Effects in SOI Technologies”, IEEE Transactions on Nuclear Science, Vol 50, No 3, pg 522-538, 2003

[18] K. Ihokura, J. Watson, “The stannic oxide gas sensor: principles and applications”, (1994), Boca Raton, Fla. ; London : CRC

[19] J.W. Gardner, “Microsensors Principles and Applications”, 1994, John Wiley & Sons Ltd, UK

[20] L. Valentini, I. Armentano, J. M. Kenny, C. Cantalini, L. Lozzi, S. Santucci, “Sensors for sub-ppm NO_2 gas detection based on carbon nanotube thin films,” Applied Physics Letters, Vol 82 No 6, February 2003, pp 961-963

[21] L. H. Nguyen, T. V. Phi, P. Q. Phan, H. N. Vu, C. Nguyen-Duc, F. Fossard, “Synthesis of multi-walled carbon nanotubes for NH_3 gas detection,” Physica E 37, 2007, pp 54-57

[22] A. Heilig, N. Barsan, U. Weimar, M. Schweizer-Berberich, J.W. Gardner, W. Gopel, “Gas Identification by modulating temperatures of SnO_2-based thick film semsors,” Sensors and Actuators B, vol 43, September 1997, pp 45-51

[23] U. Dibbern, “A Substrate for Thin-film Gas Sensors in Micro-electronic Technology”, Sensors and Actuators B, 2 (1990) 63-70

[24] J.W. Gardner, A. Pike, N.F. de Rooij, M. Koudelka-Hep, P.A. Clerc, A. Hierlemann, W. Gopel, “Integrated Array Sensor for Detecting Organic Solvents”, Sensors and Actuators B 26-27 (1995) 135-139.

[25] P. Krebs, A. Grisel, “A Low Power Integrated Catalytic Gas Sensor,” Sensors and Actuators B 13-14 (1993) 155-158.

[26] D. Lee, W. Chung, M. Choi, J. Baek, “Low Power micro gas sensor,” Sensors and Actuators B 33 (1996) 147-150

[27] D. Briand, A. Krauss, B. Schoot, U. Weimar, N. Barsan, W. Gopel, N. de Rooij, “Design and fabrication of high-temperature micro-hotplates for drop-coated gas sensors,” Sensors and Actuators B 68 (2000) 223-233.

[28] S. Fung, Z. Tang, P. Chan, J. Sin, P. Cheung, “Thermal analysis and design of a micro-hotplate for integrated gas-sensor applications,” Sensors and Actuators A 54 (1996), 482-487

[29] C. Tsamis, A.G. Nassiopoulou, A. Tserepi, “Thermal Properties of Suspended Porous Silicon Micro-Hotplates for Sensor Applications”, Sensors and Actuators B 95 (2003), 78-82.

[30] P. Furjes, C. Ducso, M. Adam, J. Zettner, I. Barsony, “Thermal Characterisation of micro-hotplates used in sensor structures”, Superlattices and Microsturctures 35 (2004) 455-464

[31] I. Elmi, S. Zampolli, E.cozzani, M. Passini, G.C. Cardinali, M. Severi, “Development of Ultra Low Power Consumption Hotplates for Gas Sensing Applications,” Proceedings of the IEEE Sensors Conference 2006, Daegu, Korea, October 22-25, 2006, p. 243-246

[32] J.W.Gardner, M. Cole, F.Udrea, “CMOS Gas Sensors and Smart Devices,” Proceedings of the IEEE Sensors Conference 2002 Atlanta, pp , 2002

[33] J.S. Suehle, R.E. Cavicchi, M. Gaitan, “Tin Oxide Gas Sensor Fabricated Using CMOS Micro-hotplates and In-Situ Processing”, IEEE Electron Device Letters, Pg 118-120, Vol 14, No 3 March 1993

[34] F. Udrea, J.W. Gardner, D. Setiadi, J.A. Covington, T. Dogaru, C.C. Lu, W.I. Milne, "Design and simulations of SOI CMOS micro-hotplate gas sensors" Sensors and Actuators B, 78 2001, pg 180-190

[35] M. Graf, D. Barrettino, K. Kirstein, A. Hierlemann, "CMOS microhotplate sensor system for operating temperatures up to 500°C", Sensors and Actuators B 117 (2006) 346-352

[36] M. Rydberg, U. Smith, "Long-Term Stability and Electrical Properties of Compensation Doped Poly-Si IC-Resistors," IEEE Transactions on Electron Devices, Vol47, No 2, February 2000.

[37] M. Afridi, J. Suehle, M. Zaghloul, D. Berning, A. Hefner, R. Cavacchi, S. Semancik, C. Montgomery, C. Taylor, "A monolithic CMOS Microhotplate based gas sensor system," IEEE Sensors Journal Vol 2, No 6 December 2002, 644 - 655

[38] Patent: J. Gardner, F. Udrea, J. Covington, "CMOS compatible tungsten micro heaters," GB Patent Application 0505192.5

[39] Y.S. Touloukian "Thermophysical Properties of Matter," the TPRC data series; a comprehensive compilation of data, NewYork, IFI/Plenum, 1970

[40] C.J. GlassBrenner, G.A. Slack, "Thermal Conductivity of Silicon and Germanium from 3°K to the Melting Point", Physical Review, Volume 134, Number 4A, 18May 1964

[41] A. Pike, J.W. Gardner, "Thermal modelling and characterisation of micropower chemoresistive silicon sensors ", Sensors and Actuators B: Chemical, Volume 45, Issue 1, November 1997, Pages 19-26

[42] J.P. Holman, "Heat transfer", 9th ed, Boston, MA: 2002

[43] J.A. Pelesko, D.H. Bernstein, "Modeling MEMS and NEMS.", 2003, Boca Raton, FL

[44] A. Gotz, C. Cane, E.Lora-Tamayo, "Specific Problems of FEM Thermal Simulations for Microsystems," Proceedings of the First International Conference on Simulation and Design of Microsystems and Microstructures, microSIM, Vol 95, 1995, pp. 137-146.

[45] A. Thakur, R. Raman, "Thermal Emissivities of Films on Substrates," Applied Energy 15 (1983), pp 1-13

[46] F. Volklein, "Thermal conductivity and Diffusivity of a thin film SiO_2-Si_3N_4 Sandwich System," Thin Solid Films, 188 (1990), pp27-33

[47] S.M.Lee, D.C. Dyer, J.W. Gardner, "Design and Optimisation of a high-temperature silicon micro-hotplate for nanoporous palladium pellistors," Microelectronics Journal 34 pp115-126, 2003

[48] D. Briand, S. Heimgartner, M. Gretillat, B. Schoot, N. F. Rooij, "Thermal optimization of micro-hotplates that have a silicon island," Journal of Micromechanics and Microengineering 12, pp 971-978, 2002

[49] T. Li, L. Wu, Y. Liu, L. Wang, Y. Wang, Y. Wang, "Micro-Heater on Membrane with Large Uniform-Temperature Area,“ Proceeding of the IEEE Sensors Conference 2006, Daegu, Korea, pp 571-575, 2006

[50] M.Baroncini, P.Placidi, G.C.Cardinali, A.Scorzoni, "Thermal characterization of a microheater for micromachined gas sensors," Sensors and Actuators A 115 (2004), pp8-14

[51] M. Arx, O. Paul, H. Baltes, "Process-Dependent Thin-Film Thermal Conductivities for Thermal CMOS MEMS", Journal of Microelectromechanical Systems, vol 9 No 1 March 2000 pg 136-145

[52] M. Asheghi, Y.K. Leung, S.S. Wong, K.E. Goodson, "Phonon-boundary scattering in thin Silicon Layers", Applied Physics Letter 71 (13) September 1997 1798-1800

[53] M. Omar, "Elementary Solid State Physics," Addison-Wesley Publishing Company, 1993

[54] Y.S JU, K.E. Goodson, "Size Effect on Thermal Conduction in Silicon-on-Insulator Devices under Electrostatic Discharge (ESD) Conditions", Journal of Applied Physics Vol 36 (1997) pp. 798-800

[55] D. Resnik, U. Aliancic, D. Vrtacnik, M. Mozek, S. Amon, "Mechanical Stress in thin film microstructures on silicon substrate," Vacuum 80 (2005), pp 236-240