

SOI Gas Sensors with Low Temperature CVD films

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Summary: A novel gas sensor has been designed and fabricated using SOI technology. The device comprises of a thin SOI membrane in which has been embedded an FET heater. The device can operate up to a maximum temperature of ca. 350 °C with a typical power consumption of 40 to 70 mW. Here we report upon a novel process that has been developed to deposit thin films of both vanadium and tungsten oxide at temperatures compatible with CMOS technology for use in resistive or FET based sensors. The CVD films are characterized and their response to CO and toluene investigated.

Keywords: SOI sensors, gas sensors, CVD films

Category: 5 (Chemical sensors)

1 Introduction

In the last two decades, there has been increasing demand for mobile, hand-held gas monitors with wide application in the environmental, automotive and medical industries. Presently, solid-state gas sensors tend to suffer from high power consumption (ca. 1 W) - especially for metal-oxide resistive gas sensors that require very high temperatures (e.g. 300 °C or more) [1]. In addition these sensors cannot detect accurately low levels (e.g. < 100 PPM) of some important hazardous gases. This makes them an impractical option for application in battery-operated units and less than ideal for automotive units. To overcome these disadvantages, we proposed and patented [2] a novel design of gas microsensors compatible with current CMOS technology, and have developed the concept within this joint EPSRC project. Our goal here is to combine an SOI CMOS resistive (or FET) gas sensor developed at the Universities of Warwick and Cambridge with a novel low-temperature post-CMOS chemical vapour deposition (CVD) process developed at University College London (UCL).

2 SOI Gas Sensors

Fig 1 illustrates the basic structure of the SOI CMOS gas sensor. In place of a passive resistive heater (e.g. platinum or polysilicon), an active *n*-channel MOSFET is used.

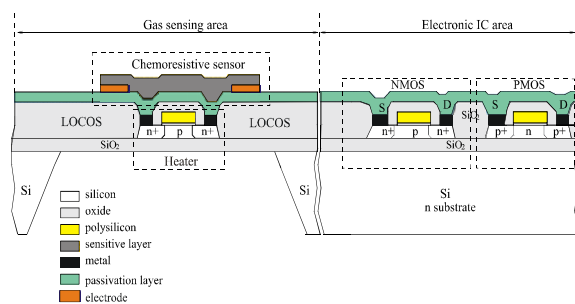


Fig. 1. Design of a smart SOI gas sensor employing an *n*-channel MOSFET heater (resistive type).

The MOSFET is ideal as a micro-heater because its power and hence its operating temperature, can be easily controlled via its gate potential. The MOSFET has a negative temperature coefficient (the current decreases at high temperatures due to reduced channel mobility) thus offering a good thermal stability. The SOI membrane and LOCOS provide vertical and lateral isolation respectively. Metal electrodes are placed above the micro-heater to form the resistor and isolated from it through subsequent IDLs (inter dielectric layers). In the FET sensor case the FET micro-heater surrounds the sensing element, with the gate oxide exposed through the IDLs.

The SOI device has been fabricated at SUMC (UK) and the resistive version is illustrated in Fig 2. The handle silicon was removed using either an isotropic dry deep RIE process or an anisotropic wet etch to leave a thin SOI membrane, shown in figure 3. The complete membrane comprises of a thin silicon layer together with an oxide/nitride passivation layers; the overall thickness being between 1 - 2 μm.

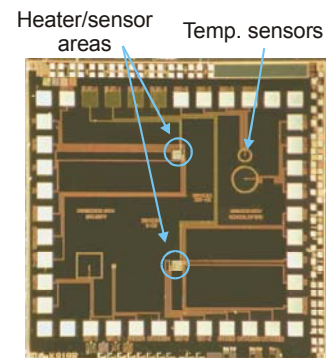


Fig. 2. Photograph SOI resistive gas sensing device and off-membrane temp sensors (5 mm by 5 mm)

The DC power consumption of the SOI devices has been measured and compared with other SOI devices fabricated via Europractice using a 0.8 μm MATRA process. The power consumption depends

upon the thickness of the SOI membrane; measured values range from 40 to 140 mW at 300 °C.

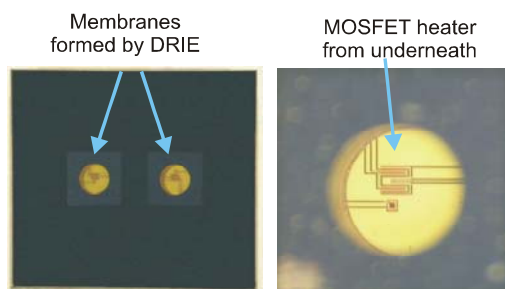


Fig. 3 Photograph of SOI MOSFET heater inside a thin translucent SOI membrane (DRIE process)

3 Thin Film Deposition

UCL have established reaction conditions for atmospheric pressure (AP) or aerosol assisted (AA) CVD that are attractive for large scale, rapid production of a variety of widely adopted gas sensing metal oxides (e.g. V_2O_5 , WO_3 , SnO_2) [3,4]. In addition, materials have been deposited *via* APCVD that are expected to exhibit interesting sensing and/or optical properties (e.g. VO_2 , $Ti_{1-x}M_xO_2$ ($M = W, Nb, V, Cr, N, Mo$)). In each case, deposition using a cold-wall horizontal bed reactor was possible at 400 °C (in some cases as low as 350 °C), temperatures well below the melting point of aluminum. In general, the films showed good, uniform coverage across the substrate with high deposition rates (assessed by cross-sectional SEM to be *ca.* 0.5-1.0 $\mu\text{m}/\text{min}$).

We summarize here the results for the deposition of V_2O_5 (*via* APCVD) and WO_3 (*via* AACVD). Reaction of VCl_4 or $VOCl_3$ with water under APCVD conditions at 350-400 °C produced uniform, clear yellow films. Film characterization by glancing angle X-ray diffraction (XRD) showed only the *orthorhombic* phase of V_2O_5 (indexed unit cell dimensions $a = 11.527(5)$, $b = 4.382(5)$, $c = 3.557(5)$ Å lie within ± 0.005 Å of literature). Depth profile studies of the film surface using X-ray photoelectron spectroscopy (XPS) showed the presence of vanadium and oxygen only (beyond the first few atomic layers). The binding energies recorded are in excellent agreement with literature (516.0 eV for V $2p_{3/2}$ and 530.5 eV for O 1s) and show a notable absence of chlorine contamination as well the presence of only one vanadium species (V^{5+}) residing in a single chemical environment. XRD/XPS analyses therefore suggest the direct, single step deposition of a single (orthorhombic) phase of V_2O_5 . This is confirmed by Raman spectroscopy, which shows identical patterns to bulk and magnetron sputtered V_2O_5 (with bands at 697, 524, 478, 401, 300, 283, 194, 145 and 103 cm^{-1}). SEM showed the films to be comprised of sub-micron platelets, suggesting film growth proceeds from the substrate surface and *via* an ‘island growth’ mechanism. AACVD has been used successfully to deposit thin, uniform blue films at

substrate temperatures of 300-400°C from the decomposition of a single source precursor tungsten hexa-phenoxide, $W(OPh)_6$ (see Figure 4). Characterization by XPS shows the films to be a single phase of WO_{3-x} , with the results being in excellent agreement (± 0.05 eV) with literature. Species present: $W^{6+} 4f_{7/2} = 35.6$ eV; $W^{6+} 4f_{5/2} = 37.8$ eV; O 1s = 530.0 eV; W 4f doublet shoulder at lower energies assigned to $W^{4+/5+}$ cations). Carbon contamination was assessed to be low, at *ca.* 2 %, by XPS. Post-annealing the films in O_2 at temperatures ≥ 400 °C afforded pale yellow films within 30 min, characterized by XPS as WO_3 (i.e. **no** $W^{4+/5+}$ cations present) with minimal carbon content (< 0.5 %).

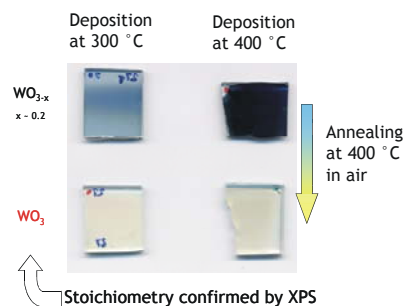


Fig. 4 Photograph of CVD films on glass substrate

Further characterization of film stoichiometry before and after annealing was carried out by XRD and Raman for films deposited at 300 & 400 °C. Raman spectroscopy shows bands of amorphous WO_{3-x} for deposition at 300 °C. At 400 °C a more crystalline film forms, with the WO_{3-x} spectrum dominated by *additional* bands that coincide with monoclinic γ - WO_3 . Upon annealing at 400 °C, Raman confirms the presence of fully oxidized, crystalline monoclinic γ - WO_3 with removal of the bands assigned to the reduced species.

3 Conclusions

A low-temperature CMOS compatible process has been developed in order to deposit thin films of vanadium and tungsten oxide on to thin SOI micro-plates. Allowing circuit integration with metal oxide sensing materials. The response of these novel resistance and FET gas sensors to CO and toluene is reported. The low power, high temperature operation will make these sensors ideal for a range of gas detection applications.

References

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