Available online at www.sciencedirect.com
ScienceDirect
Sensors and Actuators B 127 (2007) 260–266
SENSORS AND ACTUATORS B CHEMICAL
www.elsevier.com/locate/snb

Novel design and characterisation of SOI CMOS micro-hotplates for high temperature gas sensors

P.K. Guha [a,*], S.Z. Ali [a], C.C.C. Lee [a], F. Udrea [a], W.I. Milne [a], T. Iwaki [b], J.A. Covington [b], J.W. Gardner [b]

[a] Centre for Advanced Photonics and Electronics, University of Cambridge, Cambridge CB3 0FA, UK
[b] School of Engineering, University of Warwick, Coventry CV4 7AL, UK

Abstract

This paper describes the design and characterisation of a new generation of fully CMOS compatible novel micro-hotplates for high temperature gas sensors. The micro-hotplates employ advanced MOSFET heaters embedded in an SOI membrane. The heaters can operate at a ground-breaking high temperature of 550 °C for an ultra-low power consumption of 16 mW (continuous operation) and have a thermal rise time of below 10 ms. A large number of devices have been characterised over a batch of wafers and they show excellent reproducibility and reliability. The yield of the micro-hotplates after deep RIE back-etching was close to 90% while the residual stress was found to be minimal, resulting in flat and stable membranes. Electronic circuits for drive and readout have also been designed and integrated with the micro-hotplates to create a smart gas sensor.

Keywords: SOI micro-hotplate; Gas sensor; Smart sensor

1. Introduction

Hand-held, low cost and reliable gas monitors capable of detecting toxic and combustible gases are highly desirable for use in automotive, environmental and other applications. However, the relatively high power consumption and cost of commercial devices make them impractical in portable, battery-powered instruments and low-power automotive units. Presently, the most widely available resistive gas sensor (Taguchi type, sold by Figaro, Japan) has an operating temperature of typically 400 °C and power consumption of between 500 mW and 800 mW [1]. Other sensing technologies exist, for example, the catalytic pellistor. This device is used extensively for methane detection, but again is relatively expensive and has a high power consumption of 350–850 mW at 500 °C [2]. For these reasons, considerable research effort has been directed towards silicon-based micro-hotplate designs for low-power gas sensors. Predominantly these have been based on the integration of a platinum micro-heater embedded into a low stress silicon nitride membrane [3,4]. Although highly successful at reducing power consumption, platinum is not CMOS compatible hence cannot benefit from the low cost of CMOS fabrication and circuit integration. This integration of micro-hotplates into a CMOS process could well achieve the target of low cost, high reliability and low power consumption.

In the development of CMOS micro-hotplate designs, it is critical to reduce significantly the power consumption and ensure a uniform temperature distribution over the sensing area. Such goals can be considered highly challenging as traditional materials available in CMOS technology have limitations. For example, researchers have reported micro-heaters made from polysilicon or aluminium, but polysilicon has poor long-term stability due to grain boundary movement and crack propagation whilst aluminium shows electro-migration at high temperatures as well as having a relatively low melting point [5,6]. An alternative SOI CMOS heater based on a MOSFET heater structure was proposed by Gardner and Udrea some 10 years ago. The advantages of a MOSFET heater are CMOS compatibility, thus the power can be controlled via the gate terminal and that ultra-small heaters can be formed because the resistance of the heater is controlled via the gate potential. Here a MOSFET, fabricated using a standard SOI CMOS process, was used as the heater with the handle silicon beneath removed to form a thin membrane. Although successful in reaching operating temperatures of 350 °C for a power consumption of less than 100 mW, these

---

* Corresponding author at: CAPE Building, 9 J J Thomson Avenue, University of Cambridge, Cambridge CB3 0FA, UK. Tel.: +44 1223 748311; fax: +44 1223 748348.
E-mail address: pkg23@cam.ac.uk (P.K. Guha).

0925-4005/$ – see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.snb.2007.07.047

early devices were post-processed individually and thus not ideal for mass markets [7–9]. At the same time other research group's such as those of Baltes (ETH, Zurich) and de Rooij (IMT, Neuchatel) were exploring non-SOI micro-heaters fabricated inside silicon plugs [10,11].

Here we report on the design and experimental characterisation of new generation of novel SOI CMOS MOSFET micro-heaters, with batch post-processing, increased operating temperature range and reduced power consumption. Temperature sensors in the form of on-chip n^+pp^+ diodes and silicon resistors have been designed, simulated with Cadence (version 5.0.0), fabricated and experimentally characterised. Electronic circuits have also been developed and integrated with the micro-hotplates. This circuitry benefits from the well-known advantages of SOI technology, e.g. effective isolation and reduced leakage currents.

2. SOI micro-hotplate design

Here we have developed micro-hotplates for use in calorimetric and resistive gas sensors. The device contains novel shaped MOSFET micro-hotplates fabricated using a 1.0 μm SOI CMOS triple metal process by X-Fab (6 in. process, Germany). A schematic of an SOI resistive gas sensor employing a MOSFET micro-hotplate is shown in Fig. 1. The MOSFET micro-heater is embedded within the silicon layer of an SOI membrane and therefore does not require any extra fabrication steps to the standard CMOS process beyond the membrane formation (back-etch). Sensing materials are added as a post-processing step to form the gas sensors. The response of devices with sensing materials to different gases will be reported elsewhere [12].

Two different heater/membrane geometries were used with each geometry employing both p-type or n-type MOSFET heaters. Ring MOSFETs were used for the large membranes and plate MOSFETs for the small membranes. The (*W*/*L*) of the large and small MOSFETs was (471/3) and (74/2.5), respectively. The MOSFETs have the body-source shorted and the number of shorts was increased (shorting made after each 2.5 μm) above that required by the standard library design (after each 4 μm), so that they are less susceptible to the high temperatures and stresses. All the membranes were circular in design, to reduce high thermal stress points, with radii of 282 μm and 150 μm. These corresponded to heater radii of 75 μm and 12 μm, respectively.

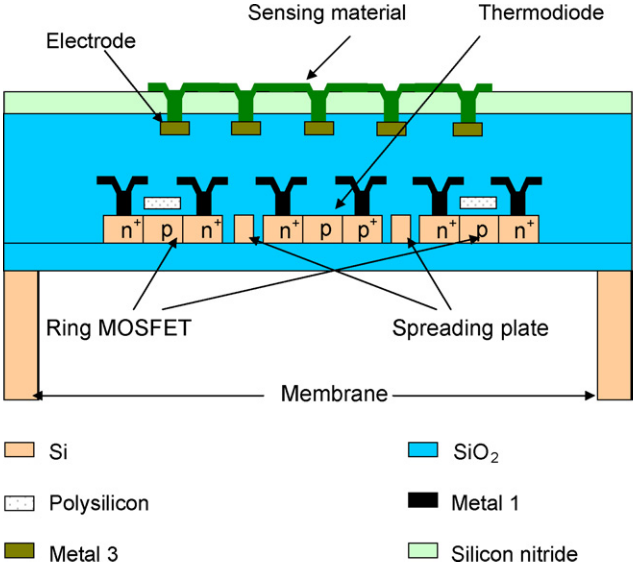


Fig. 1. Cross-sectional view of designed gas sensor (drawing not in scale).

Besides the heater, the other key elements are the sensing material, the temperature sensor, and the heat spreading plate for temperature uniformity. Resistive micro-hotplates contain interdigitated electrodes made of areas from exposed top metal layer (made with metal 3 covered by pad opening, for measuring the change in the resistance of the sensing material in the presence of gases). The membranes were formed by high precision deep reactive ion etching (DRIE) of the silicon substrate. The buried oxide layer acts as an etch stop and thermally isolates the sensing area, hence further reducing the power loss. This type of etching produces near vertical walls, compared to wet etching using KOH or TMAH and thus leads to a significant reduction in the chip area. In addition, this process resulted in a yield of almost 90%; an important factor for commercialisation.

As stated above, a further important part of the design was the integration of the temperature sensors. For the large mem-

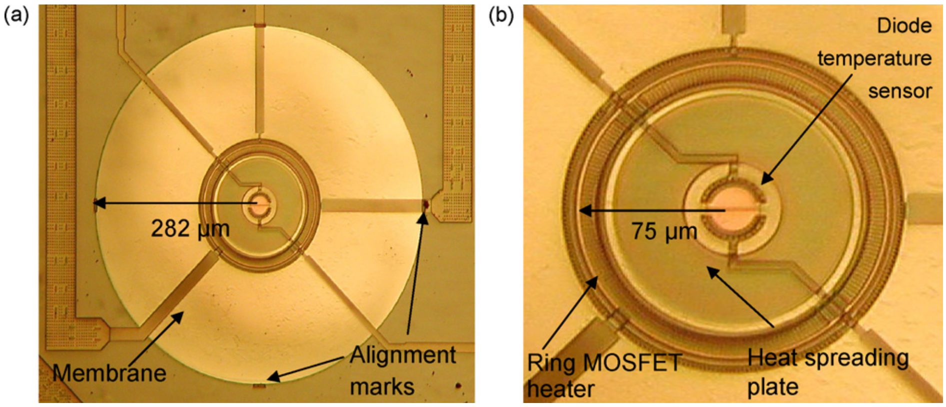


Fig. 2. (a) Large MOSFET based micro-hotplate and (b) enlarged view of the heating element.

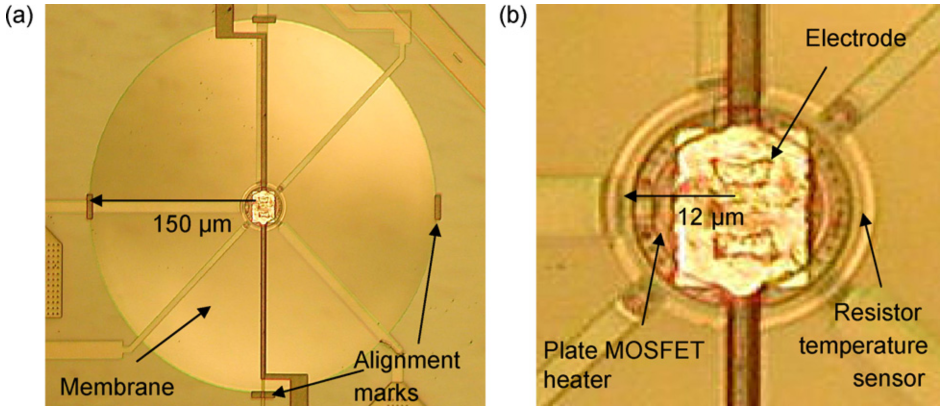


Fig. 3. (a) Small MOSFET based micro-hotplate and (b) enlarged view of the heating element.

branes, a circular n^+pp^+ diode of 18 μm radius was designed to match the shape of the ring MOSFET heater. It was located at the centre of the membrane to enable accurate temperature sensing. For the small membranes, p^+ or n^+ silicon circular ring resistor temperature sensors of 17 μm radius were designed around the FET heater. An optical image of a fabricated SOI micro-hotplate showing the main features is presented in Figs. 2 and 3 (top view). We have also tried heaters of different geometries (radii 50 μm and 100 μm) for the same large membrane size as a comparative study.

Lastly, some designs had integrated electronic circuits to condition signals from the integrated temperature sensors. A cascode current mirror circuit was designed to drive the temperature sensor. An integrated, single supply, op-amp was designed with a gain of 60 dB and a phase margin of over 60°. The op-amp is low power (around 0.3 mW, which is <2.0% of the maximum power consumption by the small heater) and can operate with a supply voltage of 4.5–5.5 V and fluctuations in temperature from −40 °C to 150 °C. An instrumentation amplifier (IA) was designed to measure the peak temperature in the membrane. The principle used here is to have one temperature sensor on the membrane and a reference sensor off the membrane; the instrumentation amplifier will therefore amplify the difference in the signals coming from the two temperature sensors (as shown in Fig. 4). The gain of the instrumentation amplifier was set to 7 ($R_1 = 8\,k\Omega$, $R_2 = 10\,k\Omega$, $R_3 = 10\,k\Omega$, $R_4 = 20\,k\Omega$) in case of resistive gas sensor and 39 ($R_1 = 4\,k\Omega$, $R_2 = 24\,k\Omega$, $R_3 = 24\,k\Omega$, $R_4 = 72\,k\Omega$) for calorimetric gas sensor, but the amplifier can be accessed from outside to control the voltage gain. An active second-order low pass filter ($f_c \sim 10$ kHz) was also integrated for the microcalorimetric gas sensor to reduce the effect of noise.

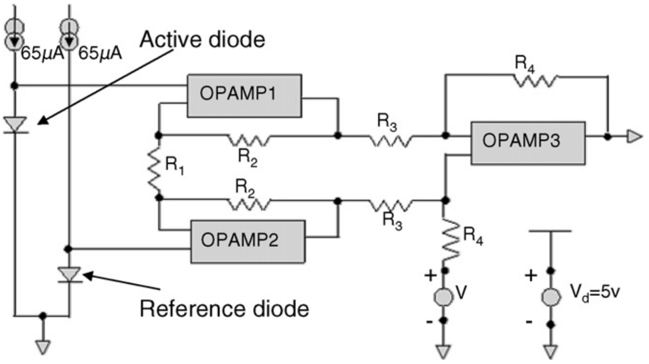


Fig. 4. Instrumentation amplifier circuit for temperature measurement.

Fig. 5 shows photographs of two of our chips, one of which has electronic circuitry integrated with the micro-hotplates. The major components visible are the resistive and calorimetric sensors, large and small micro-heaters, driving and the temperature read-out circuitry. Each 4 mm × 4 mm chip contains 64 pins.

3. Measurements and analysis

The *I–V* characteristics (in Fig. 6(a), large membrane n-type, Fig. 6(b) large membrane p-type) of the MOSFETs show that in the saturation region the drain current decreases with V_{ds} which is due to the degradation of the channel mobility caused by self-heating—this also implies that the silicon substrate was properly back-etched and the thermal isolation was efficient. The parasitic bipolar transistor was triggered at over 40 mW for large heaters and over 17 mW for small heaters, which corresponds to around 600 °C. Hence the devices can be operated reliably below 575 °C. Power measurements were carried out on the same device at five different locations on the 6 in. wafer and also from three different wafers of the same batch, and it was found that the variation in results was less than 2%. This shows the excellent reproducibility and reliability of our fabricated design. Results show that the large heaters can operate above 550 °C with a power consumption of around 36 mW. For small heaters, an operating temperature of 550 °C can be achieved for a power consumption of 16 mW (Fig. 7). To our knowledge this is the smallest DC power consumption reported in the literature. The reason for this low power consumption is the small heater size, large thin membranes (∼6 μm thick, as specified by the foundry) and PECVD nitride as the passivation layer (thermal conductivity of the nitride layer measured ∼3 W/m/K, which is far less compared to LPCVD nitride used in usual practice). In addition, we believe the reason for this high temperature survival of the MOSFET heater is the tungsten metallization, which removes the possibility of electro-migration of aluminium, and the large number of source-body contacts within the MOSFET, which prevents the bipolar effect.

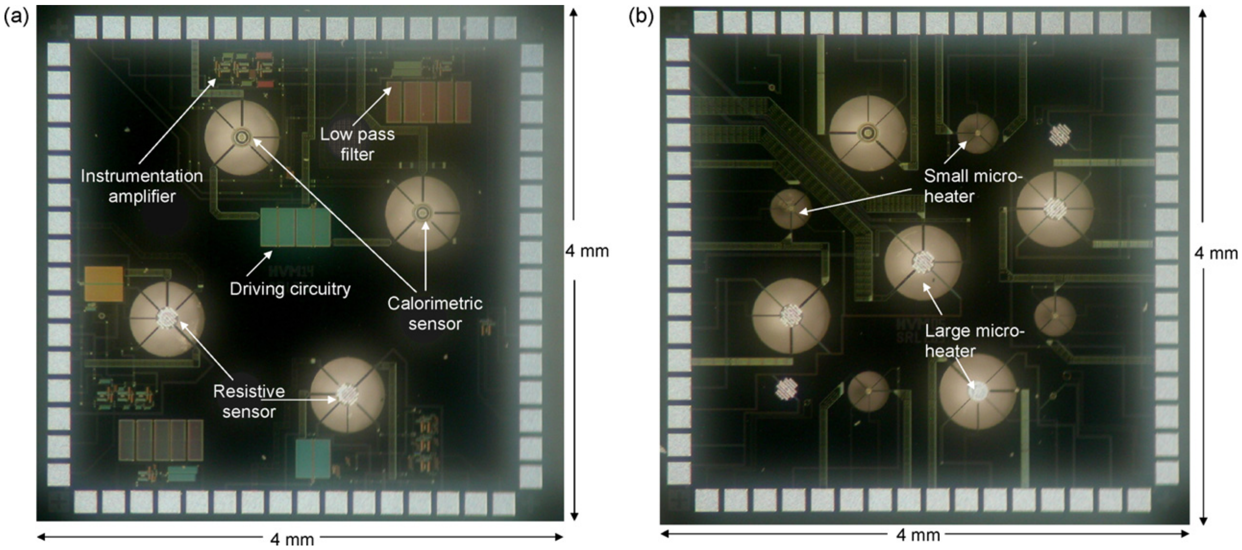


Fig. 5. (a) Photograph of the gas sensor chip with integrated electronics and (b) photograph of the gas sensor chip with discrete micro-hotplate.

Power–temperature measurement of the different sized micro-heaters on the same membrane area shows that the power consumption depends mainly on heater geometries (as shown in Fig. 8). Thus, in order to minimize the power consumption, the heater area should be reduced to an absolute minimum. However this leads to a reduced sensing area and therefore could lower sensitivity.

Thermal calibration of the temperature sensors was also performed so that the membrane peak temperature could be accurately measured. A computer-controlled hot chuck (model:

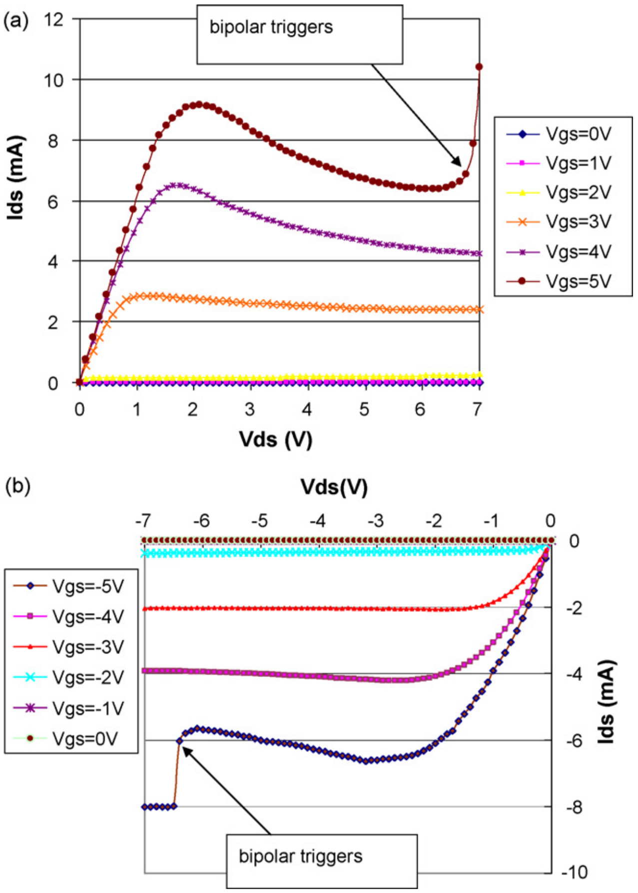


Fig. 6. (a) *I–V* characteristics of large n MOSFET and (b) *I–V* characteristics of large p MOSFET.

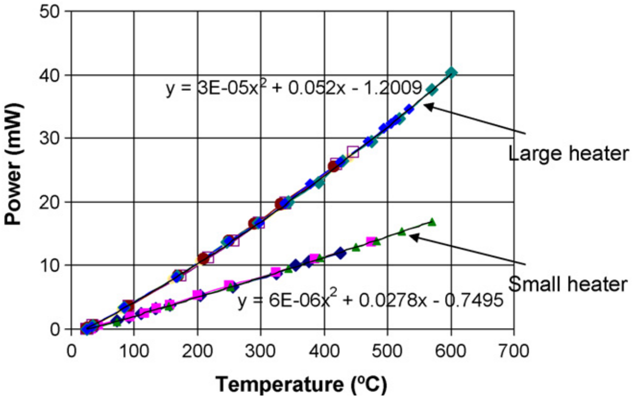


Fig. 7. Power vs. temperature of large and small MOSFET heaters.

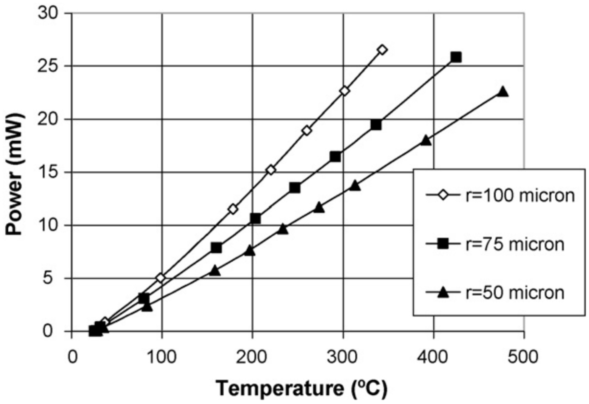


Fig. 8. Power vs. temperature of MOSFET heaters of different radii.

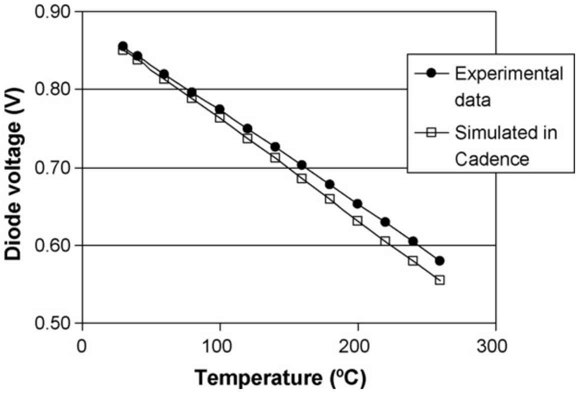


Fig. 9. Calibration of diode temperature sensor.

S-1060R-6TG, make: SEL-TEK Ltd.) with 1 °C resolution was used for this purpose. The corresponding voltage drop was measured with a 20 °C temperature interval up to 260 °C (the upper limit of the hot chuck is 300 °C). The voltage versus temperature curve of the temperature sensor is shown in Fig. 9. These results were compared with the simulated ones obtained from Cadence SPECTRE; also shown in Fig. 9. The simulation was carried out through direct extraction of the components (including parasitic elements) from the layout design and therefore they are quite close to what we have observed experimentally. The temperature coefficient of the diode was measured to be $\sim -1.2 \pm 0.005$ mV/°C when driven by a 65 μA current (number of repetitions: 4).

The peak temperature in the membrane was measured with the aid of the on-chip instrumentation amplifier. Fig. 10 shows the variation of measured instrumentation amplifier voltage with temperature; the ramp was approximately 8 mV/°C. The simulated graph in Cadence SPECTRE is close to that of the experimental result obtained.

Dynamic electro-thermal measurements were carried out to estimate the thermal rise and fall times of the MOSFET micro-hotplates. This was determined by monitoring the voltage response of the thermodiode against time. Fig. 11 shows the diode voltage versus time characteristics of the heater. The transient rise time was calculated by considering the time needed for the temperature to rise from 10% to 90% of the final stabilized voltage. The transient thermal response is very fast—maximum rise time is below 10 ms (at 500 °C).

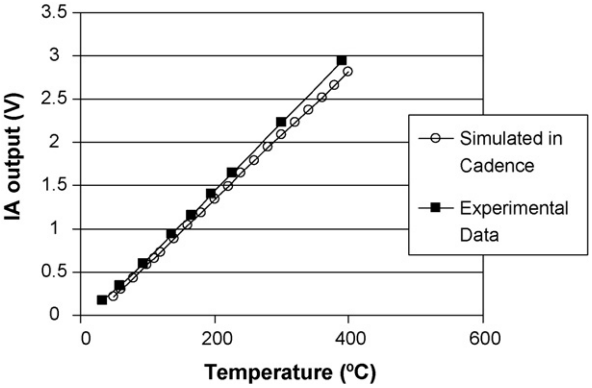


Fig. 10. Instrumentation amplifier output voltage vs. temperature.

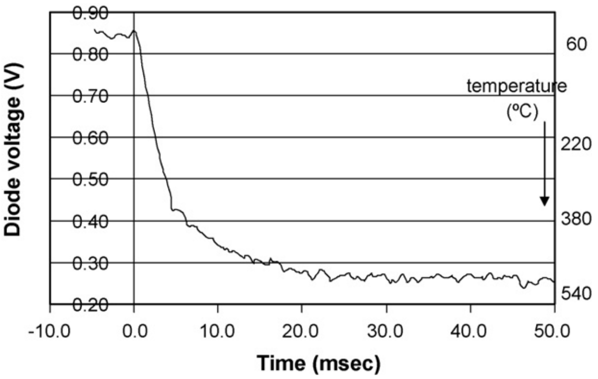


Fig. 11. Transient temperature response of large micro-heater as measured by diode temperature sensor.

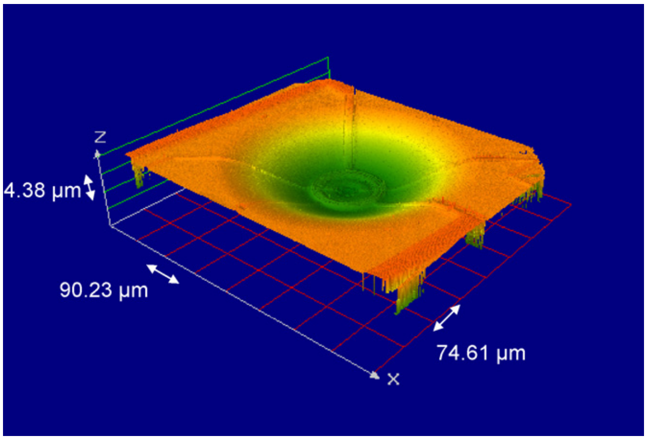


Fig. 12. Height profile of the large micro-hotplate.

The geometrical profile of the membranes was also measured with the help of an optical interferometer (Fogale Nanotech Zoomsurf 3D) to assess the deflection and hence the stress in the membranes. It was found that membrane deflection is very small (under 2%), as shown in Fig. 12; the maximum deflection for large membrane was 8.42 μm and for small membrane was 2.51 μm.

4. Conclusions

Here a new class of novel MOSFET SOI micro-heaters is reported. The design is based on an SOI CMOS process with a deep RIE back-etch, and hence permits the integration of control and signal conditioning circuits on the same chip. We have shown operation at a temperature in excess of 550 °C with nominal power consumption of 36 mW for large heaters and 16 mW for small heaters, and thermal time constants of below 10 ms. To the best of our knowledge this is the first report in the literature where MOSFETs are working (in this case as a heater) beyond 550 °C and with such lower power consumption.

We believe that the development of such low-power CMOS sensors will lead to the development of a new generation of low cost, low-power gas sensors.

Acknowledgements

The work was partly supported by the Ministry of Information and Communication, Republic of Korea, under the project no. A1100-0501-0073. Dr. Udrea acknowledges the award of the Philip Leverhulme Prize.

References

[1] J.W. Gardner, V.K. Varadan, O.O. Awadelkarim, Microsensors MEMS and Smart Devices, Wiley, Chichester, 2001, p. 283.

[2] E. Jones, in: P.T. Moseley, B.C. Tofield (Eds.), Solid State Gas Sensors, Adam Hilger, Bristol, 1987, pp. 17–31.

[3] P. Kerbs, A. Grisel, A low power integrated catalytic gas sensor, Sens. Actuator B 13 (1993) 155–158.

[4] A. Pike, J.W. Gardner, Thermal modelling and characterization of micropower chemoresistive silicon sensors, Sens. Actuator B 45 (1997) 19–26.

[5] J.S. Suehle, R.E. Cavicchi, M. Gaitan, S. Semancik, Tin oxide gas sensor fabricated using CMOS micro-hotplates and in situ processing, IEEE Electron Dev. Lett. 14 (3) (1993) 118–120.

[6] J. Laconte, C. Dupont, D. Flandre, J.P. Raskin, SOI CMOS compatible low-power microheater optimization for the fabrication of smart gas sensors, IEEE Sens. J. 4 (2004) 670–680.

[7] F. Udrea, J.W. Gardner, Smart MOSFET gas sensor, British Patent GB2321336A, November 1996 and World Patent WO98/32009.

[8] J.W. Gardner, F. Udrea, W.I. Milne, Numerical simulation of a new generation of high-temperature, micropower gas and odour sensors based on SOI technology, in: Proceedings of the SPIE Smart Electronics and MEMs, Newport Beach, USA, March 1–5, 1999, pp. 104–112.

[9] F. Udrea, J.W. Gardner, D. Setiadi, J.A. Covington, T. Dogaru, C.C. Lu, W.I. Milne, Sens. Actuator B 78 (2001) 180–190.

[10] D. Barrettino, M. Graf, W.H. Song, K. Kirstein, A. Hierlemann, H. Baltes, Hotplate-based monolithic CMOS microsystems for gas detection and material characterization for operating temperatures up to 500 °C, IEEE J. Solid-State Circuits 39 (7) (2004) 1202–1207.

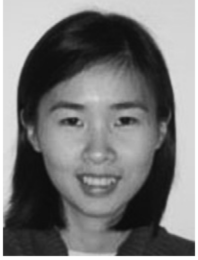
[11] D. Briand, B. van der Schoot, N.F. de Rooij, H. Sundgren, I. Lundstrom, A low-power micromachined MOSFET gas sensor, J. Microelectromech. Syst. 9 (2000) 303–307.

[12] To be communicated in IEDM 2007.

Biographies

Prasanta Kumar Guha is a final year PhD student in Department of Engineering, University of Cambridge, UK. He has a BSc (Hons) degree in physics and a BTech degree in ‘radiophysics and electronics’ from the University of Calcutta, India. He obtained his MPhil degree from Microelectronic Research Center, University of Cambridge, UK, in the year 2003. His research interest includes the design of micro-hotplates for smart sensor and analog and mixed signal circuitry for sensor integration.

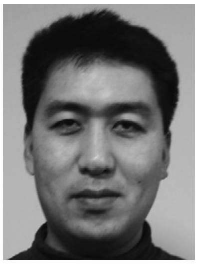
Syed Zeeshan Ali graduated from GIK Institute (Pakistan) in 2003 with a BS in electronic engineering. Since then he has been pursuing a PhD at the University of Cambridge (UK) focusing on the design of micro-hotplates for smart gas sensors, and electro-thermal modelling of power devices.



Cerdin Lee is currently an MSc student of electronics engineering at Cambridge University. Her research focus is on 700V LIGBT power devices. She has over 9 years of working experience in the semiconductor industry prior to MSc study. Her experience includes power device design, mixed signal product engineering and deep sub-micron process development.

Florin Udrea received an MSc degree in microelectronics from the Politehnica University of Bucharest, Bucharest Romania, in 1991, a second masters in smart sensors from the University of Warwick, UK, in 1992 and a PhD degree in power devices from the University of Cambridge, Cambridge, UK, in 1995. Since October 1998, he has been a reader with the Department of Engineering, University of Cambridge, UK. He was an advanced EPSRC Research Fellow from August 1998 to July 2003 and, prior to this, a College Fellow in Girton College, University of Cambridge. He is currently leading a research group in power semiconductor devices and solid-state sensors that has won an international reputation during the last 10 years. In August 2000, he cofounded, with Prof. G. Amaratunga, Cambridge Semiconductor (CamSemi), Cambridge, UK, a start-up company in the field of power integrated circuits, where he is currently the Technical Director. He published over 150 papers in journals and international conferences. He holds 22 patents in power semiconductor devices and sensors. Dr. Udrea won six Best Paper Awards as first author in IEEE international conferences.

Bill Milne is a director of the Centre for Advanced Photonics and Electronics (CAPE) and has been head of Electrical Engineering at Cambridge University since 1999 and head of the Electronic Devices and Materials Group since 1996 when he was appointed to the “1944 Chair in Electrical Engineering”. His research interests include large area Si and carbon-based electronics, thin film materials and, most recently, MEMS and carbon nanotubes and other 1D structures for electronic applications. He collaborates with various companies including Dow-Corning, ALPS, Thales, Advance Nanotech, Philips and FEI and is also currently involved in five EU projects and several UK Government funded EPSRC projects and has recently become involved in a major collaboration with ETRI (South Korea) for work on biosensors. He has published/presented ∼550 papers in these areas, of which ∼100 were invited. He is the Chairman of Cambridge Nano-Instruments an SME based in Cambridge, sits on the Advisory Board for IGNIS, a Canadian start-up company and he also sits on the Board of Dataslide as a non-executive director.



Takao Iwaki received his BSc and MSc degrees in physics from Tokyo University in 1995 and 1997, respectively. He is currently in the final year of his PhD at Warwick University. His research interests include gas sensors and microsystem technology. He is a member of the Institute of Electrical Engineers of Japan (IEEJ).

James Covington is presently an associate professor in the School of Engineering at the University of Warwick. He received his BEng 1996 in electronic engineering and remained there receiving his PhD 2000. His PhD was on the development of CMOS and SOI CMOS gas sensors for room temperature and high temperature operation. He worked as a research fellow for both Warwick University and Cambridge University on the development of gas and chemical sensors and was appointment as a lecturer in 2002. Current research interests focus on the development of silicon devices with novel materials using CMOS and SOI ASIC technology (nose-on-a-chip), and biologically inspired neuromorphic devices with applications based on environmental and biomedical engineering.

Julian Gardner is professor of electronic engineering in the School of Engineering at Warwick University. He is an author or co-author of over 350 technical papers and patents as well as six technical books in the area of microsensors and machine olfaction. He is a series editor for a book series by Wiley–VCH. He is a fellow of the IEE, IOP and Royal Academy of Engineering and senior member of the IEEE and serves on several advisory panels on sensors, e.g. for EPSRC, DTI and IEE Professional Network on Microsystems and Nanotechnology. His research interests include the modelling of silicon microsensors, chemical sensor array devices, biomimetic MEMS devices and electronic noses. He has worked with over 20 companies in the past 15 years developing commercial e-nose instruments and a consultant for various companies.