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Multi-field simulations and characterization of CMOS-MEMS high-temperature smart gas sensors based on SOI technology

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Abstract

This paper describes multiple field-coupled simulations and device characterization of fully CMOS-MEMS-compatible smart gas sensors. The sensor structure is designated for gas/vapour detection at high temperatures (>300 °C) with low power consumption, high sensitivity and competent mechanic robustness employing the silicon-on-insulator (SOI) wafer technology, CMOS process and micromachining techniques. The smart gas sensor features micro-heaters using p-type MOSFETs or polysilicon resistors and differentially transducing circuits for *in situ* temperature measurement. Physical models and 3D electro-thermo-mechanical simulations of the SOI micro-hotplate induced by Joule, self-heating, mechanic stress and piezoresistive effects are provided. The electro-thermal effect initiates and thus affects electronic and mechanical characteristics of the sensor devices at high temperatures. Experiments on variation and characterization of micro-heater resistance, power consumption, thermal imaging, deformation interferometry and dynamic thermal response of the SOI micro-hotplate have been presented and discussed. The full integration of the smart gas sensor with automatically temperature-reading ICs demonstrates the lowest power consumption of 57 mW at 300 °C and fast thermal response of 10 ms.

1. Introduction

Major types of high-temperature solid-state sensors, such as chemoresistive and calorimetric devices that can detect combustible or hazardous gases, have been developed for decades due to their simplicity and good sensitivity. However, these types of devices are prone to several problems, e.g. poor reproducibility of device characteristics, low specificity to the target gases/vapours and relatively high production cost because of labour-extensive manufacturing methods. The heater, usually a platinum resistive coil embedded in the sensor, is used as a heating element and a temperature sensor. These two classes of gas sensors operate at high temperatures between 300 °C and 500 °C to enhance sensing sensitivity; nevertheless, the operation usually results in massive power consumption [1], which is very disadvantageous to the emerging requirement of handheld systems. The development of silicon-based chemoresistive devices using oxide/nitride membranes, referred to as micro-hotplates, was continuously studied [2–4]. This sort of sensors enabled a lower power consumption level under hundreds of milliwatts at 500 °C due to the removal of massive thermal mass beneath the

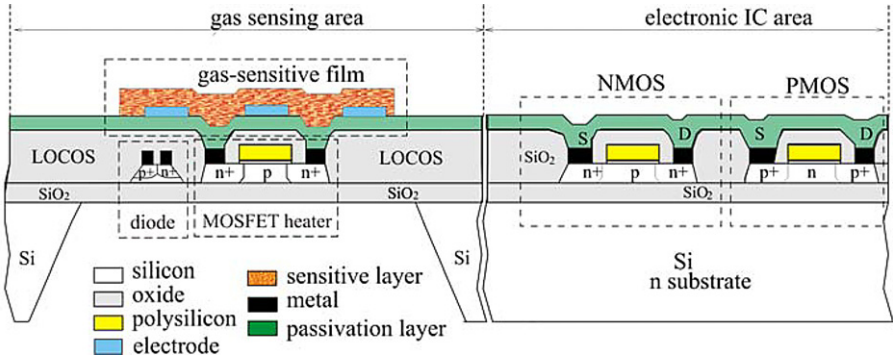


Figure 1. The schematic cross-section of an SOI chemoresistive gas sensor using the partially-depleted MOSFET heater (reprinted from [10], © 2001, with permission from Elsevier).

membrane. In addition, Pd-gate MOSFETs were successfully demonstrated as hydrogen gas sensors in 1975 and introduced MOS devices to chemical sensors for the first time [5].

To date, compared with multi-chip solutions, the monolithic integration of micro-hotplate gas sensors and CMOS transducing circuitry offers significant advantages such as low power consumption, high sensitivity, dynamic operation, miniaturized size and low fabrication cost due to the CMOS standard process. Relevant research includes CMOS-compatible sensors design and fabrication without circuit implementation [6, 7]; demonstration of a MOSFET gas sensor structured on a nitride membrane with a silicon plug underneath [8]; comprehensive design and simulations of the gas sensor and on-chip temperature transducing circuits employing SOI MOSFET micro-heaters and micro-hotplates [9–11], which were constantly reported by some authors of this paper. Afterwards, a number of studies on the monolithic integration of CMOS micro-hotplate gas sensors or micro-system array have been intensively implemented and characterized [12–18]. All the achieved efforts so far have enhanced sensor functionality and completed single-chip system integration to a new standard of next-generation gas sensing devices and hence anticipating emerging industrial and commercial applications in the future. Although most of the sensors mentioned above have made great progress, full CMOS manufacturability is still a challenge. For instance, the deposition of platinum heaters remains CMOS incompatible and this can reduce benefits from the low cost of CMOS fabrication and circuit integration.

With rising success of micro-electro-mechanical systems (MEMS) and SOI technologies, novel classes of smart sensors combining MEMS and full SOI CMOS technologies become highly prospective. These smart sensors can be implemented by using MOSFETs or polysilicon as micro-heaters, which are embedded in the SOI thin membrane after the post-CMOS micromachining process. Conventional MOSFET-based devices and integrated circuitry using the standard bulk silicon process can only operate under 200 °C, above which junction breakdown tends to cause poor stability. Since 1990s SOI wafer technology has been considered a promising candidate to sort out this application limitation. SOI devices are believed to allow higher operation temperatures and consume less power than conventional ICs, mainly because of their low leakage currents, abridged parasitic capacitances, reduced short-channel effect and high breakdown voltage [19]. But, one negative factor that limits the use of SOI technology to spread is the high cost of SOI wafers. Another disadvantage of SOI technology in CMOS or power applications is the poor thermal conductivity of the buried oxide layer, leading to a high temperature build-up inside the device. However, this disadvantage develops into an essential requirement to high-temperature gas sensors. As a result, the proposed SOI CMOS gas sensor platform can not only offer full CMOS compatibility, but also give promising potential of high-volume and low-cost production, and more importantly, the systems-on-chip (SOC) integration.

This paper primarily introduces more detailed results concerning interdisciplinary simulations and device characterization of the SOI CMOS smart gas sensors that was earlier proposed in [9, 10] with the similar design concept, featuring both chemoresistive and microcalorimetric high-temperature operation modes. Investigations into the concept of the designed sensors, sensing elements, transducing circuits and fabrication process are first provided, followed by device modelling in microelectronics, thermal transport and membrane mechanics. Furthermore, 3D coupled-effect simulations and device characterization are discussed. Comparisons of simulations and experimental results are also made and concluding remarks provided.

2. SOI CMOS smart sensors

2.1. Design

The CMOS micro-heaters, including MOSFETs and polysilicon resistors, are embedded within the silicon thin film of an SOI membrane and hence form a micro-hotplate based on electroresistive and self-heating effects. Gold or aluminium electrodes interface these micro-heaters with gas-sensing materials that are deposited onto the heating area. Various designs of heaters can be placed in or near the central area of the 500 μm $\times$ 500 μm square membrane. This new concept derives into two smart sensor structures, i.e., the chemoresistor, as illustrated in figure 1, and the microcalorimeters (micropellistors). The insulating layer of buried oxide in the SOI substrate serves a dual purpose: (1) it

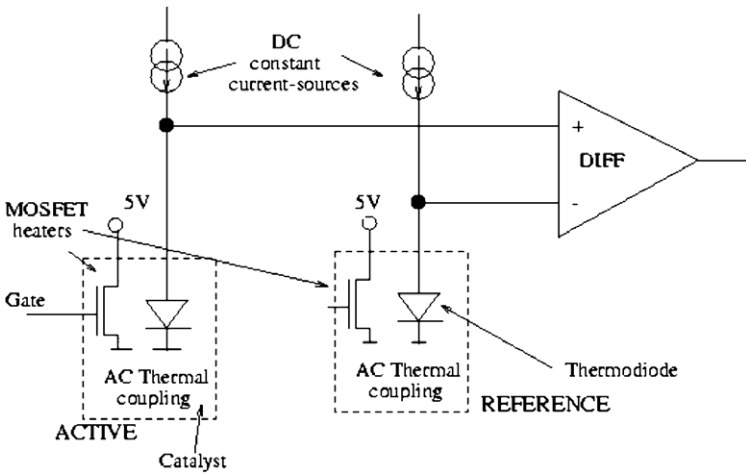


Figure 2. The differentially transducing circuits for SOI temperature read-out featuring one active and another reference sensor, both including a thermodiode on membrane or off membrane (reprinted from [10], © 2001, with permission from Elsevier).

provides a high degree of electrical isolation with associated IC areas, enabling reducing thermal interference and providing low parasitic capacitance; (2) it acts as an effective etch stop in the post-CMOS etching process and vertically isolates thermal dissipation from the heater area at high operating temperatures.

Moreover, CMOS temperature sensors such as diodes and spreading resistors are manufactured in the SOI membrane to determine operation temperatures. As a result, the heaters and temperature sensors can become fully integrated with the on-chip drive/conditioning/control electronics. For effective lateral isolation, multiple oxide trenches of 10 μm wide and 10 μm apart or local oxidation of silicon (LOCOS) are readily available in the CMOS process. These structures have been employed around MOSFET heaters for both electrical and thermal isolation due to their low thermal conductivity.

Polysilicon heaters are 12 μm $\times$ 1250 μm in size with a typical resistance of 232 Ω at room temperature. MOSFET heaters feature an interdigitated design with four p-type MOSFET strips in parallel, which are equipped with simple temperature control of the micro-hotplate via the gate voltage [10]. PMOSFET heater dimensions were 12 μm $\times$ 640 μm and an 18 μm gap has been designed for the placement of both types of temperature sensors. For smart determination of temperature difference, two amplifier circuits designated for chemoresistive and microalorimetric configurations have been implemented for each pair of micro-heaters. The former amplifier measures the differential temperature between an on-membrane heater and an on-substrate heater with a gain of 5, while the latter one amplifies the temperature rise between two on-membrane heaters with a gain of 40, as illustrated in figure 2. More detailed measurement data are given in section 4.2. The analogue circuit simulation was verified by utilizing the Spectre-S module from Cadence.

2.2. Fabrication

These smart sensors were fabricated via the 0.8 μm BiCMOS process through the Europractice program. Chips are 5.2 mm $\times$ 4.2 mm in size with four micro-heaters on the membrane and two reference replicates on the bulk substrate. The removal of bulk substrate to form a membrane structure was carried out after the BiCMOS process by the wet etching process using improved tetramethyl ammonium hydroxide (TMAH) solutions that could perform high selectivity to aluminium electrodes and bonding pads. The CMOS-compatible anisotropic etchant was 5 wt% TMAH, 1.6 wt% pure silicon powder and 0.6 wt% $(NH_4)_2S_2O_8$, which was formulated in [20] and the experiment lasted for 15–18 h etch at a temperature of 80 °C. The fabricated sensors demonstrated fair yield ($\sim$56%) of production mainly because the SOI wafer would be separated into small chips before the wet etching process. Besides, it was also attributed to the very rough back surface of the SOI wafer. Nevertheless, this issue can be further managed by utilizing the full wafer-level process and double-polished SOI wafers.

For chemoresistive sensors, interdigitated aluminium electrodes are made of three arms of the top (metal 2) layer for top deposition of gas-sensitive thin films such as SnO_2, WO_3 or nano-scale films; for microcalorimetric sensors, palladium (Pd) was deposited on electrodes to promote chemical combustion and absorb minor release of calories. Figure 3 depicts a micro-fabricated SOI chip without deposition of the gas-sensitive material.

3. Device modelling

3.1. Negative resistance and thermal transport in SOI MOSFETs

Silicon devices working at elevated power densities have been known to exhibit negative resistance in their *I–V* characteristics. This effect present in the saturation region of a MOS power transistor was initially reported by authors in the literature [21, 22]. It was pointed out that decreased drain currents at increased temperatures can be obtained by

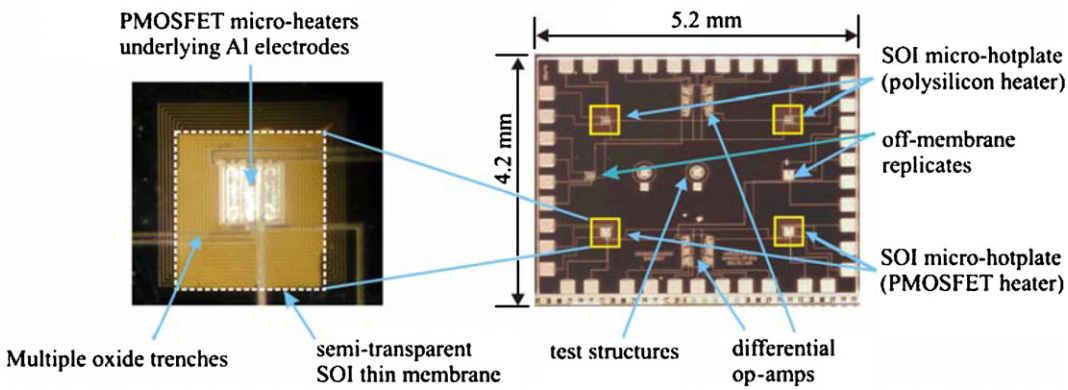


Figure 3. Micrographs of the back-etched sensor chip integrating four SOI micro-hotplates with analogue circuits.

thermal variation of the channel mobility. The temperature dependence of effective carrier mobility can be expressed as

$$\mu_{\text{eff}} = \mu_0 \left(\frac{T_0}{T}\right)^k, \tag{1}$$

where k is a property constant depending on materials between 0.5 and 2. It is considered as 1.5 for silicon. T is the operating temperature and μ_0 is the carrier mobility at room temperature T_0.

For SOI transistors, it was reported that a more significant increase in lattice temperature occurs in the channel of the SOI transistor due to the presence of the buried insulator [23, 24]. The pinch-off point is shifted at small channel lengths and the kink effect is reduced by increasing the gate voltage, both of which were caused by a temperature increase in the channel due to poor heat dissipation through the buried oxide layer, thus resulting in effective conservation of heat flow produced from MOSFET channels. The temperature may severely rise within the SOI film on account of the electroresistive effect and the first-order heat diffusion equation that was reported in [10] before:

$$\nabla \cdot (\sigma(T)\nabla\psi) = 0 \tag{2}$$

$$\nabla \cdot (\kappa(T)\,\nabla\,\mathrm{T}) + \left(\frac{J^2}{\sigma(T)}\right) = 0, \tag{3}$$

where ψ is the applied bias and $\sigma(T)$ is the temperature-dependent electrical conductivity, $\kappa(T)$ is the temperature-dependent thermal conductivity of the material(s) and J is equal to $-\sigma(T)\nabla\psi$, denoting the electrical current density. In fact, conduction and convection are two major heat transport mechanisms in SOI sensors and radiation effect can be ignored while operation temperatures are below 400 °C. In a steady-state case, the electrical power generation in an SOI MOSFET gas sensor is thermally dissipated via the membrane and surrounding atmosphere. The classical heat transfer rate q_a for free convection is defined as

$$q_a = h_a A\,(T_H - T_a)\,, \tag{4}$$

where h_a is the heat-transfer coefficient, A is the surface area and $T_H - T_a$ is the temperature difference between the heater and ambient temperature. Later, Pike and Gardner [25] developed a steady-state expression of power losses in a thin diaphragm experimentally by measuring the power consumption in still air and a vacuum pressure of 10^{-5} Torr. The experimental results were shown that the conductive term is well described by a first-order expression and the convective term by a second-order polynomial model.

3.2. Mechanics

Stresses and deflections of the smart devices are mainly induced by the significant thermal expansion and fabrication process. According to the classic plate and shell theory [26], the maximum stress in a membrane is a function dependent on the aspect ratio of membrane geometry. Furthermore, the Rankine (or maximum normal stress) criterion is employed as it holds well for brittle materials such as single-crystal silicon and oxide in the SOI structure.

More importantly, thermal stress induced by multi-layer thermal mismatch at high temperatures within the heating area of the membrane is of more concern than stresses distributed in others. For example, considering the thermal effect in a composite membrane with expansion coefficients α_s for silicon and α_o for oxide, we assume that the temperature difference ΔT_m between the upper and lower surfaces in the membrane is a function of the z-coordinate. Let us consider a thin composite membrane bent to a spherical surface due to uniform heating. Assuming the variation of temperature across the thickness of the plate follows a linear distribution and all membrane edges clamped, the heating process will produce bending moments distributed along the edges of the plate and a maximum thermal stress as [26]

$$(\sigma_T)_{\max} = \frac{-(\alpha_s - \alpha_o)E_{\text{eff}}\,\Delta T_m}{2(1-\nu)}, \qquad E_{\text{eff}} = \frac{E_1 h_1 + E_2 h_2}{h_1 + h_2} \tag{5}$$

where ν is Poisson's ratio for the membrane. Therefore, it is obvious that thermal stresses in a membrane increase with total membrane thickness (particularly in a thick-membrane case), individual expansion coefficients and effective Young's modulus.

Besides, for CMOS and MEMS devices, significant intrinsic stresses arise from the thin film process of stacked

Table 1. Some residual stresses reported in thin films. The stress unit is MPa.

Films	Sze [28]	Tabata *et al* [29]	Maier-Schneider [27]	Tait [30]	Bourounia [31]
Poly Si	–	−180 (LPCVD)	−440	–	–
Si	–	–	–	30	65 (p+ Si)
SiO_2	−300–300	–	–	–	–
Si_3N_4	−200–1000	1000 (LPCVD) 110 (PECVD)	600–1100	380	–

layers on the silicon substrate due to lattice mismatch. Relevant problems include crack propagation, delamination in composite films and substrate bowing. The load–deflection technique based on strain energy and virtual displacement approaches explains the analytic relationship for a single-layer, rectangular membrane as follows [26]:

$$q = \frac{C_1 \sigma_r h d}{a^2} + \frac{C_2 E h d^3}{a^4}, \tag{6}$$

where q is the applied load, σ_r is the residual stress, E is the Young's modulus, h is the membrane thickness and d is the membrane deflection. C_1 and C_2 constants are mainly determined by the membrane geometric factor and Poisson's ratio ν. For a double-layer membrane with thickness h_1 and h_2, if under a tensile stress, the effective residual stress can be modelled as [27]

$$(\sigma_r)_{\text{eff}} = \frac{(\sigma_r)_1 h_1 + (\sigma_r)_2 h_2}{h_1 + h_2}. \tag{7}$$

Table 1 exhibits experimentally determined residual stresses for thin films in published papers. It is noted that quantities of residual stress are greatly process and temperature dependent.

3.3. Piezoresistive and piezojunction effects

Piezoresistivity is a linear coupling between stresses and electrical resistivity, first reported by Smith due to the investigation of the piezoresistance properties of silicon and germanium [32]. Further, the piezojunction effect was reported by Hall *et al* in relation to the hydrostatic pressure on silicon pn-junctions [33]. Piezojunction effect is based on the change of the bandgap and the modification of the effective mass of charge carriers. The band widening affects the carrier mobility, the doping concentration and thus the electrical conductivity. This property is generally represented by a fourth rank tensor Π_{ijkl} and stress X_{kl} formulated as follows:

$$\frac{\delta \rho_{ij}}{\rho_0} = \Pi_{ijkl} X_{kl}, \qquad i, j, k, l = 1, 2, 3. \tag{8}$$

When the longitudinal and transverse components of a stress (tensile or compressive) applied to piezoresistive materials, the relative change in resistivity due to the stresses is mainly given by

$$\frac{\delta \rho}{\rho_0} = \pi_L \sigma_L + \pi_T \sigma_T, \tag{9}$$

where π_L and π_T are the longitudinal and transverse components of the piezoresistive coefficients, and σ_L and σ_T are the corresponding stress components. The coefficients π_L and π_T are dependent on the type of conductivity, crystalline orientation and doping concentration of the semiconductor.

The piezoresistive coefficients generally describe the conductivity change of a resistor, whereas the piezojunction coefficients account for the saturation current modification of a transistor. In addition, the effects are very anisotropic with the orientations of stresses and applied current. According to Creemer's work [34], under the maximum stress of ±200 MPa, a resistance change of ±6% in the resistor and saturation current variation of 16% and −12% under the maximum compressive and tensile stress, respectively, in the npn transistor were observed.

4. Simulation and characterization of SOI micro-hotplates

4.1. Simulation results

Multi-domain simulations were performed using the SOLIDIS module of ISE-TCAD® simulation systems, which provides a finite-element analysis (FEA) tool for 3D MEMS structures. Main variables such as the membrane length l, silicon thickness t_s, buried oxide thickness t_{box} and the total membrane thickness h are modulated for different designs. The following thermal boundary conditions are assumed: (1) the temperature along the bottom side of the silicon wafer is at ambient temperature of 300 K and (2) on the upper and bottom side of the membrane heat is dissipated through convective exchange with air. In addition, mechanical boundary conditions are (1) edges of the membrane and the bottom side of the substrate are fixed (or clamped) and (2) the temperature along the bottom side of the wafer is given by ambient temperature. The heat transfer coefficient for the upper surface of the membrane is set to 125 W m^{-2} K^{-1}, while for the lower surface, 60 W m^{-2} K^{-1} under a free convection assumption [10]. In addition, the piezoresistive coefficients for silicon and polysilicon are also introduced into the modelling process. Useful geometrical data of the MOSFET and the sensor structure employed in simulations are provided in table 2.

CMOS micro-heaters include various designs in square, meander and interdigitated with gap (25 μm). Our simulated results show that the design of interdigitated with gap has superior thermal uniformity with a maximum thermal difference of 8 K over the active area of membrane. The vertical temperature gradient across the membrane is achieved within 4 K only. 3D simulations for SOI micro-hotplate were performed to investigate corresponding thermal profiles and the maximum operating temperature. Given a power consumption of 50 mW, the thermal profiles demonstrated on the bulk SOI substrate are shown in figure 4(*a*), on an SOI membrane without the isolation structure in figure 4(*b*), on an SOI membrane with multiple oxide trenches

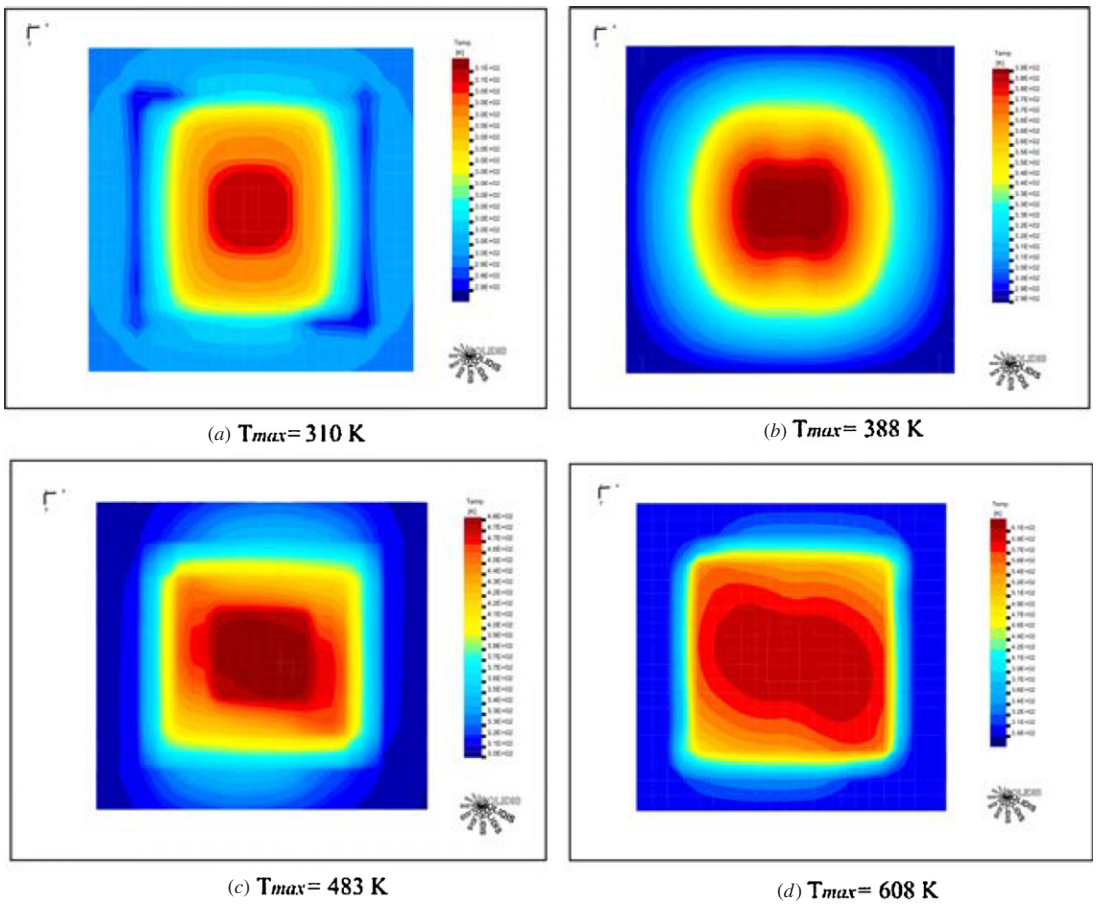


Figure 4. Various thermal profiles for an interdigitated design in the (*a*) SOI substrate without a membrane, (*b*) SOI membrane without isolation, (*c*) SOI membrane with multiple oxide trenches and (*d*) SOI membrane with LOCOS isolation.

Table 2. A geometrical data sample for the MOSFET and sensor simulations.

Description	Value
Silicon (SOI) film thickness (nm)	1200
Buried oxide film thickness (nm)	610
Gate oxide thickness (nm)	17.5
Oxide thickness (polysilicon–metal 1) (nm)	700
Oxide thickness (metal 1–metal 2) (nm)	1200
Polysilicon thickness (nm)	500
Metal 1 thickness (nm)	740
Metal 2 thickness (nm)	1050
Passivation thickness (nm)	1800
Substrate thickness (μm)	500
Tin oxide thickness (μm)	10
Gas sensitive (active) area	200 μm × 200 μm
CMOS heater area	200 μm × 200 μm
Membrane area	500 μm × 500 μm

in figure 4(*c*) and on an SOI membrane with LOCOS isolation are shown in figure 4(*d*), respectively. As can be seen, it is evident that the combination of the SOI membrane and LOCOS is the most effective in raising the operation temperatures by significantly reducing the conductive heat loss; however, significant compressive stress may be produced in the LOCOS structure and thus the membrane can be heavily buckled. To compromise this issue, the multiple shallow trench isolation is a good trade-off to make a satisfactory micro-hotplate possible.

The thickness of the SOI membrane, in general, has major impact on power dissipation of the membrane despite the presence of LOCOS or trench isolations. As shown in figure 5, the membrane with a smaller l/h aspect ratio results in higher power consumption for the same temperature rise and there exists increasing variation between curves with different aspect ratios. Moreover, the thermal flow is also influenced by the vertical composition of the SOI membrane. Our simulated results proved that a thinner silicon film above buried oxide layer helps reduce power losses. Figure 6 depicts the power consumption versus operating temperature with respect to the SOI thickness ratio (t_{box}/t_{si}) of buried oxide to the silicon film while the membrane aspect ratio stayed constant. Compared with these results, altering the SOI thickness ratio t_{box}/t_{si} is less dominant on power consumption than the modulating aspect ratio l/h; however, the former can be useful for further modulation when necessary. These simulations indicate the consequence of thermoelectrical power reduction while selecting appropriate specifications of SOI micro-hotplates. Furthermore, it has been known SiO_2 is a more brittle material than silicon and may introduce significant compressive stress

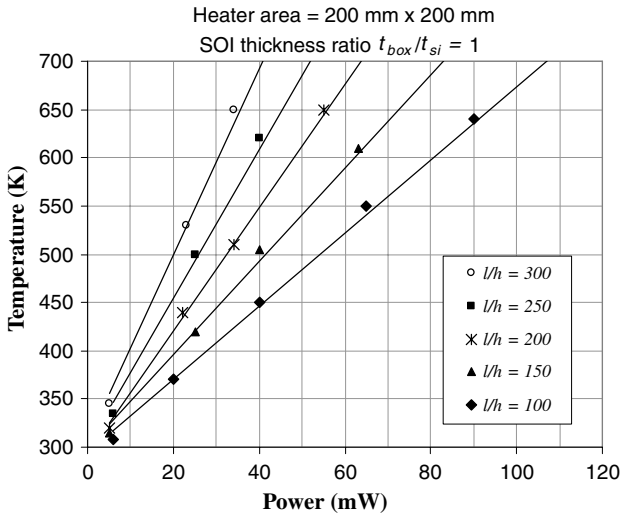


Figure 5. Simulated results of power consumption versus operating temperature with different SOI membrane aspect ratios.

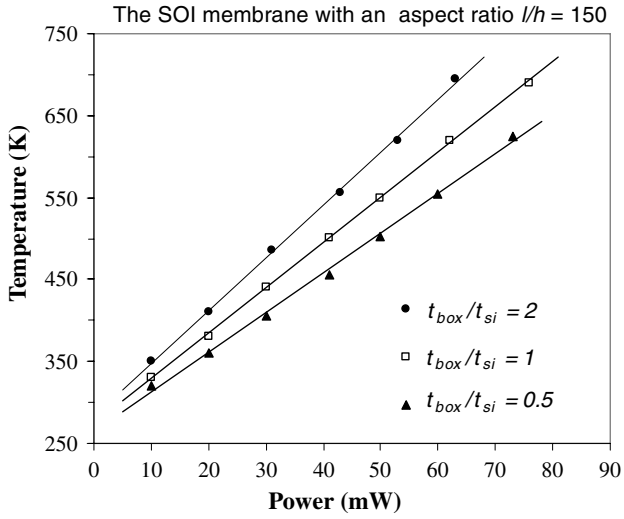


Figure 6. Lattice temperature versus power consumption for FET heaters with various buried oxide/silicon thickness ratios.

into the membrane causing a buckled surface. Ideally, the thicker membrane with a smaller l/h value possesses higher mechanical stability and resists more deformation, but this will increase power consumption. It is noteworthy that the thermal stress induced from the elevated temperature is not only intensified by the vertical thermal gradient across the membrane, but also dominated by the thermal expansion mismatch due to the multi-layer configuration, including aluminium metal tracks and sensitive-material deposition.

In addition, the influence of the membrane thickness ratio t_{box}/t_{si} on membrane stress analysis was investigated and shown in figure 7. A clear trend suggests the maximum stress rises with an increasing membrane thickness ratio, especially evident above 400 K. It can be justified that a larger thickness ratio, which means a thinner layer of Si in the SOI membrane, may result in the significant decrease of the effective Young's

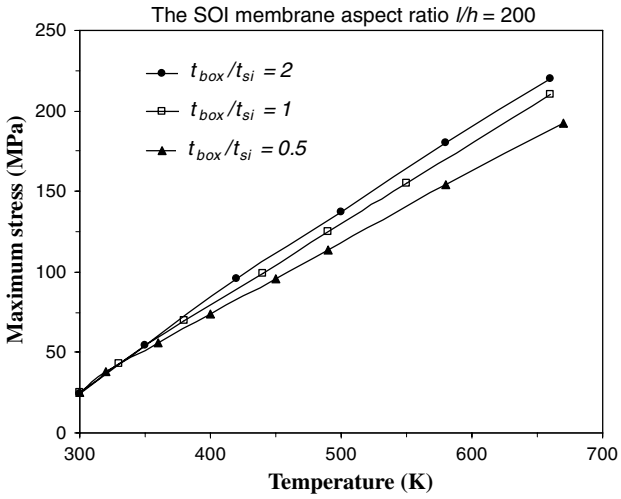


Figure 7. Temperature versus maximum stress for FET heaters with various SOI thickness ratios.

modulus ranging between those of the Si film (190 GPa) and the SiO_2 layer (80 GPa), as previously expressed in equation (5). In this case, the change of the effective Young's modulus dominates, thus exhibiting elevated maximum stress, and vice versa.

It was also intriguing to examine critical stresses over the membrane and find out where the weak points are in the SOI membrane. For instance, locations such as clamped edges, the interface between silicon film and LOCOS corners around micro-heaters and aluminium electrodes sputtered on the passivation layer are vital to the device operation and lifespan. Table 3 summarize the relevant simulation results. Knowing that the failure stress of Si is 6.9 GPa, these calculated stresses indicate that proficient membrane robustness can be achieved. However, it is notable that film defects resulting from fabrication steps, such as pinholes and cracks, are very possible to reduce membrane strength and operation lifetime, causing an impact on the reliability issue.

4.2. Static and dynamic device characterization

MOSFET output and polysilicon resistive characteristics were investigated for both devices on the SOI substrate (before wet etching) and SOI membrane (after wet etching), as shown in figure 8. The grey *I–V* curves denoting FETs on SOI membranes obviously depart from the dark curves for the devices on the SOI substrate, and saturation currents decline with the increasing applied source–drain bias. These examples account for the total combination of the degradation of carrier mobility mainly due to a quick temperature rise in the membrane caused by self-heating and the change of silicon conductivity caused by developed stresses within the membrane. The results are not unexpected since MOSFETs built on the membrane exhibit significant reduction in source–drain current compared to those on the substrate, thus restraining the kink effect which is often shown in substrate devices. Besides, improved protection against the parasitic bipolar turn-on in SOI devices is also expected. We foresee

Table 3. Special investigations into some critical regions of the membrane. These data were extracted from a simulated example with $l/h = 200$, $t_{box}/t_{si} = 0.5$ and temperature = 590 K.

	Stresses		
Locations	Max. stress (MPa)	Rankine stress (MPa)	Max. deflection (μm)
Clamped membrane edge	850	302	$\approx$0
Si interface with LOCOS corners	510	125	7.0
SOI silicon film	985	530	9.3
Al electrodes	1100	448	9.3

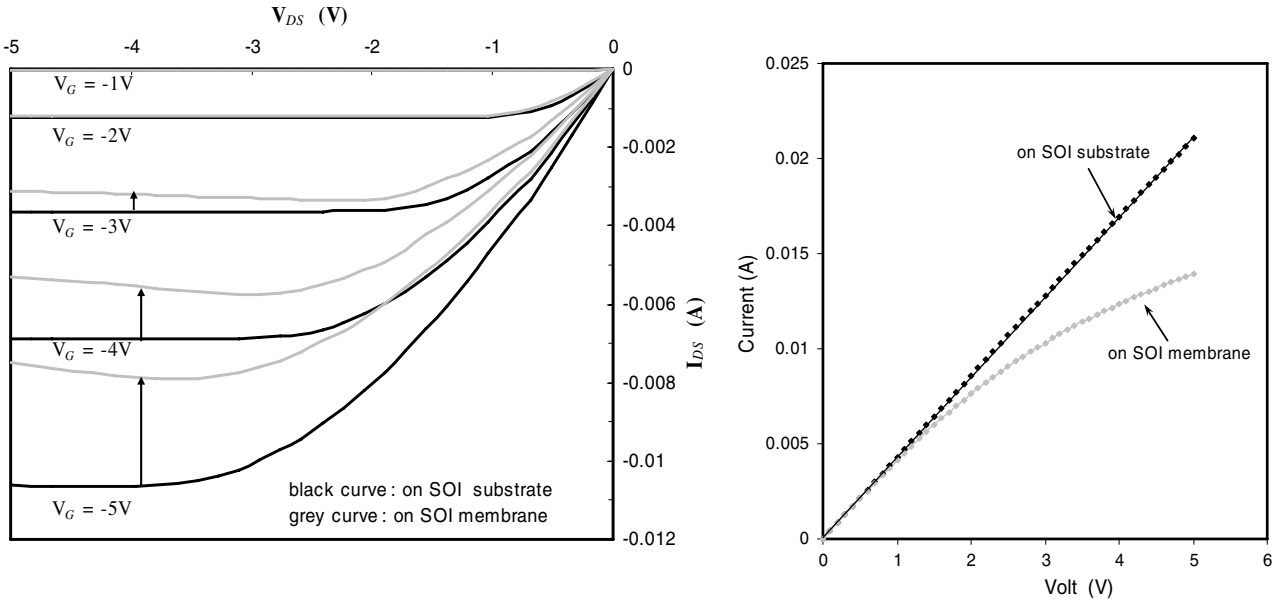


Figure 8. The output characteristics of PMOSFET (left) and polysilicon (right) heaters before and after the formation of SOI membranes.

a further increase of V_G in excess of 5 V may bring about the device breakdown. Similarly, the polysilicon resistor demonstrates a decreasing resistance change with micro-hotplate temperature build-up. The nominal sheet resistance of the silicide poly is 2.35 Ω at 25 °C and the evident variation of resistance is found to be nearly 50% for voltage up to 5 V. The TCR of the polysilicon film derived from measurements is 2.102×10^{-3} K^{-1}.

While verifying temperature rises from the diode temperature sensors, the on-chip transducing circuits using multi-stage differential op-amps are driven at +5 V and −5 V, which offer 40 μA constant currents for thermodiodes embedded within active and reference heaters. For chemoresistive operation mode the output voltage of an op-amp was measured across the active heater on the membrane and the reference heater on the substrate can account for the absolute temperature relative to room temperature. Similarly, an op-amp operating across both active and reference heaters on membrane can offer the differential temperature for microcalorimetric operation mode. For microcalorimetric operation the temperature sensing circuit can detect temperature difference up to 70 °C. To measure the electro-thermal response of the micro-hotplate, the gate voltage was swept from 0 to −10 V in 0.5 V steps at a constant drain voltage of −5 V for PMOSFET heaters. With

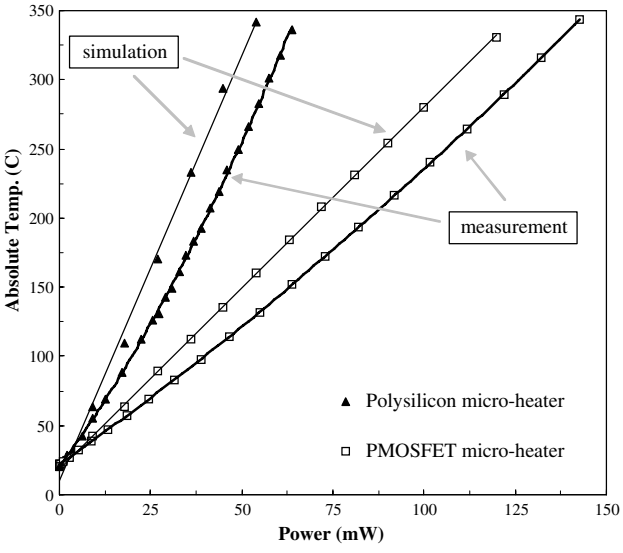


Figure 9. Both simulation and experimental results of power consumption versus operation temperature for polysilicon and PMOSFET micro-hotplates.

the measured temperature coefficients of −1.52 mV °C^{-1} for the diode and 318 Ω °C^{-1} for the spreading resistor, low power

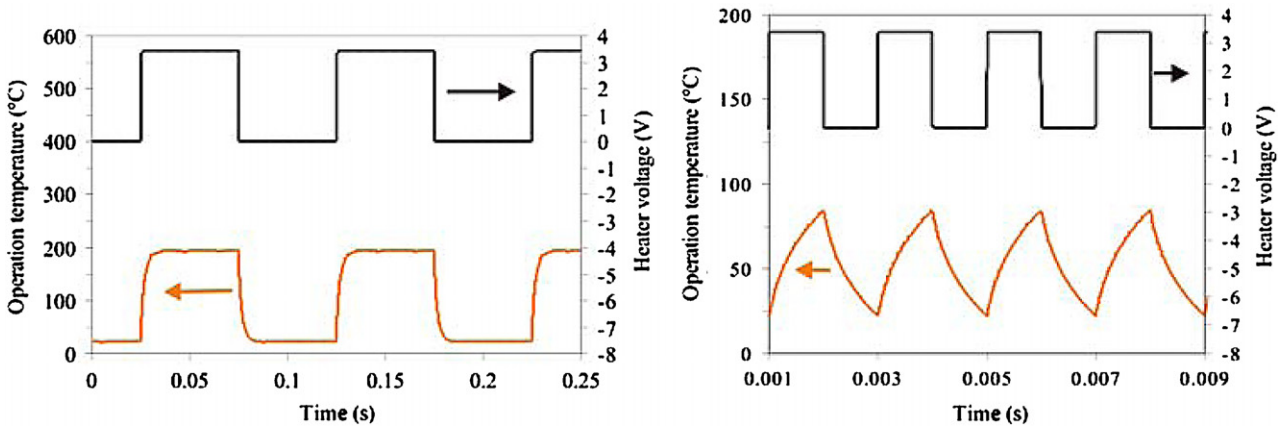
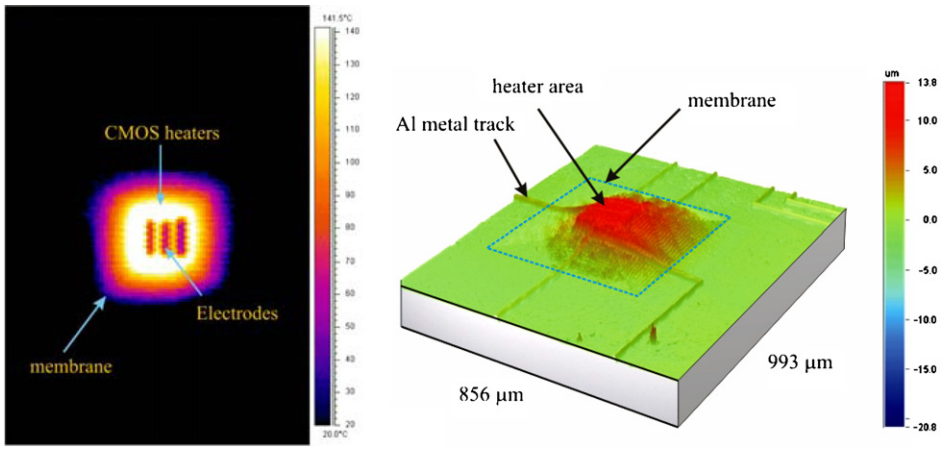


Figure 10. The dynamic and transient experiments for polysilicon-driven micro-hotplates pulsed at (*a*) 10 Hz and (*b*) 500 Hz, respectively.



(*a*) (*b*)

Figure 11. (*a*) A typical thermal image exhibiting the corresponding temperature profile, sensor configuration and the maximum temperature over 140 °C. (*b*) 3D profile denoting the maximum deflection of 13.8 μm at high temperatures in excess of 300 °C.

Table 4. Summary of the electro-thermal characteristics of MHPs with different design parameters.

Heaters	Dimensions $W \times L$ μm (W/L)	Lateral isolation	Membrane area	Ratios of membrane (l/h) (t_{box}/t_{si})	Measured temperature coefficient (mW °C^{-1})
PMOSFET	640 × 12 (53.3)	Multiple trenches	(535 μm)^2	161.3 *0.51*	0.42
Polysilicon resistor	1250 × 12 (104.2)	Multiple trenches	(627 μm)^2	202.2 *0.51*	0.20

supplies of 57 mW from the polysilicon heater and 126 mW from the PMOSFET heater for chemoresistive operation were successfully characterized. More manufacturing details of the micro-heaters and micro-hotplates are listed in table 4 and note that the temperature coefficient of a micro-hotplate is obviously more dependent on the heater's width to length ratio (W/L) than others. Electro-thermal characterization of both CMOS heaters as a function of temperature is illustrated in figure 9. FEM simulation results are also provided for comparisons and significant variation is observed. This gap can be mainly attributed to the characterized results that are well expressed by a second-order polynomial in favour of Pike and Gardner's model [25], which is dissimilar with simulator's conventional first-order theory. Besides, the imperfect back-etching process causing substantial damage to the buried oxide layer or asymmetrical membrane shape may also decline the constancy.

Furthermore, the MOSFET/polysilicon micro-heaters were modulated in pulses and the temperature response monitored to clarify the dynamic characteristics of the SOI micro-hotplate. The heater was pulsed with an input bias from 0 to 6 V in different experiments with frequencies from 10 Hz up to 1 kHz. These dynamic measurements prove the thermal response time of the micro-hotplate is close to 10 ms. The superior transient response and thermal characteristics allow effectively dynamical operation instead of static operation

to significantly reduce the power consumption [35]. The equivalent thermal resolution of the temperature sensor with transducing differential amplifiers is shown as accurate as 0.01 °C, as estimated. Part of dynamic measurements for the polysilicon-driven chemoresistor is shown in figure 10.

4.3. Imaging verification of SOI micro-hotplates

A thermal image representing the thermal profiles of these high-temperature SOI micro-hotplates was verified by an Amega 880 infrared camera based on an average emissivity of 0.2 for the micro-hotplate as shown in figure 11(*a*). In addition, with a Wyko NT-2000 interferometer, the electro-thermal deformation of the SOI micro-hotplate operating at high temperature is also characterized in figure 11(*b*). It is clearly shown that the maximum deformation of the membrane during operation was estimated as 10.7 μm regardless of the membrane thickness, which was comparable to the simulated results in table 3. To reduce membrane deflection and obtain good manufacture yield, a small (<1 mm^2) and thick (>5 μm) membrane is empirically considered; however, this may lead to lower the membrane aspect ratio hence increasing more power losses. Deliberate trade-off to meet sensor's functional specifications can be carefully achieved by these useful results.

5. Conclusions

Multidisciplinary investigations including physical modelling, FEM simulation and device characterization into feasibility and operational performance of smart gas sensors using SOI CMOS technology have been presented in this paper. The proposed platform utilizes CMOS-compatible (MOSFETs and polysilicon) micro-heaters embedded in thin membranes to raise the operation temperature up to 300 °C over the sensor area only at the cost of 57 mW and facilitates fast transient response of 10 ms. With constant development of the SOI sensor platform over the years, comprehensive efforts in terms of the design of the heater configuration, sensor elements, differentially transducing ICs for temperature control, mechanical stability and static/dynamic characterization of the micro-hotplate have been made through our previous and current publications. More importantly, the novel smart sensor enables prompt temperature measurement, simple control via the applied gate voltage and the full integration of associated drive/transducing circuitry without thermal impact from sensors. Careful assessment in consideration of the maximum stress, membrane deflection, thermal uniformity and power consumption could be carried out for device optimization. From these favourable results it is promising to make such a CMOS-MEMS platform ideal for advanced high-temperature and low-power applications in portable gas/vapour sensory systems.

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References

[1] Gardner J W 1994 *Microsensors, Principles and Applications* (New York: Wiley) pp 242–3
[2] Gall M 1991 The Si planar pellistor: a low power pellistor sensor in Si thin-film technology *Sensors Actuators* B **4** 533–8
[3] Pike A and Gardner J W 1997 Thermal modelling and characterisation of micropower chemoresistive silicon sensors *Sensors Actuators* B **45** 19–26
[4] Gardner J W *et al* 2001 Silicon planar microcalorimeter employing nanostructured films *Proc. Transducers '01 (Germany)* pp 820–3
[5] Lundström I *et al* 1975 Hydrogen sensitive MOS field effect transistor *Appl. Phys. Lett.* **26** 55–57
[6] Suehle J *et al* 1993 Tin oxide gas sensor fabricated using CMOS micro-hotplates and in situ processing *IEEE Electron Dev. Lett.* **14** 118–20
[7] Reay R J *et al* 1994 Thermally and electrically isolated single crystal silicon structures in CMOS technology *IEEE Electron Dev. Lett.* **15** 399–401
[8] Briand D *et al* 2000 Design and fabrication of high-temperature micro-hotplates for drop-coated gas sensors *Sensors Actuators* B **68** 223–33
[9] Udrea F and Gardner J W 1996 Smart MOSFET gas sensor *UK Patent* GB2321336A and *World Patent* WO98/32009
[10] Udrea F *et al* 2001 Design and simulations of SOI CMOS micro-hotplate gas sensors *Sensors Actuators* B **78** 180–90
[11] Guha P K *et al* 2007 Novel design and characterisation of SOI CMOS micro-hotplates for high temperature gas sensors *Sensors Actuators* B **127** 260–6
[12] Afridi M Y *et al* 2002 A monolithic CMOS microhotplate-based gas sensor system *IEEE Sens. J.* **2** 644–55
[13] Wollenstein J *et al* 2003 A novel single chip thin film metal oxide array *Sensors Actuators* B **93** 350–5
[14] Laconte J *et al* 2004 SOI CMOS compatible low-power microheater optimization for the fabrication of smart gas sensors *IEEE Sens. J.* **4** 670–80
[15] Barrettino D *et al* 2004 Hotplate-based monolithic CMOS microsystems for gas detection and material characterization for operating temperatures up to 500 °C *IEEE J. Solid-State Circuits* **39** 1202–7
[16] Graf M *et al* 2005 Transistor heater for microhotplate-based metal–oxide microsensors *IEEE Electron Dev. Lett.* **26** 295–7
[17] Graf M *et al* 2006 Micro hot plate-based sensor array system for the detection of environmentally relevant gases *Anal. Chem.* **78** 6801–8
[18] Guo B *et al* 2007 A monolithic integrated 4 × 4 tin oxide gas sensor array with on-chip multiplexing and differential readout circuits *Solid-State Electron.* **51** 69–76
[19] Bruel M 1995 Silicon on insulator material technology *Electron. Lett.* **31** 1201–2
[20] Yan G *et al* 2001 An improved TMAH Si-etching solution without attacking exposed aluminium *Sensors Actuators* A **89** 135–41
[21] Sharma D, Gautier J and Merckel G 1978 Negative dynamic resistance in MOS devices *IEEE J. Solid-State Circuits* **13** 378–80
[22] Hsarma D and Ramanathan K 1983 Modeling thermal effects on MOS *I–V* characteristics *IEEE Electron. Dev. Lett.* **4** 362–4
[23] McDaid L *et al* 1989 Physical origin of negative differential resistance in SOI transistors *Electronic Lett.* **25** 827–8
[24] Su L T *et al* 1994 Measurement and modelling of self-heating in SOI NMOSFETs *IEEE Trans. Electron Devices* **41** 69–75

[25] Pike A and Gardner J W 1997 Thermal modelling and characterisation of micropower chemoresistive silicon sensors *Sensors Actuators* B **45** 19–26
[26] Timoshenko S and Woinowski-Krieger S 1959 *Theory of Plates and Shells* (New York: McGraw-Hill)
[27] Maier-Schneider D *et al* 1992 Computer-aided characterization of the elastic properties of thin films *J. Micromech. Microeng.* **2** 173–5
[28] Sze S M 1988 *VLSI Technology* (New York: McGraw-Hill)
[29] Tabata O *et al* 1989 Mechanical property measurements of thin films using load-deflection of composite rectangular membranes *Sensors Actuators* **20** 135–41
[30] Tait R and Mitchell A 1994 Mechanical limitations in the performance of integrated acoustic sensors *Sensors Actuators* A **41–42** 455–9
[31] Bourouina T, Vauge C and Mekki H 1995 Variational method for tensile stress evaluation and application to heavily boron-doped square-shaped silicon diaphragms *Sensors Actuators* A **49** 21–7
[32] Smith C S 1953 Piezoresistance effect in germanium and silicon *Phys. Rev.* **94** 42
[33] Hall H H *et al* 1951 The effects of pressure and temperature on the resistance of pn-junction in germanium *Phys. Rev.* **84** 129–32
[34] Creemer J F 2002 Modelling of the piezojunction effect of bipolar transistors *PhD Dissertation* Delft University, The Netherlands
[35] Cavicchi R E *et al* 1996 Optimized temperature-pulse sequences for the enhancement of chemically specific response patterns from micro-hotplate gas sensors *Sensors Actuators* B **33** 142–6