Post-CMOS wafer level growth of carbon nanotubes for low-cost microsensors—a proof of concept

2010 Nanotechnology 21 485301

(http://iopscience.iop.org/0957-4484/21/48/485301)

Nanotechnology **21** (2010) 485301 (7pp) doi:10.1088/0957-4484/21/48/485301

Post-CMOS wafer level growth of carbon nanotubes for low-cost microsensors—a proof of concept

Sumita Santra[1,5], Syed Z Ali[4], Prasanta K Guha[1,2], Guofang Zhong[1], John Robertson[1], James A Covington[3], William I Milne[1], Julian W Gardner[3] and Florin Udrea[1,4]

[1] Engineering Department, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, UK
[2] Electronics and Electrical Communication Engineering Department, Indian Institute of Technology Kharagpur, Kharagpur-721302, India
[3] School of Engineering, University of Warwick, Coventry CV4 7AL, UK
[4] Cambridge CMOS Sensors Ltd, Wellington House, East Road, Cambridge CB1 1BH, UK

E-mail: ss778@cam.ac.uk

Received 10 June 2010, in final form 15 August 2010
Published 4 November 2010
Online at stacks.iop.org/Nano/21/485301

Abstract
Here we demonstrate a novel technique to grow carbon nanotubes (CNTs) on addressable localized areas, at wafer level, on a fully processed CMOS substrate. The CNTs were grown using tungsten micro-heaters (local growth technique) at elevated temperature on wafer scale by connecting adjacent micro-heaters through metal tracks in the scribe lane. The electrical and optical characterization show that the CNTs are identical and reproducible. We believe this wafer level integration of CNTs with CMOS circuitry enables the low-cost mass production of CNT sensors, such as chemical sensors.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Carbon nanotubes (CNTs) are one of a family of nanomaterials that have been widely studied since their discovery nearly two decades ago [1]. Their outstanding thermal, mechanical and chemical properties, nanometre size and large current carrying capacity (per unit cross-section) make them attractive for many applications. Researchers have already successfully demonstrated the use of CNTs as a transistor [2], simple logic gates [3], non-volatile memory [4], sensors [5, 6], field emitting tips [7], nanotweezers [8], switches [9] and a nanotube radio [10]. These applications are mainly focused on the use of a single or CNT discrete nanodevice. More recently, there have been reports on the growth/deposition of large quantities of CNTs (e.g. in the form of unaligned spaghetti-like or aligned forest-like) on predetermined positions; these devices could be useful for applications like chemical sensing [11] and flow rate sensing [12].

Nanostructured materials are a promising candidate for detecting chemicals because their very high surface area and small dimensions can lead to much higher sensitivity. In fact, researchers [13, 14] and industrialists [15] have successfully demonstrated that different nanomaterials (particularly CNTs) have high sensitivity to a large number of different gases and vapours which are important in the process industries, environmental monitoring, personal safety, medicine and even in security. CNT sensors generally react with gases at room temperature or relatively low temperatures (<200 °C) compared to metal oxide gas sensors and have a relatively fast response. Compared to commercially available chemical sensors, CNT-based sensors offer the possibility of compact, low-power, low-cost sensor arrays, suitable for use in battery-operated, portable and wireless applications.

Because of the advantageous properties of CNTs, many experts believe that they could, in the future, replace silicon-based microelectronics devices. However, there are several key challenges that must be addressed before CNTs are

[5] Author to whom any correspondence should be addressed.

capable of competing with state-of-the-art present CMOS (complementary metal oxide semiconductor) technology. One of the main barriers is the lack of technology to realize at low unit cost reliable, reproducible CNTs on the wafer level, i.e. a lack of technology for batch fabrication. Hence an alternative and perhaps more realistic approach is to grow and integrate CNTs on CMOS wafers and use CNTs to improve the performance of existing CMOS technology—a hybrid approach.

A number of groups have reported recent efforts to grow CNTs on wafer. Kong *et al* [16] described the growth of single-walled (SW) CNTs using a chemical vapour deposition (CVD) technique. They deposited $Fe(NO_3)_3{\cdot}9H_2O$, $MoO_2(acac)_2$ and alumina nanoparticles in the liquid phase, patterned with an electron beam and lifted off to form regularly spaced catalytic islands on the silicon surface. Franklin *et al* [17] reported the patterned CVD growth of SWCNTs on full 4 inch SiO_2/Si wafers. They used a deep ultraviolet photolithography technique to form the catalytic islands over the entire wafer and carried out by CVD at 900 °C. Hayamizu *et al* [18] have reported a scalable and reliable bottom up and top down hybrid approach where individual nanotubes are hierarchically assembled by two self-assembly stages into closely packed and aligned nanotube films that they denoted as 'CNT wafers'. Li *et al* [19] and Kang *et al* [20] showed successful self-assembly of CNTs into aligned networks or multilayer systems using Langmuir–Blodgett and substrate oriented growth. Krishnan *et al* [21] showed the wafer level growth of CNTs in porous alumina template. They used plasma enhanced chemical vapour deposition (PECVD) for the decomposition of acetylene, keeping the substrate voltage at −550 V to initiate a DC glow discharge of plasma for alignment of CNTs. Monica *et al* [22] used a dielectrophoresis (DEP) technique with several lithography patterned electrodes to deposit CNT networks after ultrasonicating them in dimethylformamide solution. Young-Moon *et al* [23] presented the vertical integration of CNTs in full 6 inch wafers for interconnect applications. They implemented the integration processes by using the bottom electrodes and via hole patterning followed by CNT growth, planarization and patterning of the top electrodes.

The above mentioned methods are encouraging, however, if we want to take full advantage of already established reliable, reproducible, cheap integrated circuit (IC) technology and try to integrate CNTs on fully processed CMOS wafers, these methods are not suitable because they are either too complicated (using several different steps that are not CMOS friendly) or use very harsh environmental conditions in which to grow CNTs—i.e. they will damage any on-chip circuits.

In this paper we report for the first time a concept for growing CNTs at the post CMOS wafer stage. The CNTs were grown locally and optimized on a fully processed (i.e. the wafer already contains CMOS circuits and devices) silicon on insulator (SOI) CMOS wafer. The integration of the two technologies (nanotechnology and conventional SOI CMOS) is of significant interest both from a device and application perspective. This is because CNTs are being used for the detection of different gases and vapours and SOI CMOS has the capability of low leakage current and higher operating

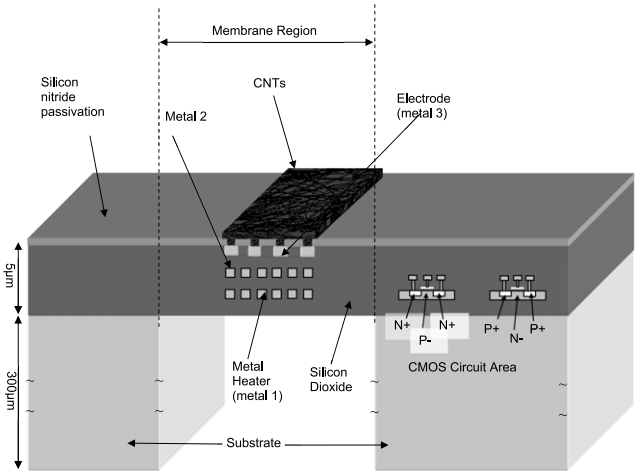

Figure 1. Schematic representation of the SOI micro-hotplate and integrated CMOS cells.

temperatures than conventional bulk silicon technology. The CNTs were characterized with SEM and Raman spectroscopy. Long term electrical resistance measurement was also carried out to check the stability of the CNTs, which is particularly useful for resistive chemical sensor applications. We believe this concept of local growth for wafer level realization of CNTs will open avenues to integrate CNTs with CMOS technology in a process suitable for mass manufacturing and thus will help to achieve a new generation of CNT microsensors suitable for embedding in portable devices such as mobile phones.

2. Device design and fabrication

The basic structure of our CNT-based chemical sensor is shown in figure 1. It was designed in Cadence 5.0 and fabricated using a 1.0 μm (three metal layers) SOI CMOS process from a commercial foundry. The SOI process handles 6 inch wafers with a 0.25 μm silicon active layer, and a 1.0 μm buried oxide layer. The device contains an embedded micro-heater and exposed interdigitated sensing electrodes. The interconnect metal (tungsten) of the high-temperature SOI process was used to form a resistive micro-heater. The use of tungsten metallization allows the device to operate at the very high temperatures (more than 600 °C) required for on-chip sensing material growth (if required) and gas sensor operation. A micro-heater made of tungsten is much more stable at higher temperatures than both aluminium (which suffers from electromigration) and polysilicon (unstable grain boundary) that have been used in reported CMOS micro-hotplate designs [24, 25]. The resistive micro-heater can also be readily used as a temperature sensor, as its resistance increases almost linearly with temperature. The top layer of the devices is a stable silicon nitride passivation. The interdigitated sensing electrodes (aspect ratio here is 56) were formed from the top metal layer (metal 3), and are used to measure the change in resistance of sensing material, i.e. CNTs in the presence of a gas. The passivation above the electrodes was etched away by the same process step used for exposing the bond pads. The CMOS steps were followed by

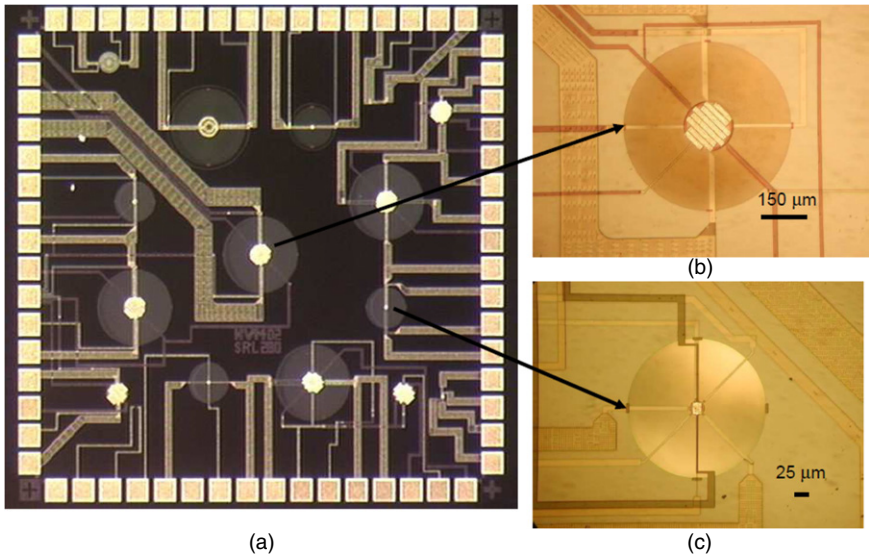

Figure 2. (a) An optical microscope picture of the 4 mm × 4 mm chip. (b) Zoomed in view of the large device with the interdigitated electrode. (c) Zoomed in view of the small device.

a deep reactive ion etching (DRIE) of the whole wafer in a separate microelectrical mechanical systems (MEMS) foundry (Silex Microsystem, Sweden) to form a mainly oxide–nitride membrane (ca. 5 μm thick) in predefined areas. The SOI membrane structure reduces the power consumption down to about 2.55 μW μm^{-2} for the micro-hotplate at 600 °C. It was found that it is possible to raise the membrane temperature to a very high value (up to 800 °C) while maintaining the rest of the chip and electronics close to room temperature, thus suitable for reliable CMOS circuit performance. The top view of the fabricated chip is shown in figure 2. As can be seen, structures with two different geometries were used (membrane diameters 560 and 300 μm, the corresponding micro-heater diameters were 150 and 25 μm). Details of the micro-heater design and characterization were reported in [26]. The devices have ultra-low power consumption of 45 mW to reach 600 °C for the large heater and only 16 mW for the small heater (2.55 and 3.26 μW μm^{-2}, respectively), fast transient times (10 ms for the large and 2 ms for the small device to reach 600 °C), and showed extremely good reproducibility within a wafer, and from wafer to wafer. The nonlinear power (P) versus temperature (T) plot of the large micro-heater is shown in figure 3. It can be well approximated by a second order polynomial function.

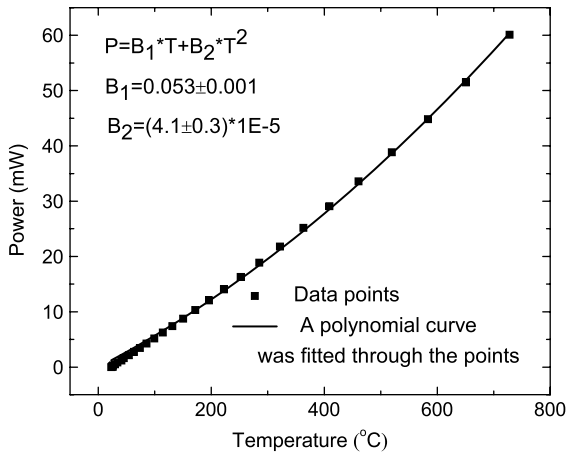

Figure 3. Power versus temperature plot of the large micro-heater. A polynomial curve was fitted through the data points.

3. Local growth

A novel local growth technique [27, 28] was used (contrary to conventional bulk heating of the entire substrate at elevated temperature) [16, 17, 21, 29, 30] to grow CNTs on-chip (i.e. *in situ*) over the micro-hotplate regions. This method allows precise control of the position and growth time. Tungsten micro-heaters (which are thermally isolated from the rest of the CMOS chip) were used to heat up the membrane to form small catalytic islands and then CNTs were grown using a thermal CVD technique. PECVD was found to be unsuitable because of plasma arcing and high thermal stresses that caused the SOI membrane to rupture. So, unlike the bulk heating of the entire chip, which could cause degradation of CMOS devices and interconnects due to high growth temperatures (>450 °C), this novel technique allows CNTs to be grown on-chip in localized regions; thus one does not need to use additional costly lithographic/processing steps. Furthermore, this method does not need any additional heating of the precursor gases.

For the CNT growth, first the chips were sputtered with a 2–4 nm iron (Fe) catalyst all over the chip (except the bond pads, which were masked to avoid shorting). Then the devices were mounted onto a ceramic package (CPG06864, Spectrum Semiconductor, USA) and connected via a printed circuit board to the power supply. The chips were then transferred to a CVD chamber to grow the CNTs. The chamber was pumped down to 0.2 mbar using a standard rotary pump. The micro-heater was powered through a computer controlled external power supply so that the membrane could reach a high temperature. The CNT growth process was optimized by varying the growth temperature, gas ratio and time of

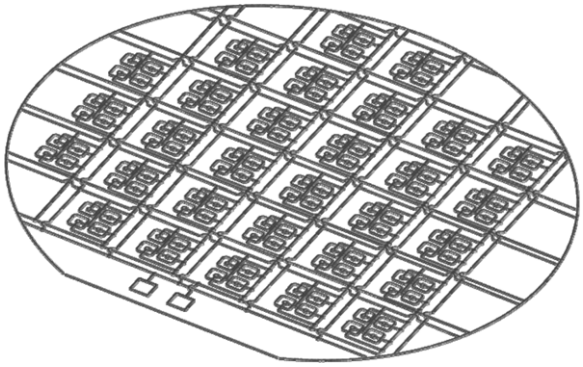

Figure 4. A schematic diagram of the wafer level carbon nanotube growth.

growth. When the temperature over the micro-heater region was 400 °C, high purity ammonia (150 sccm) was introduced into the chamber. The heating rate was set to 30 °C s^{-1} to minimize any thermo-mechanical stress in the membrane. The micro-heater was operated at 725 °C for 30 s to form the small catalyst Fe islands. Then acetylene (75 sccm) was introduced through a separate line. The partial pressure was set to 4 mbar during the growth process. The corresponding heater power was 55 mW at 725 °C. As the gases were released into the chamber, more power was required due to convective cooling to keep the heaters at the specific temperature (which was needed for the CNT growth). To achieve this control, a software program was written to control the power supply and hence to maintain a constant temperature (725 ± 1 °C) over the heater region. The deposition time was typically 10 min, after which the gases were turned off and the devices were allowed to cool. It was found that the use of much higher temperatures (>800 °C) gives better quality CNTs, but can also rupture the membrane. The nanotubes are formed due to the decomposition of acetylene, from which carbon dissolves and diffuses through the catalyst. The CNTs grown by this method are only formed over the heater region (because other parts of the chip are not hot enough to form small catalyst islands). The CNTs formed in this way are spaghetti or mat like, which are useful for gas sensing applications and offer better conducting path ways than say vertically aligned nanotubes.

4. Wafer level growth

It would be prohibitively time consuming to grow CNTs on individual heaters using a local growth technique. However, the local growth concept can be extended to grow CNTs on the whole wafer. The basic scheme is shown in figure 4. The concept is that all the micro-hotplates, spread across the wafer, are connected to each other via tracks in the scribe lanes between chips. This allows the heating of each micro-hotplate on the wafer at the same time and, hence, local growth of CNTs on each micro-hotplate simultaneously. After CNT growth, the dicing of the wafer removes the connection between the chips, leaving each chip as an independent gas sensor with its own micro-hotplate. Such a technique is necessary for large volume manufacturing of nanomaterial-based gas sensors.

Here, we connected some of the micro-heaters present on adjacent chips (although not all the micro-heaters across the wafer), to verify the concept. A cadence layout of two micro-hotplates on two adjacent chips, but connected together in parallel, is shown in figure 5. This is done by connecting the

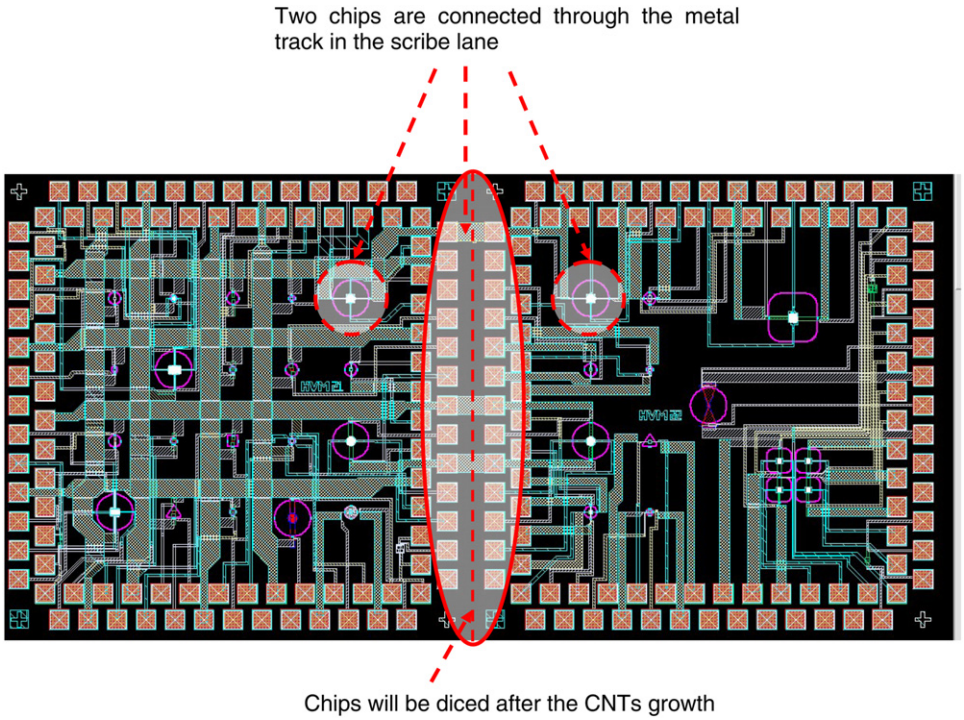

Figure 5. A Cadence layout of two micro-hotplates on two adjacent chips, but connected together in parallel. The chips will be separated after the dicing through the dotted line.

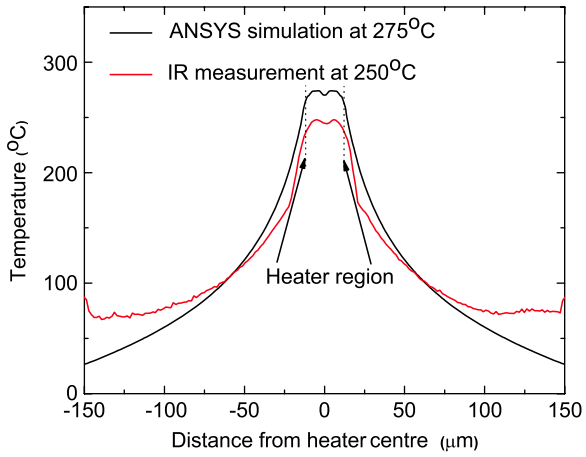

Figure 6. ANSYS simulation at 275 °C and infra-red (IR) camera measurement at 250 °C was performed. The results showed that the membrane temperature is relatively uniform (5% deviation) over the heater area whilst it falls rapidly beyond that, i.e. towards the edge of the membrane.

pads of the two chips using the space between them. The CNTs were grown using a local growth technique on two micro-heaters simultaneously.

The heating of the micro-hotplates at the wafer level can be performed in two different ways.

The simplest method is to provide a direct voltage to each micro-hotplate (H_1–H_n) simultaneously to heat it up—thus each micro-hot plate is effectively in parallel with each other.

The other method is to have a constant current circuit along with each micro-hotplate (H_1–H_n). An external voltage will power up the circuit, which in turn will power up the micro-hotplate.

In the first method one can use more than the process specified voltage (e.g. in our case the CMOS is a 5 V process) if required. Although it is not possible to control current through individual heaters in this method. On the other hand, the second method is more complicated, but results in a much more controlled growth and hence more uniform growth temperature across the wafer. A supply voltage of 5 V can be used to bias the circuits, however the voltage drop across the tracks can affect the performance of the current source.

5. Characterization

ANSYS simulations were carried out to evaluate the temperature distribution across the SOI membrane. Infra-red (IR) camera measurement was also performed at 250 °C (this is the maximum temperature allowed by the equipment) to verify the simulations experimentally. The results showed that the membrane temperature is relatively uniform (5% deviation) over the heater area whilst it falls rapidly beyond that, i.e. towards the edge of the membrane (shown in figure 6). The temperature consistency ensures uniform growth of CNTs over the heater region. Again, as the membrane edge is close to room temperature, this will guarantee the reliable performance of on-chip electronic circuits.

An optical microscope picture of two chips with simultaneously grown CNTs is shown in figure 7. The surface morphologies of the samples and size distribution of the nanotubes were characterized using a SEM operated at 2 keV, which is shown in figure 8. The nanotubes formed were of diameter 20–50 nm and length 3–4 μm.

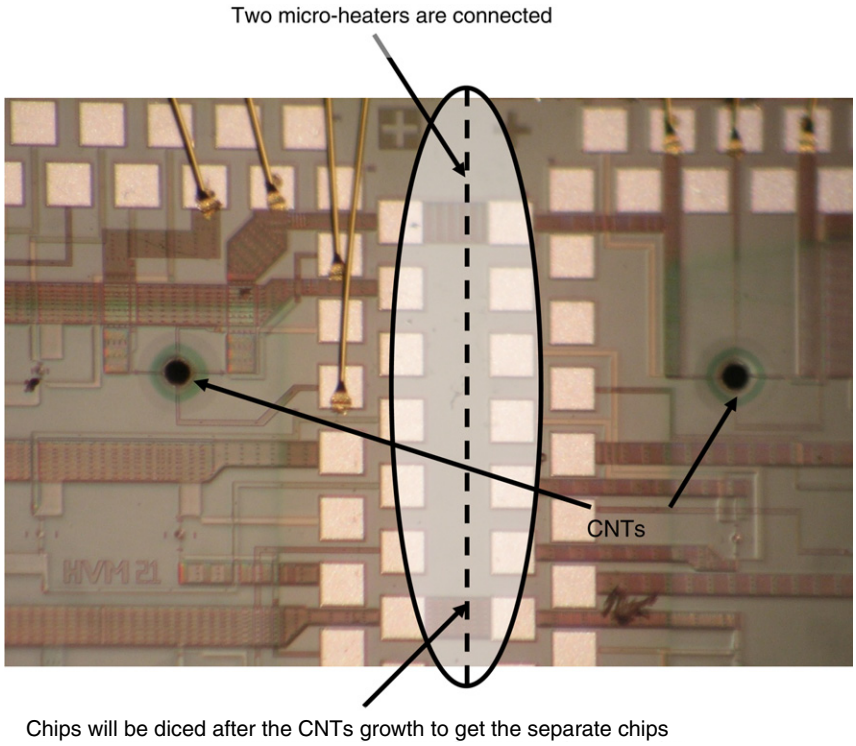

Figure 7. Optical microscope picture of the CNTs which were locally grown simultaneously on two micro-heaters present at adjacent chips.

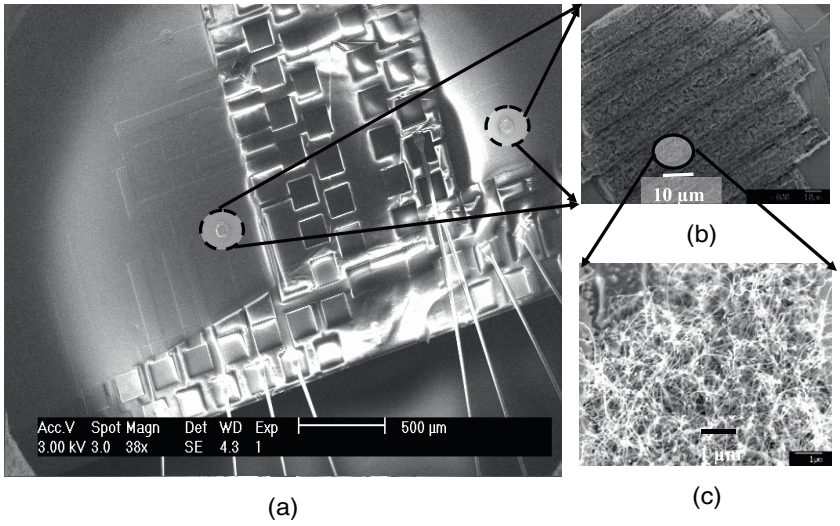

Figure 8. (a) SEM picture of the MWCNTs which were locally grown simultaneously on two micro-heaters present at adjacent chips. (b) MWCNTs were grown on the interdigitated electrode. (c) Zoomed in view of the spaghetti like MWCNTs on the interdigitated electrode.

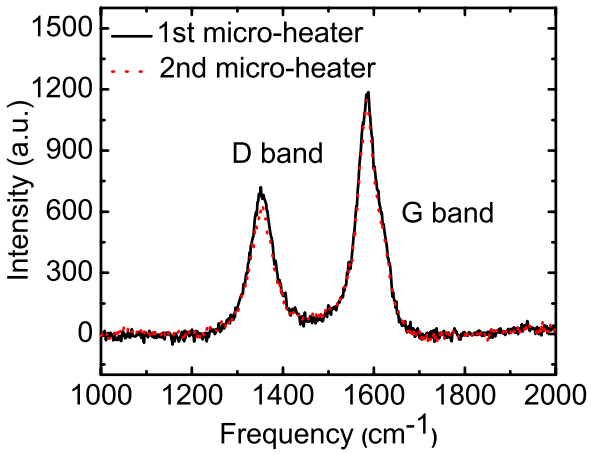

Figure 9. Raman spectra of the MWCNTs which were grown on two micro-heaters simultaneously. Note that the D/G ratio is same on the two sensors.

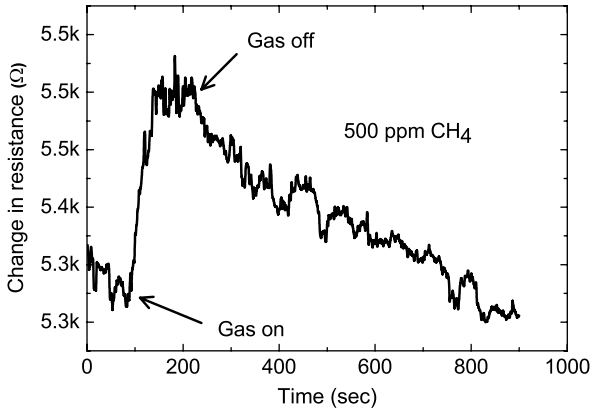

Figure 10. Change in resistance of the fabricated SWCNT methane gas sensor in 500 ppm partial pressure (with baseline in a vacuum). The concentration of methane was 500 ppm.

The CNTs were also characterized by Raman spectroscopy. It was found that the ratio between two characteristic lines (i.e. D/G—the two main characteristic lines (tangential mode (G band) and disordered induced mode (D band))) is similar for simultaneously grown CNTs (shown in figure 9), which implies that CNTs on different sensor devices are essentially identical in quality.

The electrical measurements between the electrodes gave the CNT resistance value of 0.5–10 kΩ. A long term continuous run at room temperature was performed for 100 h to check the reliability of the CNTs. The maximum change in voltage was found to be only 2%. We tested the CNT sensors with NO_2 gas and the results are presented elsewhere [31] and also performed methane (CH_4) testing (in 500 ppm partial pressure—with baseline in a vacuum) which is shown in figure 10. The response time was around 50 s, with the recovery period being much longer. Single wall CNTs were also grown using the same local growth technique (shown in figure 11).

6. Conclusion

In this work, we present a novel concept of wafer level localized growth of spaghetti like CNTs on a fully processed CMOS substrate. A standard SOI CMOS process was used to fabricate the basic gas sensor (which incorporated a tungsten micro-heater and interdigitated electrodes) and on-chip circuitry from a commercial foundry. The dielectric membrane reduces the power consumption, for a given operating temperature (e.g. 500 °C), while providing isolation from the electronic circuits present adjacent to the membrane. CNTs were grown onto interdigitated electrodes with tungsten micro-heater local growth at 725 °C. This technique was extended to grow CNTs on more than one device to show the concept of wafer level growth by powering several micro-heaters simultaneously. CNTs grown by this method were found through Raman spectroscopy to be practically identical and reproducible. We believe that this novel concept of integrating CNTs on fully processed CMOS wafers is a

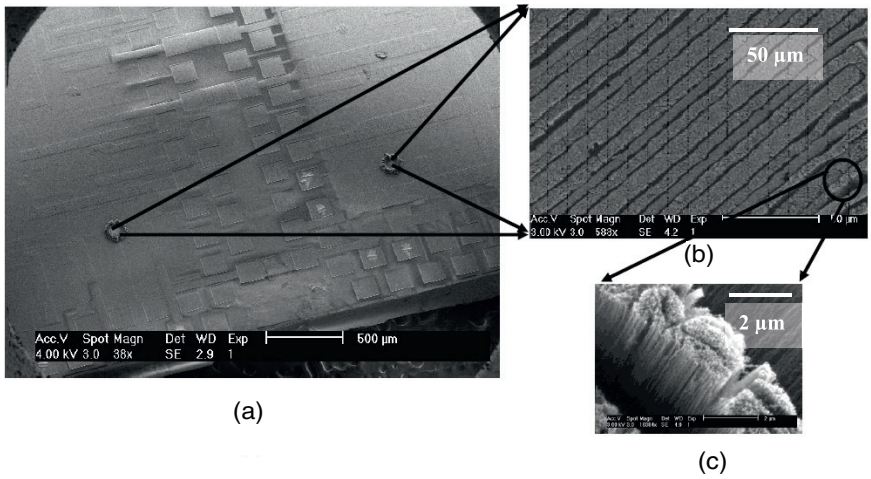

Figure 11. (a) SEM picture of the locally grown SWCNTs on two micro-heaters at adjacent chips. (b) SWCNTs were grown on the interdigitated electrode. (c) Zoomed in view of SWCNTs on the interdigitated electrode.

step forward towards low cost, high volume, reproducible and high yield. Hence opening up new markets, such as miniaturized CNT sensors for mobile phones or PDAs. Operating CNTs at 125 °C would require less than 7.5 mW DC power consumption, which is equivalent to 10 nW μm^{-2} of an SOI micro-hotplate. Pulsing the heater will reduce the average power consumption to below 100 μW at 125 °C.

Acknowledgments

This work has been supported by the Engineering and Physical Sciences Research Council (EPSRC), UK under the project no. EP/F004931/1, EP/F002971/1 and EC Framework VII 'Technotubes' project.

References

[1] Iijima S 1991 *Nature* **354** 56
[2] Tans S J, Verschueren A R M and Dekker C 1998 *Nature* **393** 49
[3] Bachtold A, Hadley P, Nakanishi T and Dekker C 2001 *Science* **294** 1317
[4] Rueckes T, Kim K, Joselevich E, Tseng G Y, Cheung C L and Lieber C M 2000 *Science* **289** 94
[5] Kong J, Franklin N R, Zhou C W, Chapline M G, Peng S, Cho K J and Dai H J 2000 *Science* **287** 622
[6] Stampfer C, Helbling T, Obergfell D, Schoberle B, Tripp M K, Jungen A, Roth S, Bright V M and Hierold C 2006 *Nano Lett.* **6** 233
[7] Dai H J, Hafner J H, Rinzler A G, Colbert D T and Smalley R E 1996 *Nature* **384** 147
[8] Kim P and Lieber C M 1999 *Science* **286** 2148
[9] Jang J E, Cha S N, Choi Y J, Kang D J, Butler T P, Hasko D G, Jung J E, Kim J M and Amaratunga G A J 2008 *Nat. Nanotechnol.* **3** 26
[10] Jensen K, Weldon J, Garcia H and Zettl A 2007 *Nano Lett.* **7** 3508
[11] Snow E S, Perkins F K, Houser E J, Badescu S C and Reinecke T L 2005 *Science* **307** 1942
[12] Ghosh S, Sood A K and Kumar N 2003 *Science* **299** 1042
[13] Li J, Lu Y J, Ye Q, Cinke M, Han J and Meyyappan M 2003 *Nano Lett.* **3** 929
[14] Kawano T, Chiamori H C, Suter M, Zhou Q, Sosnowchik B D and Lin L W 2007 *Nano Lett.* **7** 3686
[15] http://www.nano.com/
[16] Kong J, Soh H T, Cassell A M, Quate C F and Dai H J 1998 *Nature* **395** 878
[17] Franklin N R, Li Y M, Chen R J, Javey A and Dai H J 2001 *Appl. Phys. Lett.* **79** 4571
[18] Hayamizu Y, Yamada T, Mizuno K, Davis R C, Futaba D N, Yumura M and Hata K 2008 *Nat. Nanotechnol.* **3** 289
[19] Li X L, Zhang L, Wang X R, Shimoyama I, Sun X M, Seo W S and Dai H J 2007 *J. Am. Chem. Soc.* **129** 4890
[20] Kang S J, Kocabas C, Ozel T, Shim M, Pimparkar N, Alam M A, Rotkin S V and Rogers J A 2007 *Nat. Nanotechnol.* **2** 230
[21] Krishnan R, Nguyen H Q, Thompson C V, Choi W K and Foo Y L 2005 *Nanotechnology* **16** 841
[22] Monica A H, Papadakis S J, Osiander R and Paranjape M 2008 *Nanotechnology* **19** 085303
[23] Young-Moon C, Sunwoo L, Hong Sik Y, Moon-Sook L, Hajin K, Intaek H, Yoonho S, In-Seok Y, Chung U I and Joo-Tae M 2006 *IEEE-NANO 2006: 6th IEEE Conf. on 2006 Nanotechnology* vol 1, p 262
[24] Suehle J S, Cavicchi R E, Gaitan M and Semancik S 1993 *IEEE Electron Device Lett.* **14** 118
[25] Laconte J, Dupont U, Flandre D and Raskin J P 2004 *IEEE Sensors J.* **4** 670
[26] Ali S Z, Udrea F, Milne W I and Gardner J W 2008 *J. Microelectromech. Syst.* **17** 1408
[27] Haque M S, Teo K B K, Rupensinghe N L, Ali S Z, Haneef I, Sunglyul M, Park J, Udrea F and Milne W I 2008 *Nanotechnology* **19** 025607
[28] Dittmer S, Mudgal S, Nerushev O A and Campbell E E B 2008 *Low Temp. Phys.* **34** 834
[29] Chhowalla M, Teo K B K, Ducati C, Rupesinghe N L, Amaratunga G A J, Ferrari A C, Roy D, Robertson J and Milne W I 2001 *J. Appl. Phys.* **90** 5308
[30] Wang X, Zhang Y, Haque M S, Teo K B K, Mann M, Unalan H E, Warburton P A, Udrea F and Milne W I 2010 *IEEE Trans. Nanotechnology* doi:10.1109/TNANO.2009.2038787
[31] Udrea F *et al* 2007 *Int. Electron Devices Mtg* p 831