University of Warwick

MSc Thesis

High Quality Relaxed Germanium Layers on Silicon

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Abstract

In recent years there has been considerable research in germanium, taking advantage of both its electrical and mechanical properties for a wide range of applications, including: CMOS based devices, photodetectors for optoelectronic purposes and the recent demonstration of a germanium laser. However, due to its low natural abundance, the use of bulk germanium wafers is not economically viable for mass production. Industrial fabrication processes are designed around using (0 0 1) silicon substrates, so for any new technology to be easily adopted by industry it must be compatible with (0 0 1) silicon. Hence germanium is typically incorporated onto silicon substrates using epitaxy. The growth of layers of high quality germanium on a (0 0 1) silicon substrate is an important step towards the exploitation of germaniums properties as a semiconductor by industry.

Unfortunately, due to the 4.2% lattice mismatch between silicon and germanium, it is difficult to achieve high quality epitaxial growth of germanium on (0 0 1) silicon. This research focuses on this problem and attempts to suggest how growth quality can be improved. The effect of growth conditions and hydrogen annealing on the growth quality is studied. The strain/relaxation of the germanium layer and the interdiffusion between the layer and the substrate is also explored.

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Chapter 1

Motivation and Thesis Outline

1.1 Motivation

Germanium has many advantages over silicon as a semiconductor. Its high mobility makes it ideal for MOSFETS and its direct band-gap makes it highly suitable for photonics. For economic and technical reasons, the adoption of germanium by industry requires germanium to be easily integrated with the industry standard (001) silicon platform. If high quality layers of germanium can be grown on silicon (001) wafers this integration can be achieved. Unfortunately germanium on silicon (001) heteroepitaxy normally gives rise to high surface roughness [49] . This roughness is due to islanding from Stranski-Krastanow (S-K) growth [18]. The 4.2% lattice mismatch between silicon and germanium causes the S-K growth after an initial period of 2D growth. Germanium on silicon (001) heteroepitaxy also suffers from high densities of both misfit-dislocations and threading-dislocations. This research will investigate how the germanium layer quality can be improved through varying the epitaxial growth parameters, including growth temperature and annealing. High resolution X-ray diffraction and atomic force microscopy will be used to characterise the germanium layers grown for the research.

1.2 Thesis Outline

In Chapter 1 the motivation for research into layers of high quality germanium on silicon is discussed and a brief outline of this thesis is given.

Chapter 2 gives some of the basic physics properties of germanium and silicon. The most useful applications of high quality layers of germanium on silicon are discussed, including how high quality germanium layers are vital for a complete silicon photonics platform.

Chapter 3 reviews previous attempts at growth of high quality germanium layers by different groups. Some of the attempts mentioned use a growth method very similar to that used in this research.

Epitaxial growth of germanium using reduced pressure chemical vapour deposition with germane precursor is introduced in Chapter 4. The initial stages of germanium growth are described.

Chapter 5 details the techniques used in this research (atomic force microscopy, high resolution x-ray diffraction and tunneling electron microscopy), along with any relevant theory. The analysis of the results is also discussed.

In Chapter 6 the wafers grown for this research are described and results from each technique described in chapter 5 are presented.

Qualitative and quantitative explanations are given in Chapter 7 for the results in Chapter 6.

In Chapter 8 Directions for future research are discussed.

Finally in Chapter 9 all research is summarised in a conclusion.

Chapter 2

Applications and Basic Properties of Germanium

2.1 Basic Properties of Germanium and Silicon

Germanium and Silicon both have the same crystal structure, face centered diamond cubic (See Figure 2.1). This is the same structure as diamond.

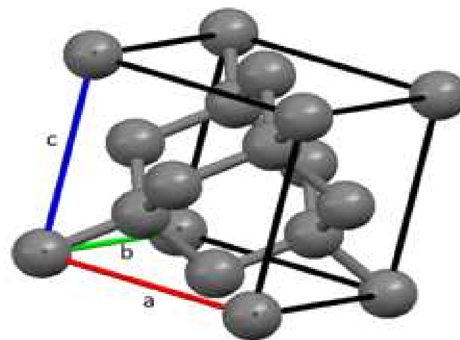


Figure 2.1: *Face centered diamond cubic structure of silicon or germanium*

The lattice parameter of relaxed silicon/germanium is the distance labelled (a), (b) or (c) on Figure 2.1. The lattice parameter of Silicon is 0.54310 nm and the lattice parameter of germanium is 0.56575 nm [16]. The lattice parameters of germanium and silicon have a 4.17% mismatch. The lattice mismatch (f_m) is calculated from equation 2.1, where a_s is the lattice parameter of the substrate and a_l is the lattice parameter of the layer.

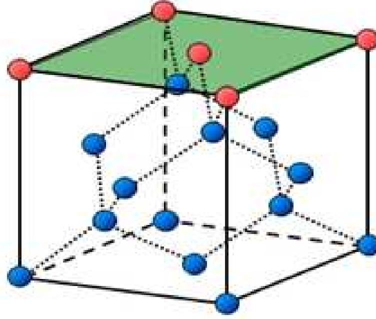


Figure 2.2: *(001) plane of silicon*

$$f_m = ((a_s - a_l)/a_l) \quad (2.1)$$

The vast majority of semiconductors use (001) oriented silicon substrates; the high mobility (001) plane of silicon is illustrated in Figure 2.2. This is the substrate orientation used in all silicon substrates in this research.

2.2 Applications of Relaxed Germanium Layers on Silicon Substrates

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

Germanium has a distinguished history as a semiconductor. The first ever transistor (figure 2.3) was made using germanium [3] in 1947. But since then Silicon has been the dominate semiconductor used in industry, being used in the vast majority of devices.
Moores law states that the number of transistors on an integrated circuit doubles every two years [38] (Figure 2.4) and the Si industry has not only followed this trend for half a century, but also used this trend to push CMOS scaling. This can be achieved by increasing the size of the integrated circuit or by shrinking the size of the MOS transistors used. There are many advantages to scaling down MOS transistors, these include packing more transistors in a smaller area and increased frequency response.

Figure 2.3: *Replica of first transistor*

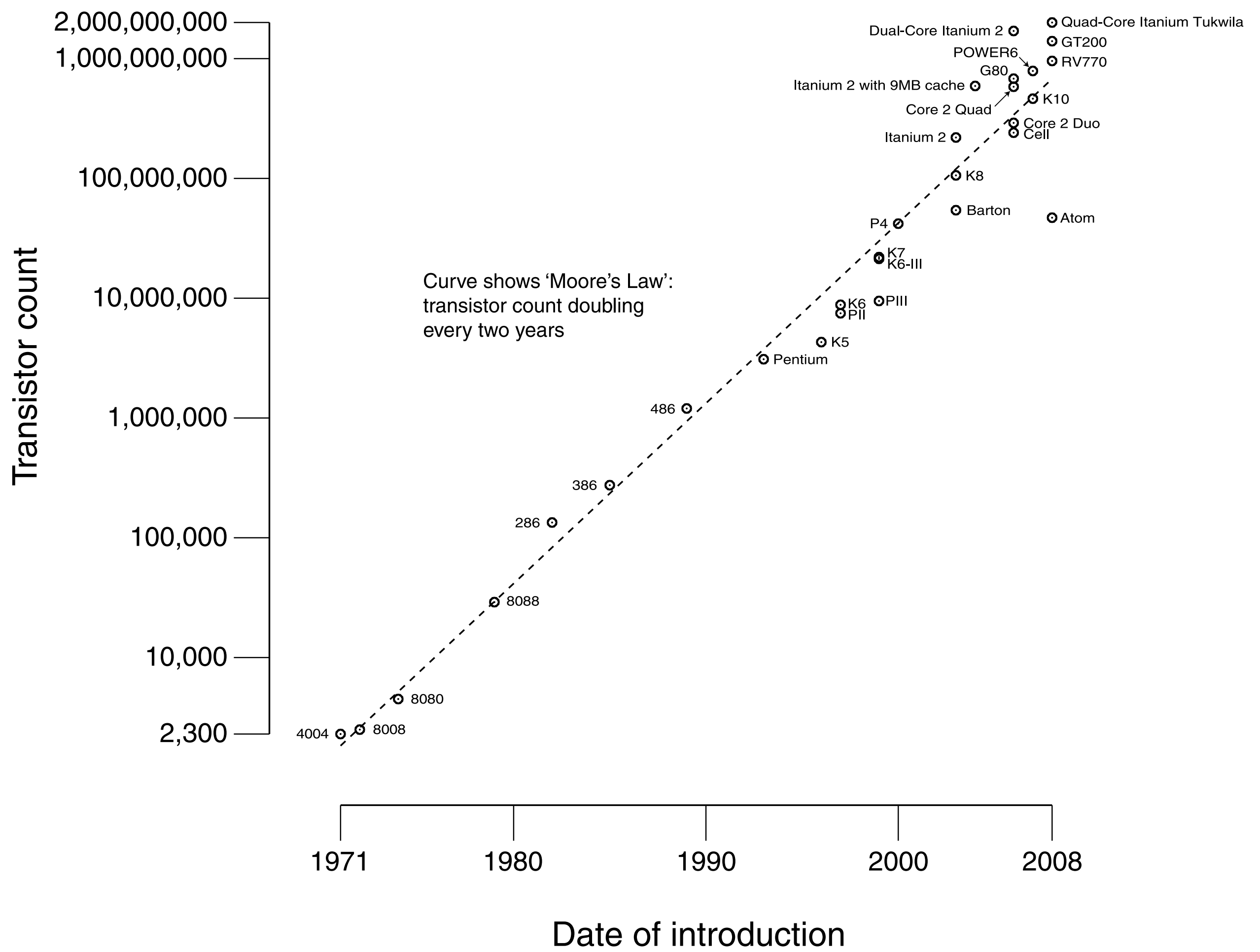


Figure 2.4: *Transistor Count vs. year and Moore's law*

For the continued scaling of CMOS into the nano-scale, a move away from bulk silicon to a semiconductor with a higher mobility may be necessary. The following table (Table 2.1) lists the electron and hole motilities for silicon, germanium and gallium arsenide (a Ill-V material). The most likely candidates to replace silicon are germanium or Ill-V materials. Ill-V materials often have poor hole mobility (See GaAs in Table 2.1), so germanium is a good option. Germanium has very favourable properties as a semiconductor, when compared to silicon. It can be seen that germanium has much higher mobility for electrons and holes than silicon. This is due to germanium having a lower transport mass for both electrons and holes [55].

Carrier motilities.cm^2/Vs	Silicon	Germanium	Gallium Arsenide (GaAs)
Hole	480	1900	400
Electron	1350	3900	8500

Table 2.1: *Carrier mobilities for silicon and germanium [27]*

Carrier mobility can be described as how easily a carrier can travel in a particular material. High carrier mobility is useful in transistors, since it gives a higher drive current. The carrier mobility of germanium can be improved further by compressive strain. Germanium can be used to fabricate both n and p type MOSFETs, with germanium p type MOSFETS showing an improvement on those made with silicon [31]. Since industry has invested heavily in the fabrication of silicon based devices, for any new technology to be economically viable, it must be compatible with the existing silicon fabrication process. A possibility would be to use germanium substrates, but this method has many disadvantages. Due to the low natural abundance of germanium, the price of raw germanium is very high compared to silicon, making the use of germanium wafers prohibitively expensive. Germanium substrates are more brittle than their Si counterparts, so have to be manufactured thicker so as to avoid damage when they are handled. Germanium has a higher atomic mass than silicon and when this is combined with an increased substrate thickness, the germanium substrates could become prohibitively heavy, especially for the larger 500mm and 450mm wafers now

standard for silicon.

If high quality layers of germanium can be grown on silicon substrate, the advantages of germanium MOSFETS can be exploited with only a relatively small increase in the cost of fabrication. The growth of high quality crystalline germanium layers on Silicon (001) wafers is a challenge that must be overcome before the adoption of germanium MOSFETS by industry [54]

Photonics - Photodetectors

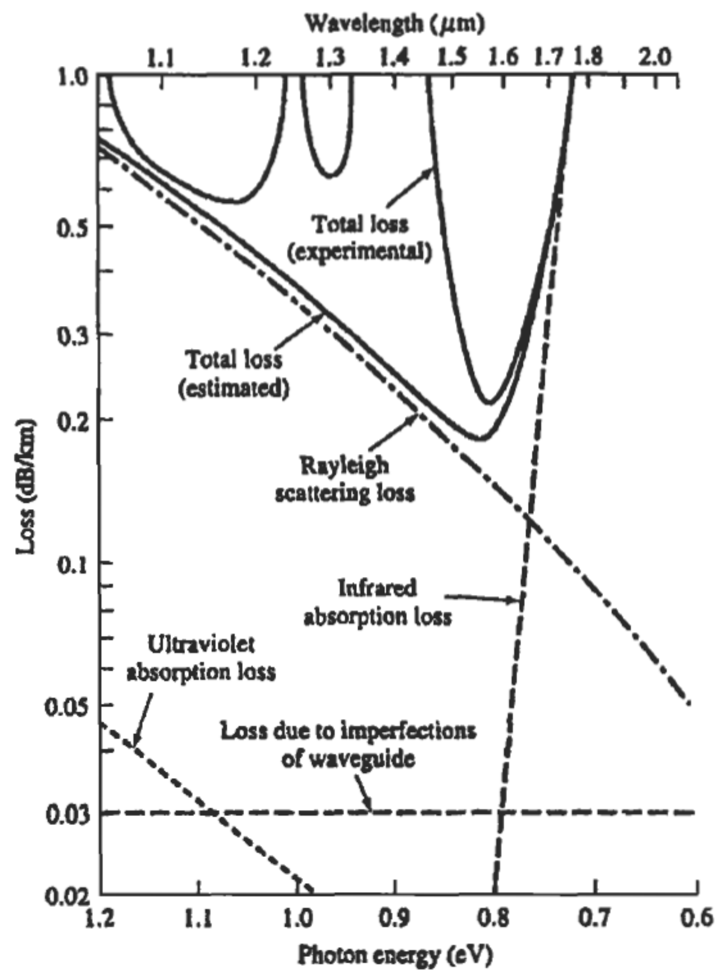


Figure 2.5: *Transmission loss in silica-based fibers. Taken from page 18 of [15]*

The integration of optoelectronics into the industry standard silicon platform has many benefits for industry, including being far cheaper than the hybrid intergration of III - V

devices and giving faster interconnects between chips.

Optical fiber is commonly made of silica, due to its cost, mechanical and optical properties. Silica has three transmission windows, two of which lie in the near-infrared. It can be seen in Figure 2.5 that the approximate wavelengths of the near-infrared transmission windows are 1300 nm and 1550 nm. The band-gap of Silicon makes it unsuitable for use in photo-detectors at these wavelengths, so an alternative material such as high Ge composition SiGe alloy or pure germanium must be used instead.

When the lowest conduction band minimum in a semiconductor is situated directly above the valence band maxima in K-space, it is known as a direct band-gap material (See Figure 2.6 A)). If a semiconductors lowest conduction band minimum is not situated directly above the valence band maximum it is known as an indirect band-gap material (See Figure 2.6 B)). Both energy and momentum must be conserved in any transition between the valence and conduction bands, so indirect band-gap materials have to involve a phonon and a photon in the transition. Hence, indirect band-gap materials are poor at absorbing light, because for light to be absorbed a lattice vibration must induce a dipole. Direct band-gap materials tend to be better at absorbing light, since no lattice vibration is needed for absorption. Silicon is an indirect band-gap material whereas germanium has a direct band-gap (See P12), hence germanium is better suited for use in photodetectors.

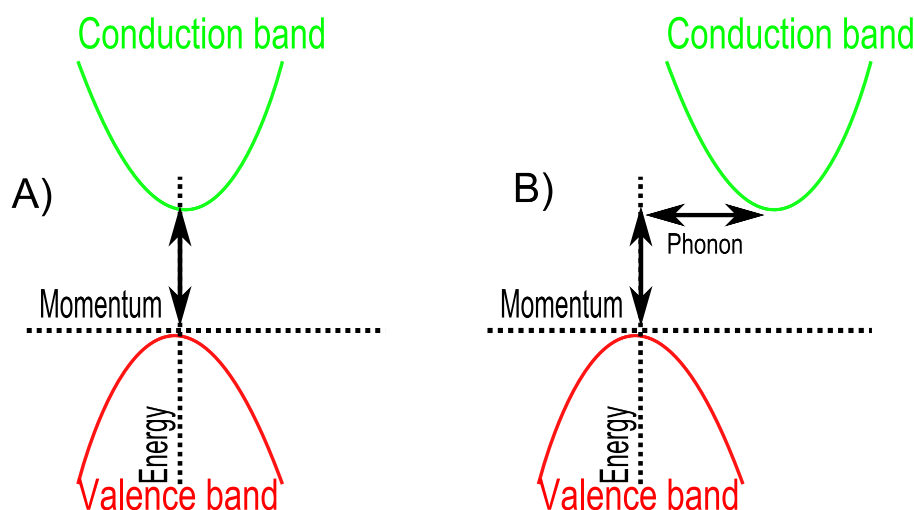


Figure 2.6: *A) Direct band-gap semiconductor B) Indirect band-gap semiconductor*

High quality layers of Germanium on Silicon have been used in near-infra-red photo-detectors

[12] and have been shown to be highly efficient. The performance of the photodetectors is dependant on the quality of the germanium layers, with a reduced threading-dislocation density giving improved performance [10]. If high quality layers of germanium can be grown on silicon substrates, it will be a big step towards a complete optoelectronics platform integrated on a silicon substrate.

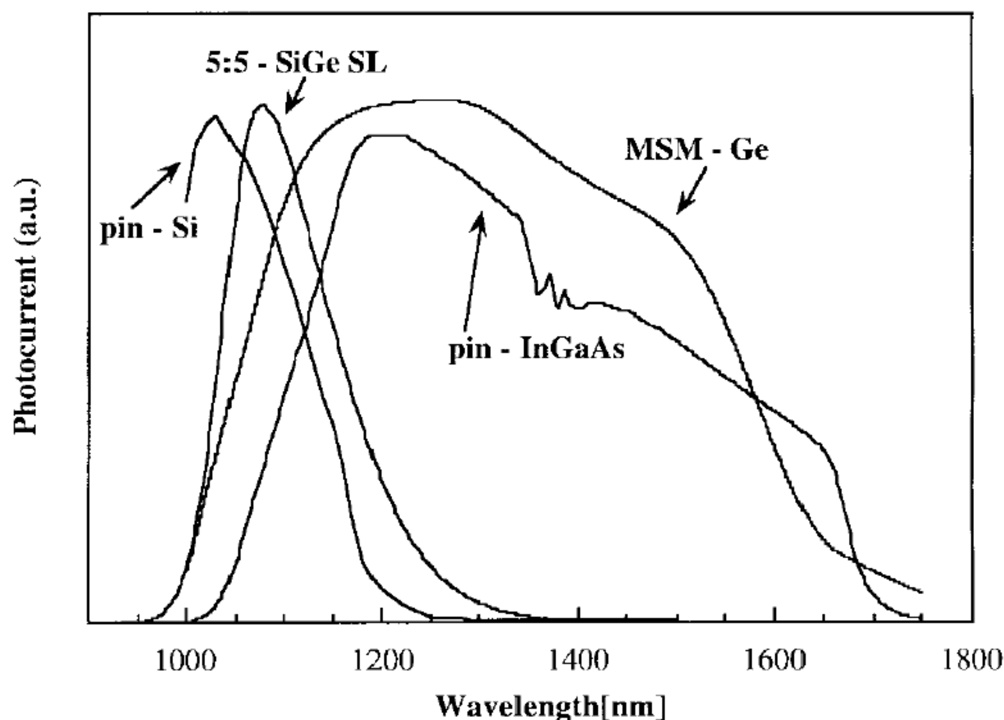


Figure 2.7: *NIR photocurrent spectral response of MSM Ge photodetectors, compared with Si, SiGe:SL and InGaAs p-i-n photodiodes. Taken from [9]*

Photonics - lasers

Integrating an efficient laser on Si is a further important step towards a complete optoelectronic integrated circuit on Si. Ideally, the laser would emit at 1550 nm, for use with silica optical fiber as discussed above. Unfortunately, since silicon is a indirect band-gap material, it is also a poor light source. Photon emission is phonon mediated and has a low probability [50]. If a layer of high quality germanium could be grown on a silicon substrate then the direct bandgap of Ge could be used to make an efficient laser, while keeping production costs

low.

A prototype of such a Ge on Si laser has recently been demonstrated by Jifeng Liu from MIT [33]. A laser of this kind is perfectly suited to use, since the direct band-gap of Ge is 0.8 eV (see Figure 2.8) corresponding to 1550 nm as required.

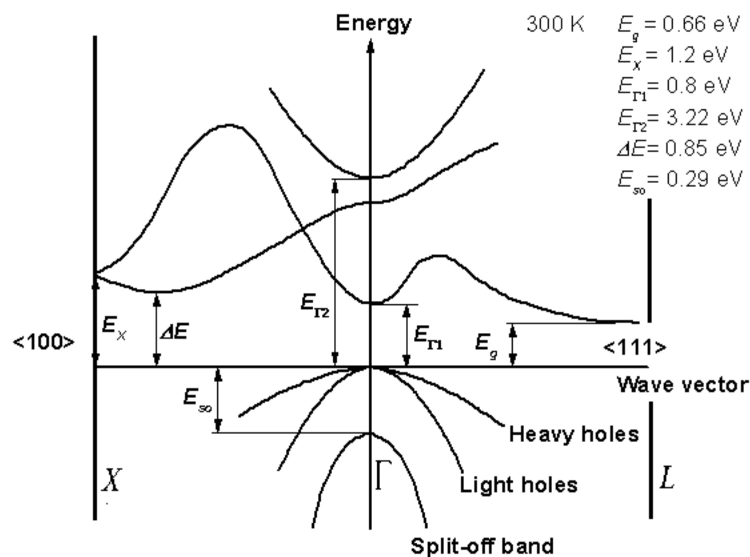


Figure 2.8: *Band structure of Germanium. Adapted from [25]*

Germanium is known as a pseudo-direct bandgap material. This means that it only has a small difference between its direct and indirect gap (0.136 eV). To compensate for the difference, the MIT laser uses heavy n type doping to fill the L valley conduction band. When carriers are then injected into the n type material, electrons are forced into the Γ band where they undergo a direct bandgap transition and recombine with holes. The recombination emits light at 1550 nm [33]. To further compensate for the difference between direct and indirect gaps, bandgap tuning by tensile strain in the Ge layer was used to lower the Γ - minimum with respect to the L - minimum. This tensile strain was caused by a mismatch in the coefficients of thermal expansion of Si and Ge and will be covered in great detail later on in this research. Despite this impressive result from MIT, there is still some way to go before a room temperature, electrically pumped laser will be available, so this topic of key technological interest right now.

Chapter 3

Epitaxial Growth

Epitaxy is the growth of a single-crystal film which adopts the crystalline structure and orientation of an underlying crystalline substrate. The two methods commonly used for growing Ge and Si layers are chemical vapour deposition (CVD) and molecular beam epitaxy (MBE) .

In MBE, the material required for the layer being grown is evaporated from heated cells in an ultra high vacuum environment. The evaporated material is collaminated into a beam and then directed towards the surface of a heated substrate. After hitting the substrate, the atoms/molecules migrate across the surface of the substrate before being incorporated onto its surface [4]. MBE is very useful in research, because all the growth parameters are independent. In MBE, the flux of material hitting the substrate surface (and hence growth rate) can be varied independently of the growth temperature. However, this flexibility also means that it is difficult to realise a stable industrial process and, together with the inherently slow MBE growth rate, means it is not the favoured epitaxy technique for production.

In CVD, layers are grown by passing precursor gases over the surface of the substrate. Many different variations of CVD exist, including Ultra High Vacuum CVD, Atmospheric Pressure CVD, Low Pressure CVD, Plasma-Enhanced CVD and Laser-enhanced CVD. All of the samples used in this research have been grown by Reduced Pressure CVD (RP-CVD), using an ASM Epsilon 2000 reduced pressure reactor. CVD is the growth method favoured by the semiconductor industry, due to its speed and reproducibility of results, including high

uniformity across large wafers and reproducibility over time from wafer to wafer. For the remainder of this study only RP-CVD will be considered.

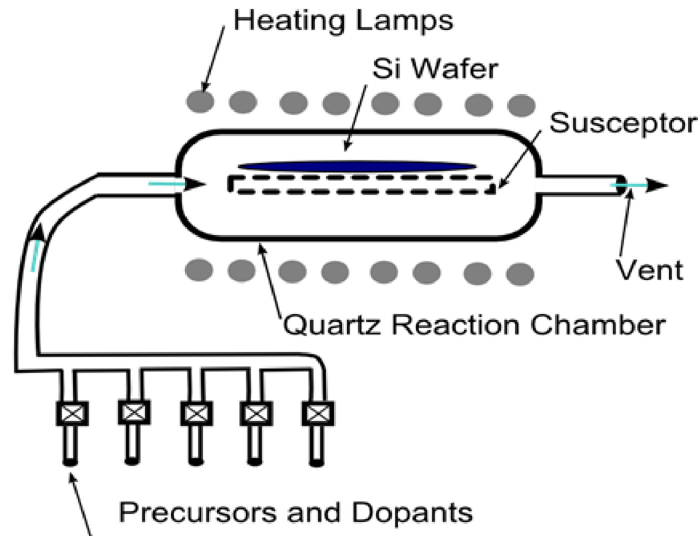


Figure 3.1: *Simplified diagram of RP-CVD reactor*

3.1 Reduced pressure Chemical Vapour Deposition

Figure 3.1 shows a typical reaction chamber used in RP-CVD. The CVD growth process can be split into steps, as illustrated in Figure 3.2.

Precursors and Chemical Reactions

The precursor used for epitaxial Ge growth in this research is Germane GeH_4. At approximately 280K [22] germane thermally decomposes on a surface to give a germanium deposit. The growth of Ge by GeH_4 can be described as:

$$GeH_4 \longrightarrow Ge + 2H_2 \tag{3.1}$$

Further details on the reactions occurring in epitaxy using germane can be found in Ref [63].

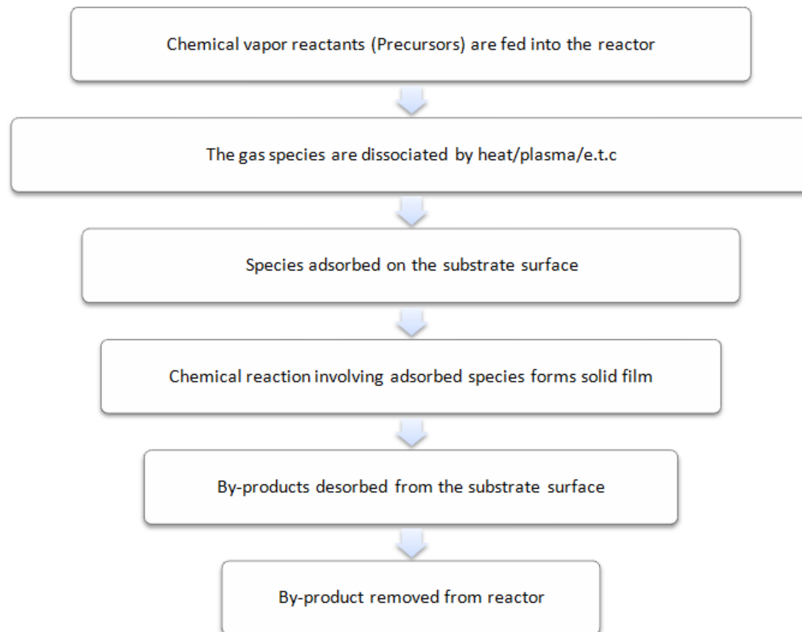


Figure 3.2: *Flow chart illustrating steps in growth by CVD*

Growth Rate

In CVD the growth rate can be split into two regimes, temperature limited growth and mass flow limited growth. If the temperature is low, the deposition rate is limited by the reaction rate which is dependant on the temperature (over abundance of reactants). If the temperature is high, the reaction rate is limited only by the supply of reactants, which is controlled by the mass flow rate. In Ref [13] the two growth rate regimes of germanium grown from GeH_4 were observed, with the transition between regimes occurs at approximately 375°C, which can be seen in Figure (3.3).

3.2 Epitaxial Growth of Ge on Si(001) - Growth morphology's

Epitaxial growth morphology can be categorized into three distinct types [4], Frank-van der Merwe morphology, Volmer-Weber morphology and Stranski-Krastanov morphology. Each growth morphology can be described by theory in terms of free energies, of the substrate

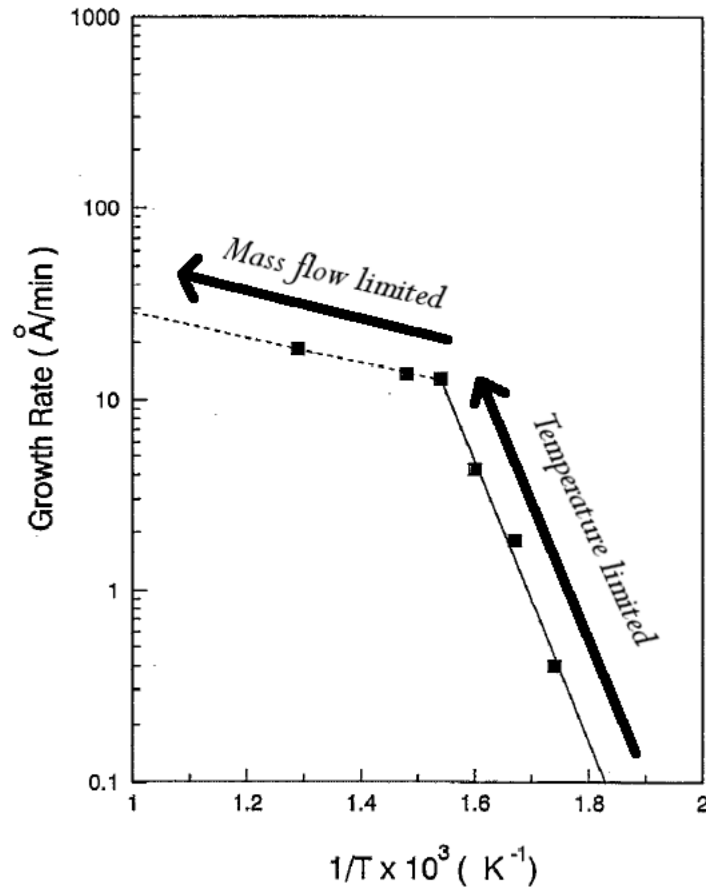


Figure 3.3: *Growth rates as a function of inverse temperature for ultra high vacuum CVD of germanium using GeH_4. Adapted from [13]*

σ_s, interface σ_i and of the layer σ_f, by using the assumption of thermodynamic equilibrium. Thermodynamic equilibrium is when a system is in chemical, mechanical and thermal equilibrium, i.e no chemical, mechanical or thermal processes are taking part in the system. A system reaches thermodynamic equilibrium when the free energy is at a minimum. Although epitaxy is often under dynamic equilibrium, it is useful to first consider the thermodynamic case.

Frank-van der Merwe Morphology

For the case where:

$$\sigma_s \succ \sigma_i + \sigma_f \quad (3.2)$$

The film grows layer by layer forming single crystal, 2D flat films (See Figure 3.4). This is due to the adatoms preferring to attach to surface sites.

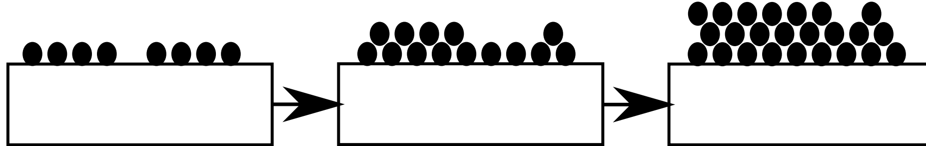


Figure 3.4: *Frank-van der Merwe morphology*

Volmer-Weber morphology

For the case where:

$$\sigma_s \prec \sigma_i + \sigma_f \quad (3.3)$$

The film grows in 3D islands (See Figure 3.5), giving a rough surface. This is due to the attractions between adatoms being stronger than that between the adatom and the surface.

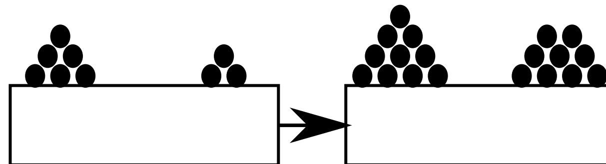


Figure 3.5: *Volmer-Weber morphology*

Stranski-Krastanov (SK) morphology

SK morphology is a combination of the two previously mentioned growth modes (See Figure 3.6) and is common where there is a lattice mismatch between substrate and layer. It can be split into three stages. First, the adsorbate grows pseudomorphically, forming layer by layer what is known as the 'wetting layer' on the substrate. However, due to the lattice

mismatch causing strain in the wetting layer, when the thickness reaches a certain limit, 3d island growth takes over. Eventually, the 3D islands begin to coalesce.

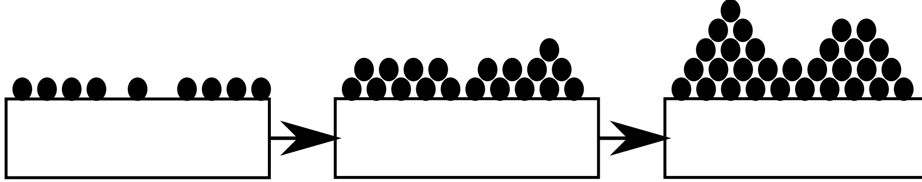


Figure 3.6: *Stranski-Krastanov (SK) morphology*

There is extensive experimental evidence of SK morphology when Ge is grown on Si (001) [18], [71], [23].

Dynamic Equilibrium

The thermodynamic explanation given earlier for the different growth modes does not fully explain the growth observed in germanium. The explanation uses the assumption of thermodynamic equilibrium, the free energy of the 3d clusters competing against that of the epitaxial film. However, kinetic processes are also responsible for the formation of 3D islands [69], [37]. In [69], the intrinsic stress of the germanium film during growth is presented, for different growth temperatures (see figure: 3.7). Intrinsic stress has been shown to be a good indicator to follow the stages of S-K growth. From figure: 3.7, the different gradients clearly indicate the three stages of growth (I , II , III). The first stage, (I), on Figure (3.7) has a film stress near the bulk misfit stress of Ge on Si. This coincides with the formation of the wetting layer of S-k growth. The second stage ,(II), on Figure (3.7), has smaller film stress than stage (I). This coincides with island growth, the islands help to relieve the stress because in their top layers the lattice spacing can return to a value approaching the Ge's bulk value. In the third stage, (III), the stress is reduced still further, this is due to the merging of Ge islands.

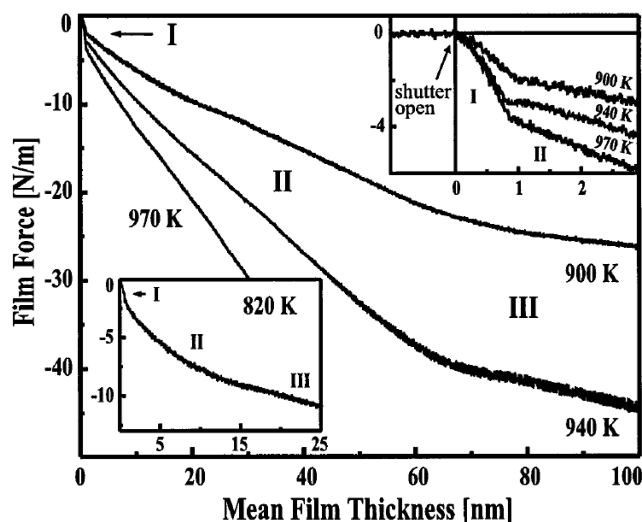


Figure 3.7: *Representative examples of the film forces of Ge/Si*(001) *vs average mean film thickness, from [69]. Measured in situ during growth using a cantilever beam device for a Ge on Si(001) layer grown by MBE. Taken from [69]*

3.3 Epitaxial Growth of Ge on Si(001) - Nucleation and Early Stages of Growth

In Goldfarb *et al* [20] the initial stages of growth of Ge on Si (001) by GeH_4 (using gas source MBE [1]) were studied using low-energy electron diffraction (LEED/Auger) and reflection high-energy electron diffraction (RHEED). Initially, the (2 x N) reconstruction is seen on the 2D strained wetting layer [68] . This is caused by the strain energy from the lattice mismatch, with the (2 x N) reconstruction forming strain-relieving trenches. In the film near each trench, the Ge can relax slightly, this relieves the strain. The (2 x N) reconstruction can be described a periodic array of missing dimers of the (2 x 1) dimer reconstruction, where each Nth dimer of the (2 x 1) reconstruction is absent [68] . In the STM images in Figure (3.9) the (2 x N) reconstruction can be seen. The geometry of the (2 x N) reconstruction is shown in figure 3.8 for N=6.

[1] Gas source MBE while similar to CVD, does have some differences. Growth processes observed during gas source MBE can only be used as a guide to those occuring during CVD

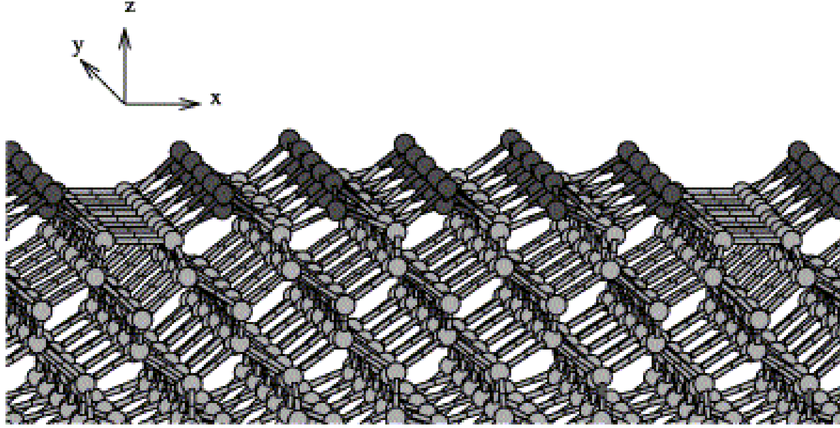


Figure 3.8: *Geometry of the (2n) reconstruction of Ge on Si(0 0 1) when n=6, where light spheres are Si and dark spheres are Ge. Dimer rows, missing-dimer trenches and normal to the surface lie along mutually perpendicular x, y and z directions. Taken from [46]*

.

3.4 Epitaxial Growth of Ge on Si(001) - Critical Thickness

The applications discussed in Chapter 2 all require layers of Ge that are thicker than what is known as the *critical thickness.* When an epilayer is grown on a substrate with a small lattice mismatch, the first layers to be grown are strained to accommodate the mismatch. At the critical thickness, the strain energy becomes so large that plastic relaxation occurs and misfit dislocations are introduced at the Ge/Si interface to relieve the strain [51].
For pure Ge on Si grown with MBE, a value of the critical thickness has been experimentally determined using grazing-incidence x-ray diffraction in [70]. The MBE grown Ge layer begins to relax after 3 to 4 monolayers, this coincides with when island growth starts. The early stages of growth of Ge on Si (0 0 1) by MBE have slight differences to the early stages of growth of Ge on Si (0 0 1) grown using CVD. When Ge is grown using germane by CVD, the thickness of the wetting layer before the critical thickness is reached has been found to be dependant on temperature. In [20], a range of $\sim$ 4 ML at 620 K to $\sim$ 9 ML at 700 K was recorded. The reason for this is thought to be the effect of the hydrogen acting as

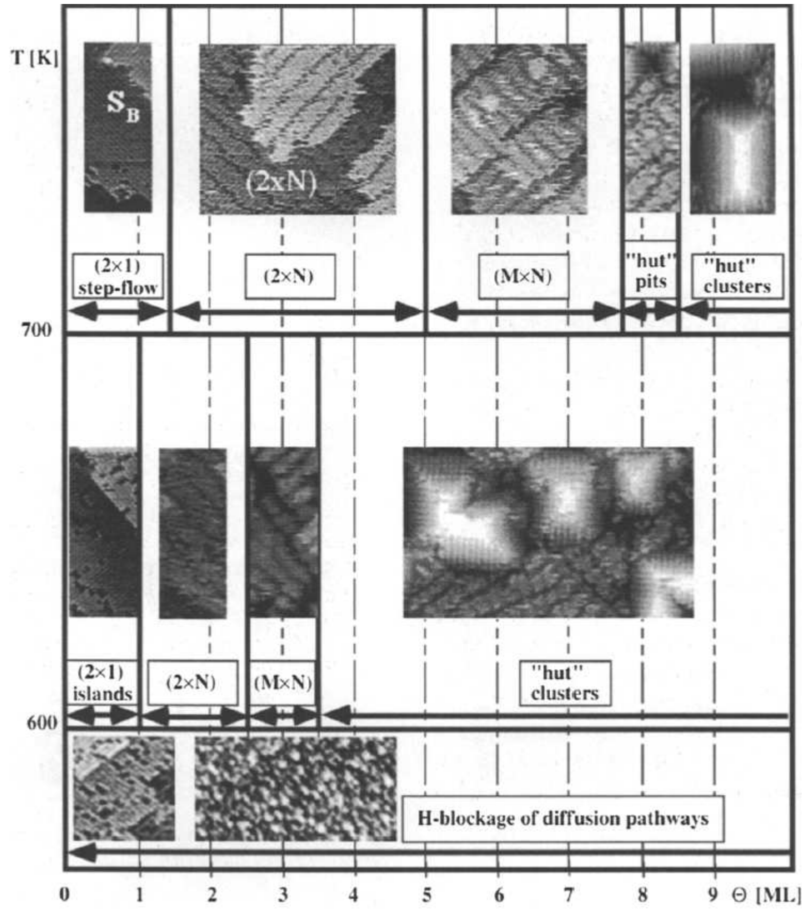


Figure 3.9: *Diagram describing the main stages of Ge/Si(001) growth from GeH_4 using gas source MBE, at $10^{-6} < p < 5 \times 10^{-5}$ Pa. Taken from [20]*

a surfactant during the early stages of growth [68], [28]. This can be seen in figure 3.9, where at higher temperatures the wetting layer is thicker before the growth of hut clusters occurs. If a thick wetting layer is grown at a higher temperature, a rectangular (M x N) grid is formed on the surface. This provides more strain relief than the (2 x N) reconstruction, since the (2 x N) reconstruction only provides strain relief in one-dimension [68].

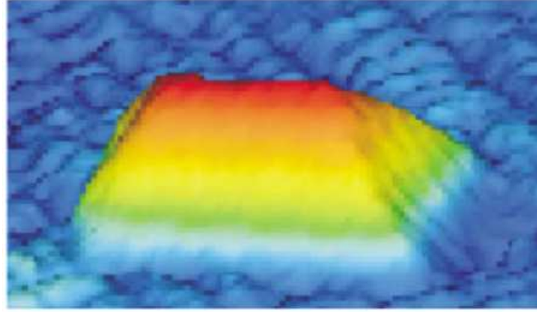


Figure 3.10: *Perspective representation of STM data of a Ge hut cluster on Si, with image area 300 nm x 300 nm. Taken from [21]*

3.5 Epitaxial Growth of Ge on Si(001) - 2D to 3D transition and Ge Hut Clusters

The evolution of Ge on Si(001) hut clusters has been the subject of research by many groups, because they can potentially be used as quantum dots with applications in devices. After the critical thickness has been exceeded, island growth can occur. The transition from 2D growth to 3D growth with the formation of hut clusters has been shown to take place after approximately 3 monolayers [18], [32] for Ge growth by MBE, coinciding with the critical thickness. In CVD the formation of islands has also been shown to occur after the critical thickness.

The reason for hut cluster growth is the misfit strain remaining in the wetting layer. Hut cluster growth helps to relax the misfit strain because in the upper layers of the hut cluster, the Ge's lattice parameter is free to tend towards its bulk value (See Figure 3.11). This has been confirmed by x-ray measurements in [60] that showed that at the Ge/Si interface the hut clusters were almost fully strained, before a continuous relaxation to the top of the hut cluster, where the Ge was relaxed.

The clusters are 'streched' pyramids, with (105) faces aligned along $\langle 100 \rangle$ and $\langle 010 \rangle$ on the Si substrate. These hut clusters could be used to produce quantum dots without using lithography and have a possible application in optoelectronics [68]. If the islands are sufficiently small, electron-hole pairs can be captured and recombine, emitting light.

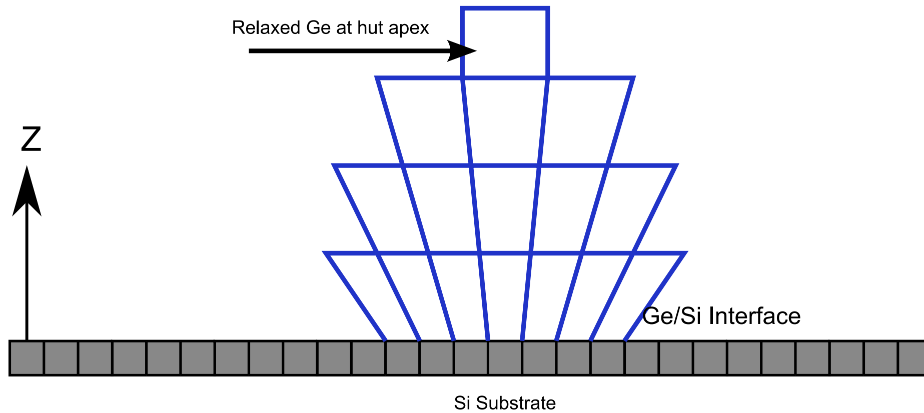


Figure 3.11: *Diagram illustrating relaxation of Ge hut cluster from interface to apex*

If growth is continued, the 3d pyramidal huts reach a critical volume and they grow into domes with octagonal bases [17] , [35]. This is energetically favourable, with pyramidal huts having more energy than domes [52]. The critical volume for dome formation has been found to vary with growth conditions [35].

3.6 Epitaxial Growth of Ge on Si(001) - Suppression Of 2D To 3D Transition At Low Temperature

The 2d to 3d transition of the Stranski-Krastanov growth mode (i.e hut clusters) can be avoided for Ge on Si (0 0 1) grown with CVD if a low growth temperature is used. In [21], layers of Ge were grown at 330°C and reflection high energy electron diffraction (RHEED) was then used to find the in-plane lattice parameter during growth and x-ray diffraction was to find the strain after cooling. It was found that at 330°C, no 3D growth was observed and approximately 90% of the relaxation mainly occurred during the first 2 ML of growth. Cross sectional TEM was used to observe the modes of relaxation and stacking faults were observed in the (1 1 1) plane and misfit dislocations at the interface. This suppression of the 3D transition is highly desirable since it allows Ge buffer layers to be grown, that are of sufficient quality that high quality layers of Ge cn be grown on top.
The low temperature suppression of the 3D transition is due to the surface diffusion of Ge. While temperature will affect the surface diffusion, it is likely that it is the presence of

hydrogen that is suppressing the 3D growth. This is backed up by research done by MBE is the presence of hydrogen. In [28], MBE is used to grow Ge with and with out hydrogen. The presence of hydrogen was found to lower the diffusivity for the Ge adatom.

Chapter 4

Techniques

This chapter describes the characterisation techniques used in this thesis. The following techniques are described, high resolution x-ray diffractometry (HR-XRD), atomic force microscopy (AFM) and transmission electron microscopy (TEM). The simplified theory and method are described for each technique.

4.1 X-Ray Diffraction

High resolution x-ray diffractometry can be used to find lattice spacing very accurately and hence find the degree of strain/relaxation. All X-Ray diffraction in this study was carried out using a Panalytical X'Pert PRO Materials Research Diffractometer. The diffractometers x-ray tube was operated at 45kV and 40 mA, producing $CuK\alpha_1$ x-rays. Before hitting the sample the x-ray beam passes through a collaminating slit and a 4 bounce Ge(220) hybrid monochromator, giving a collaminated, monochromatic beam. A Ge crystal was positioned in front of the x-ray detector, the use of an analyser crystal in this manner is called triple-axis diffractometry [6] . The Ge crystal reduces the angular acceptance of the detector and in combination with the beam collaminator, defines a small volume of reciprocal space (see section on reciprocal space mapping). This allows high resolution reciprocal space maps to be produced for samples, giving detailed information about layers. A GPW3011 Gas Proportional Detector with automatic attenuator was used for the bulk of the XRD work.

Rocking curves

The degrees of freedom for the sample and detector are illustrated in Figure (4.1). In a rocking curve, ω is fixed and $\omega - 2\theta$ is "rocked" around a Bragg peak.

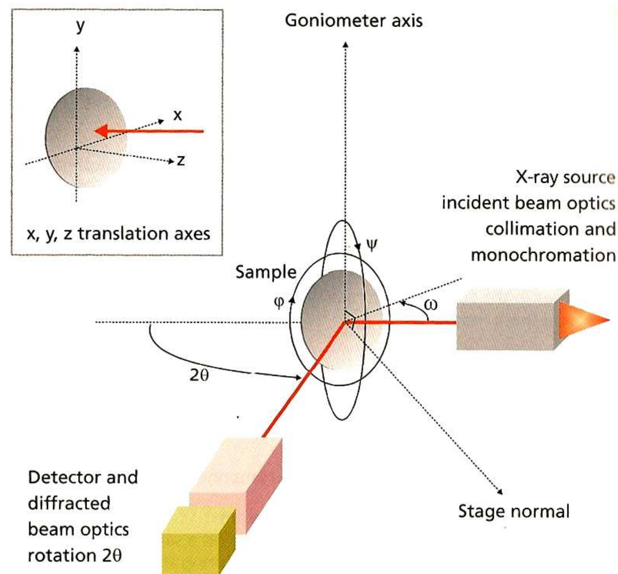


Figure 4.1: *Key components of diffractometer. Taken from [47]*

Reciprocal space mapping

Reciprocal space maps are comprised of a collection of rocking curves, over a range of angles for ω. The rocking curves are translated into reciprocal space using Panalyticals X'Pert Epitaxy software.

Theory -Understanding Ewalds Sphere and Reciprocal Space

The reciprocal space lattice axis (b_1, b_2, b_3) are defined as being:

$$b_1 = \frac{a_2 \times a_3}{a_1 \cdot (a_2 \times a_3)} \tag{4.1}$$

$$b_2 = \frac{a_3 \times a_1}{a_2 \cdot (a_3 \times a_1)} \tag{4.2}$$

$$b_3 = \frac{a_1 \times a_2}{a_3 \cdot (a_1 \times a_2)} \tag{4.3}$$

From Figure 2.1 it can be seen that the angles between the unit cell lattice vectors are $\alpha, \beta, \gamma = 90^0$. Since the cross product of two vectors with an angle of 90^0 is 1 , (4.1, 4.2, 4.3) simplify to:

$$b_1 = \frac{1}{a_1} \tag{4.4}$$

$$b_2 = \frac{1}{a_2} \tag{4.5}$$

$$b_3 = \frac{1}{a_3} \tag{4.6}$$

This result is very useful in interpreting reciprocal space maps (RSM's). To understand diffraction in reciprocal space, a geometrical construct called Ewalds Sphere is often used (See figure 4.2).

Ewalds sphere has a radius of $1/\lambda$ and passes through the origin of the reciprocal lattice. The incident x-rays enter the sphere along a radius. Diffraction will occur if a reciprocal lattice point lies on the circumference of the circle, i.e the conditions for Braggs law are met when a reciprocal lattice point lies on the circumference of Ewalds sphere.

Diffraction occurs when:

$$K_f - K_i = Q \tag{4.7}$$

Where K_f is the wave vector of the diffracted wave, K_i the wave vector of the incident wave and Q is defined as the scattering vector. The following shows that this is equivalent to the conditions for Braggs law being met:

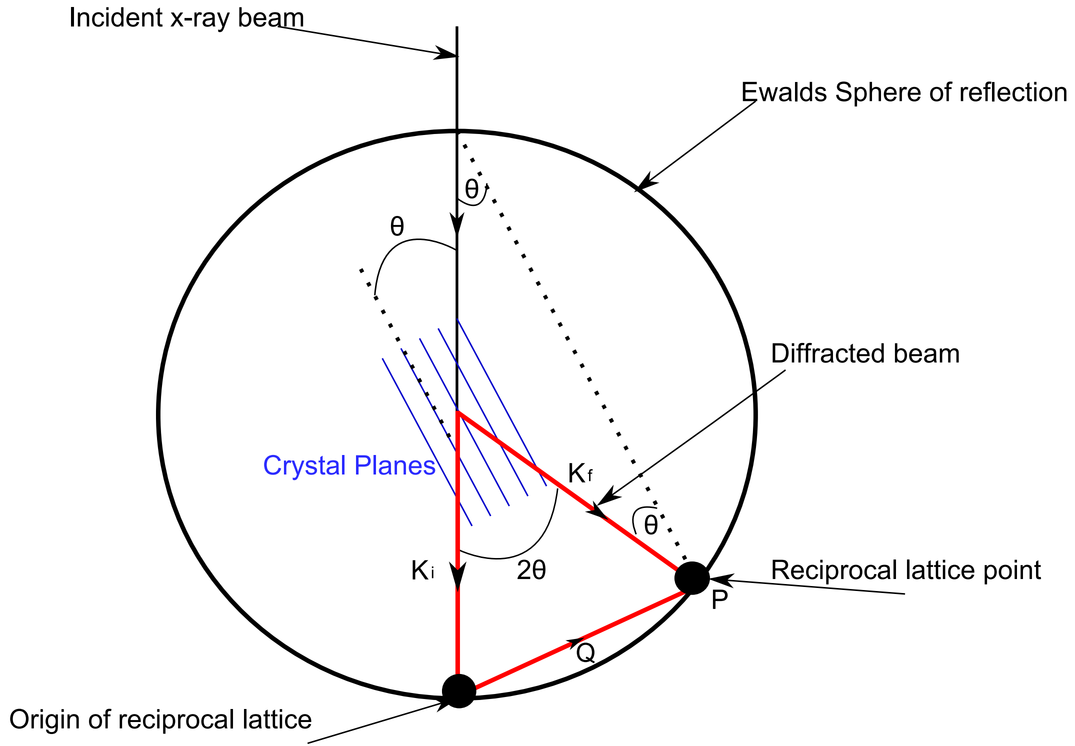


Figure 4.2: *Ewalds sphere*

From figure (4.2) and its radius $1/\lambda$:

$$Sin\Theta = \left(\frac{|Q|}{2}\right) / \left(\frac{1}{\lambda}\right) \tag{4.8}$$

Since in reciprocal space, from 4.4, 4.5 and 4.6 (Where d is the spacing between planes)

$$|Q| = 1/d \tag{4.9}$$

$$Sin\Theta = \lambda/2d \tag{4.10}$$

For XRD on silicon and germanium, to infer structural information, the Bragg peaks from symmetric (004) and asymmetric (224) Miller planes are the most commonly used. These planes are illustrated in figure 4.3. As can be seen from figure (4.3), the Bragg peak from the (004) planes only carries information about the out of plane lattice parameter, a_z, while

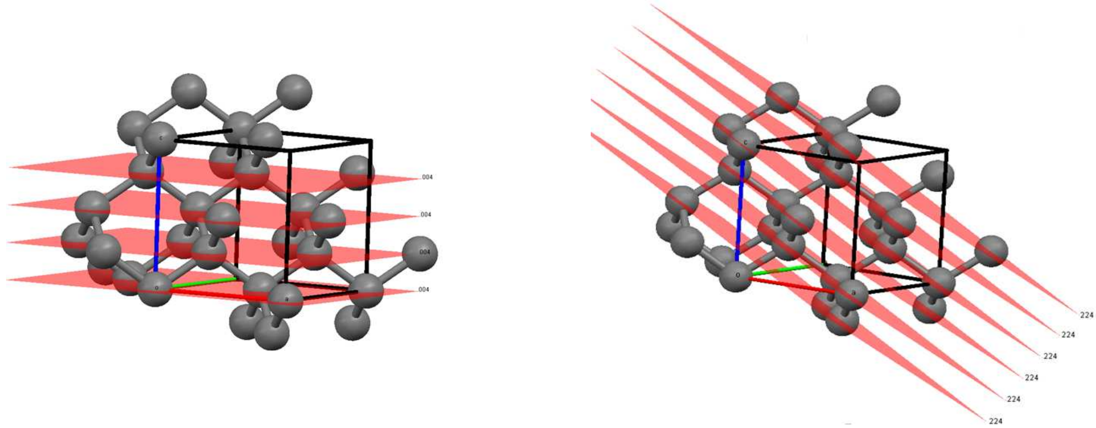


Figure 4.3: *(004) (left) and (224) (right) planes in Silicon/Germanium*

the peak from the (224) set of planes carries information about both the in plane and out of plane lattice parameters a_x and a_z. Due to this the (004) and (224) peaks are useful because they can be used to determine the size of both in plane and out of plane lattice parameters. For a given material, in this case Ge and Si, the reciprocal lattice can be illustrated by a pattern of dots (See figure 4.4. Each point in the reciprocal lattice has a distance of $1/d_{hkl}$ from the origin 0, thus diffraction occurs at each point. A diagram of this kind is useful, because it lets us choose a region of reciprocal space to investigate.

From figure 4.4 it can be seen that the reciprocal lattice points for Ge are always slightly closer to the origin than those for Si. This is because the distance to the origin is proportional to the reciprocal of the crystals lattice parameter and Ge has a larger lattice parameter than Si.

Structure Factors

The measure of the scattering amplitude of a wave by an isolated atom is given by the atomic form factor, f, in Equation (4.11). Where $\rho_e(r)$ is the charge density, Q the scattering vector and r the radius.

$$f = \int_{at} \rho_e(r)\, e^{(-iQr)} dr \tag{4.11}$$

The resultant wave scattered by the collective atoms in a unit cell is called the *structure*

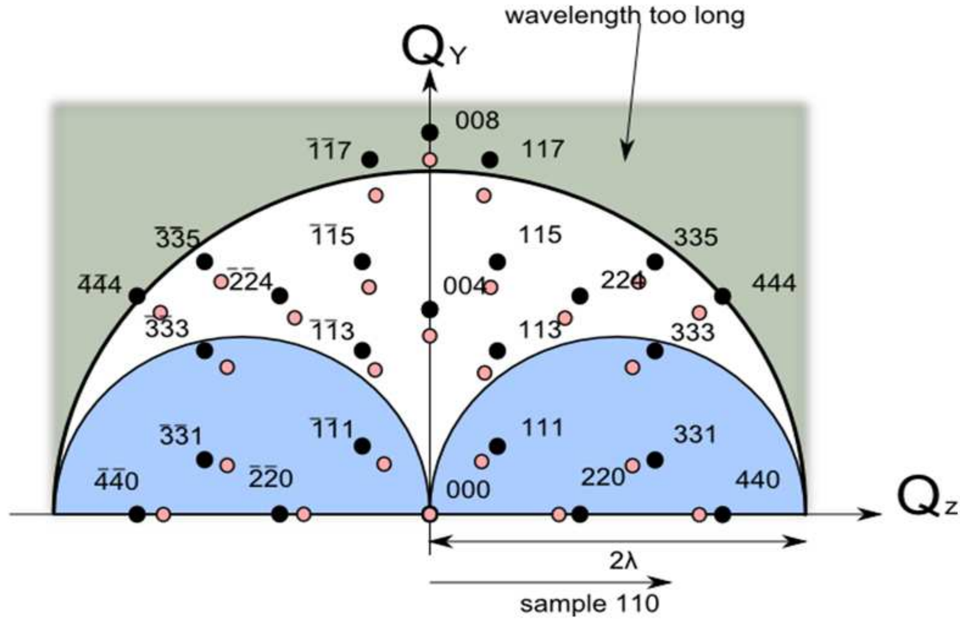


Figure 4.4: *Reciprocal lattice points for Si (black) and Ge (Pink). The Miller indices refer to the adjacent Si peaks, with their Ge counterparts displaced towards the origin*

factor, F. It can be found by integrating over the total charge distribution of the unit cell. This is given by equation (4.12).

$$F = \int_{uc} \rho_e(r) e^{(-iQr)} dr \tag{4.12}$$

An approximation of (4.12) can be found by summing all the waves scattered by individual atoms in the unit cell [5]. Since Equation (4.11) is the wave scattered by an individual electron, this gives Equation 4.13, where N is the total number of atoms in the unit cell, numbered by n, counted from 1 to N.

$$F = \sum_{n=1}^{N} \int_{at} \rho_e(r) e^{(-iQ(r-r_n)))} dr \tag{4.13}$$

For a single atom the integration over the charge distribution is already known from the atomic form factor given in equation 4.11. This can be used to simplify Equation (4.13) giving Equation (4.14) where f_i is the atomic form factor of the nth atom and r_n is the vector specifying the position of atoms in the unit cell (given by $r_n = u_n a + v_n b + w_n c$, where u, v and w are the atoms positions measured in units of the unit cell vectors).

$$F = \sum_{n=1}^{N} f_n e^{(-iQr_n)} dr \tag{4.14}$$

The Laue conditions state that $Q \cdot (a+b+c) = 2\pi\,(h+k+l)$. The explanation and proof of the Laue equations for refraction was excluded for brevity, but can be found in [5]. If the Laue conditions and the full expression for r_n are substitute into Equation (4.14), a final expression expression for the structure factor is given, Equation (4.15).

$$\boxed{F = \sum_{n=1}^{N} f_n e^{(2\pi i(hx_n+ky_n+lz_n))} dr} \tag{4.15}$$

The structure of Si and Ge is based on the cubic unit cell. In the FCC lattice there atoms located at $(0,0,0)$, $\left(\frac{1}{2},0,\frac{1}{2}\right)$,$\left(\frac{1}{2},\frac{1}{2},0\right)$ and $\left(0,\frac{1}{2},\frac{1}{2}\right)$. When these positions are substituted into Equation (4.15), it gives Equation (4.16).

$$F = f_n\left(1 + e^{(\pi i(h+l))} + e^{(\pi i(h+k))} + e^{(\pi i(k+l))}\right) = \begin{cases} 4f, & \text{all } hkl \text{ even or odd} \\ 0, & n \text{ mixed} \end{cases} \tag{4.16}$$

Equation (4.16) gives a non zero structure factor if h,k,l are all even or all odd. This is the first condition for a bragg peak to be visible in Si or Ge.

In the unit cells of Si and Ge, there are also atoms attached to the basis of the lattice points at $(0,0,0)$ and $\left(\frac{1}{4},\frac{1}{4},\frac{1}{4}\right)$. When these positions are substituted into Equation (4.15), it gives Equation (4.17).

$$F = f_n\left(1 + e^{\left(\frac{\pi}{2} i(h+k+l)\right)}\right) = \begin{cases} 2f, & h+k+l = 2n \\ 0, & 0 \text{ otherwise} \end{cases} \tag{4.17}$$

For Equation (4.17) to give a non zero structure factor, $h+k+l$ must not be an odd multiple of two. This is the second condition for a bragg peak to be visble in Si or Ge.

The exact values for the structure factors for Silicon are given in Table 4.1. Since the square of the structure factor gives the intensity of the bragg peak, it can be seen why the (0 0 4) and (2 2 4) peaks are used for XRD in this study, both giving a large intensity in comparison with other peaks.

Crystal Plane	$\lvert F_{hkl}\rvert$ $\lvert F_{hkl}\rvert /V$ in Electron Units per Cubic $\mathring{A}$ for One Crystal of silicon
001	0
001	0
004	0.39
111	0.38
222	0
333	0.24
011	0
022	0.45
044	0.31
112	0
224	0.34
113	0.34
115	0.24

Table 4.1: *Values of $\lvert F_{hkl}\rvert$ for Silicon.*

Interpreting Reciprocal Space Maps

Figure 4.5 shows a real example of an (0 0 4) and (2 2 4) RSM. A relaxed Ge layer will have $a_x = a_y = a_z$, with each 4.2% less than the values for Si. This will mean that the Ge(0 0 4) peak is shifted along the Q_y axis towards the origin (with respect to the Si peak) on the RSM and the (2 2 4) Ge peak is on a line from the Si (2 2 4) peak to the origin. However, biaxial tensile strain causes the out of plane lattice parameter to increase and the in plane lattice parameter to decrease. The causes the Ge peak to shift in the direction of the arrow shown in Figure (4.5). Under biaxial compressive strain the shift is in the opposite direction. If the Ge layer is fully strained it will take on the Si in-plane lattice parameter and so the (2 2 4) peak will occur at the same Q_z value as Si.

To obtain values for the unit cell lattice parameters (a_1, a_2, a_3) from a RSM, Equation (4.9) can be used to give d_{hkl}, the distance between each plane crystal plane. This can then be

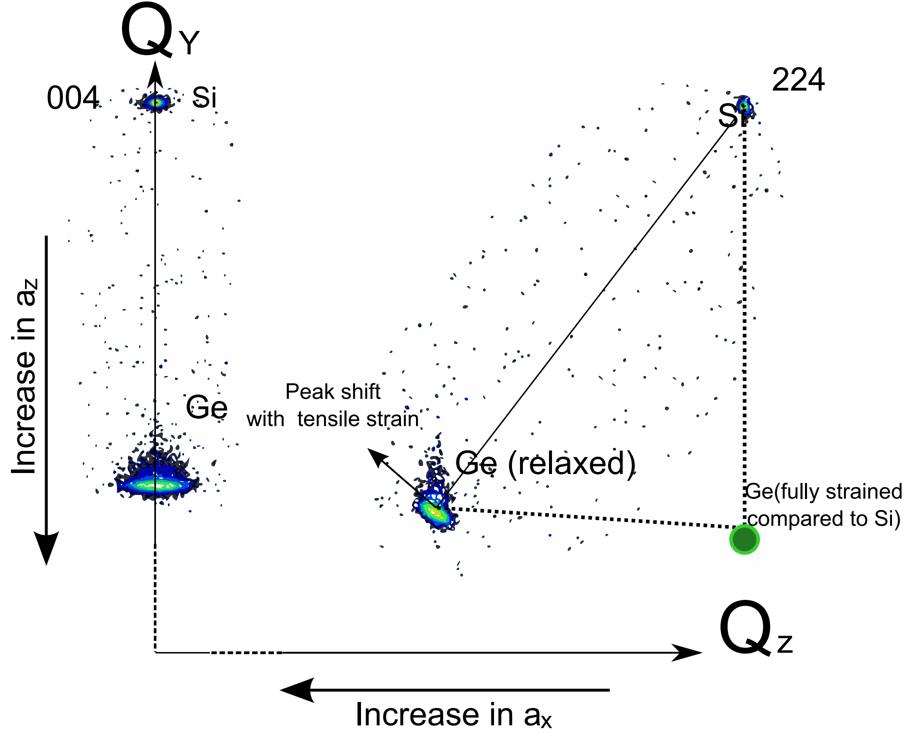


Figure 4.5: *RSM of approx 40nm layer of Ge on Si, with the affect of strain on the Ge Peak illustrated*

used in conjunction with Equation 4.18 (The plane spacing in an orthogonal crystal system with miller index (hkl)) to give the crystals lattice parameters. If the Ge layer is tilted when compared to the substrate, the tilt must be taken into account when calculating its lattice parameters.

$$d_{hkl} = \frac{1}{\sqrt{\left(\frac{h}{a_x}\right) + \left(\frac{k}{a_y}\right) + \left(\frac{l}{a_z}\right)}} \tag{4.18}$$

From the lattice parameters of the Si substrate and Ge layer, the Ge layers relaxation can be found using (4.19), where $a_{substrate} = a_{Si}$ and $a_{layer} = a_{Ge}$. If the Ge has its bulk lattice parameter it will be 100% relaxed and if it takes the lattice parameter of the Si substrate the relaxation will tend towards 0%. If the Ge layers relaxation goes above 100%, it is referred to as being over-relaxed and is under tensile strain.

$$R = \frac{a_{substrate} - a_{layer}}{a_{substrate} - a_{layer(bulk)}} \tag{4.19}$$

Panalytical X'Celerator X-Ray Detector

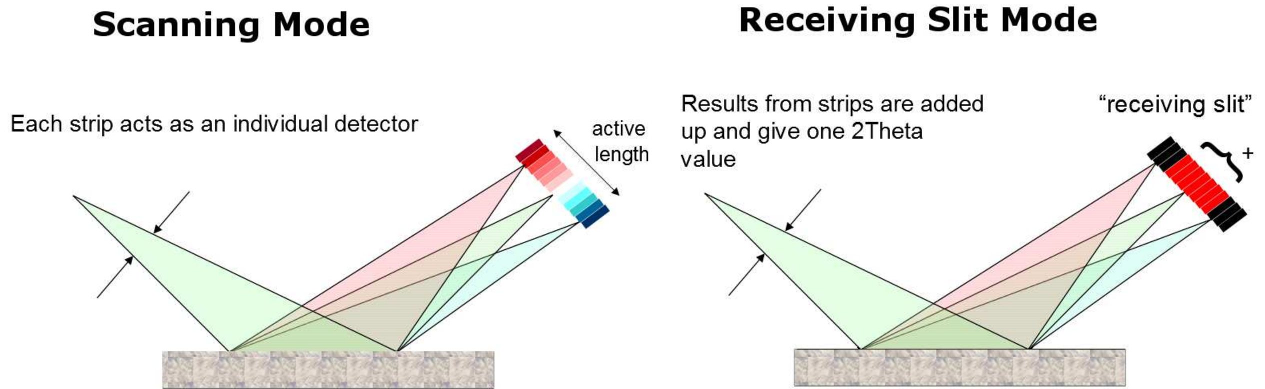


Figure 4.6: *Illustration of scanning mode and receiving slit modes of X'Celerator detector*

One RSM was taken using a Panalytical X'Celerator detector. The X'Celerator detector is a solid state x-ray detector comprised of 128 parallel detector strips on one substrate. The X'Celerator has two modes [48], scanning mode and receiving slit mode (See figure (4.6)). In scanning mode, each strip acts as an individual detector. This ability to measure the x-ray fluence at more than one angle concurrently greatly reduces the time taken for a $\omega - 2\theta$ scan. In receiving slit mode, the results from each strip are summed to give one 2θ value. This mode is used for alignment. The reason for using the X'Celerator detector for one RSM is to investigate if it is suitable for future XRD measurements on Ge layers on Si and to see how it compares to the GPW3011 Gas Proportional Detector.

Using The Panalytical X'Celerator Detector

To explore the possibility of reducing the time taken to produce each RSM, an RSM (showing 004 and 224 Bragg peaks) was produced using a Panalytical X'Celerator detector instead of the the standard Panalytical PW3011 Gas Proportional detector. Sample a) (See Chapter 6 was used for this study. The X'celarator detector gave the relaxation of the Ge layer as 95.5% with an uncertainty of 6% where as the pw3011 detector gave the relaxation as 100.5% with an uncertainty of 0.7%. The X'celerator detector took $\approx$ 30 mins for the RSM while

the pw3011 took $\tilde{2}4$ hours. For comparison, the RSM from each detector is given in Figures (4.7) and (4.8). In the RSM from the X'celerator detector (Figure) there is a broadening in the 2θ direction, giving stretched peaks. This effect appears most pronounced in the Si 224 peak.

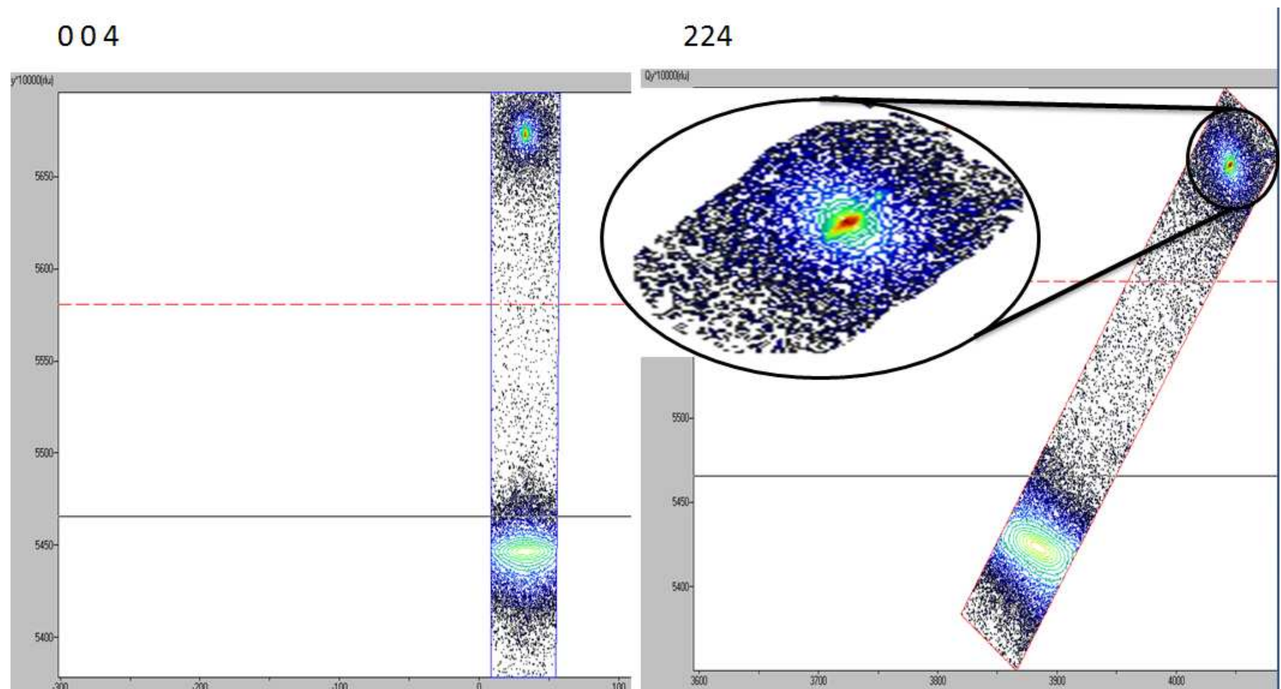


Figure 4.7: *RSM obtained from as grown wafer with a growth temperature of* $500° C$*, using Panalytical PW3011 Gas Proportional detector*

X-Ray Detector Comparison, X'Celerator and Gas Detectors

The relaxation measured with the X'Celerator detector has an uncertainty of 6% compared with an uncertainty of of 0.7% for the PW3011 Gas Proportional detector. The large error clearly shows that the the X'Celerator detector is unsuitable for research of this kind, where a very accurate value for the crystals lattice parameter is needed. For this reason, only the PW3011 Gas Proportional detector was used in this research. In figure (4.8) the Bragg peaks recorded with the X'Celerator detector can be seen to be 'streched', this is due to the detectors poor resolution in the 2θ direction. It is this that gives a large uncertainty in the position of the peak, giving a large error for the relaxation.

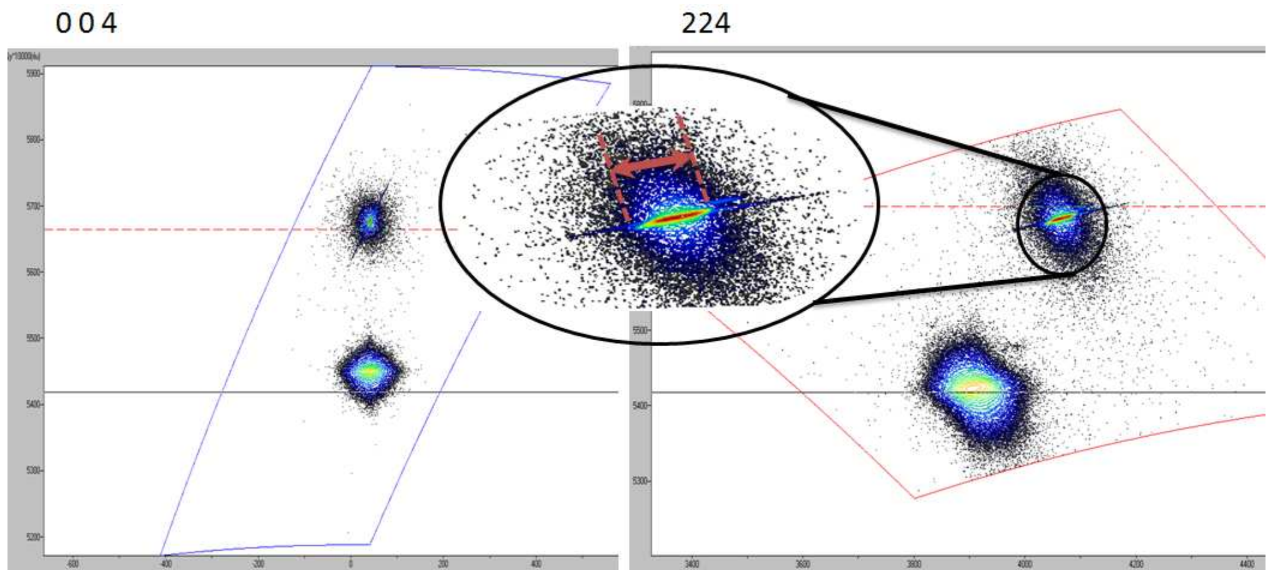


Figure 4.8: *RSM obtained from as grown wafer with a growth temperature of* $500°C$*, using Panalytical X'Celerator detector*

Though the X'Celerator detector is inaccurate for lattice parameter measurement, due to its high scanning speed (30 mins Vs 24 hours for Gas Proportional detector) it might be very useful for other tasks in semiconductor characterisation. If two points in reciprocal space can be mapped in 30 mins, then the entire portion of reciprocal space observable by the x-ray machine (See Figure (4.4) could be mapped in a short time period. An example of when this would be useful would be when working with a substrate with a non-standard orientation. The entire accessible reciprocal space could be quickly mapped using the X'Celerator detector, then specific bragg peaks singled out for further scans using the more accurate gas proportional detector.

4.2 Atomic Force Microscopy

Experimental Technique - Contact Mode

All the Atomic Force Microscopy (AFM) results presented in this thesis were produced using a Veeco Multimode AFM with a Nanoscope IIIa controller (See Figure 4.9) in contact mode. AFM is capable of resolving the height profile of a surface, with very high magnification (

≈ $0.2nm$ vertical resolution)

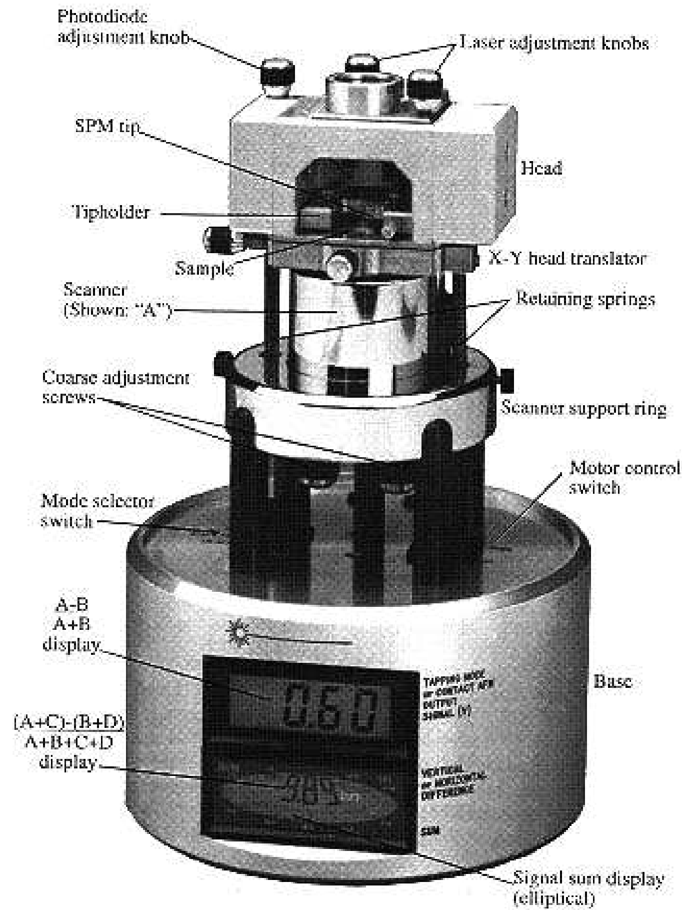


Figure 4.9: *Veeco Multimode AFM. Reproduced from Veeco training manual (Veeco 2000) Digital Instruments.*

The following outlines the operation of the AFM in contact mode: The sample is mounted on a piezoelectric stage and a cantilever with tip attached is lowered towards the surface of the sample. As the tip approaches the sample, forces between the surface and sample cause the cantilever to bend, according to Hooke's law. The tip does not make mechanical contact with the surface. The deflection of a laser beam from the cantilever is measured using a split photo-diode detector. A constant laser deflection is maintained by using feedback from the photo-diode to control the height of the sample. If a constant laser deflection is maintained, then the force between the sample and the tip remains constant. The sample is rastered over an area set by the software and the computer records the z position of the sample at each (x,y) position and from this an image of the samples surface morphology is formed.

For all the AFM imaging in this work, a silicon nitride tip and cantilever was used, with a tip size of $\approx 20nm$.

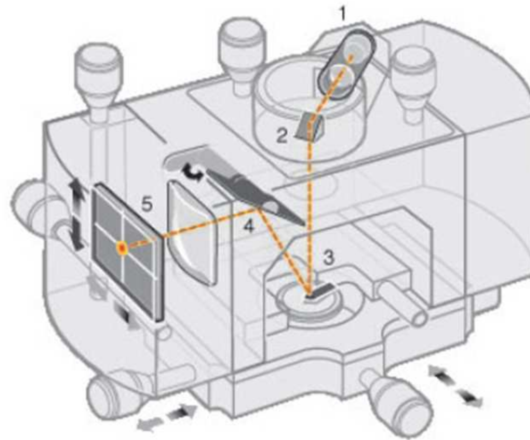


Figure 4.10: *AFM Head of Veeco Multimode AFM. The labelled parts are: 1)Laser, 2)Mirror, 3)Cantilever, 4)Tilt Mirror and 5)Photo-detector. Reproduced from Veeco training manual (Veeco 2000) Digital Instruments.*

Analysis of AFM Images

All the AFM images were analysed by Veeco Nanoscope (2007) software. Before a value of the RMS surface roughness can be found from the surface image, the image must be processed to remove artefacts. Care must be taken not to reduce actual features during image processing.

Applying a 3rd order *Flatten* operation to each image corrects for vertical offsets in adjacent scan lines. There are many reasons for offsets occurring, including tip damage and dirt on the sample surface. The *Flatten* operation works by using each scan line in a selected area to calculate a least-square fit 3rd order polynomial for each line before subtracted it out [67].

Applying a x,y 3rd order *plane fit* to the image further increases its quality. The *Flatten* operation works by calculating a single polynomial for the whole image and then subtracts it from the image [67] .

The average roughness (R_a) and height range can be found using the *Roughness* operation [67]. If the image contains any anomalies, these can be excluded from the roughness

measurement by drawing a box around only the part of the image that is anomaly free.

4.3 Transmission Electron Microscopy

All transmission electron microscopy (TEM) work presented in this research was carried out by project students Toby Gould and Leigh Sangan using a JEOL JEM-2000 FX tunnelling electron microscope. TEM uses a focussed beam of high energy electrons to form an image of a sample.

A simplified description of how the transmission electron microscope operates is as follows (see Figure 4.3): A thermionic electron gun produces a stream of electrons from a tungsten filament. A voltage of approx 200kV accelerates the electrons towards an anode, giving a stream of electrons down the microscope. Magnetic condenser lenses are then used to produce a thin and coherent beam. The beam is passed through a condenser aperture, this controls the spot size of the beam, stopping any electrons at large angles. The beam then hits the mounted sample and is transmitted through parts of it. The magnetic objective lens expands the beam into an image. This is then magnified through more magnetic lenses which correct for artefacts and change the orientation of the image. Finally the image is projected on a phosphor image screen or CCD camera, allowing the final image to be observed.

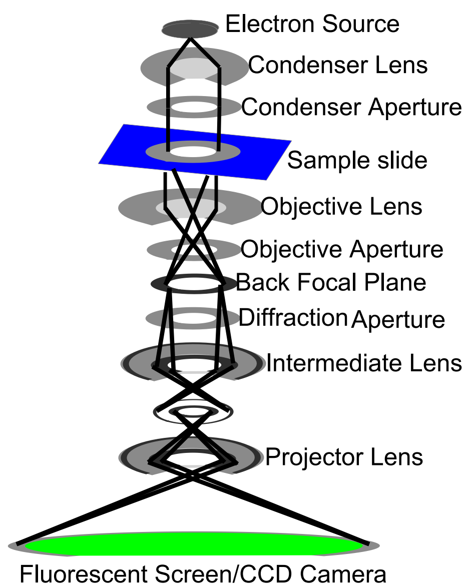


Figure 4.11: *Simplified diagram of TEM*

Chapter 5

Review of Previous Work

As can be seen in Chapter: 2, high quality layers of Ge on Si have many applications. Due to this, it has already been the focus of much research by many groups using many different techniques. In this chapter, some of the most successful techniques used will be summarised.

5.1 Germanium-On-Insulator (GeOI) Substrates

GeOI From Proprietary Techniques

Silicon substrates with a layer of high quality germanium on insulator are available commercially through companies such as Soitec using proprietary techniques such as NanoCleave^{TM}and Smart-Cut^{TM}. Soitec uses a patented Smart-Cut^{TM}process to transfer thin layers of germanium to a silicon substrate. The steps involved in the Smart-Cut^{TM}process are given in Figure 5.1. A layer of silicon oxide is deposited on a Ge transfer wafer and the Si handle wafer oxidised. Before the handle and transfer wafers are bonded, a high dose of H^+ is implanted into the Ge layer. After the donor and handle wafers are then bonded, an anneal causes a build up of H_2 in the defects from the implantation. The pressure of the H_2 causes the wafer to split, freeing the transfer wafer from the handle wafer, but leaving a layer of oxide and Ge attached. Chemical-mechanical polishing (CMP) is then used to produce a smooth surface, giving a layer of high quality Ge on a silicon substrate. A very low defect density can be achieved, since the density in the layer will be largely controlled by the density

in the transfer wafer, which can be grown with a very low density of defects. GeOI wafers grown with proprietary techniques are expensive and less readily available when compared to silicon wafers [8]. futhermore, only a limited range of wafer sizes or Ge thicknesses are available.

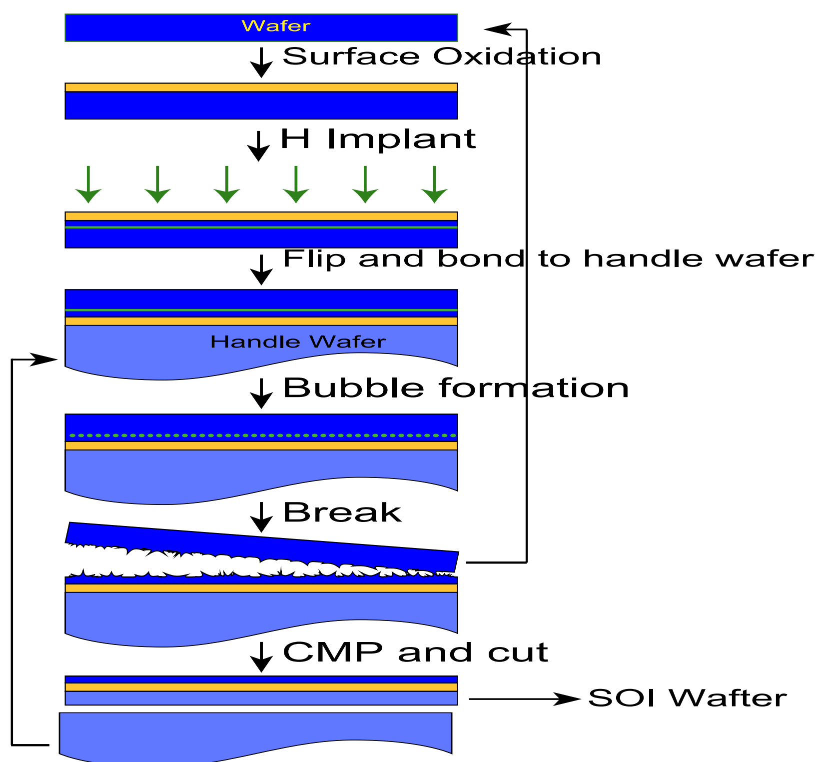


Figure 5.1: *Smart-Cut^{TM}process*

GeOI From Ge-Condensation Technique

Ge or high Ge concentration SiGe, on insulator substrates can be grown by a relatively new method, known as the *Ge-Condensation Technique* [65]. Ge-Condensation Technique involves the dry oxidization at high temperature (1000°C - 1200°C)of a SiGe layer, that has been grown on a silicon-on-insulator (SOI) substrate (See Figure 5.2. The Si in the Sige layer is oxidized preferentially and the Ge atoms are rejected from the growing surface oxide layer and travel into the SiGe layer. The Ge atoms remain in the SiGe layer, since the buried oxide layer prevents further travel. This means that the percentage of Ge in the sandwiched SiGe layer increases with oxidation time.

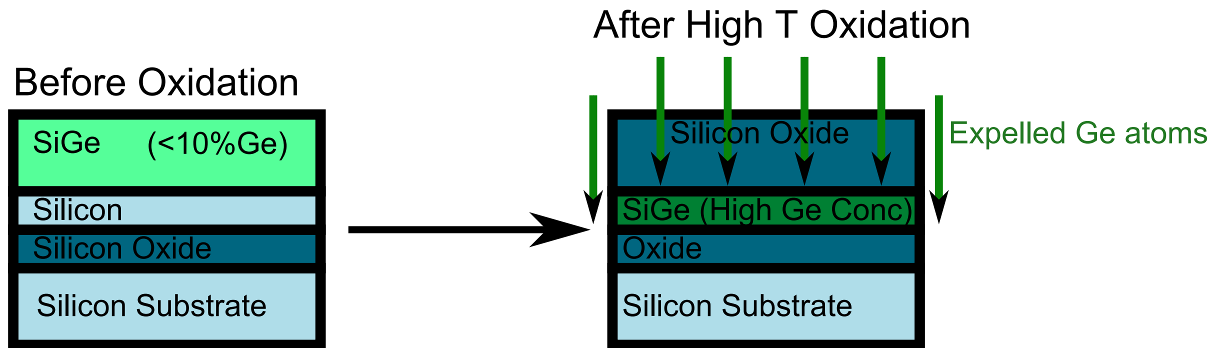


Figure 5.2: *The Condensation technique for SGOI/GeOI formation*

The condensation technique can be used to produce layers of SiGe with very high Ge concentration, approaching pure germanium. In [40] the high temperature oxidization was continued until all the Ge had condensed, giving a thin, pure layer of GeOI. The Ge layer thickness in [40] was reported to be 7nm with an RMS roughness value of 0.4 nm. Growing thick layers of Ge (needed for optoelectronics) with the condensation technique is difficult, with prohibitively long oxidation times needed. A solution to this problem is using a thin Ge layer formed by the condensation technique followed by epitaxial regrowth.

5.2 Growth of High Quality Relaxed Ge Layers Using Compositional Grading

In the growth of relaxed III - V compounds with a lattice mismatch, the use of compositional grading to give a higher quality final layer has been used since the 70's [2]. The same approach can be used for growing Ge on Si, where graded SiGe is used between the the Si substrate and the Ge layer. Unfortunately, when the graded SiGe layer has a high Ge content, high crosshatch surface roughness has been reported in the graded layer along with a high TDD [14]. In [14] a technique for reducing threading dislocation density (TDD) using CMP is presented. The graded SiGe layer is grown upto 50% Ge content before removing 500 nm using CMP. While this technique does give good results, and the final Ge layers are suitable for device fabrication [53], the additional CMP step makes for a relatively complicated process.

5.3 Two Step CVD Growth With Low Temperature Buffer Layer

Two step growth was originally put forward by Colace et al [11] and has been shown to give good results. It is this technique that is used for the Ge layers grown for this research.

The method used to grow the Ge layers has two distinct stages. First a thin low temperature Ge buffer layer is grown, then a thicker high temperature Ge layer is grown on top. Due to the low growth temperature of the first layer and the effect of the hydrogen acting as a surfactant, the first layer can be grown past the critical thickness for transition to 3D growth for the Stranski Krastanov growth mode without 3D growth occurring (As discussed in Chapter 3), with plastic relaxation occurring. The high temperature layer then reduces the dislocation density with a reduction in overall growth time [24].

In Figure 5.3 the RMS roughness of Ge layers is plotted against growth time, for layers with and without low temperature buffer layers. The advantage of using the low temperature buffer layer is apparent, with a large reduction in surface roughness visible when such a buffer layer is used.

The technique has since been improved upon and is often accompanied by one or more annealing stages following growth. This anneal helps to reduce the threading dislocation density [24]

5.4 Multiple Hydrogen Annealing for Heteroepitaxy

In Ammar Nayfeh's thesis [43], he describes Ge on Si layers grown with a newly developed CVD process known as Multiple Hydrogen Annealing for Heteroepitaxy (MHAH) for Ge on Si(0 0 1). The MHAH process gives a smoother layer with fewer threading dislocations reaching the surface (see Figure 5.4)

The following details the method used for MHAH. After a hydrogen bake, a 200nm Ge layer was grown using GeH_4 at 400 °C for 15 mins. The wafer is then annealed for 60 mins at 825 °C. Then a second 200nm Ge layer is grown using GeH_4 at 400 °C for 15 mins, the same

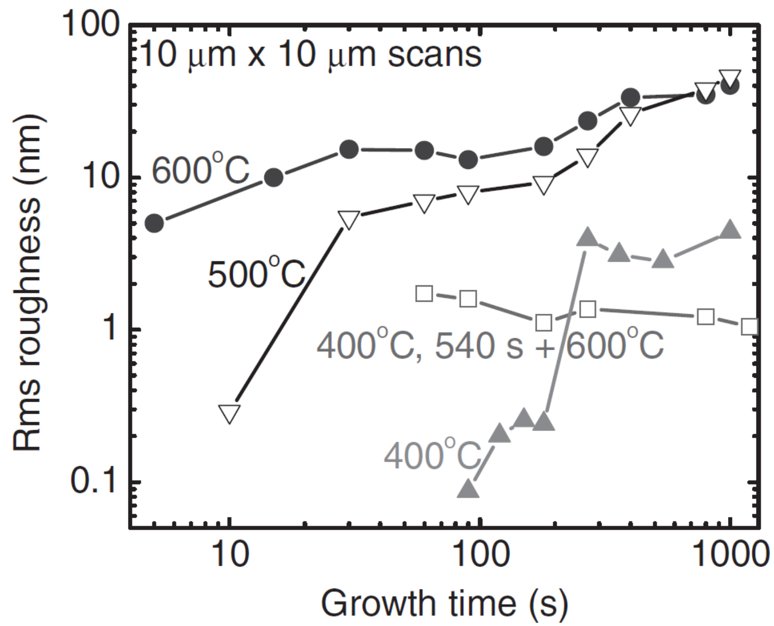


Figure 5.3: *Root mean-square roughness of Ge layers grown at* 400, 500 *and* 600° *C without the buffer layer and at* 600° *C with low temperature buffer layer grown at* 400° *C using* GeH_4 *as a precursor. Taken from [49]*

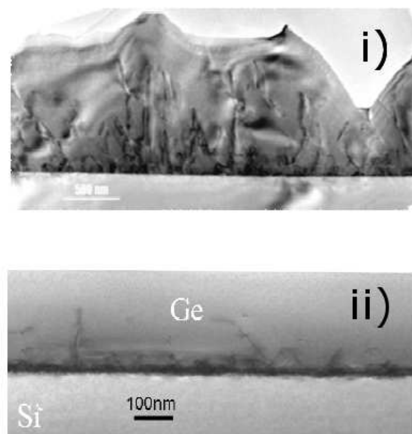


Figure 5.4: *i) Cross section TEM on unannealed Ge On Si Layer. Misfit dislocations can be seen forming at the interface before propagating to the surface as threading dislocations ii) Cross section TEM on Ge On Si grown using MHAH process. Dislocations can be seen to be confined to the interface*

parameters used for the first layer. The wafer is then annealed for a second time for 60 mins at 825 °C.

The Stanford group have had great success with Ge grown on Si (001) using MHAH and have managed to use them in devices such as Ge on Si MOSFET's [42] and Ge on Si photodetectors [45].

5.5 Selective Growth

Ge can be grown epitaxially on a Si substrate that has been patterned with oxide. This can be useful for devices, such as in high speed photodetectors [34]. Ge grown selectively should undergo elastic relaxation giving a low TDD. Unfortunately this has been shown not to be the case, with very high defect densities being recorded [8]. The window size used for Ge growth has been shown to be connected to the TDD. In [66], the role of window size on Ge growth quality is investigated and it was found that that the Ge layer quality increases with a reduction in window size. The reason for this is the misfit dislocations only have to travel to the edge of the window, as opposed to the edge of the wafer to terminate. This gives a reduced chance of interaction and multiplication. The smaller the window, the less chance of interaction and multiplication.

5.6 Summary Of Growth Techniques

In the following table, the results from attempts at MHAH, the two step growth technique and compositional grading are given. The results from other growth techniques are excluded, since they are not directly comparable to the growth method used in this research (Two step growth with hydrogen anneal), due to cost, simplicity etc.

	Layer Thickness	TDD	RMS Roughness	Relaxation
Hartmann, J.M et al [24] (Two Step CVD Growth With Low Temperature Buffer Layer)	$400 - 1600nm$	$9 \times 10^8 cm^{-2}$, reduced to $\prec 2 \times 10^8 cm^{-2}$ with 10x (875 C, 10 min) thermal cycling	$0.6nm$ for the unannealed layer and $2.0nm$ with 10x (875 C, 10 min) thermal cycling	102% without thermal cycling, 115% with
Saraswat et al (MHAH) [43], [42], [45]	$400nm$	$1 \times 10^7 cm^{-2}$	$2.5nm$	$\approx 100\%$
Currie et al [14] (compositionally graded SiGe buffer)	$23\mu m$ buffer, $1.5\mu m$ buffer,	$1.1 \times 10^7 cm^{-2}$	$36nm$	Not given
Currie et al [14] (compositionally graded SiGe buffer with CMP)	$11\mu m$ buffer, $1.5\mu m$ buffer,	$2.1 \times 10^6 cm^{-2}$	$24nm$	Not given

Table 5.1: *Summary Of Growth Techniques*

Chapter 6

Thick Germanium Layers on Si (001)

In this chapter, original research is presented. The method used for the wafer growth is explained and the parameters varied between wafers tabulated. For all wafers, the results from the following chracterization techniques are given: (004) Rocking curves from HR-XRD, layer relaxation calculated from RSM's, surface morphology from AFM, RMS surface roughness from AFM and layer thickness from TEM.

6.1 Wafers Grown Using RPCVD

To investigate the effects of annealing and growth temperature, 10 wafers were grown using GeH_4 as a precursor. The samples were grown using the two step growth with low temperature buffer layer technique.

The following describes the method used for growth: All the wafers were grown with the same low temperature buffer layer, $40nm$ of Ge grown at 500°C . The high temperature layers were grown at a range of different temperatures between 500°C and 700°C, with an approximate thickness of $460nm$. The total thickness of all Ge growth was targeted at $500nm$. As the growth temperature increased it was necessary to slightly decrease the growth time to maintain a comparable thickness, due to the growth rate variation. For each temperature, 2 samples were grown , with one being annealed at 830°C in hydrogen for 10 minutes, the other being left as grown. Table 6.1 summarises the samples grown.

Wafer	Growth Temperature	Anneal at 830°C, for 10 minutes
a	500	No
b	500	Yes
c	550	No
d	550	Yes
e	600	No
f	600	Yes
g	650	No
h	650	Yes
i	700	No
j	700	Yes

Table 6.1: *Growth conditions varied in growth of wafers*

6.2 Roughness and Surface Morphology of Thick Germanium Layers on Si(001) from AFM

To record the roughness and surface morphology of the Ge layer, AFM was used (See Chapter 4 , Techniques). Two $20\mu m$ x $20\mu m$ scans were taken from each wafer in different locations and the final RMS roughness value for each wafer was taken as an average over the two positions. One $10\mu m$ x $10\mu m$ scan was also taken from each wafer for presentation. Figures (6.1, 6.2, 6.3, 6.4, 6.5,) show the $10\mu m$ x $10\mu m$ scan from each wafer.
From Figures (6.1, 6.2, 6.3, 6.4, 6.5,), a trend can immediately be observed: For all wafer pairs grown at the same temperature, the annealed wafer has less fine surface detail. This is very clearly visible in the scans shown in Figure (6.1).
The results from the image analysis for RMS roughness and Rmax are plotted against the high temperature Ge layer growth temperature in Figure (6.6) and Figure (6.7), from which the following trends can be observed. At low growth temperature, the wafers have both high RMS roughness and Rmax, with both values being vastly lower for the annealed wafers. The

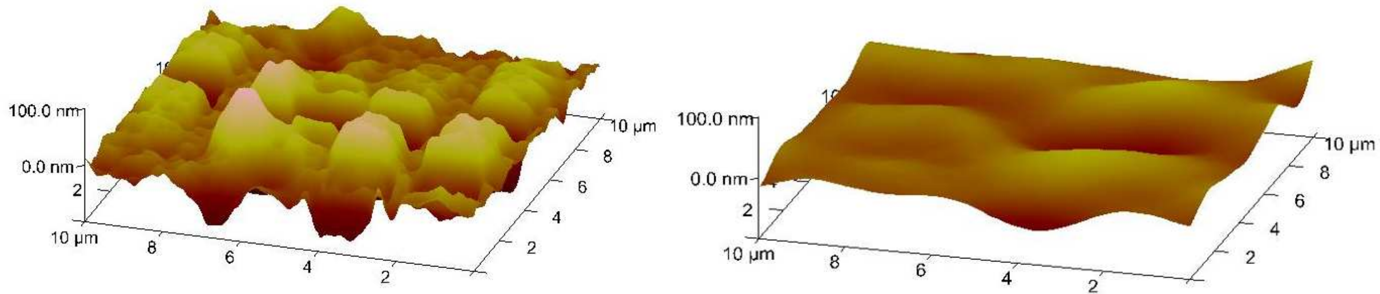


Figure 6.1: *$10\mu m$ x $10\mu m$ AFM scans of Ge layers grown at $500°C$ (wafers a,b). The left image is as grown and the right has been annealed in hydrogen in situ*

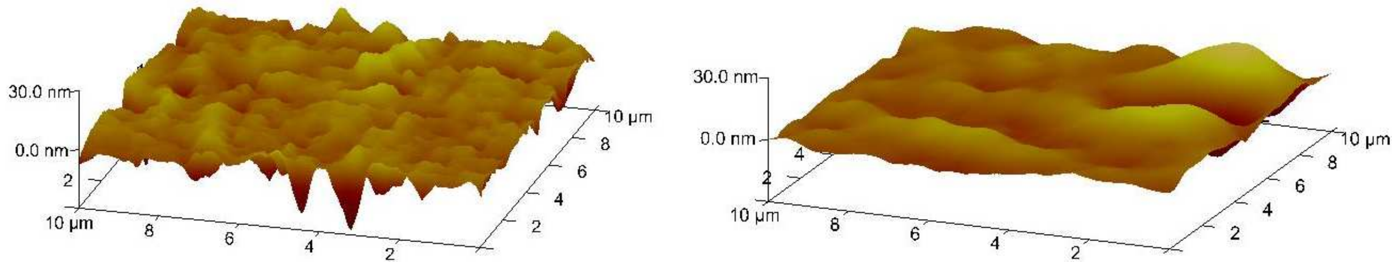


Figure 6.2: *$10\mu m$ x $10\mu m$ AFM scans of Ge layers grown at $550°C$ (wafers c,d). The left image is as grown and the right has been annealed in hydrogen in situ*

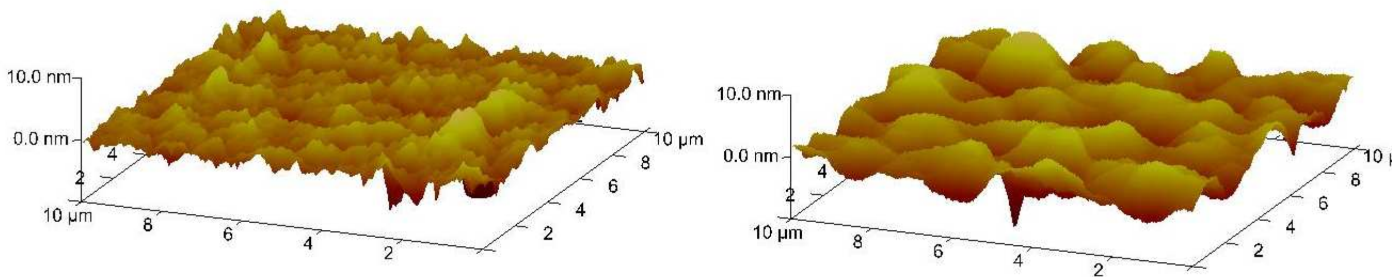


Figure 6.3: *$10\mu m$ x $10\mu m$ AFM scans of Ge layers grown at $600°C$ (wafers e,f). The left image is as grown and the right has been annealed in hydrogen in situ*

RMS roughness and Rmax quickly drop as growth temperature increases, before reaching a plateau at $\approx 600°$C. As growth temperature increases to its maximum of 700°C, the RMS roughness stays reasonably constant for the unannealed wafers, but shows a small increase for the annealed wafers. For Rmax however, as the growth temperature reaches its maximum,

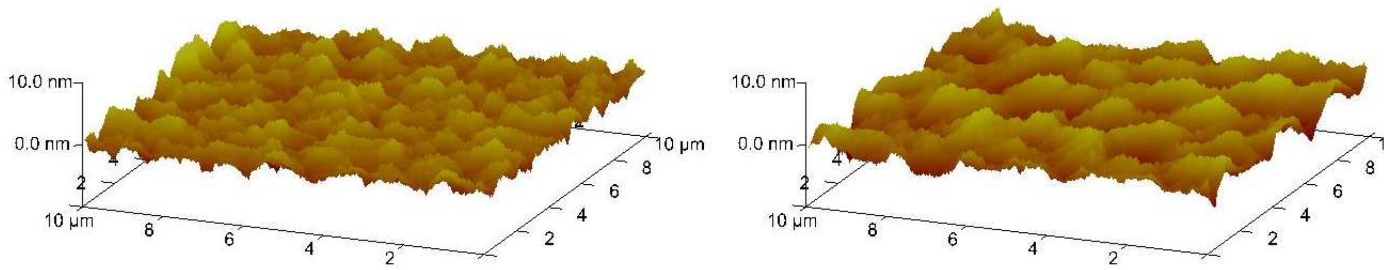


Figure 6.4: *$10\mu m$ x $10\mu m$ AFM scans of Ge layers grown At $650°C$ (Wafers g,h). The left image is as grown and the right has been annealed in hydrogen in situ*

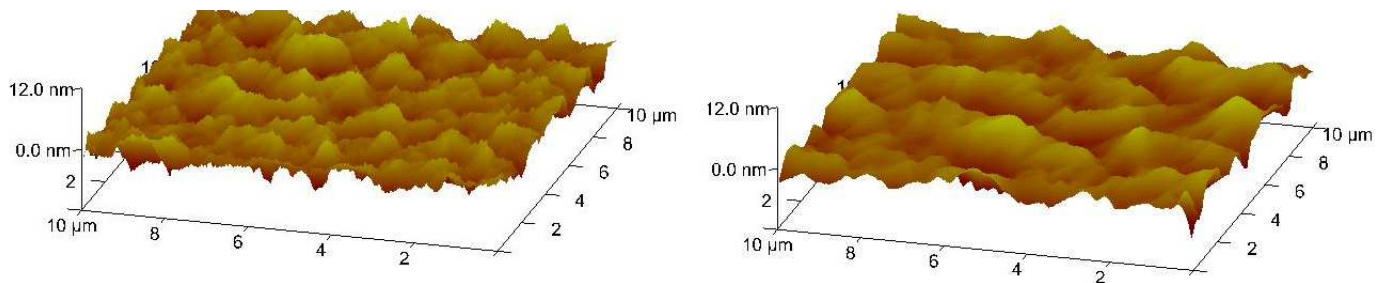


Figure 6.5: *$10\mu m$ x $10\mu m$ AFM scans of Ge layers grown At $700°C$ (Wafers g,h). The left image is as grown and the right has been annealed in hydrogen in situ*

the unannealed wafers show a small reduction, whereas the annealed wafers show a small increase.

6.3 XRD of Thick Germanium Layers on Si(001)

For all wafers, high resolution x-ray diffraction was used to determine the in plane and out of plane lattice parameter. (004) rocking curves were taken for each wafer (See Chapter 4 for explanation of rocking curves), both as grown and after annealing rocking curves are shown in Figure (6.8).

For the annealed wafers in Figure (6.8), the right hand side of the Ge peak is skewed for all the rocking curves. Since this is not observed in the rocking curves for as grown wafers in Figure 6.8, it can be assumed to be due to the 10 minute hydrogen anneal. This possibility of the hydrogen anneal causing the skewed peaks will be discussed in Chapter (7)

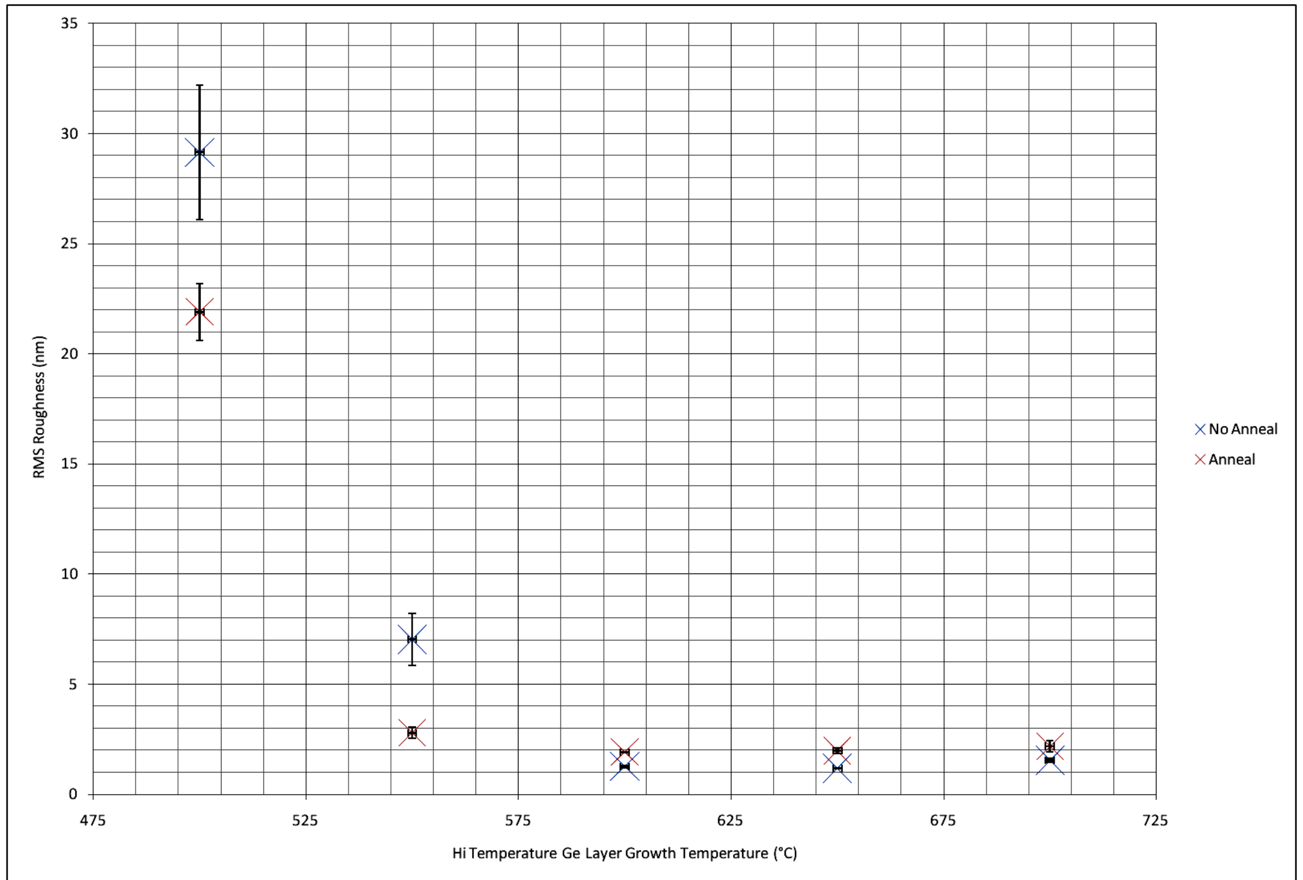


Figure 6.6: *RMS surface roughness Vs high temperature layer growth temperature for wafers with and without anneal*

In Figure (6.8), the Ge peak can be seen to move towards the Si peak as the growth temperature is increased. This means that the out of plane lattice parameter and hence relaxation is increasing with growth temperature. The reason for this will be explained in Chapter (7). In the strained state the Ge in-plane lattice parameter is reduced to the Si value, so the out of plane lattice parameter is larger, (by Poisson's ratio) than in relaxed Ge.
Reciprocal space maps (RSM's) showing the (004) and (224) peaks (See Chapter 4) were also taken for each wafer. The RSMs were used to determine the relaxation of the Ge layer. The Ge layer relaxation obtained from the RSMs is shown in figure 6.9. For the unannealed samples, the same trend as in Figure (6.8) is observed, with over relaxation for the wafers grown at higher temperatures.

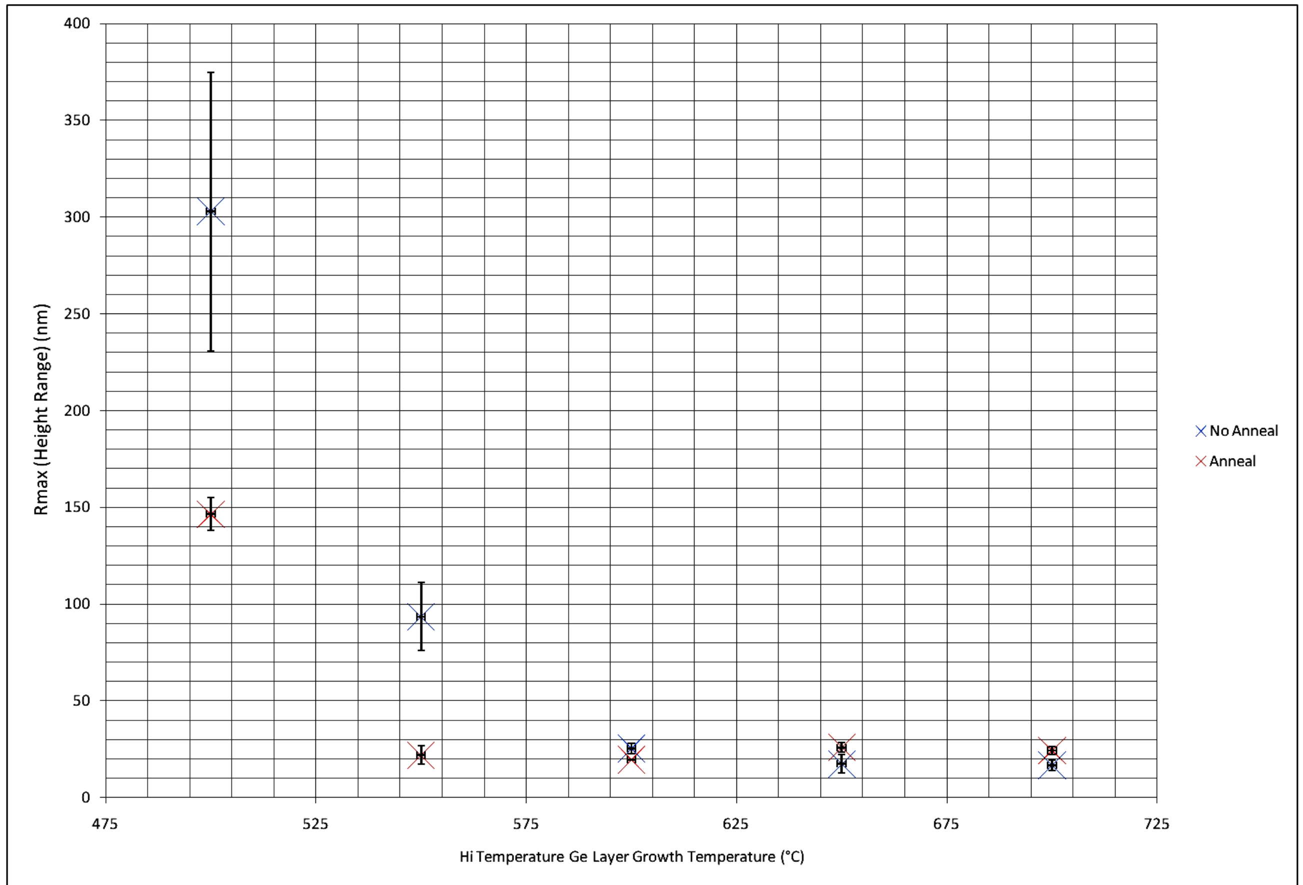


Figure 6.7: *Rmax (height range) Vs high temperature layer growth temperature for wafers with and without anneal*

6.4 Ge Layer Thickness From TEM

TEM [1]was used to measure the thickness of the Ge layers. The results are given in Table 6.2

The thickness measurement for wafer j was an anomalous result, most likely caused by human error, and so was not included.

1

[1]All TEM carried out by project students Toby Gould and Leigh Sangan

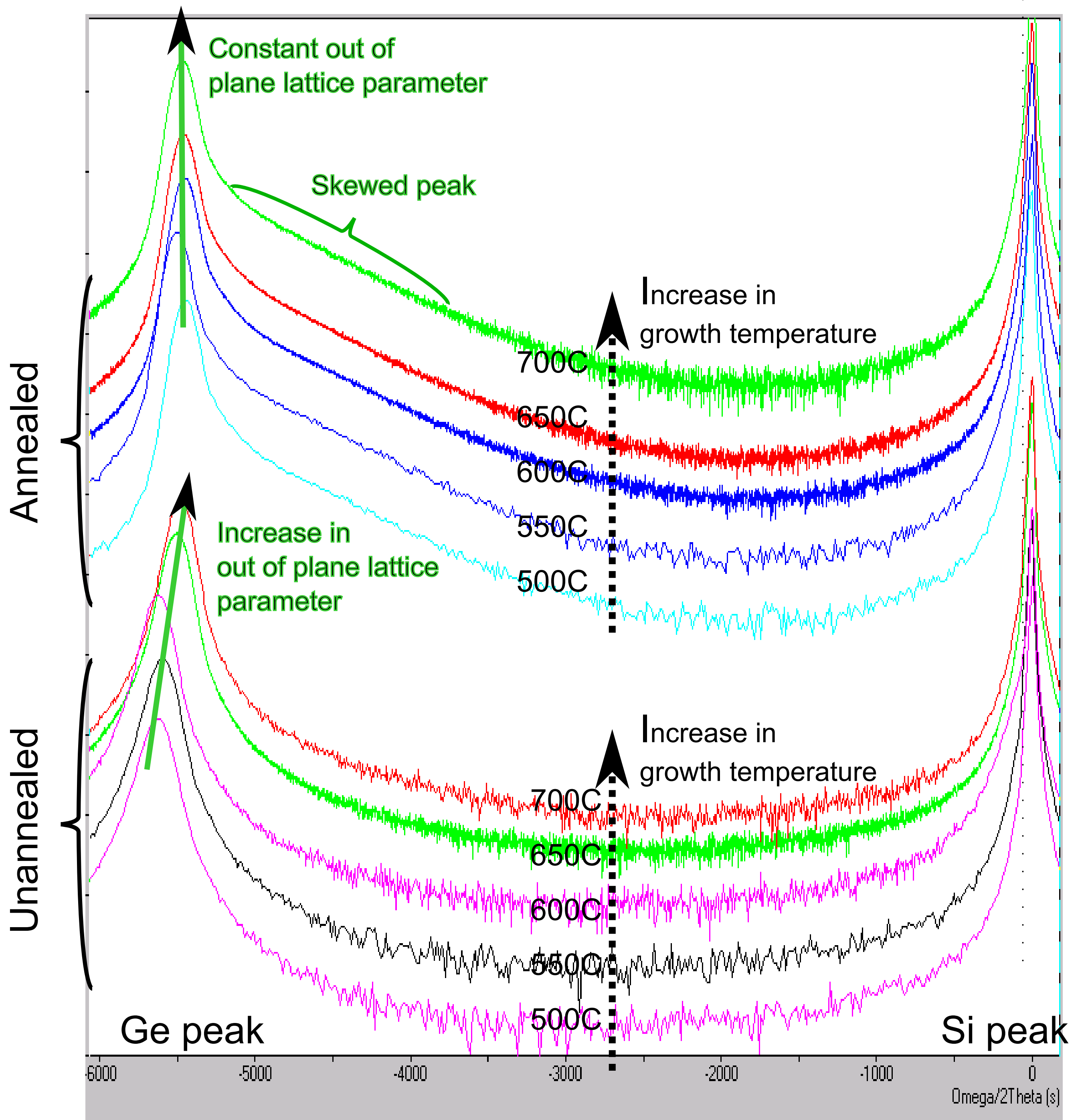


Figure 6.8: *Rocking curves from as grown samples and annealed samples*

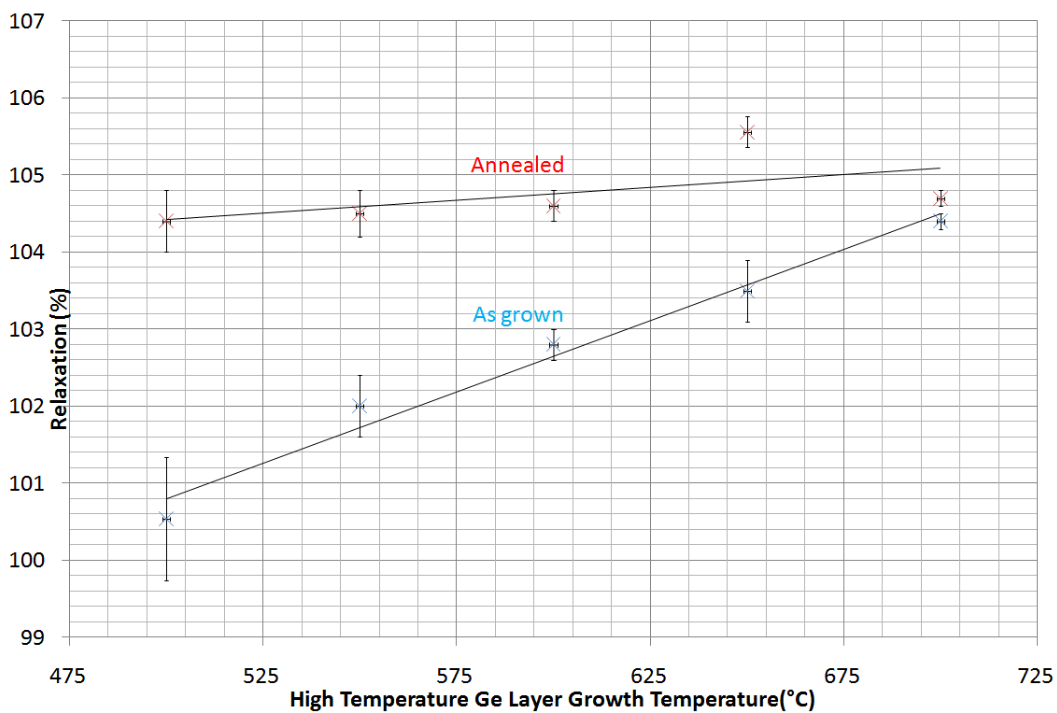


Figure 6.9: *Relaxation obtained from RSM's for annealed and as grown wafers, with linear trend-lines fitted*

Wafer	Thickness Measured By TEM $\pm 4nm$
a	470
b	459
c	561
d	458
e	454
f	456
g	453
h	458
i	445
j	-

Table 6.2: *Ge layer thickness from TEM*

Chapter 7

Discussion of Results

7.1 Over-Relaxation Observed in Ge Layers

The over-relaxation measured using XRD in the Ge layers in Chapter 6 from the RSM's and observed in the Ges peak shift has been observed in previous attempts at Ge growth on Si, as well as in GaAs growth on Si [29]. In Suh *et al* [62], a rocking curve is given for a $1.2\mu m$ Ge on Si layer and the Ge peak shows a peak shift towards the Si peak, as seen in this research in Figure (6.8). In cannon *et al* [7], the over relaxation or strain is measured with XRD and the Ge direct band gap E_g^Γ is measured with photo-reflectance. It was found that the strain decreases the direct bad gap and gives an adsorption edge located at $1610nm$. This makes the strained Ge a suitable material for L band communications.

The over-relaxation is caused by the mismatch in thermal expansion coefficients (a_t) of Ge and Si (See Table 7.1)

	$a_t\ m^{-1}\ k^{-1}$
Silicon [72]	$(3.725(1 - e^{[-5.8810^{-3}(t-124)]}) + 5.548 \times 10^{-4}t) \times 10^{-6}$
Germanium [58]	$(5.6569 + 34.22 \times 10^{-6}t + 10.17 \times 10^{-9}t^2 - 0.66 \times 10^{-12}) \times 10^{-6}$

Table 7.1: *Temperature dependant thermal expansion coefficients*

Since Ge has a larger coefficient of thermal expansion than Si, when the the layers are heated

during growth, the Ge layer expands more than the Si substrate, but the additional thermal energy allows the atoms to rearrange themselves to be commensurate with the substrate. Upon cooling, the Ge layer contracts more than the Si substrate but now the atoms do not have the freedom to move. The over relaxation occurs when the bonds between the substrate and Ge layer prevent the Ge layer from fully relaxing. The over relaxation causes tensile strain in the Ge layer.

Theoretical Explanation of Over-Relaxation

The following explanation is adapted from [44] where a general example for calculating thermal stresses in thin films is given. A similar approach has been used by Ishikawa *et al* [26]. Though the heterostructure has an internal stress distribution, it must be in mechanical equilibrium. For mechanical equilibrium, the net force (F) and bending moment (M) must be zero for any cross section of the heterostructure. This can be expressed by Equations (7.1 7.2). When the Ge layer shrinks relative to the substrate, because the Ge is bonded to the Si, both the Ge layer and Si substrate are forced to have the same length. Hence the Ge layer stretches and the substrate contracts, with the tensile forces in the Ge layer counteracted by the compressive forces in the Si substrate (See Figure 7.2). The heterostructure will also have unbalanced end moments, so it will bend concave upwards (with radius of curvature R) as illustrated in Figure (7.1) to counteract the unbalanced moments.

$$F = \int \sigma dA = 0 \tag{7.1}$$

$$F = \int \sigma y dA = 0 \tag{7.2}$$

If Equation (7.2) is applied to the heterostructure, then the clockwise and anticlockwise moments acting on a cross-section of the heterostructure must be equal to each other. This can be expressed by Equation (7.3), which can be derived from Figure 7.3. Where d_{Ge}, d_{Si} are the thicknesses of the Ge layer and Si substrate, M_{Ge}, M_{Si} are the moments in the Ge Layer and Si substrate and F_{Ge}, F_{Si} the forces in the Ge layer and Si substrate.

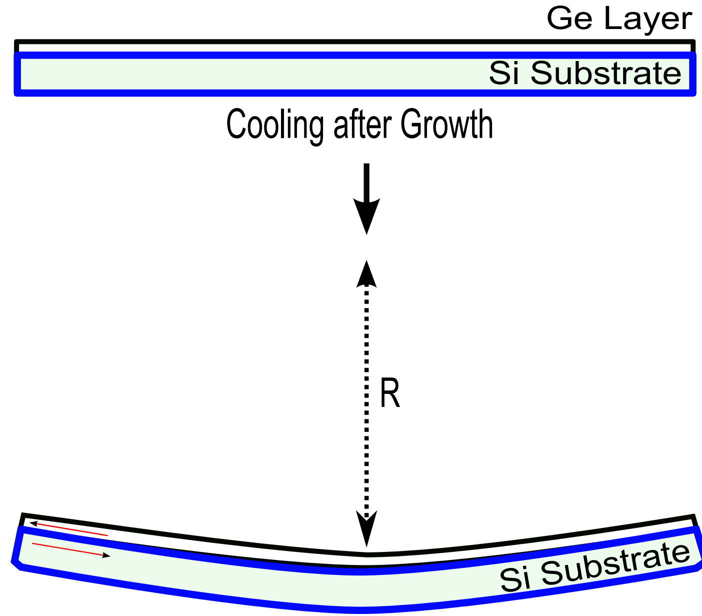


Figure 7.1: *Schematic diagram illustrating how the wafer is strained after cooling. The red arrows show the direction of stress. R is the radius of curvature of the wafer*

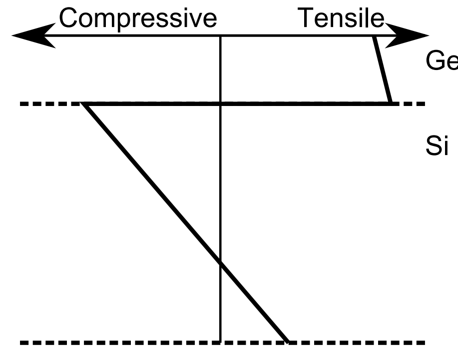


Figure 7.2: *Schematic diagram showing stress distribution in cross section of Ge on Si heterostructure*

$$\frac{(d_{Ge} + d_{Si})\,F_{Si}}{2} = M_{Ge} + M_{Si} \tag{7.3}$$

From [44], the bending moment in a stressed beam is given by Equation (7.4). Where Y is the Young's modulus of the beam, d its thickness and w its width.

$$M = \frac{Y d^3 w}{12R} \tag{7.4}$$

Equation 7.4 can the be substituted into Equation 7.3, to give Equation (7.5)

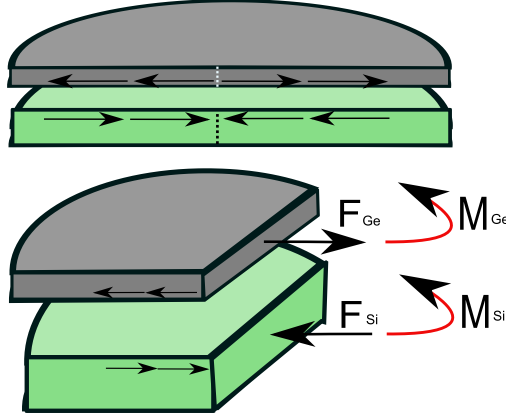


Figure 7.3: *Forces and moments in cross-section of wafer*

$$\frac{(d_{Ge} + d_{Si})\, F_{Ge}}{2} = \frac{wY_{Ge}d_{Ge}^3}{12R} + \frac{wY_{Si}d_{Si}^3}{12R} \tag{7.5}$$

Equation (7.5) can be now be rearranged to give Equation (7.6), then Equation (7.7) This is a form of Stoney's equation and gives the stress in the Ge layer.

$$F_{Ge} = \frac{wY_{Ge}d_{Ge}^3}{6R\,(d_{Ge} + d_{Si})} + \frac{wY_{Si}d_{Si}^3}{6R\,(d_{Ge} + d_{Si})} \tag{7.6}$$

$$\sigma_{Ge} = \frac{F_{Ge}}{d_{Ge}w} = \left(\frac{1}{R}\right) \frac{Y_{Ge}d_{Ge}^3 + Y_{Si}d_{Si}^3}{6d_{Ge}\,(d_{Ge} + d_{Si})} \tag{7.7}$$

Using Hookes Law, the in plane strain of the Ge layer can then be found. This is given in equation (7.8)

$$e_{||-Ge} = \left(\frac{1}{R}\right) \frac{Y_{Ge}d_{Ge}^3 + Y_{Si}d_{Si}^3}{Y_{Ge}6d_{Ge}\,(d_{Ge} + d_{Si})} \tag{7.8}$$

To calculate the strain from Equation (7.8, a value for the radius of curvature is needed. This could be measured experimentally or calculated using Equation (7.9) (Taken from Ishikawa et al [26]) Where T_H and T_L are the heated and cooled temperatures of the wafer and $\alpha_{T(Si)}$ and $\alpha_{T(Ge)}$ are the high and low temperatures of the wafer respectively. Y_{Si} and Y_{Ge} are the Young's moduli for silicon and germanium and are given by 7.10, the Young's modulus for a (001) crystal, where c_{11} and c_{12} are the crystals elastic constants.

$$\frac{1}{R} = \frac{6Y_{Ge}Y_{Si}d_{Ge}d_{Si}\left(d_{Ge}+d_{Si}\right)\int_{T_H}^{T_L}\left[\alpha_{T(Si)}\left(T\right)-\alpha_{T(GE)}\left(T\right)\right]}{3Y_{Ge}Y_{Si}d_{Ge}d_{Si}\left(d_{Ge}+d_{Si}\right)^2+\left(Y_{Ge}d_{Ge}+Y_{Si}d_{Si}\right)\left(Y_{Ge}d_{Ge}^3+Y_{Si}d_{Si}^3\right)} \tag{7.9}$$

$$Y = \left(c_{11}+2c_{12}\right)\right)\left(c_{11}-c_{12}\right)/\left(c_{11}+c_{12}\right) \tag{7.10}$$

The theoretical relaxation for Ge layers as a function of growth temperature is hence given in Figure 7.4. For the Ge layer thickness in the calculations, the average thickness of the Ge layers grown on wafers $(a \succ j)$, $468nm$, as measured by TEM was used for the Ge layer thickness.

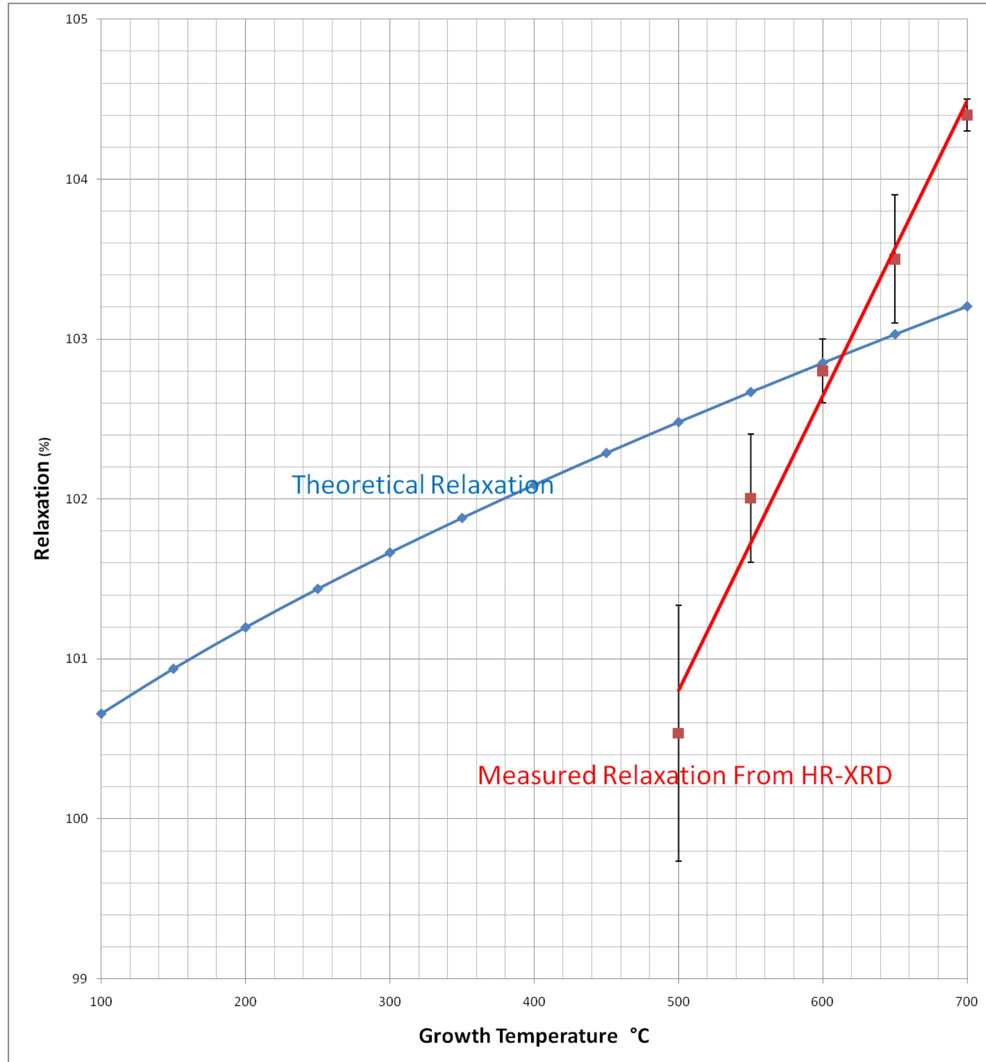


Figure 7.4: *Theoretical Ge layer relaxation as a function of high temperature layer growth temperature.*

Comparison Of Theoretical Over-Relaxation With Over-Relaxation Measured using HR-XRD

In Figure 7.4 it can be seen that while the slope of the theoretical relaxation model does not fit the results (gradient is significantly lower than experimental data), the model is giving values roughly in the same range. Possible reasons for the model not fitting the experimental data include:

- The use of an average value for the Ge layer thickness. In Table 6.2 it can be seen that there a sizeable fluctuation in the grown layer thickness.
- Incorrect values for the temperature dependant thermal expansion coefficients for Si and Ge. The values used for Si and Ge came from results published in 1974 and 1968 respectively. The accuracy of temperature dependant thermal expansion coefficients may have improved significantly since these results were published.
- The use of a model that does not correctly describe the physical system. The model used treats the wafer as a single beam bending in one direction. This may be over-simplification, since the wafer is bending in two directions.

7.2 Diffusion at interface with Anneal

The inter-diffusion of Ge and Si following annealing has been previously indicated [19]. If inter-diffusion occurs, a thin SiGe layer will be formed, with a smaller relaxed lattice parameter than pure Ge. SiGe would produce a peak to the right of Ge on a (004) rocking curve, hence it is reasonable to speculate that the skewed peaks observed in Figure 6.8 are caused by inter-diffusion between the Ge layer and the Si substrate.

In [19], the diffusion of Si-Ge is studied in detail. $300nm$ Ge layers were grown on Si substrate by CVD, these were then capped with SiO_2 before being annealed at temperatures between 705 - 900°C for a range of times. Secondary ion mass spectrometry (SIMS) was then used to measure the Ge diffusion profile. The results can be seen in Figure (7.5). Inter-diffusion

occurred for all anneal times, with Ge atoms being observed at up to $50nm$ in to the Si substrate and Si atoms being observed upto $250nm$ in to the Ge layer. This is interesting, since it shows that the diffusion of Si in Ge is far higher than that of Ge in Si, but hardly suprising given the relative atomic sizes and stronger bonding in Si than in Ge.

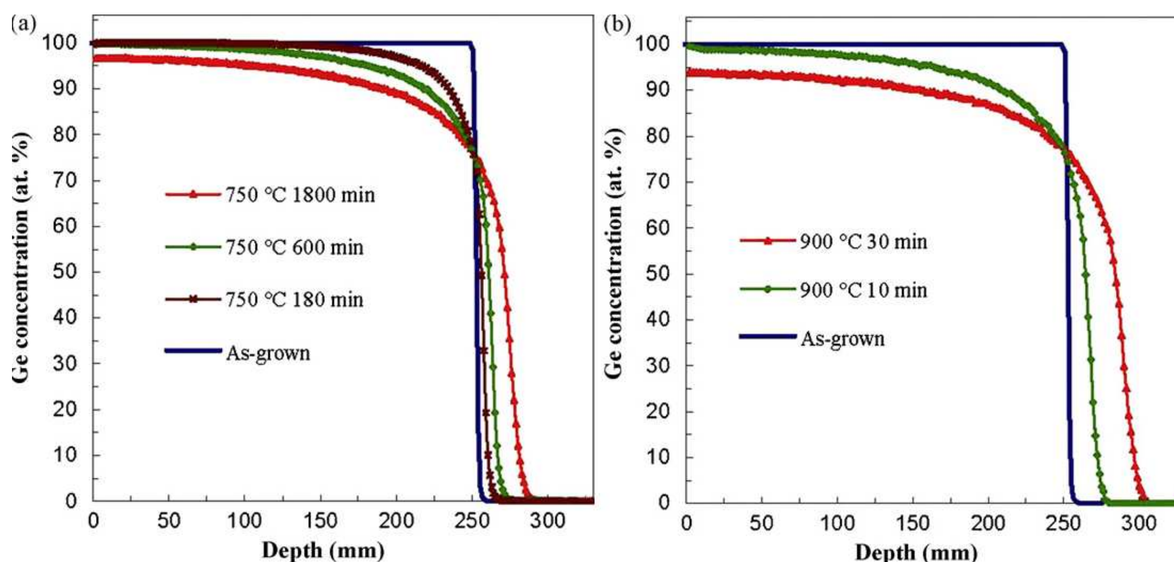


Figure 7.5: *Ge depth concentration profiles before (line) and after diffusion annealing (lines + symbols) at 750 .C (a) and 900 .C (b). Taken from [19]*

.

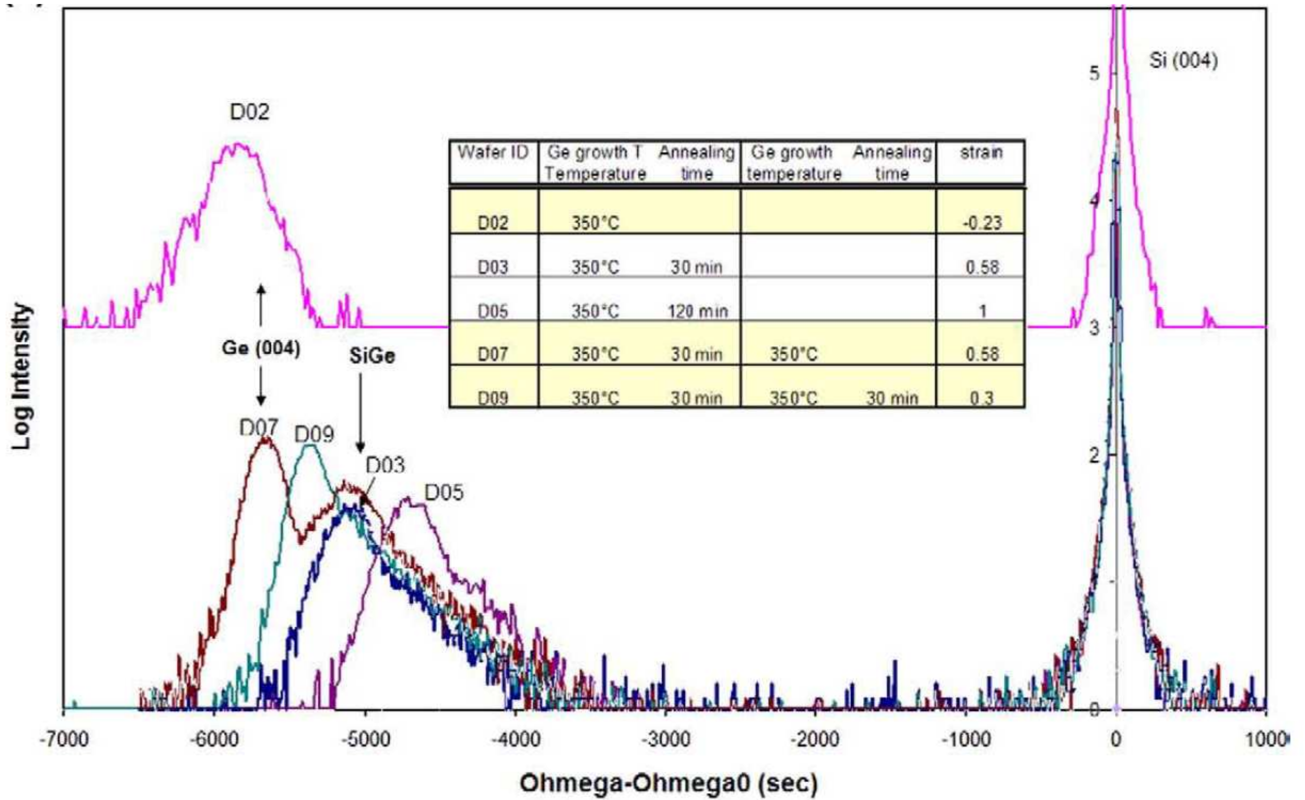
Terzieva *et al* [64] have taken (0 0 4) rocking curves for a number of samples of Ge on Si (0 0 1), where the Ge peaks show the same broadening towards the Si peak as Figure (6.8).

Theoretical Diffusion At Interface With Anneal

Diffusion is governed by Fick's second law, the 'diffusion equation', Equation (7.11), where C is the concentration (number density), D is the diffusion coefficient of the species in question and t is time.

$$\frac{\partial C}{\partial t} = \nabla \cdot (D \nabla C) \tag{7.11}$$

A solution for the diffusion equation can be given for a pair of infinite solids [56], taking $u = (x - a) / 2\sqrt{Dt}$, where x is the distance from the interface, and a is the distance from



Wafer ID	Ge growth T Temperature	Annealing time	Ge growth temperature	Annealing time	strain
D02	350°C				-0.23
D03	350°C	30 min			0.58
D05	350°C	120 min			1
D07	350°C	30 min	350°C		0.58
D09	350°C	30 min	350°C	30 min	0.3

Figure 7.6: *(004) Rocking Curves from Ge on Si(0 0 1) with (D11, D13, D15, D17) and without (D04) in-situ hydrogen anneal. Taken from [64]*

.

the center of a slice to the interface at $x = 0$:

$$c(x,t) = \frac{c}{\sqrt{\pi}} \int_{-\infty}^{x/2\sqrt{Dt}} exp\left(-u^2\right) du \tag{7.12}$$

Equation (7.12) can be rewritten using the error function [56], to give a simplified form of the solution for a pair of infinite solids:

$$c(x,t) = \frac{c^{'}}{2} \left[1 + erf^{\left(\frac{x}{2\sqrt{Dt}}\right)}\right] \tag{7.13}$$

Where the error function $erf(z)$, is given by Equation 7.14.

$$erf(z) = \frac{2}{\sqrt{\pi}} \int_{0}^{z} e^{\left(-u^2\right)} du \tag{7.14}$$

From equation 7.13, a theoretical diffusion profile can be found, giving the concentration

of the diffusant beyond the interface. Since it can be assumed that the the majority of the diffusion between materials is that of Si atoms into the Ge layer, a theoretical diffusion profile will only be found for Si diffusing into the Ge layer. For the calculation of the diffusion profile, a value of D, the diffusion coefficient of Si in Ge is needed. The value used was $2.9 \cdot 10^{-18}$ $(m^2 s^{-1})$, from [57], for the anneal temperature of 830°C.

The theoretical diffusion profile is shown in figure 7.7. If this calculated profile is correct, then a large amount of Si will have diffused into the Ge layer during anneal. The diffusion profile could also have been calculated using the thin film solution to the diffusion equation [36];, however, the infinite solid solution was used instead because the diffusion length is far shorter than the thickness of the Ge layer and because the use of the infinite solid solution in literature [1], [61] for epitaxial layers of a comparable thickness.

7.3 Affect Of High Temperature Ge Layer Growth Temperature On Roughness

From the results in Chapter 6, it can be seen that the high temperature layer growth temperature affects the surface roughness. At low growth temperatures $\prec 600^{\circ C}$, very high surface roughness was observed, but the roughness improved as the growth temperature increased. This could be due to the temperature dependence of adatom mobility. At low temperatures, the low mobility would mean the adatoms are unable to travel to fill in the troughs in the surface, giving high RMS roughness and Rmax. While at high growth temperatures the adatoms are able to travel into troughs on the surface, giving a smooth surface.

7.4 Affect In-Situ Hydrogen Anneal on Roughness

From the results in Chapter 6, it can also be seen that the in-situ hydrogen anneal affects the surface roughness. For the very rough Ge layers (low growth temperatures), the anneal gave a large reduction in surface roughness. However, for the very smooth Ge layers this effect was reversed, with the anneal giving a small increase in surface roughness.

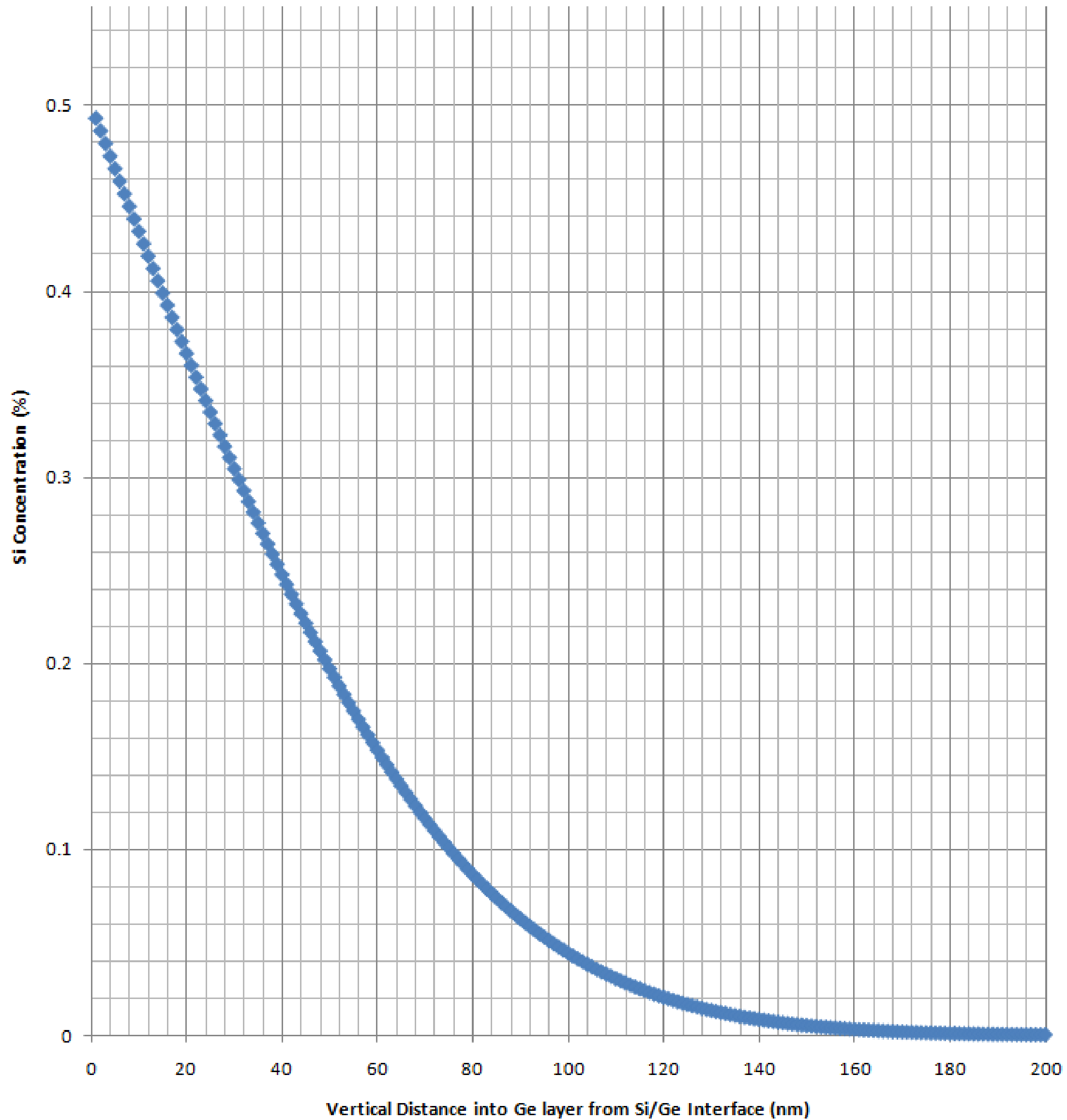


Figure 7.7: *Si concentration with vertical distance into Ge layer.*

Reduction In Roughness With Hydrogen Anneal

The affect of the surface roughness reduction with hydrogen anneal is observed and explained by Nayfeh *et al* in [41] and summarized in Figure 7.8. A reduction in RMS surface roughness of upto 90% is recorded for annealing. For a 200nm layer grown by GeH_4 at 825° and annealed in hydrogen at 825°C, RMS roughness was reduced from 15nm to a final roughness value of 3nm.

The explanation given for the roughness reduction by hydrogen anneal is an increased surface

mobility. During the anneal, $Ge-H$ clusters are formed that have a lowered diffusion barrier ($\tilde{9}2$ meV at 800°C). Due to the lower diffusion barrier, more diffusion can occur across the surface, resulting in a smoother surface.

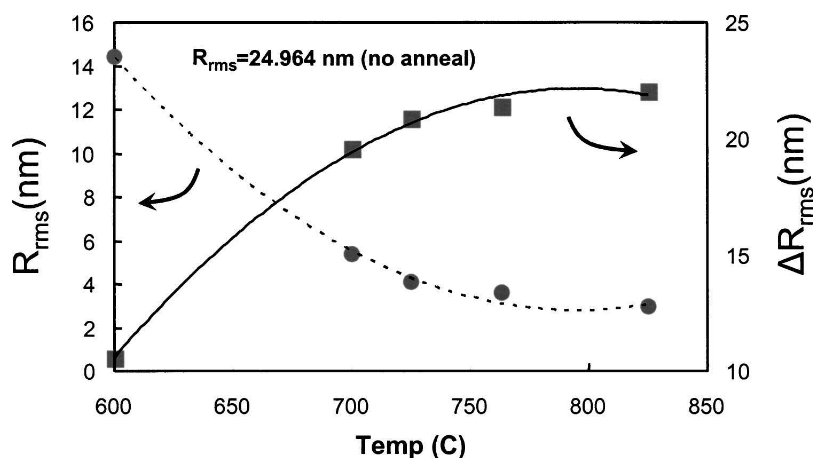


Figure 7.8: *RMS roughness of Ge grown on Si vs. 1 hour hydrogen anneal temperature (dashed line) and change in RMS roughness after anneal (between as-grown and annealed wafer) vs. 1 hour hydrogen anneal temperature (solid line). Taken from [41]*

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A more detailed explanation for the reduction in surface roughness with anneal is given in Nayfeh's thesis [43], where he discusses the free energy of surface atoms.

Increase In Roughness With Hydrogen Anneal

For the very smooth Ge layers grown at higher temperature, the hydrogen anneal increased the roughness. This effect has also been previously recorded, in [30], where for a 150nm Ge on Si(0 0 1) layer grown with GeH_4 at 310°, the RMS roughness increased from $\approx 1nm$ to $\approx 4nm$ on in-situ annealing in hydrogen at 850°. However, for annealing at lower temperatures ($\approx$ 650°), the roughness decreased.

7.5 Review of Ge layer Quality and Comparison to Previous Work

For the Ge layers grown in this study to be useful to industry and to be deserving of future research, then they should be at least approaching the quality of layers grown by other groups in previous work. Since the dislocation density for the layers grown in this study has not been found, the quality of the layers will have to be judged solely on surface roughness. The RMS surface roughness of the Ge layers mentioned in Chapter (5) ranges from 0.6nm to 2.5nm. The lowest roughness value of 0.6nm was achieved by Hartmann *et al* [24] Using the low temperature buffer layer method. The lowest RMS roughness value achieved in the wafers grown in this research was for wafer (i), with a value of 1.5nm RMS roughness. The difference in values suggests that further work should be done on refining the growth recipe used in this research to give improved roughness values.

Chapter 8

Possible Future Research and Improvement of Design of Germanium Layers

8.1 Future Characterisation Work

Before suggestions can be made on ways to improve the quality of the Ge layer by variation in growth parameters, further characterisation work should be done on the set of wafers grown for this research.

Threading Dislocation Density and Selective Defect Etching

If the layers of Ge grown in this research were to be used in devices, besides surface roughness, the important layer parameter would be threading dislocation density (TDD). Using a technique called selective defect etching, the TDD can be found. In selective defect etching, an etchant is used that has a faster etch rate when it is in proximity to a threading dislocation than its etch rate for the rest of the material. This increased etch rate produces a pit in the location of the threading dislocation. The etch pits can then be counted using a differential interference contrast (DIC)/Normarski microscope and a value for the TDD

can be calculated. In [59], etchants suitable for the Ge layers grown in this research are discussed.

Layer Profile With Depth and Secondary Ion Mass Spectrometry

Secondary ion mass spectrometry (SIMS) can be used to give the composition of a material as a function of depth. This would be very useful in this research since it would show if the theoretical diffusion profile for Si in the Ge layer (Given in Chapter 7) is correct by giving an accurate composition profile for the wafer.
SIMS works by focussing a primary ion beam onto the surface of the sample, then collecting the secondary, ejected ions. The secondary ions are then analysed using a mass spectrometer, which can give element of the ejected ion and thus the composition of the material it originated from.

8.2 Future Theoretical Work

The theory given in this research could be imroved upon to give a more accurate desription of the experimental results.

Theoretical Over-Relaxation In Ge Layers

The theoretical over-relaxation of the Ge layers deviates by $\approx 1\%$ from the experimental value. This could be due to the method used to find the theoretical over-relaxation. Another approach to give a value for the theoretical over-relaxation would be to use a software package that uses the finite element method (FEM)) to model the wafer.

8.3 Design of Germanium Layers

To give higher quality layers than those grown for this research, more wafers could be grown to investigate the growth parameters not covered here. Possibilities include:

The design of the low temperature buffer layer, such thickness and growth temperature. The temperature and time of the hydrogen anneal (a lower anneal temperature has given good results in [30]. Alternative precursors to Germane such as Digermane could be trialled, having shown promising results in ref [39].

If the intended usage of the Ge layers was known it would be useful in further development of the layers. For some applications of the layers, a high TDD or surface roughness may be acceptable and the growth time of the layer may be the critical factor. The thickness of the Ge layer may also be very important in some applications, such as photodetectors.

Chapter 9

Summary of Thesis Work

10 wafers were grown using RP-CVD with a GeH_4 precursor using the two step growth with low temperature buffer layer technique. The effects of the high temperature layer growth temperature and a 10 min, 830°C hydrogen anneal on layers of Ge grown via the two step growth method was investigated. The growth temperature of the high temperature layer was varied between 500°C and 700°C and the total thickness of the complete Ge layer was targeted at $500nm$.

The wafers were characterised using the following techniques:

- High resolution x-ray diffraction (RSM's and rocking curves)
- Atomic force microscopy
- Transmission electron microscopy

The Ge layer relaxation was calculated from the x-ray diffraction results and over relaxation was found. The reason for the over relaxation has been given and theoretical values of the relaxation calculated. While the theoretical relaxation did not exactly match the measured relaxation, it followed the same general trend.

Skewed Ge peaks were seen in the rocking curves from the annealed Ge layers, this was postulated to be due to diffusion between the Si substrate and the Ge layer. A theoretical profile for Si diffusion in the Ge layer was calculated and showed large amounts of diffusion. This backed up the claim that the skewed peaks were caused be diffusion.

Overall tthe results show great promise for thid method of producing relaxed Ge layers on Si (0 0 1) substrates and follow up studies should certainly be considered.

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