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Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. All experimental data presented was carried out by the author, or (where stated) by specialists under the author's direction.

Publications and Presentations

Publications

J. Parsons, E. H. C. Parker, D. R. Leadley, R. J. H. Morris, T. J. Grasby and A. D. Capewell. Misfit Strain Relaxation and Dislocation Formation in Supercritical Strained Silicon on Virtual Substrates. *Appl. Phys. Lett.*, 91:063127, 2007.

J. Parsons, C. S. Beer, D. R. Leadley, A. D. Capewell and T. J. Grasby. Evaluation of Relaxation and Misfit Dislocation Blocking in Strained Silicon on Virtual Substrates. *5th International Conference on Silicon Epitaxy and Heterostructures Proceedings, Thin Solid Films*, Submitted, 2007.

G. Nicholas, T. J. Grasby, D. J. F. Fulgoni, C. S. Beer, **J. Parsons**, M. Meuris, M. M. Heyns. High Mobility Strained Ge pMOSFETs With High-κ/Metal Gate. *IEEE Electr. Device Lett.*, 28:825, 2007.

Presentations

G. Nicholas, A. D. Capewell, D. J. F. Fulgoni, M. J. Palmer, T. J. Grasby, L. J. Nash, **J. Parsons**, T. E. Whall and E. H. C. Parker. New Generation SiGe Virtual Substrates for SSOI. *European Materials Research Society*, Nice, France, 2006.

T. J. Grasby, **J. Parsons**, T. E. Whall and E. H. C. Parker. Terrace Graded Virtual Substrates. *Advanced Silicon Devices and Technologies for ULIS Era*, Warsaw, Poland, 2006.

J. Parsons, C. S. Beer, D. R. Leadley, A. D. Capewell and T. J. Grasby. Evaluation of Relaxation and Dislocation Blocking in Strained Silicon. *Ultimate Integration on Silicon Conference*, Leuven, Belgium, 2007.

J. Parsons, C. S. Beer, D. R. Leadley, A. D. Capewell and T. J. Grasby. Evaluation of Relaxation and Misfit Dislocation Blocking in Strained Silicon on Virtual Substrates. *5th International Conference on Silicon Epitaxy and Heterostructures*, Marseille, France, 2007.

Abstract

The relaxation of variable thickness strained silicon layers on 20% and 50% germanium composition virtual substrates have been quantified using two independent methods. High resolution X-ray diffraction offers a means to measure relaxation directly, and a defect etching technique has been developed from which relaxation can be determined by the measurement of dislocation densities. Comparisons between the relaxation of tensile strained silicon in this work and compressively strained $Si_{1-x}Ge_x$ in other works, suggest that strained silicon is unusually stable to relaxation.

Observation of dislocation structures with defect etching and transmission electron microscopy have shown that the additional stability arises from the interaction of dislocations which inhibits glide. Extended stacking faults, which only form when the strain is tensile (and are therefore absent in compressively strained $Si_{1-x}Ge_x$), are more effective at impeding dislocation glide and it is their increased density in thicker layers which yield enhanced stability, even after high temperature annealing.

Chapter 1

Introduction

By the end of 2005, the Semiconductor Industry Association estimated the global semiconductor market to be worth in excess of $225 billion. With around 93% of the market share belonging to silicon, and the rest attributed to various optoelectronic applications [SIA, 2006]. The dominance of silicon as the basis for electronic device technology is due its abundance (and therefore low cost), and the excellent material quality of its oxide, SiO_2.

Semiconductor market growth is driven by the desire for the increased performance of future computer micro-processors. This has lead to reductions in the length scales of the most common type of transistor, the metal-oxide semiconductor field effect transistor (MOSFET), which allows ever higher densities to be packed together into processors. The observation that "the number of transistors on a chip doubles about every two years" by Intel co-founder, Gordon Moore, in 1965 gradually became accepted as a target for industry growth. *Moore's Law*, as it became know, is shown in figure 1.1, together with the major Intel® processor generations since 1970.

Fulfilling Moore's prophecy paved the way for the first International Technology

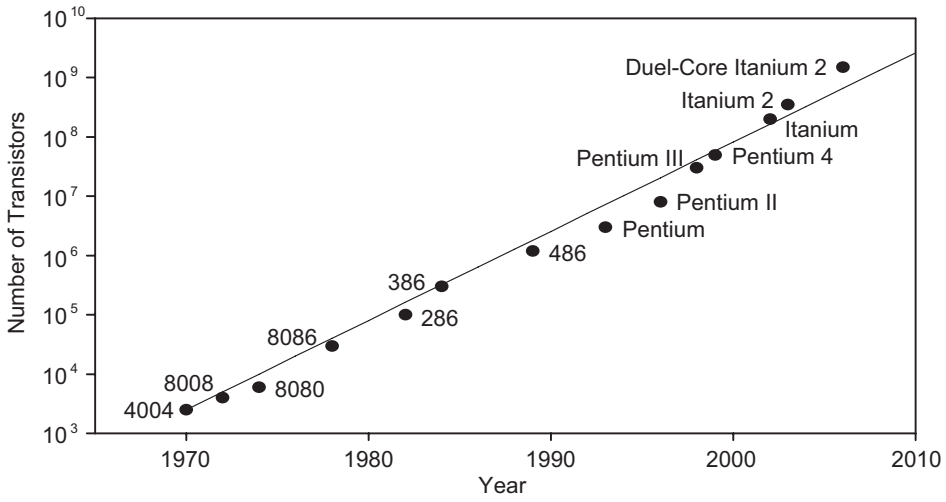

Figure 1.1: Graph showing release dates of principal generations of Intel® processors and the total number of transistors they contain, together with Moore's Law. Taken from Intel [2006].

Roadmap for Semiconductors (ITRS) in 1992. The ITRS Roadmap has been published every two years since, and lays down the scaling and technological targets to satisfy Moore's Law for the following 15 years [ITRS, 2006].

Unfortunately, scaling cannot continue indefinitely. As length scales become ever smaller, transistor performance begins to suffer from fundamental problems such as the leakage of current MOSFETs by the quantum tunnelling of electrons. Research has therefore been directed into new materials to boost transistor performance before scaling limits are reached with bulk silicon. The cost of setting up new fabrication facilities means that to be acceptable to the industry, new materials must be mass producible with great fidelity and preferably scalable to some degree. One such option is the engineering of strain into existing semiconductor materials such as silicon.

Chapter 2

Theoretical Discussion

In this chapter the fabrication and design of silicon-germanium virtual substrates and strained silicon layers will be discussed. Dislocation formation, propagation and interactions will be considered in detail for strained silicon-germanium systems.

2.1 Silicon and Germanium

Silicon and germanium both occur in nature as crystalline diamond lattice structures, in which each atom is covalently bonded to four neighbouring atoms. The diamond structure unit cell consists of two inter-penetrating face-centred cubic unit cells, one of which is displaced along the body diagonal by a quarter of the unit cell lattice parameter relative to the other. A simplified diagram of the diamond structure unit cell is shown in figure 2.1.

Bulk silicon and germanium have lattice parameters of 5.431Å and 5.658Å respectively [Dismukes et al., 1964], and so the lattice parameter of germanium is 4.17% larger than that of silicon. Germanium is fully miscible with silicon, and will form any alloy of $Si_{1-x}Ge_x$ from $x = 0$ to 1, which is a random alloy, with no long-range

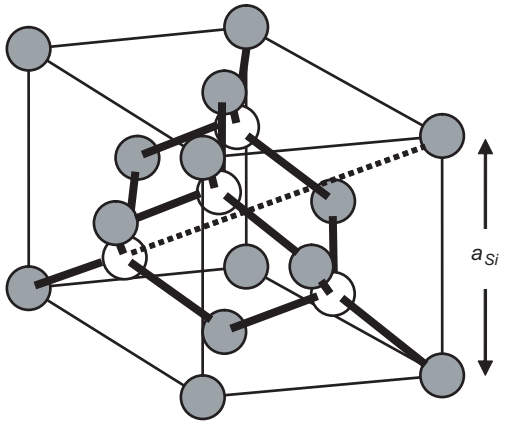

Figure 2.1: Simplified diagram showing the arrangement of atoms in the diamond structure unit cell of silicon, where a_{Si} is the lattice parameter. White atoms denote the face-centred cubic unit cell interpenetrating the face-centred cubic unit cell of grey atoms.

order within the crystal lattice. The lattice constant of any $Si_{1-x}Ge_x$ alloy (a_{SiGe}) can therefore be described by Vegard's law, even though the local lattice constants between neighbouring atoms varies. Vegard's law for any germanium composition, x, is an interpolation between the lattice constants of silicon (a_{Si}) and germanium (a_{Ge}) and can be formulated as [Kasper et al., 1995]:

$$a_{Si_{1-x}Ge_x} = a_{Si}(1-x) + a_{Ge}x + [0.0273(x^2 - 10x)] \tag{2.1}$$

The final term is an empirically determined correction factor for $Si_{1-x}Ge_x$, formulated to account for the slight discrepancy between theoretical and empirically obtained lattice parameters.

The 4.17% lattice mismatch between the two elements can be utilised to fabricate strained (or *pseudomorphic*) layers. Deposition of $Si_{1-x}Ge_x$ atoms on a silicon substrate to form a comensurate interface will result in a layer under biaxial compressive strain in

the plane of growth due to the larger bulk lattice constant of $Si_{1-x}Ge_x$ (figure 2.2 (a)). The interface between the two materials is known as a *misfit interface*, and the in-plane compression of the $Si_{1-x}Ge_x$ layer will be accompanied by an extension of the lattice in the growth direction, according to the Poisson ratio. Alternatively, the growth of silicon on a substrate of bulk $Si_{1-x}Ge_x$ will result in a biaxially tensile strained layer (figure 2.2 (b)).

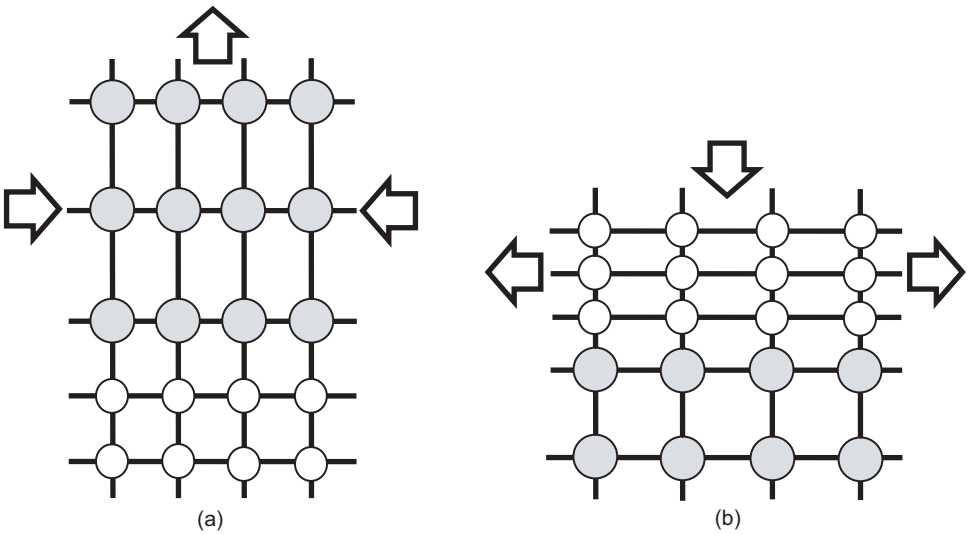

Figure 2.2: Schematic representation of layers under (a) in-plane compressive and (b) in-plane tensile strain. Layers with a larger lattice constant are shown in grey, and layers with a smaller lattice constant are in white.

The strain (ϵ) in the layer due to the lattice mismatch (or misfit) can be expressed in terms of the lattice constants of the layer, a_{layer}, and substrate, $a_{substrate}$:

$$\epsilon = \frac{a_{substrate} - a_{layer}}{a_{substrate}} \tag{2.2}$$

$$= 0.0417x \tag{2.3}$$

For silicon-germanium strained layers, ϵ will vary with germanium composition from zero to 0.0417 and will be negative [positive] for compressive [tensile] strain.

The introduction of strain into silicon has a profound effect on its electrical properties, which are highly desirable for the manufacture of future electronic devices.

2.1.1 Strained Silicon

Tensile strained silicon has an enhanced charge carrier mobility, μ, (electrons or holes) above that of bulk silicon [Takagi et al., 1996]. Such carriers move through strained silicon with an increased velocity, v, relative to bulk material under an applied electric field, E. This is given by:

$$v = \mu E \tag{2.4}$$

The mobility of a charge carrier is defined by the mean scattering time, τ (the average time between scattering events along its path), the effective mass of the carrier, m^*, and the electric charge it carries, e:

$$\mu = \frac{e\tau}{m^*} \tag{2.5}$$

Charge carrier mobility is therefore increased by decreasing m^*, and/or increasing τ. Mobility enhancements in strained silicon are believed to be achieved by a combination of both effects.

In bulk silicon, the conduction band is composed of a set of six-fold degenerate bands, Δ_6, associated with electron transport along the six $<001>$ crystal directions (figure 2.3 (a)). The energy minima of each band forms an elliptical surface of constant energy in k-space, the surface area of which describes the number of momentum states available to electrons.

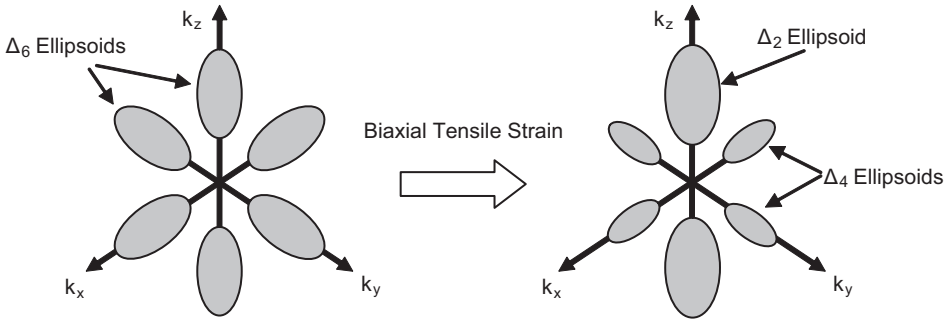

Figure 2.3: Schematic diagram showing the conduction bands in (a) bulk silicon and (b) tensile strained silicon. Adapted from Rim et al. [2003].

Intervalley scattering occurs between all six ellipsoids as they are degenerate in energy. The application of strain in the x-y plane (figure 2.3 (b)) pseudomorphically deforms the crystal and breaks the degenerate state into a four-fold (Δ_4) and a two-fold set (Δ_2) [Rim et al., 2003]. Under tensile strain Δ_4 is reduced in energy, resulting in an energy gap between Δ_4 and Δ_2, which becomes larger with more strain. Occupancy of the lower energy bands is favoured, which reduces the total number of states electron can scatter into.

Strain has a similar effect on the valence band in bulk silicon, which is composed of a two degenerate bands for the transportation of light holes (LH) and heavy holes (HH) (figure 2.4 (a)). Tensile strain shifts the LH band to a lower energy (for holes energy is taken in the opposite sense to electrons) resulting in a strain dependant energy gap which reduces intervalley scattering (figure 2.4 (b)). The spin-orbit (SO) band is also shifted to a higher energy than the LH and HH bands, further reducing scattering.

The curvature of an energy band affects m^* for all the carriers occupying it. The LH band shifts to a lower energy under tensile strain, and the curvature of the band is affected such that light holes become heavier than heavy holes. In the conduction band,

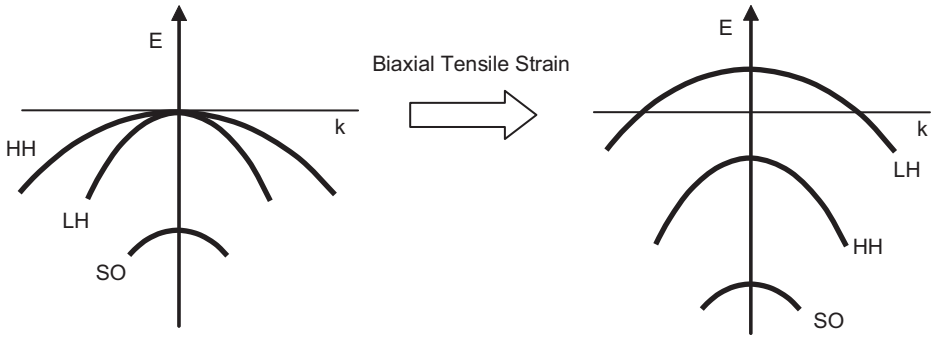

Figure 2.4: Schematic diagram showing the valence bands in (a) bulk silicon and (b) tensile strained silicon. Adapted from Rim et al. [2003].

a reduction in the curvature of the Δ_2 bands also results in a reduction in m^*.

In order to make use of the enhancements to carrier mobility in strained silicon, a reliable method for its fabrication must be available. The most common approach to the production of globally strained layers is that of the *virtual substrate*.

2.1.2 $Si_{1-x}Ge_x$ Virtual Substrates

Bulk $Si_{1-x}Ge_x$ crystals of any germanium composition possess a larger lattice constant than bulk silicon, and will induce biaxial tensile strain into deposited silicon overlayers. Unfortunately, the production of bulk $Si_{1-x}Ge_x$ single crystal wafers is problematic due to the differences in melting temperature, density and lattice constant between the two materials [Matsui et al., 1998]. Germanium is also a less abundant element than silicon, which effectively rules out economic mass production of such wafers on the scale required to satisfy the needs of the entire electronics industry.

Virtual substrates are created by the deposition of $Si_{1-x}Ge_x$ layers, typically several μm, onto a silicon substrate several millimetres thick. This reduces the amount of germanium consumed and makes virtual substrate fabrication a more economically

attractive prospect. The $Si_{1-x}Ge_x$ will initially be under compressive strain during the early stages of crystal growth when the layer is thin. By growing the layer in excess of a *critical thickness* (discussed in section 2.3.2, it will relax towards the $Si_{1-x}Ge_x$ bulk lattice constant, creating a template for the inducement of strain into layers grown on its surface (hence the name "virtual" substrate).

2.2 Epitaxial Growth

Deposition of crystalline material in a layer-by-layer fashion is commonly referred to as *epitaxy*. Controlled epitaxial growth is mainly accomplished by two techniques; molecular beam epitaxy (MBE) and chemical vapour deposition (CVD). For a detailed account of MBE systems and growth kinetics, see Herman and Sitter [1989].

2.2.1 Chemical Vapour Deposition

CVD is capable of producing high-purity crystalline materials with a high throughput, making it the favoured industrial tool. CVD systems use gaseous precursors to deposit material through chemical reactions with a heated substrate. There are many types of CVD reactors [Greve, 1993] which vary over a wide range of gas pressures (from atmospheric to ultra-high vacuum) and temperatures (approximately 700 - 1300°C, for silicon related applications). A cross-sectional diagram of a typical low-pressure CVD (LPCVD) system is shown in figure 2.5.

Epitaxial growth takes place inside a quartz reactor. Multiple heaters above and below the substrate control growth temperature which is monitored by thermocouples in the susceptor, on which the substrate lies. Precursor gases are pumped through the chamber together with a carrier gas, which is typically nitrogen or hydrogen, the choice of which influences the growth process.

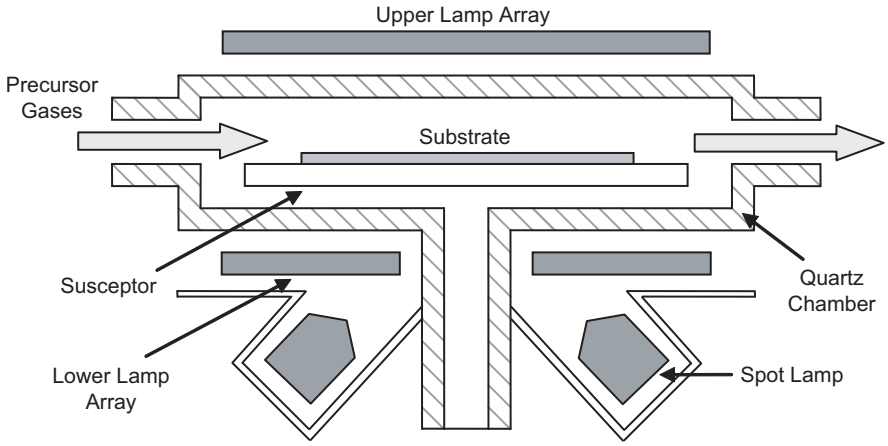

Figure 2.5: Cross-sectional diagram of a typical quartz chamber low-pressure CVD system.

Prior to introduction into the CVD system, substrates are cleaned to remove contaminants and oxide from the surface. A dilute hydrofluoric acid (HF) dip is often used as part of the cleaning process, which terminates the surface of the substrate with hydrogen, preventing oxidation for several hours. For more information on cleaning processes, see Kern [1993].

For the growth of silicon, the simplest precursor gas is silane (SiH_4), which undergoes the following simple reactions [Maiti et al., 2001]:

$$SiH_4 + 2* \rightarrow SiH_3 * + H* \tag{2.6}$$

$$SiH_3* \rightarrow Si * + 3H^+ \tag{2.7}$$

Where "$*$" represents a free bonding site on the substrate surface, and "X$*$" is a chemical species bonded to the surface. Surface sites are atoms on the substrate surface which are free to form a chemical bond.

In equation 2.6, silane molecules are adsorbed onto the substrate at two adjacent

surface sites. One is occupied by a hydrogen atom from the silane molecule, and the other by SiH_3. The Si atom becomes fully dehydrogenated in equation 2.7, and H_2 gas is evaporated. This can occur by the intermediate formation of SiH_2 and/or SiH, until the silicon adatom is incorporated onto the growth surface of the crystal. Figure 2.6 shows some of the different silane adsorption processes.

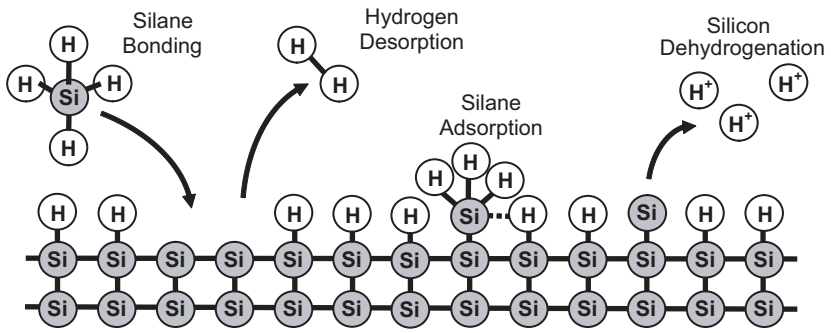

Figure 2.6: Diagram representing the bonding processes for silane on a silicon substrate surface during CVD epitaxy. Adaped from Greve [2001].

Another commonly used precursor for depositing silicon is dichlorosilane (SiH_2Cl_2), which undergoes the same adsorption processes as silane. Chloride ions in the reacting mixture also terminate surface sites, which become free by the liberation of hydrochloric acid (HCl). The presence of HCl helps reduce contaminants during the CVD process by etching any silicon deposits off the chamber walls [Hull and Bean, 1999].

Hydrogen, when used as a carrier gas plays an important role in the epitaxy process. It acts as a *surfactant* [Tounié and Ploog, 1993] which helps keep the surface of the growing layer smooth. It readily terminates surface sites, which influences the growth rate as silane can only bond with the substrate surface once two hydrogen ions have been desorbed. This is a thermally activated process, so deposition is limited by hydrogen liberation at low temperatures, and the supply of silane at high temperature.

Nitrogen performs no surfactant or surface termination roles, and therefore gives a higher growth rate when it is used as a carrier gas.

Germane (GeH_4) is used for germanium deposition, which undergoes the same reaction processes as silane. It adsorbs more readily than silane, and dehydrogenates more freely after adsorption. This affects the growth rate of silicon-germanium in a complex way. For low germanium composition $Si_{1-x}Ge_x$ epitaxy, the easier dehydrogenation of germanium atoms creates more surface sites for silane or germane adsorption, which increases growth rate. At higher germanium compositions, the surface of the substrate contains more germanium atoms (and fewer hydrogen atoms) which decreases the adsorption of germane, leading to an overall decrease in growth rate [Robbins et al., 1991].

2.2.2 Growth Kinetics of Silicon-Germanium

Strain plays an important role in the growth of crystal surfaces. In its absence (homoepitaxy), the surface follows van der Merwe growth [Frank and van der Merwe, 1949] where adatoms fill an entire layer before nucleating another on top (figure 2.7 (a)). The opposite extreme to this is Volmer-Weber growth [Volmer and Weber, 1926] for highly lattice mismatched materials, in which island clusters nucleate because it is energetically favourable for deposited material to grow on itself, rather than the substrate (figure 2.7 (b)). Strain can actually be relieved in this fashion, due to the change in lattice constants produced by surface undulations. In the intermediate case where there is a lower lattice mismatch, growth will initially commence in a van der Merwe fashion, with a switch to Volmer-Weber growth as the layer becomes thicker. This is due to the accumulation of strain energy as the lattice mismatched layer becomes thicker, and is called Stranski-Krastanov growth [Stranski and Krastanov, 1938] (figure 2.7 (c)). In general, strained layer epitaxy will occur via Stranski-Krastanov or Volmer-Weber growth, with

the formation of islands favoured by higher strain [Hull and Bean, 1999].

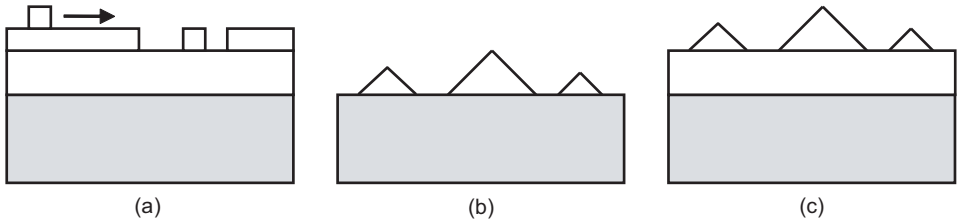

Figure 2.7: Schematic illustration of the three epitaxial growth modes (a) van der Merwe growth, (b) Volmer-Weber growth and (c) Stranski-Krastanov growth. Taken from [Hull and Bean, 1999].

2.3 Relaxation and Dislocations

The thickness of material grown under strain is limited by the critical thickness. Whilst thinner layers will remain strained under normal conditions, thicker layers will undergo relaxation by the formation of dislocations.

2.3.1 Basic Dislocation Theory

Dislocations Formed by Strain

The growth of a lattice mismatched layer (such as in figure 2.2) has an associated areal elastic energy density stored at the misfit interface, E_h, given by [People and Bean, 1985]:

$$E_h \approx 2G\left(\frac{1+\nu}{1-\nu}\right)h\epsilon^2 \tag{2.8}$$

Where h is the thickness of the strained layer, G is its bulk shear modulus, ν is Poisson's ratio and ϵ is the strain in the layer (see equation 2.2). As the thickness of

the layer increases, E_h will become large enough to break atomic bonds at the strained interface (this thickness will be discussed in section 2.3.2), and plastic deformation of the crystal will induce relaxation towards its bulk lattice constant. These deformations displace material along lines which form discontinuities in the lattice structure and break the commensurate nature of the misfit interface. The resulting discontinuity is called a *dislocation* and is shown in figure 2.8 for a compressively strained interface.

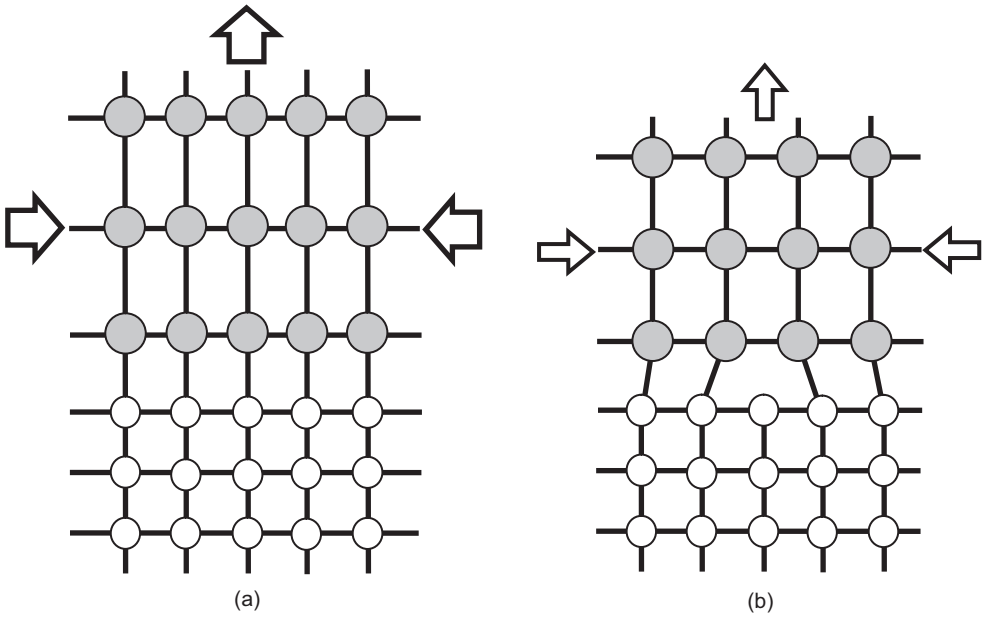

Figure 2.8: Simplified diagram showing (a) a compressively strained layer (in grey) and (b) partial relaxation of the layer by a dislocation. The line direction of the dislocation is directed into the plane of the page. Adapted from Hull and Bacon [2002].

Burgers Vectors

A dislocation is defined by its *Burgers vector*, which points along the direction of the displacement of the crystal lattice, with a magnitude equal to the displacement. Burgers vectors can be determined by tracing a closed circuit from lattice point to lattice point

in a perfect crystal and comparing it to the same circuit traced around a dislocation. In the dislocated material, the starting point will not meet the ending point, and the vector needed to close the circuit defines the direction of the Burgers vector (figure 2.9) [Cottrell, 1964].

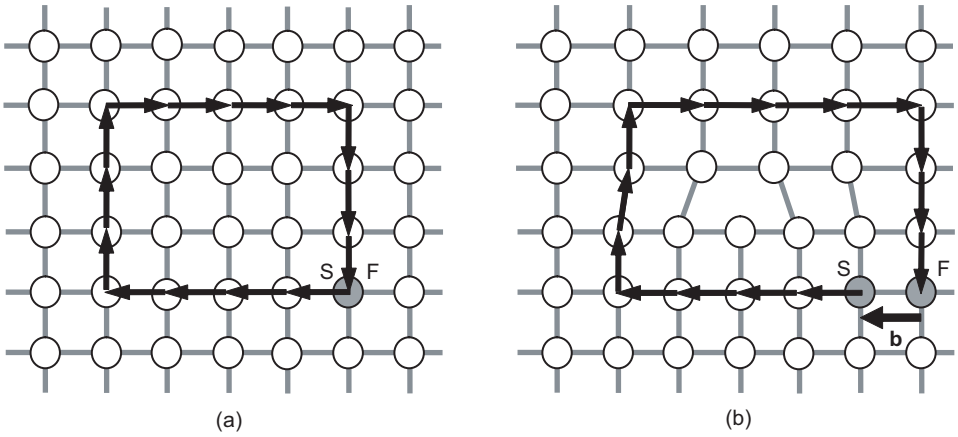

Figure 2.9: Diagram showing (a) the construction of a closed circuit in a perfect crystalline material starting at point S and finishing at point F, and (b) the failure of the same circuit to close around a dislocation. This is used to define the direction of the Burgers vector, $\mathbf{b}$. Adapted from Cottrell [1964].

The orientation of the Burgers vector relative to the line direction of a dislocation gives rise to a naming convention. If they are mutually perpendicular (as in figure 2.9), the dislocation is termed an *edge dislocation*. When parallel, the dislocation is a *screw dislocation*. Any other angle is called a *mixed dislocation*, for which the Burgers vector has both edge and screw components. The Burgers vector of a dislocation must be constant along the whole length of the dislocation, otherwise there will be additional displacements introduced into the crystal lattice. Burgers vectors are therefore conserved in splitting reactions, which will be discussed in section 2.5.2.

Dislocations should not be regarded as physical objects, but instead as a bound-

ary between regions of crystalline material that are displaced relative to each other. Therefore, dislocations cannot terminate within the lattice and must form as a closed loop, or terminate at a free surface (such as the edge of the wafer, an impurity within the crystal, or the surface of the layer). The component of a dislocation that lies at the misfit interface is termed a *misfit dislocation* and contributes to the relaxation of the strained layer. *Threading dislocations* are the non-strain relieving components of dislocations that do not lie at the misfit interface. Dislocations formed during growth are "grown into" the material, as deposited material maintains the crystal structure, preserving the presence of dislocations.

Glide of Dislocations in Silicon-Germanium

Dislocations can move under the influence of strain by a process known as *glide*. Glide occurs by the sliding of one plane of atoms over another, which propagates the threading dislocation component forward, and lengthens the misfit dislocation at the strained interface. This is shown in figure 2.10.

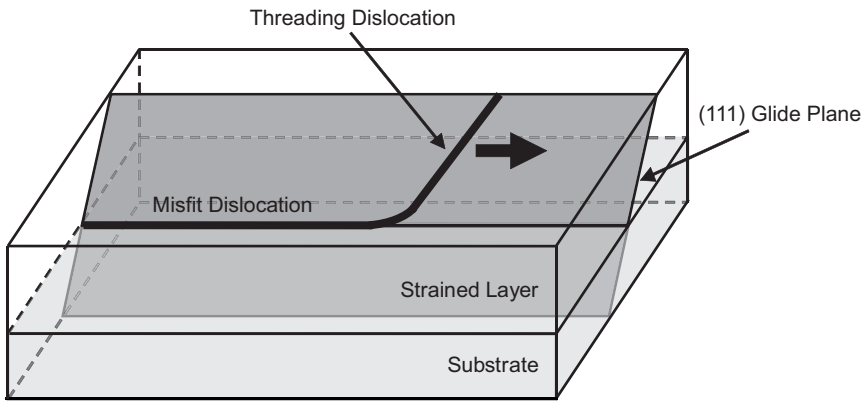

Figure 2.10: Simplified diagram showing dislocation glide which increases the length of the misfit component at the strained interface.

The glide-planes within the material are normally the set of planes with the highest density of atoms, and the direction of displacement (in which the Burgers vector points) is the direction on that plane in which the atoms are closest packed. In silicon and germanium (and all face-centred cubic and diamond crystals) the highest density of atoms are found on the $\{111\}$ planes, and the closest packed atoms are along the $<101>$ directions (see figure 2.11). Dislocations in silicon and germanium therefore have a Burgers vector given by $\mathbf{b} = \frac{a}{2} <101>$ (where a is the lattice constant of the material), as this is the shortest atomic translation vector along the closest atomically packed direction. $\mathbf{b}$ has a magnitude of 3.9Å in bulk silicon.

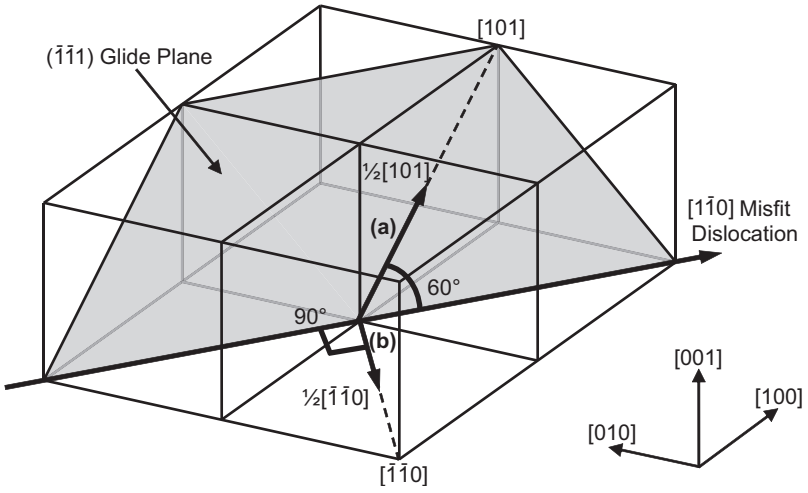

Figure 2.11: Simplified diagram showing the orientations (a) 60° and (b) 90° Burgers vectors for a $[1\bar{1}0]$ misfit dislocation. Taken from Nash [2005].

The misfit dislocation line directions are formed along $<110>$ directions in silicon and germanium, where the $\{111\}$ glide-planes intersect the (001) strained interface plane. Burgers vectors (along the $<101>$ directions) form an angle of 60° with the dislocation line directions (along $<110>$) and hence are mixed dislocations.

Edge dislocations (where the Burgers vector forms an angle of 90° with the dislocation line) can also form for which the Burgers vector is equal to $\frac{a}{2}$ <110>. Although they each relieve more strain than 60° dislocations, (see section 2.5) they cannot glide along the {111} glide-planes, and can only propagate by a higher energy process known as climb. For this reason 60° dislocations are the predominant dislocations at lower strain. Increasing the growth temperatures has been shown to increase the numbers of 90° dislocations formed [Hull and Bean, 1989].

Relaxation of a Single Dislocation

Each dislocation contributes to the relaxation of the strained layer along its length, L, by the degree of displacement it causes at the misfit interface. This is determined by resolving the Burgers vector (the magnitude of which gives the total displacement) into the misfit interface plane. Relaxation along the <110> directions is given by the component of the in-plane Burgers vector, $\mathbf{b}_a$, which lies perpendicular to the displacement line direction, $\mathbf{u}$, as shown in figure 2.12.

This component is termed the effective Burgers vector, $\mathbf{b}_{eff}$. By considering the unit cell geometry of the diamond structure in figure 2.12, the magnitude of the Burgers vector is given by $\mathbf{b} = \frac{\sqrt{{a_x}^2+{a_z}^2}}{2}$, where a_x is the in-plane lattice constant (see equation 2.1) and a_z is the out-of-plane lattice constant of the unit cell. This leads to an equation for the magnitude of the effective Burgers vector [Bugiel and Zaumseil, 1993]:

$$b_{eff} = \frac{a_x}{2\sqrt{2}} \tag{2.9}$$

The line density of misfit dislocations, ρ_{MD}, in a given area, A, is determined by the total length of misfit dislocations revealed that area, L_T, divided by the area.

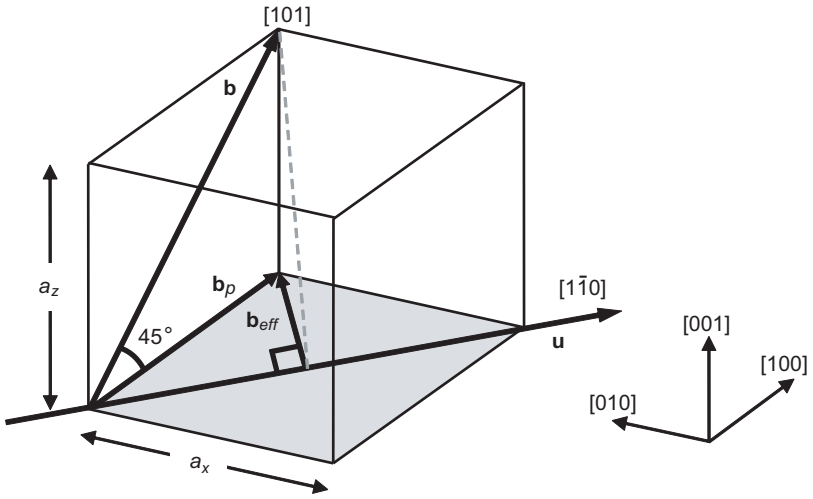

Figure 2.12: Schematic representation of the components of a Burgers vector, $\mathbf{b}$, for a 60° dislocation orientated along $[1\bar{1}0]$ in a single unit cell of base dimension a_x and height a_z.

Together with b_eff, the total relaxation per unit area caused by misfit dislocations, $\delta_M D$, can be determined:

$$\delta_{MD} = \frac{L_T}{A} b_{eff} = \rho_{MD} b_{eff} \tag{2.10}$$

With a suitable experimental technique for revealing misfit dislocations at a strained interface, it is possible to calculate the amount of relaxation per unit area using equation 2.10. However, it is assumed that all revealed dislocations are of 60° type. This will not always be the case, as some dislocations in highly strained layers may be of 90° type [Hull and Bean, 1989]. Further complications arise in tensile strained layers, as will be discussed in section 2.5.2.

2.3.2 Critical Thickness

The critical thickness for any strained layer is defined as the minimum thickness required to form misfit dislocations at the strained interface. Several different mathematical models have been formulated to describe this, most of which are refinements to the two presented in this section.

Matthews and Blakeslee Mechanical Equilibrium Theory

The model proposed by Matthews and Blakeslee [Matthews and Blakeslee, 1974] is based on a mechanical equilibrium argument which considers the strain acting on a threading dislocation. Sufficient strain at the misfit interface layer will exert a force, F_h, on the threading dislocation and cause it to glide, forming a misfit dislocation as shown in figure 2.13.

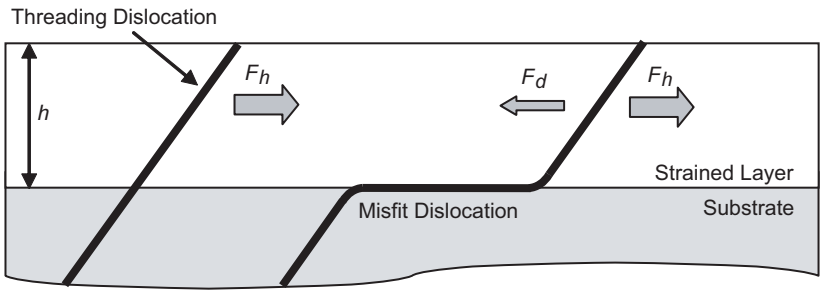

Figure 2.13: Cross-sectional diagram showing the forces acting on a threading dislocation during glide, as used to formulate the Matthews and Blakeslee mechanical equilibrium criterion. Adapted from People and Bean [1985].

F_h will increase with thickness, h, and can be approximated from equation 2.8:

$$F_h \approx G\left(\frac{1+\nu}{1-\nu}\right) bh\epsilon \tag{2.11}$$

Where b is the displacement distance of the lattice (i.e., the magnitude of the Burgers vector). The dislocation has a "tension" associated with it, which arises from the energy needed to reconfigure atomic bonds to propogate the misfit dislocation as the associated threading dislocation glides. This is approximated by:

$$F_d \approx \frac{Gb^2(1-\nu\cos^2\theta)}{4\pi(1-\nu)}\ln\left(\frac{h}{b}\right) \tag{2.12}$$

Where θ is the angle between the Burgers vector and the dislocation line. F_h must exceed F_d before the dislocation will glide. The minimum thickness at which this will occur is when $F_h = F_d$. By equating equations 2.11 and 2.12, the critical thickness, h_c, can be calculated:

$$h_c \approx \frac{b(1-\nu\cos^2\theta)}{4\pi(1+\nu)\epsilon}\ln\left(\frac{h_c}{b}\right) \tag{2.13}$$

People and Bean Energy Balance Theory

The approach made by People and Bean is very similar to an earlier theory proposed by Van der Merwe [der Merwe, 1963]. Both theories deal with minimising energy to determine critical thickness, but differ in that People and Bean considered the energy required to *nucleate* dislocations in initially dislocation-free layers [People and Bean, 1985, 1986].

Nucleation has an associated activation energy, making it a higher energy process than dislocation glide (the later is therefore predominant when there are pre-existing dislocations). The boundaries of a crystal structure locally lower the energy barrier for nucleation, so in the absence of impurities, dislocations nucleate as *half-loops* from the surface, as shown in figure 2.14.

Nucleated half-loops expand under the influence of strain until they reach the

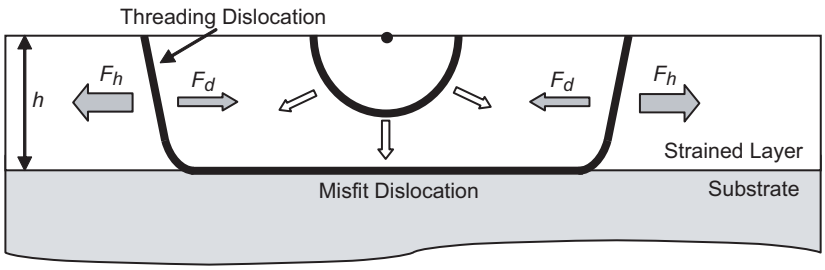

Figure 2.14: Cross-sectional diagram showing the forces acting on a nucleated half-loop dislocation, as used in the People and Bean critical thickness model. Adapted from People and Bean [1985].

misfit interface, and glide proceeds by the motion of both threading components along the same glide-plane. Each threading dislocation component of the half-loop dislocation is subjected to the same balance of forces as a gliding threading dislocation in figure 2.13. People and Bean approximated the areal activation energy density for the creation of an isolated dislocation by:

$$E_d \approx \left(\frac{Gb^2}{8\pi\sqrt{2}a(x)}\right)\ln\left(\frac{h}{b}\right) \tag{2.14}$$

Where $a(x)$ is the lattice constant of the strained layer, given by equation 2.1. The minimum (critical) thickness required to nucleate the first 60° dislocations is given by equating 2.8 and 2.14:

$$h_c \approx \left(\frac{1-\nu}{1+\nu}\right)\left(\frac{b^2}{16\pi\sqrt{2}\epsilon^2 a(x)}\right)\ln\left(\frac{h_c}{b}\right) \tag{2.15}$$

Figure 2.15 shows a plot of the Matthews and Blakeslee and People and Bean critical thickness regimes (equations 2.13 and 2.15) for a layer of $Si_{1-x}Ge_x$ grown on a silicon substrate (or a layer of silicon grown on a bulk $Si_{1-x}Ge_x$ substrate), using the values $b = 3.9$Å, $G = 65$GPa, $\nu = 0.28$ [Hull and Bean, 1999], $\theta = 60°$, $a(x)$ as dictated

by equation 2.1, and ϵ as given by equation 2.3 as a function of germanium composition.

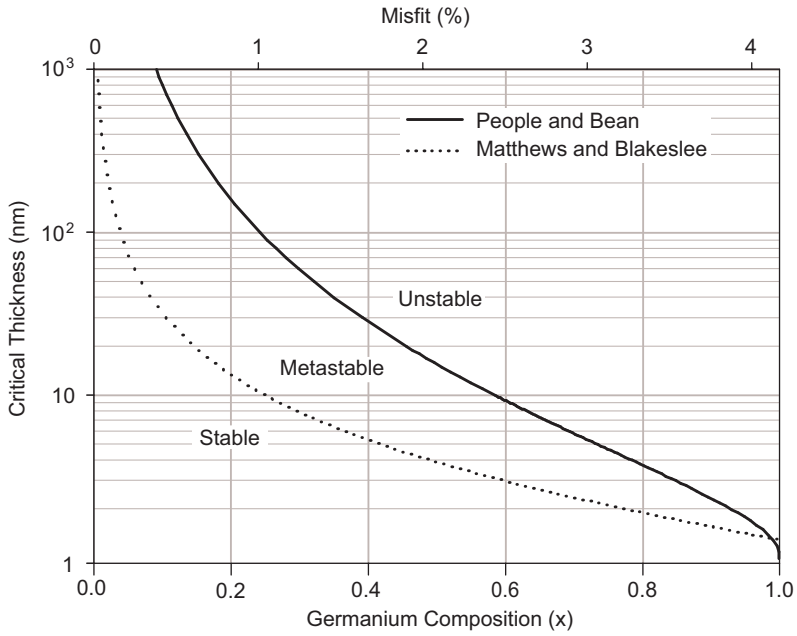

Figure 2.15: Graph showing the critical thickness regimes of Matthews and Blakelee (equation 2.13), and People and Bean (equation 2.15).

Below the Matthews and Blakeslee curve strain provides an insufficient force for dislocation glide, and no misfit dislocations form. Any layers falling into this regime are termed *stable*. The People and Bean curve describes the thickness at which dislocation nucleation will occur. Layers thicker than this criterion are therefore *unstable*.

Layers in the region between the curves are termed as *metastable*. In this region there may be no relaxation at reduced growth temperatures, as there may be insufficient energy for dislocation glide or nucleation. Extensive work by Houghton [1991] has lead to a family of curves in the metastable regime described by a semi-empirical model for the temperature dependence of critical thickness. A larger *ultrametastable* critical thickness regime that described by People and Bean can be obtained at very low temperatures

(<550°C) [Kasper et al., 1995].

2.3.3 Interactions Between Dislocations

Pinning Events

A misfit dislocation contributes to the total relaxation of a strained layer, but contains a large degree of localised stress due to the distortion of the atomic bonds along its length [Weertman and Weertman, 1966]. If another dislocation glides along a <110> direction orthogonal to this dislocation line, it would require a higher degree of driving strain than in the rest of the layer to overlay a length of misfit dislocation in this distorted region.

Freund [1990] derived mathematical expressions to describe this interaction. In this model it is assumed that the presence of the strain field adds a retarding force to the gliding threading dislocation, which forces the dislocation to glide in a channel region thinner than the strained layer thickness, h_*. This is shown in figure 2.16.

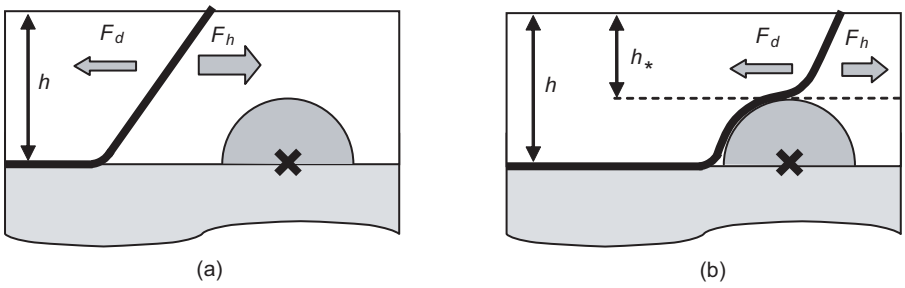

Figure 2.16: Cross sectional view showing a threading dislocation (a) gliding towards an orthogonal misfit dislocation, marked by the cross with surrounding strain field in grey, (b) being forced to glide in a smaller channel region, h_*.

If there is insufficient strain in h_* for the dislocation to continue gliding, it will become pinned and will progress no further. The minimum strain required for glide in h_* is given by the Matthews and Blakeslee critical thickness (equation 2.13). This gives

an estimate of the minimum strain, ϵ_0, below which a dislocation will become pinned:

$$\epsilon_0 = \frac{b}{2\pi}\left[\frac{1}{(h-h_*)} + \frac{1}{2h_*}\ln\left(\frac{8h_*}{b}\right)\right] \tag{2.16}$$

This equation relies on an estimate of the quantity h_*, which varies between zero and h. The minimum strain required for pinning coincides with the minimum of h_* in equation 2.16, and so h_* must satisfy:

$$\frac{2{h_*}^2}{(h-h_*)^2} + 1 = \ln\left(\frac{8h_*}{b}\right) \tag{2.17}$$

Equations 2.17 and 2.16 together define a critical thickness for dislocation pinning, below which all dislocations will become pinned. This is plotted in figure 2.17.

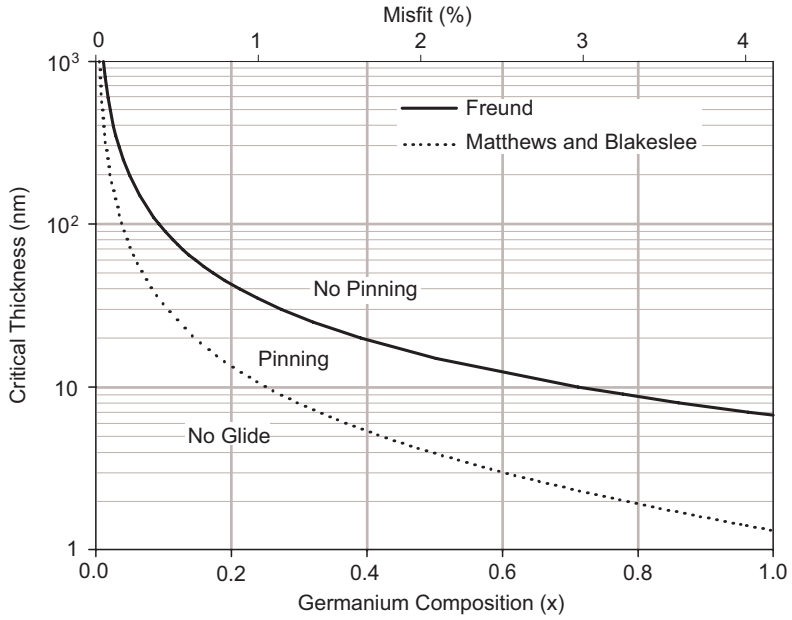

Figure 2.17: Graph showing the Freund dislocation pinning regime (equation 2.16), together with the critical thickness of Matthews and Blakeslee (equation 2.13).

More detailed calculations by Freund have shown that the additional retarding

force should be at a minimum if the Burgers vectors of the two interacting dislocations are parallel, and at a maximum when they are perpendicular. Observations of strained $Si_{1-x}Ge_x$ layers on silicon substrates, however, disagreed [Stach et al., 2000]. All dislocations were pinned in the predicted pinning regime, and no pinning events were observed for much thicker layers (as expected). Close to the pinning critical thickness, pinning only occured when Burgers vectors were parallel (the reverse of what is expected). In addition to these conclusions, it was also shown that dislocation pinning results in very stable configurations which require greater stresses than associated with the initial interaction for release.

Over-Relaxation

Relaxation along the length of a misfit dislocation is perpendicular to its line direction (see section 2.3.1). A group of closely spaced misfit dislocations running parallel to each other can form a region of "over-relaxation", where the local relaxation is much higher than in the rest of the layer. A threading dislocation gliding through this region will experience a reduced strain, inhibiting its glide. While this alone may be insufficient to impede progress, computer simulations have identified this as a possible contributory factor in dislocation pinning [Schwarz, 2003], in which the reduced strain makes dislocations more sensitive to pinning. No empirical evidence exists to verify this result.

2.3.4 The Modified Frank-Read Mechanism

The interaction of pre-existing dislocations can lead to the formation of more dislocations through *multiplication*. The *modified Frank-Read mechanism* (MFR mechanism) is the most widely accepted theory for dislocation formation by multiplication. It was first proposed to explain the presence of dislocations pushed deep into the silicon substrate

of compositionally graded virtual substrates [LeGoues et al., 1992], but had already been noted prior to this in single strained layer epitaxy [Meyerson et al., 1988].

The Frank-Read process [Hirthe and Lothe, 1982] forms the basis for the mechanism, in which a pinned misfit dislocation subjected to a large enough strain can unpin itself by bowing down towards the substrate and forming a closed loop around the dislocations pinning it in place. The process reforms the original pinned misfit dislocation and creates an additional dislocation loop which is free to expand. More dislocation loops can be formed in the same fashion (from the replaced pinned dislocation), until the relaxation is enough to negate the stress of the layer.

In the MFR mechanism, two crossing dislocations with parallel Burgers vectors on orthogonal glide-planes form the source. A splitting reaction reforms the two dislocations into corner shaped dislocations, each straddling both glide-planes (figure 2.18 (a)). One of the corners is bent down towards the substrate, along the intersection line between the two glide-planes [Lefebvre et al., 1991].

This corner dislocation expands as a half-loop along both glide-planes, where it begins to close-up by the typical Frank-Read mechanism (figure 2.18 (b)). The loop expands and closes in on itself, forming a whole loop which replaces the initial corner dislocation. Further expansion leads to intersection with the surface, forming a half-loop. The two threading dislocations can then glide along the two orthogonal glide-planes, and contribute to relaxation in both directions (figure 2.18 (c)).

The replaced corner dislocation may undergo the same process if sufficient strain exists. This results in a network of dislocations, all with the same Burgers vector (figure 2.18 (d)). Mutual repulsion between the dislocations, with equal Burgers vectors, forces previously nucleated dislocations into the substrate.

The presence of such a network can lead to the pinning of orthogonal gliding

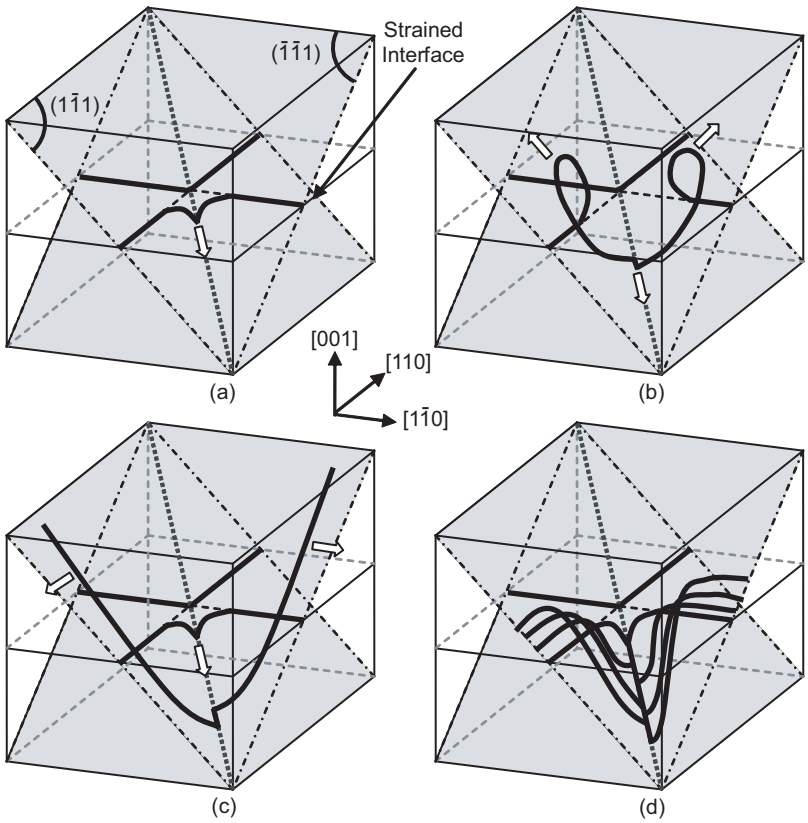

Figure 2.18: Schematic representation of the modified Frank-Read process showning (a) a splitting reaction, (b) the Frank-Read mechanism closing a half-loop, (c) expanding half-loop to reach the surface, and (d) a pile-up formed by the expansion of dislocation half-loops along two glide-planes. Adapted from LeGoues et al. [1992]

dislocations, the threading components of which terminate at the surface in a dense line known as a dislocation *pile-up*. Such a high concentration of threading dislocations would be potentially disastrous for electronic device performance. Unfortunately, dislocation pile-ups form as a direct consequence of the MFR mechanism, but are actually *beneficial* to the fabrication of virtual substrates.

2.4 The Structure of a Virtual Substrate

Electronic devices fabricated on strained layers containing dislocations suffer from a degraded electrical performance compared to dislocation free layers [Fiorenza et al., 2004]. Misfit dislocations can act as diffusion pathways for dopants (which make the strained silicon electrically active) and allow charge to flow down them, increasing the current leakage from the device.

Virtual substrates must therefore be designed to keep the density of threading dislocations low. Surface roughness must also be kept to a minimum as thin strained overlayers will adopt the same roughness which interferes with the precise nature of manufacturing nanometre scale devices.

2.4.1 Basic Designs

Constant Composition Layers

The simplest virtual substrate is a layer of $Si_{1-x}Ge_x$ grown on a silicon substrate in excess of the critical thickness to ensure its surface is relaxed. In the absence of pre-existing dislocations and sources of nucleation, relaxation occurs around the People and Bean critical thickness by half-loop nucleation. All misfit dislocations are confined to the single misfit interface at the silicon substrate, which leads to numerous dislocation

pinning events. This limits glide, and increases the need for more dislocations to nucleate for relaxation to progress. The result is a virtual substrate with a very high density of threading dislocations, typically $>10^9 \text{cm}^{-2}$ [Herzog et al., 2000].

Step Grading

Step graded virtual substrates consist of a number of constant composition layers grown with increasing composition. A simple four tier step graded structure is shown in figure 2.19 up to 20% germanium composition. This divides the single misfit interface of the previous case into several lower mismatched interfaces.

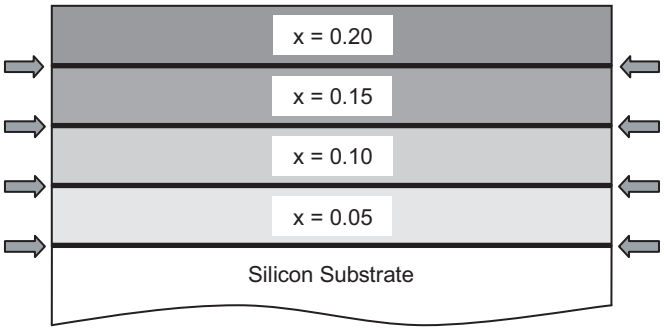

Figure 2.19: Schematic representation of a step graded virtual substrate, with misfit interfaces is arrowed.

Fewer misfit dislocations are required to relax each layer, reducing the number of pinning events at each interface. Threading dislocations which become pinned are able to glide with the growth of another misfit interface and contribute to the relaxation of that layer. This reduces the need to nucleate dislocations, and leads to an overall reduction in the density of threading dislocations at the surface depending on the lattice mismatch of each interface, to around 10^6 - 10^7cm^{-2} (for the case of a $Si_{0.7}Ge_{0.3}$ virtual substrate, [Watson et al., 1994]).

Linear Grading

Almost all modern virtual substrates use linear grading techniques in some fashion, where the germanium composition is increased gradually with layer thickness from zero up to the final desired value. A thick constant composition layer is added, to ensure the upper layers of the graded region are relaxed, which also spatially separates misfit dislocations from the surface. An example of linear grading up to 20% is shown in figure 2.20.

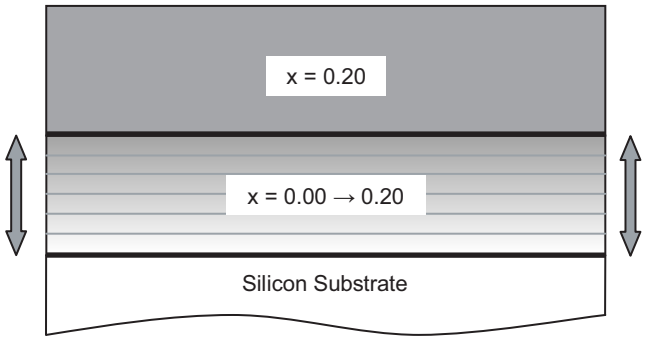

Figure 2.20: Schematic representation of a linear graded virtual substrate, the continuum of misfit interfaces is denoted by the arrowed region.

Linear grading is similar to step grading in that misfit interfaces are spatially separated with a low lattice mismatch to minimise dislocation interactions. Instead of discrete interfaces on which dislocations are confined, there is now a continuum of misfit interfaces. Dislocations form along any lattice plane in this region, greatly reducing the likelihood of interactions between dislocations on the same plane.

The growth of compositionally graded material is favourable for the MFR mechanism to act on any dislocations involved in splitting reactions. Dislocations nucleated through multiplication can glide on different misfit interfaces, rather than many dislocations gliding on only one (see figure 2.18. The MFR mechanism results in many dislocation pile-ups at the surface, but may also be responsible for an overall reduction

in the density of threading dislocations by large scale annihilation, from the proposed "self-alignment" of multiplication sources [LeGoues, 1994]. Misfit dislocations also result in surface steps of around 2.5Å [Lutz et al., 1995], and as the MFR process occurs throughout the entire graded region along both <110> directions, large surface step *crosshatching* forms along these directions [Fitzgerald et al., 1999]. Densities of threading dislocations are typically in the range of 10^5 - $10^6 cm^{-2}$ across a wide range of compositions [Bogumilowicz et al., 2006], and are linked to the compositional grading rate [Dutarte et al., 1994].

Terrace Grading

Terrace graded virtual substrates consist of both linear graded regions and constant compositional steps. An example for 20% final germanium content is shown in figure 2.21.

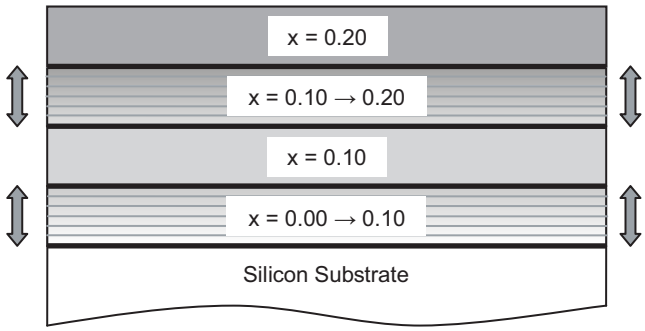

Figure 2.21: Schematic representation of a terrace graded virtual substrate, the continua of misfit interfaces are denoted by the arrowed regions.

In linear graded structures the number of threading dislocations pinned in pile-ups will increase as the structure grows, and more misfit interfaces are created. By introducing constant composition terraces into the structure, pile-ups formed in each of

the graded regions cannot permeate the entire structure as they are spatially separated by strain free layers from the initial MFR source. This limits the total number of pile-ups reaching the surface, which subsequently reduces the surface roughness (smaller surface steps are created), and the density of threading dislocations (fewer dislocations are pinned in pile-ups, reducing the requirement for nucleation). The surface of a terrace graded virtual substrate still retains the characteristic undulating crosshatch pattern.

Early work on terrace grading demonstrated improvements over linear grading techniques [Capewell et al., 2002]. Subsequent studies showed the possibility of the complete elimination of pile-ups, with threading dislocation densities in the region of 10^4 - $10^6 cm^{-2}$, up to 50% germanium [Nash, 2005].

2.4.2 Advances in Virtual Substrate Fabrication

Novel implementation of compositional grading is not the only way to improve virtual substrates. Thinner virtual substrates can be fabricated to reduce the amount of material consumed, and heating issues associated with devices fabricated from strained silicon overlayers on thick virtual substrates [Olsen et al., 2006]. Two methods have been employed to achieve this, both of which involve the deliberate introduction of defects into the crystal structure of the virtual substrate to promote dislocation nucleation. The first is to implant ions into the $Si_{1-x}Ge_x$ (such as Si^+ [Holländer et al., 2006], H^+ [Trinkaus et al., 2000] or He^+ [Khan et al., 2007]) so that subsequent annealing leads to dislocation nucleation.

In the second method, defects are introduced during the low temperature growth of an initial $Si_{1-x}Ge_x$ seed layer. The low temperature limits adatom mobility, which leads to imperfect crystalline growth. Elevated growth temperatures for subsequent layers allow dislocations to nucleate from the seed layer [Myronov and Shiraki, 2007].

Chemical mechanical polishing (CMP) has also been employed as an intermediate stage of growth, or as the final step. This flattens the surface and ultimately reduces roughness and crosshatching [Sawano et al., 2003], and can be used to improve any virtual substrate structure without the need to redesign or implant.

Strained Silicon on Insulator

Another silicon based structure which is of great interest to the electronics industry is that of silicon-on-insulator (SOI). The insulating layer of SiO_2 to which the silicon is bonded, affords better electrical isolation for each device, allowing a greater density of devices to be packed together [Taraschi et al., 2004]. Transferral of a strained silicon layer from a virtual substrate onto an insulating platform therefore creates a structure with the advantages of an insulating platform, combined with the charge carrier mobility enhancements of strained silicon.

Such structures can be achieved using techniques such as SmartCut^{TM} [Bruel, 1996], in which the surface of the strained silicon is bonded to a thick layer of SiO_2 on a silicon substrate, and the virtual substrate removed. This leaves a rough surface containing residual $Si_{1-x}Ge_x$ from the virtual substrate, which can be removed with CMP. The quality of the strained silicon still depends on the virtual substrate on which it was grown prior to transferal, and so a low density of threading dislocations is desirable.

To aid a satisfactory bond with the oxide, the strained silicon layer must be smooth and also preferably thick, as some material is consumed by the CMP process. The growth of thick layers of strained silicon on virtual substrates, however, not only leads to the onset of dislocation glide and relaxation, but also to the generation of additional dislocation structures within the layer.

2.5 Relaxation of Strained Silicon

The relaxation of compressively strained $Si_{1-x}Ge_x$ layers on silicon substrates has been extensively researched in the development process of virtual substrates. Tensile strained silicon, however, remains comparatively less well studied, especially for layers far in excess of the critical thickness. Such layers have recently been found to be beneficial to device performance, due to the large spatial separation between devices and the misfit dislocation interface [Lauer et al., 2004; Lochtefeld, 2006]. A fuller understanding of the relaxation of tensile strained silicon as the critical thickness is exceeded forms the basis of this work.

Previous studies have indicated an enhanced stability, when compared to similarly strained $Si_{1-x}Ge_x$, for the relaxation of strained silicon a few times the Matthews and Blakeslee critical thickness, even after annealing [Samavedam et al., 1999]. Interaction and pinning of dislocations has been cited as the possible cause of this unexpected behaviour. To understand the stability of strained silicon, it is important to consider the different relaxation processes tensile and compressively strained layers undergo.

2.5.1 Partial Dislocations

A 60° dislocation is termed a perfect dislocation because the displacement of the lattice is by a whole number of lattice positions. This is actually not strictly true, as each 60° dislocation forms by two distinct displacements of a fractional number of lattice spacings, or *partial* dislocations.

In a hard sphere representation of a face-centred cubic structure, the $\{111\}$ atomic planes stack in a repeating "ABCABC" sequence along the $<111>$ surface normal directions, as shown in figure 2.22 (a). The atoms is plane "B" engage in the hollows of the underlying "A" plane, which in turn engage in hollows of the "C" planes

(which are not the hollows situated above "A" planes). The passage of a perfect 60° dislocation along a "B" glide-plane requires all lattice sites to move from one "B" site to another, along the direction of the Burgers vector, as shown in figure 2.22 (b). This requires energy, which is roughly proportional to the square of the Burgers vector, $\mathbf{b}_1$ (equation 2.14). A reduction in the energy can be made if the displacement occurs as a two step process with shorter Burgers vectors, $\mathbf{b}_2$ and $\mathbf{b}_3$, as ${\mathbf{b}_1}^2 > {\mathbf{b}_2}^2 + {\mathbf{b}_3}^2$ [Amelinckx, 1979]. In figure 2.22 (b), the displacement is shown to occur via intermediate "C" sites.

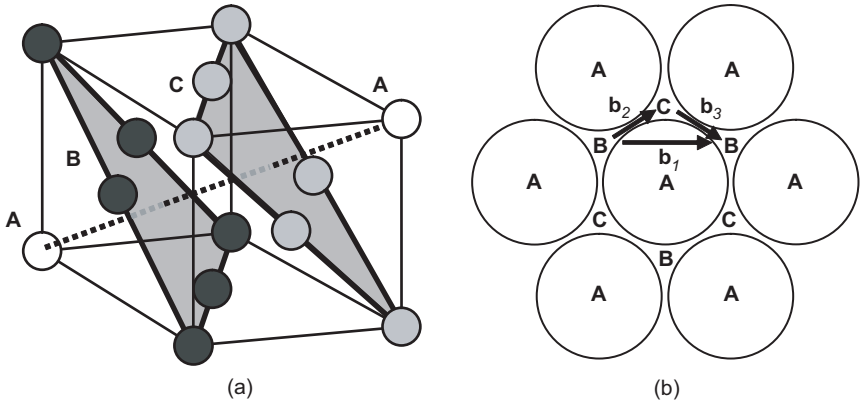

Figure 2.22: Simplified hard sphere representations of a face-centred cubic lattice showing (a) stacking of the $\{111\}$ planes, and (b) a top-down view of the stacking sequence. Taken from Cottrell [1964].

$\mathbf{b}_2$ and $\mathbf{b}_3$ are known as *Shockley partial dislocations* [Hull and Bacon, 2002], and are displacements by a fractional number of lattice spacings. Two displacements occur within the material (one after the other) as the 60° dislocation glides along, implying a dissociation (or splitting) of the Burgers vector, $\mathbf{b}_1$, into two distinct components:

$$\begin{gathered} \mathbf{b}_1 \rightarrow \mathbf{b}_2 + \mathbf{b}_3 \\ \tfrac{1}{2}[101] \rightarrow \tfrac{1}{6}[112] + \tfrac{1}{6}[2\bar{1}1] \end{gathered} \tag{2.18}$$

Note that in this reaction, the Burgers vector is conserved. The $\frac{1}{6}[112]$ dislo-

cation is a 90° partial dislocation (the Burgers vector forms an angle of 90° with the dislocation line direction along one of the <110> directions), and the $\frac{1}{6}[2\bar{1}1]$ a 30° partial dislocation. In general, all 60° dislocations are dissociated to some degree, with the two partial dislocations spatially separated by displaced material known as a *stacking fault*.

2.5.2 Extended Stacking Faults

A stacking fault is a 2-dimensional dislocation along which atomic planes do not engage in the correct stacking sequence. They are caused by the displacement of atoms from one stacking site to another by a partial dislocation. Figure 2.23 shows one partial dislocation in a crystal lattice at point P running into the plane of the page, which locally disrupts the stacking sequence from "ABCABCABC" to "ABCACABC". A second partial dislocation is required to re-established the normal stacking sequence (not shown in this figure, but will occur at the top of the grey stacking fault region). As a dislocation glides, one partial will lead and establish the stacking fault, while the second will trail behind and annihilate the stacking fault as it moves forward.

Mutual repulsion of the partial dislocations increases the size of the intervening stacking fault, but the formation energy of an area of stacking fault acts to reduce it. This leads to an equilibrium size [Zho and Cockayne, 1995], which in $Si_{1-x}Ge_x$ has been measured to be around 3nm [Baston, 2000]. Performing a Burgers circuit (see figure 2.9) around the individual partial dislocations will reveal the true orientation of their Burgers vectors, while a circuit draw around both partial dislocations and the stacking fault will yield the Burgers vector of a perfect 60° dislocation. Partial dislocations are normally neglected for this reason, but in tensile strained layers partial dislocations and stacking faults can become more important features.

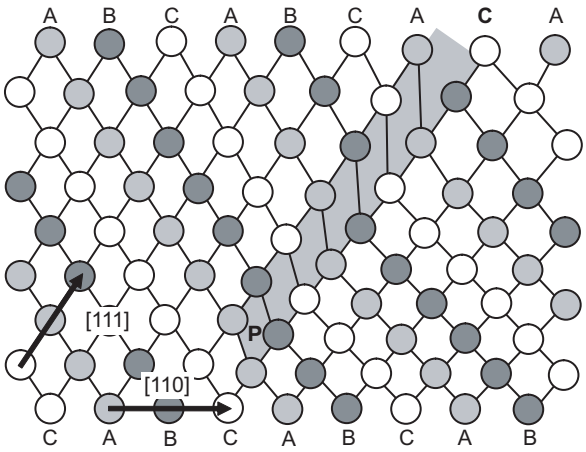

Figure 2.23: Simplified hard sphere representation of a cross section through a stacking fault (in grey) caused by one partial dislocation at point P, running into the plane of the page. Adapted from Kosevich [1979].

The 90° partial dislocation of a dissociated 60° dislocation experiences a larger driving force than the 30° partial under both compressive and tensile strain (due to $\cos\theta$ in equation 2.12). However, in compressive strain the 30° partial dislocation leads the 90° partial (it is the first displacement of the two stage process shown in figure 2.22 (b)) so is unable to pass the 30° partial, and the stacking fault remains at its equilibrium size [Marée et al., 1987]. In tensile strained material the situation is reversed and the 90° partial dislocation leads in the dissociation. As the 90° partial feels the stronger force, it can glide away from the 30° partial, and extend the intermediate stacking fault, as shown in figure 2.24. This only occurs if the strain energy exceeds the areal energy density of the stacking fault. The areal energy density is estimated to be in the range of 55 - 75mJ m^{-2} [Hull et al., 1992].

The presence of extended stacking faults in strained silicon is undesirable for the potential fabrication of electronic devices, as they increase current leakage in a similar

fashion to the presence of threading dislocations [Yang et al., 2000].

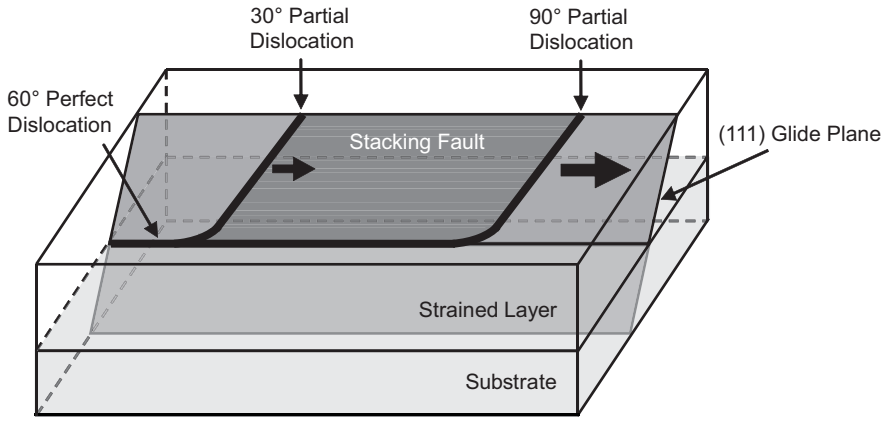

Figure 2.24: Schematic diagram of the formation of an extended stacking fault in a tensile strained layer. Adapted from Marée et al. [1987].

Figure 2.24 shows that an extended stacking fault formed in a tensile strained silicon layer is bounded by the 90° partial dislocation at the misfit interface. Relaxation along the length of the stacking fault can therefore be determined by resolving the Burgers vector $\mathbf{b}_{90} = \frac{1}{6} <112>$ into the plane of the strained interface, as described in section 2.3.1. This gives an effective Burgers vector for a stacking fault of:

$$b_{SF} = \frac{a_x}{3\sqrt{2}} \tag{2.19}$$

The relaxation of a given line density of stacking faults, ρ_{SF}, can therefore be determined using equation 2.10 by substituting $\mathbf{b}_{eff}$ for $\mathbf{b}_{SF}$:

$$\delta_{SF} = \rho_{SF} b_{SF} = \frac{L_T}{A} b_{SF} \tag{2.20}$$

2.5.3 Microtwins

As the 90° partial dislocation leads in the dissociation process of a 60◦ dislocation under tensile strain, it will also lead in the surface nucleation of a dislocation half-loop. A 90° partial dislocation can nucleate from the surface, without the need to nucleate a trailing 30° partial dislocation (as Burgers vector conservation does not apply at a free surface), and form a half-loop which encloses an area of stacking fault on a $\{111\}$ glide-plane, with the same effective Burgers vector as equation 2.19.

Regions of high strain formed along surface steps [Christian and Crocker, 1979], provide favourable regions for half-loop nucleation. The nucleation of a 90° partial dislocation adds an additional atomic scale step on the surface, further lowering the energy barrier for nucleation [Wegscheider and Cerva, 1993]. If another 90° partial dislocation were to nucleate on an adjacent glide-plane, their mutual repulsion will force the intial 90° partial dislocation deeper into the substrate. The resulting formation is known as a *microtwin* structure. Subsequent 90° partial nucleation events widen the microtwin, and push pre-existing partials deeper still, forming a stack of partial dislocations along a $\{111\}$ direction, as shown in figure 2.25.

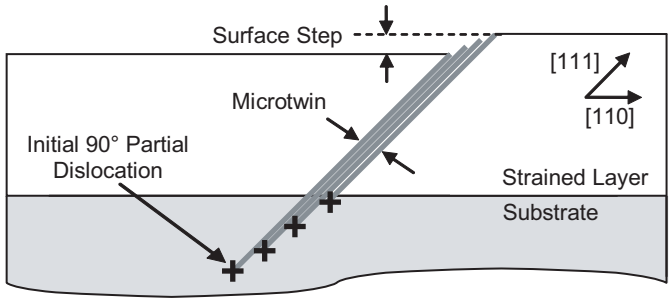

Figure 2.25: Cross-sectional view of a microtwin formed by the successive nucleation of 90° partial dislocations on adjacent glide-planes, which forms a step on the surface along its length. Adapted from Wegscheider and Cerva [1993].

The relaxation caused by a microtwin can only be ascertained if it is known how many partial dislocations it contains. It has been shown in other material systems that the number of dislocations contained within a microtwin increases with the strained layer thickness [Halley et al., 2002].

Microtwins also form in compressively strained layers by the surface nucleation of 30° partial dislocations, which lead in the dissociation process. However, the energy required is much larger than for the nucleation of 60° dislocations, and so are almost never observed in $Si_{1-x}Ge_x$ [Wegscheider et al., 1990].

Chapter 3

Experimental Techniques

In this chapter, the operating principals of the experimental techniques used in the rest of this work are described. Included are the relevant theories behind their implementations, and the motivations for their use.

3.1 Transmission Electron Microscopy

Transmission electron microscopy (TEM) allows the detailed imaging of virtual substrates at high levels of magnification (up to x500000). It is especially useful for determining the thickness of epitaxial layers, and observing dislocations at misfit interfaces. TEM requires samples that are transparent to impinging electrons for image formation, which equates to a sample thickness of a few hundred nanometres.

To achieve this, samples are mechanically ground to a thickness of $<15\mu$m, and ion milled until perforation. They can be prepared either for cross-sectional analysis (XTEM) along the $<110>$ directions, or for plan-view analysis (PVTEM) along the [001] direction. The nature of sample preparation provides a limited viewable area of some a few hundred μm^2. For more information on sample preparation, see Goodhew

et al. [2001].

In this work, all the TEM images were obtained using a JEOL JEM-2000FX microscope. Lenses in the electron microscope consist of electromagnetic coils and act in a similar way to convex lenses in a conventional optical microscope, bringing off-axis electrons into focus. This is illustrated in figure 3.1, with a comparison between a normal optical transmission microscope and a transmission electron microscope.

At the top of the column a tungsten filament is heated to induce the thermionic emission of electrons, which are accelerated towards a grounded anode at a normal operating voltage of 200kV. A Wehnelt cap over the filament acts to converge the electron beam. The whole column is kept under high vacuum ($<10^{-7}$mbar), to minimise electron interactions with matter.

The electron beam is initially collimated by a condenser aperture before it passes through two condenser lenses which control the width of the beam and its intensity. After passing through the sample, the electron beam is magnified by the objective lens to produce an intermediate image. This is magnified by the projector lens onto a phosphor screen to produce the final image, the focus of which is achieved with the objective lens. Photographic plates can be exposed to the electron beam by moving the screen aside, to record the final image. Figure 3.2 shows two example images taken of strained silicon in cross-section and plan-view.

3.1.1 Contrast in the TEM

Electrons passing through the sample are diffracted by planes of atoms within the crystal structure, giving a diffraction pattern which can be imaged in diffraction mode by adjusting the strength of the first projector lens. A selective area diffraction aperture (which is moved out of the beam during imaging), is used to limit formation of the

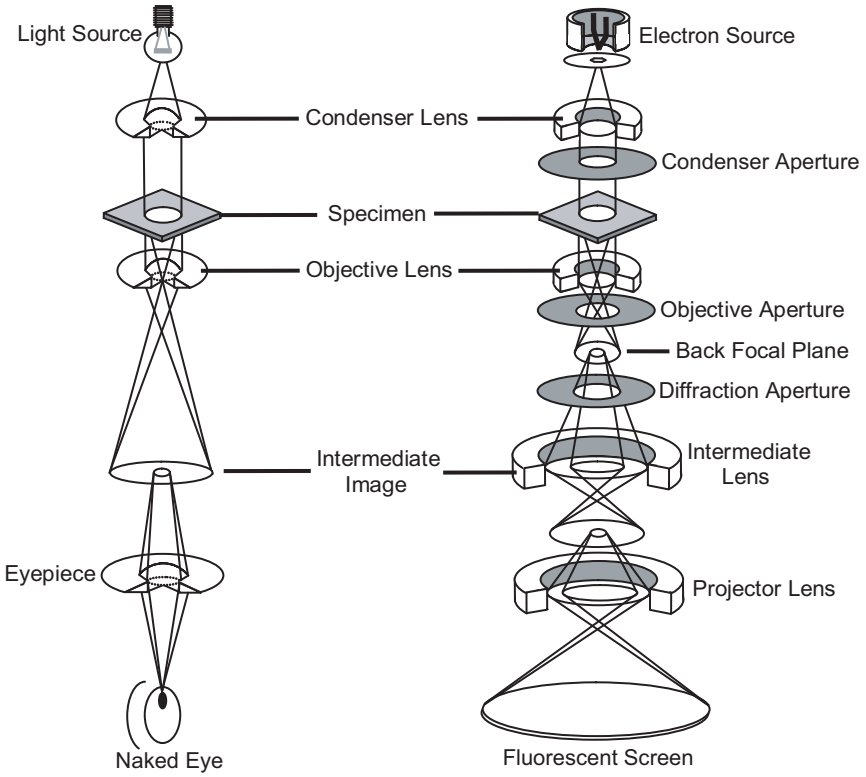

Figure 3.1: Schematic comparison between a conventional transmission optical microscope and a transmission electron microscope, highlighting all the main features of operation.

diffraction pattern to only the electrons passing through a selected area of the sample. By tilting the sample in the beam, it is possible to find an orientation such that electrons either pass straight through the sample or are diffracted by a single set of planes. The resulting *two-beam diffraction condition* has only two spots, the [000] of the straight through path, and another corresponding to the diffracting set of planes.

Contrast is achieved by isolating one of these beams using the objective aperture and allowing it to form the final image. The electrons forming the other spot in the diffraction pattern are discarded, and hence features on planes from which they were

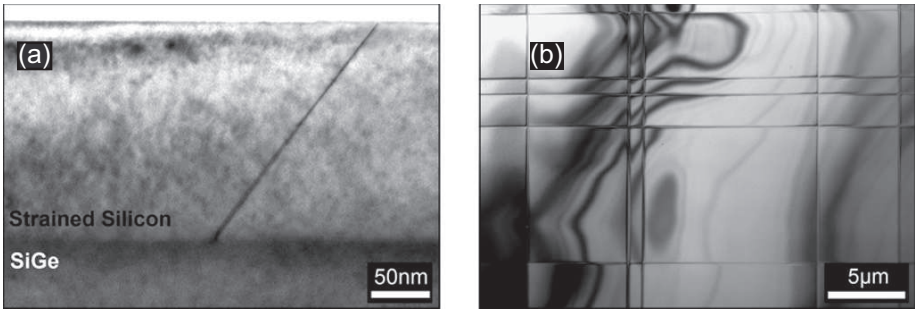

Figure 3.2: TEM images obtained using a [220] diffraction condition from strained silicon layers in (a) cross-section, showing a stacking fault orientated along [111] and (b) plan-view, showing 60° misfit dislocations at the strained interface.

diffracted appear dark. Isolation of the [000] spot forms a bright-field image, which is used for all images presented in this work.

To produce a high level of contrast for dislocations, it is necessary to orientate the sample so that diffraction occurs from a set of planes displaced by the dislocations. This displacement is defined by the general displacement vector, $\mathbf{R}$. Zero contrast will occur if the electron incidence (or diffraction) vector, $\mathbf{g}$, is directed along planes perpendicular to $\mathbf{R}$. This is called the *invisibility criterion*, and is expressed by $\mathbf{g}.\mathbf{R} = 0$. In general for mixed and edge type dislocations, the invisibility criterion will only be satisfied if *both* $\mathbf{g}.\mathbf{b}$ and $\mathbf{g}.(\mathbf{b} \times \mathbf{u})$ are zero. Often both conditions can never be satisfied simultaneously, and in practice a dislocation is considered invisible if $\mathbf{g}.\mathbf{R} < \frac{1}{2}$ [Thomas and Goringe, 1979].

The invisibility criterion also applies to stacking faults. A stacking fault is a displacement of the $\{111\}$ planes of atoms in the crystal along its length, AB, as described in section 2.5.2 and shown in figure 3.3. It will be invisible if $\mathbf{g}$ is perpendicular to $\mathbf{R}$, as shown in figure 3.3 (a), as the diffracting planes are not disrupted by the stacking fault. If $\mathbf{g}$ is not perpendicular to $\mathbf{R}$ as shown in figure 3.3 (b), interference

between electrons passing through the material above and below the stacking fault occurs, producing a characteristic light and dark fringe pattern along AB (figure 3.2 (a)). In general 60° dislocations, 90° partial dislocations and stacking faults display a high level of contrast under {220} diffraction conditions. A more detailed analysis is used to prove the existence of extended stacking faults in strained silicon in section 4.2.1.

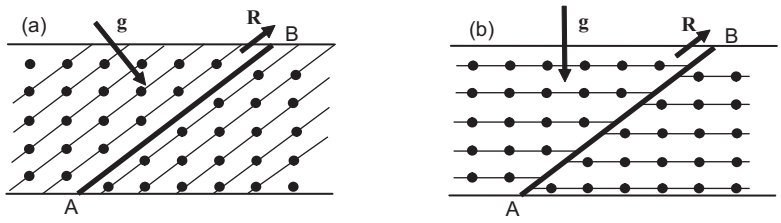

Figure 3.3: Simplified diagram showing a stacking fault, AB, displacing reflecting planes of atoms in a crystal. In (a) $\mathbf{g}.\mathbf{R} = 0$ and no contrast occurs. In (b) $\mathbf{g}.\mathbf{R} \neq 0$ and interference is created between electrons as they pass through the fault. Adapted from Hull and Bacon [2002].

3.2 High Resolution X-Ray Diffractometry

High resolution X-ray diffraction (HRXRD) is used to measure lattice constants in crystalline samples, which are dependent on both strain and composition. In this work, a Philips PW1835 diffractometer was employed to accurately determine the relaxation state of constant composition layers in virtual substrates, their exact germanium composition, and the relaxation of strained silicon layers. A schematic diagram of a typical X-ray diffraction spectrometer is shown in figure 3.4 [Bowen and Tanner, 1990], which consists of an X-ray source and detector which are capable of rotating about a sample stage with a high degree of precision ($\sim$0.0001°).

The sample stage is also capable of very precise movements of rotation (ϕ) and

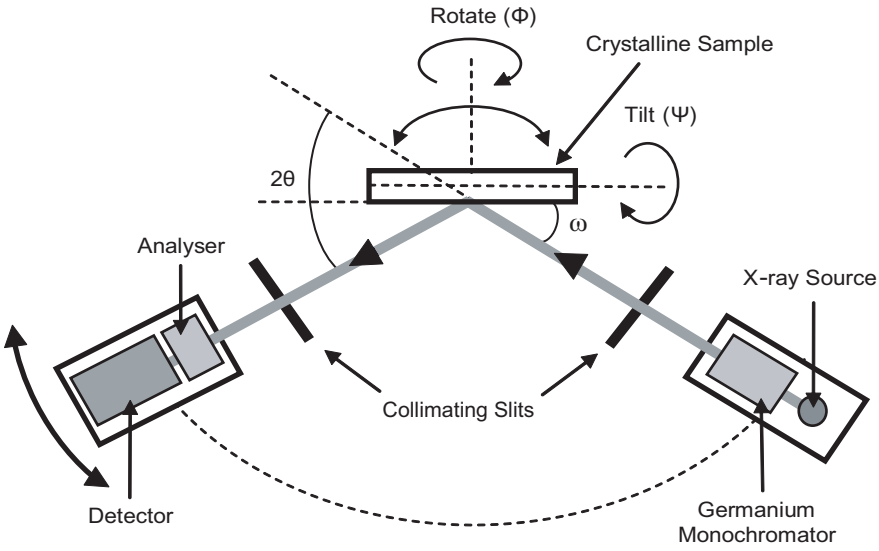

Figure 3.4: Schematic diagram of a high resolution X-ray diffractometer showing all the principal angular movements.

tilt (ψ), to orientate the sample in the X-ray beam. At the source, a hybrid germanium crystal monochromator ensures a high intensity of monochromatic Cu Kα_1 X-rays are emitted, and collimates the divergent beam.

A monochromatic beam of X-rays incident on a crystalline sample will be diffracted by planes of atoms. The diffraction pattern is made up of a series of points forming a *reciprocal space* in which each point represents a set of equivalent diffraction planes, as defined by their surface normal vectors. The spacing of the reciprocal lattice points contains information on the lattice spacings present in the crystal.

Reciprocal space can be "mapped" by varying the angle between the crystal surface and the X-ray source, ω, and between the X-ray source and the detector, 2θ. These two angles traverse two directions in reciprocal space, as shown in figure 3.5. Moving both angles together achieves a third direction, in which the detector is rotated

twice as fast as the sample, $\omega/2\theta$. 2-dimensional reciprocal space maps (RSMs) are formed by scanning $\omega/2\theta$ for a range of ω values around specified reflections. The total range of accessible reflections is limited by the wavelength of the X-ray source (λ) to a region of $\frac{2}{\lambda}$. Additionally, the mappable area of reciprocal space is restricted by the X-ray incidence angle, which must be greater than zero ($\omega > 0$), and less than the total exit angle ($\omega < 2\theta$).

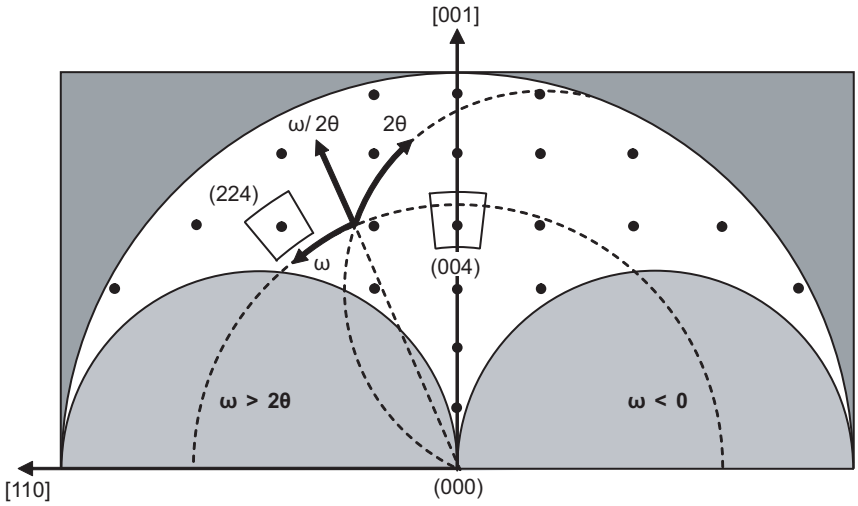

Figure 3.5: Schematic diagram showing scanning directions in reciprocal space and the range of accessible reflections of a (001) orientated crystalline sample. RSMs around reflections [004] and [224] are shown. Taken from Bowen and Tanner [1990].

For (001) orientated virtual substrates, the relaxation of $Si_{1-x}Ge_x$ constant composition layers and their composition are important parameters, as they dictate the degree of strain a silicon overlayer will be subjected to. To calculate these properties, both the in-plane lattice constant, a_x, and the growth direction lattice constant, a_z, must be determined. The symmetric [004] reflection can be used to directly determine a_z, as this is the lattice constant separating the planes of diffraction, as shown in figure 3.6 (a). Information on both a_z and a_x can be obtained from the asymmetric [224] reflection,

the planes of which are separated by a combination of both lattice constants, which is shown in figure 3.6 (b). a_x and a_z can therefore be extracted from scans of both reflections, making it is possible to determine both strain and germanium composition from two RSMs. The use of two different reflections also allows for the compensation of other factors which effect the position of reciprocal space (diffraction) points, such as the tilt or twist of epitaxial layers relative to the substrate [Erdtmann and Langdo, 2006].

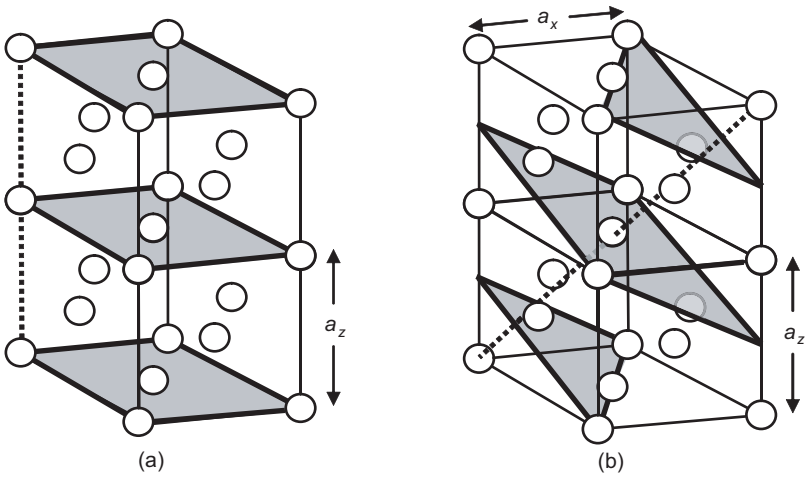

Figure 3.6: Schematic diagram of face-centred cubic crystals, illustrating sets of (a) (004) planes, and (b) (224) planes. The surface normal vectors are shown as dashed lines.

3.2.1 Interpreting Reciprocal Space Maps

The 4.17% difference between the lattice constants of bulk silicon and germanium means that reciprocal space points forming the diffraction patterns of both materials are in close proximity in reciprocal space. Scanning a virtual substrate will produce peaks associated with the silicon substrate, constant composition layers and strained silicon layers. The

relative position of these within the (004) and (224) RSMs allows the determination of germanium composition and strain.

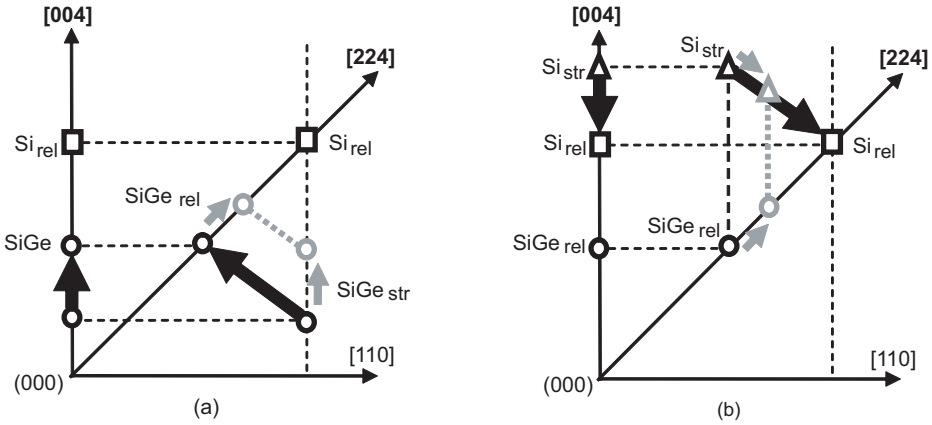

Figure 3.7: Schematic representation showing the main features of (224) and (004) RSMs (along marked directions) with each peak feature marked for (a) a pseudomorphic $Si_{1-x}Ge_x$ layer on a silicon substrate, and (b) a strained silicon on a relaxed virtual substrate. Adapted from Bauer et al. [1995].

Figure 3.7 (a) shows how the X-ray peaks for a compressively strained $Si_{1-x}Ge_x$ layer, $SiGe_{str}$, on a silicon substrate, are affected by relaxation in reciprocal space along the [224] and [004] directions [Bauer et al., 1995]. Partial relaxation shifts the detected peak along a path in reciprocal space (marked by black arrows) between the position of $SiGe_{str}$ (fully strained) and $SiGe_{rel}$ (fully relaxed). This represents the change in lattice constants with relaxation from pseudomorphic to bulk.

In grey are the strained and relaxed peak positions for $Si_{1-x}Ge_x$ of lower Ge content. Peaks of such layers lie closer to Si_{rel}, along the lines indicated by the smaller grey arrows. Again this is a direct consequence of the smaller lattice parameters, as given by equation 2.1. The relative positions of Si_{rel} and $SiGe_{str}$ in reciprocal space can be used to determine germanium content, and the exact degree of strain (or relaxation).

Dedicated X-ray analysis software, Philips X'pert Epitaxy, was used to calculate the strain and germanium content of constant composition layers in virtual substrates, and the degree of relaxation in strained silicon layers from RSMs.

The same principals can be applied to the relaxation of tensile strained silicon. In this case the strained silicon layer, with associated peak Si_{str} in figure 3.7 (b), is commensurate with the underlying $Si_{1-x}Ge_x$ of the virtual substrate. Relaxation is therefore determined by the relative positions of Si_{str} and $SiGe_{rel}$, with the added complication that the $Si_{1-x}Ge_x$ may be residually strained. This is measured (together with germanium composition) from the positions of $SiGe_{rel}$ and Si_{rel}, and therefore the relaxation of the strained silicon layer can only be accurately determined if all three peaks can be resolved accurately.

X-ray diffraction planes become warped by the presence of misfit dislocations, and surface roughness which can broaden peaks in an effect known as *mosaicity* [Erdtmann and Langdo, 2006]. Both the $SiGe_{rel}$ peak from the virtual substrate, and the Si_{str} peak from the strained silicon layer will therefore be affected by mosaicity. By contrast, the peak associated with the silicon substrate (Si_{rel}) displays little peak broadening because of its high crystalline quality. Mosaicity makes peak position determination problematic, especially for thinner layers (such as strained silicon) where the intensity of the peak may be close to the background noise level.

3.3 Atomic Force Microscopy

Atomic force microscopy (AFM) is an atomic scale technique employed in this work to scan topographical features on the surface of strained silicon and virtual substrates. Its primary use is to determine the root-mean-squared (RSM) roughness, which is a measure of the average distance of the surface from a plane, and the total height

range (Z-range) roughness of a surface. Measurements were performed using a Digital Instruments contact mode atomic force microscope. A simplified diagram of an atomic force microscope in operation is shown in figure 3.8.

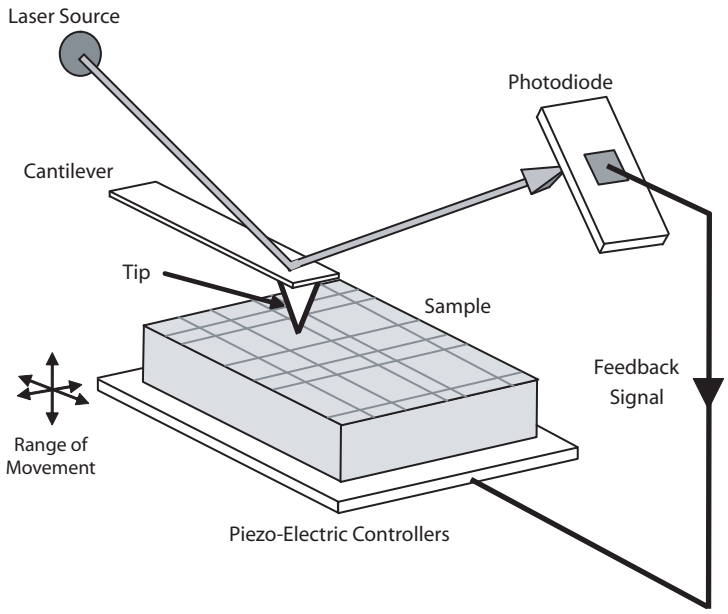

Figure 3.8: Simplified diagram showing the basic operation of AFM in which feedback control is used to keep the deflection of the cantilever constant. Adapted from [Amelinckx et al., 1997].

In contact mode the silicon-nitride tip attached to the cantilever (which has a radius of only a few nanometres), is brought into "soft contact" with the surface of the sample. This occurs when the tip is close enough to the sample surface to feel a repulsive force from interatomic forces, but does not make mechanical contact with it. The force is large enough to bend the cantilever so it follows the shape of the surface under the tip as the sample is rastered beneath it, which is controlled by piezo-electric ceramics, which allow sub-Angström resolution (subject to tip dimension) in the x, y and z-directions.

A laser directed onto the cantilever is deflected onto a photodiode detector as the cantilever bends. In constant force mode, the deflection of the cantilever is kept at a constant pre-set value by varying the height of the sample beneath the tip. This is done by sending a feedback signal from the photodiode to the piezo-electric controlling the z-direction (height) of the sample, so that any variation in the deflection of the cantilever is immediately followed by a correctional movement of the sample in the z-direction. A topographical map of the surface can then be built up from the signal relayed to the z-direction piezo-electric controller as the sample rasters in the x and y-directions. Raw cantilever deflection data can also be used to construct more detailed, but non-quantitative map of the surface. Figure 3.9 shows example height and deflection topographs taken from a strained silicon surface.

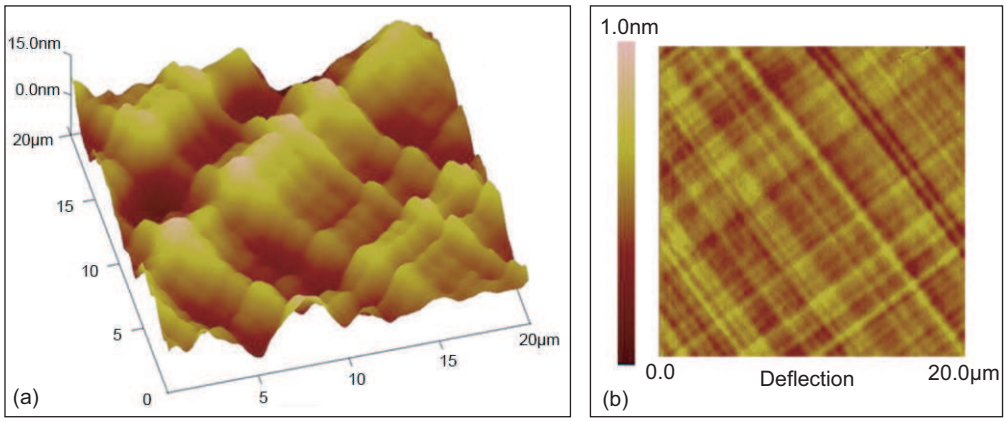

Figure 3.9: AFM 20μm^2 scans obtained from a strained silicon surface showing (a) height map and (b) deflection data of the same area.

The rastering rate limits the resolution of the data obtained, as does the sharpness of the AFM tip. In this work, the frequency of the motion of the tip relative to the surface was fixed at 1Hz. Any dirt in the scan area will be displayed as a sharp peaked feature on the topography map, making measurements of RMS and Z-range roughness

inaccurate, so it is essential that a clean area is selected for scanning. Both quantities were determined from each topography map using Digital Instruments NanoScope software.

3.4 Defect Etching

The threading and misfit dislocations content of strained silicon layers are important properties when considering such layers for use in the fabrication of electronic devices. Defect etching is widely used to reveal the presence of threading dislocations and other defects. Etchants designed to have a higher etch rate in their vicinity compared with the rest of the material are known as selective etchants. In chapter 4, the ability of defect etching to reveal dislocations in strained silicon is considered in detail.

A number of selective chemical etchants have been developed for $Si_{1-x}Ge_x$ alloys, which rely on the same basic chemical reactions. Each consists of an oxidising agent, hydrofluoric acid and a solvent (normally H_2O). In this study a dilute Schimmel etchant solution was used which comprises of CrO_3 (0.75M) : HF (50%) : H_2O, mixed in the ratio 2 : 4 : 3 [Archer, 1982].

The oxidising agent (CrO_3) continuously oxidises the sample surface, which the HF disolves [Kulkarni, 2003]. Each sample is exposed to the etchant for a dictated amount of time, after which the sample is immersed in de-ionised water. During the etchant exposure, the sample is continuously agitated to prevent bubbles forming and shielding areas on the surface from being etched.

3.5 Differential Interference Contrast Microscopy

The differential interference contrast microscope (DIC, or Nomarski microscope) is used to enhance the contrast of step features on the surface of defect etched samples. It provides a non-quantitative view of height features and roughness, which are normally invisible with conventional microscopy [Loveland, 1970]. A typical DIC microscope is shown schematically in figure 3.10.

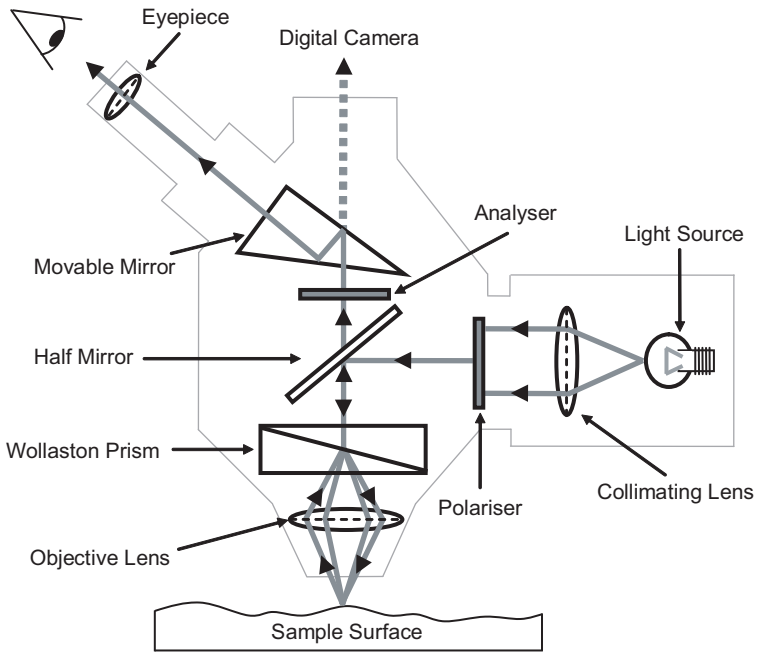

Figure 3.10: Schematic representation of a typical DIC microscope. Adapted from Capewell [2002].

Collimated light entering the microscope from the light source is first plane polarised, and then reflected into a Wollaston prism, where the light is split into two perpendicularly polarised beams. Both beams are focused onto the surface of an etched sample by the objective lens. Upon reflection from the surface, the objective lens focuses

the beams back into the Wollaston prism, where they are re-combined. Interference cannot occur between the beams due to their differing polarisation states; this only occurs once the light has passed through the analysing polariser which is crossed relative to the first polariser.

Light from the two beams illuminating a step feature on the surface of the sample (i.e. a dislocation etch pit) will become phase shifted relative to each other on reflection. Re-combination of the two beams will produce interference due to the phase shift. This causes a darkening or lightening in the final image around the area of the step feature, giving that area an enhanced contrast. Images of the surface can be recorded with a digital camera, or a mirror can be placed in the path of the beam to reflect the light into the microscope eyepiece.

3.6 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) is used to determine material composition as a function of depth. An Atomika 4500 SIMS profilometer was employed in this work to measure the diffusion of germanium from virtual substrates into strained silicon layers after annealing.

SIMS concerns the detection of ions ejected from the surface of the sample under study using a high intensity primary beam of ions. O_2^+ ions were used in this work at an energy of 500eV, directed at normal incidence onto a 250μm^2 area. The secondary ions sputtered from the surface are then detected by a quadruple mass spectrometer, the relative quantities of which provides information on the different elemental species and their concentrations in the material. By measuring the depth of the crater formed on the surface, the erosion rate of the ion beam into the sample can be determined and composition calculated as a function of depth [Benninghoven et al., 1987].

The depth resolution of SIMS when applied to strained silicon layers on virtual substrates is limited by several factors. Undulations on the surface due to crosshatching being the greatest limitation. Dislocations at the misfit interface can cause preferential erosion which leads to erroneous results, as the erosion rate of the material is usually assumed to be constant. Incident ions intermixing the surface atoms within the penetration depth of the primary ion beam can also cause a broadening of the SIMS depth profile [Dowsett, 2003]. These effects can be minimised by selection of samples with a smoother surface and lower dislocation content, and by keeping the energy of the primary ions low ($<$1keV).

Chapter 4

Defect Etching

Defect etching is used extensively used to reveal the presence of defects and dislocations in silicon and germanium. It is widely used to determine threading dislocation densities, which are frequently quoted without additional corroboration. This chapter aims to explore the etching process and provide a better understanding of the technique used throughout the rest of this work.

4.1 Etch Rate of Dilute Schimmel Etchant

4.1.1 Etch Rate of $Si_{1-x}Ge_x$

The etch rate of Schimmel etchant is known to vary widely with germanium composition in $Si_{1-x}Ge_x$ alloys. It is also known to vary with strain, temperature, and the amount of H_2O in solution [Werner et al., 2004]. The mechanism behind etchant selectivity to dislocations still remains poorly understood. One theory suggests the local strain fields around dislocations increase the local etch rate above that of the surrounding material [Kulkarni, 2003].

To determine the etch rate of $Si_{1-x}Ge_x$ by the dilute Schimmel etchant variant chosen for this study, LPCVD grown virtual substrates were used covering a wide range of x values. Each virtual substrate was grown with a constant composition layer at least 1μm thick, from which the etch rate was determined (the full structure of the virtual substrates will therefore not be described). The etch rate of silicon was determined from a thick epitaxial layer of bulk silicon ($>$1μm) grown on a silicon substrate. Relaxation and germanium composition for each virtual substrate was determined from RSMs obtained using HRXRD. All samples were found to be $>$98% relaxed.

The calculation of an etch rate requires the amount of material removed by the etchant to be accurately measured. To do this, an area on the surface of each sample was protected from the Schimmel etchant with Apiezon W black wax. After etching, the wax was dissolved in toluene, to leave a step between the etched and protected areas. Step heights were measured with a Talystep profiler, which is normally capable of resolving features of around 2nm on smooth surfaces in a stable environment. In this study the roughness of the crosshatched surfaces after etching limits accuracy to $\sim$10nm. Virtual substrates generally have a smoother surface than direct growth of $Si_{1-x}Ge_x$ layers on silicon substrates, making them more suitable for such measurements.

Etching was conducted in a standard fume cupboard with a continual airflow which maintained the ambient temperature at 19$\pm$1°C. Samples taken from each virtual substrate were exposed to the etchant for varying lengths of time. After etching the removal of black wax with toluene was confirmed to leave a residue free surface with the DIC microscope. Step heights were measured at three places along their length, from which the mean etch depth was calculated. Etch rates were then determined from mean etch depth versus exposure time plots, an example of which is shown in figure 4.1.

Figure 4.2 shows the etch rate of dilute Schimmel etchant across the whole range

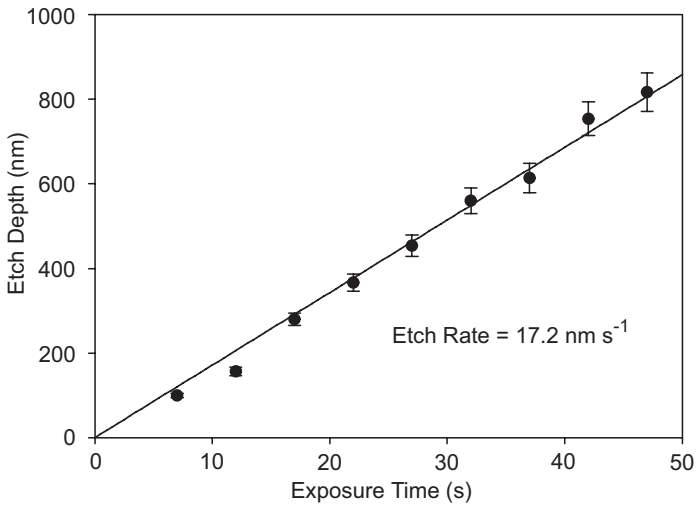

Figure 4.1: Example graph showing mean etch depth as a function of exposure time to dilute Schimmel etchant for a range of samples taken from a 31% virtual substrate.

of germanium compositions. A clear increase in the etch rate is observed, reaching a maximum of 23nm s^{-1} at 18%, which steadily decreases with increasing composition. Similar behaviour was previously observed when cooling the dilute Schimmel etchant to 2°C [Werner et al., 2004], and also with a dilute Secco etchant [Bray et al., 2005]. For pure germanium, there was no detectable surface step after exposure to the etchant for 10min, indicating an etch rate of approximately $<$0.02nm s^{-1}

Schimmel and Secco based etchants work by a two stage processes; oxidation of the surface, followed by its removal by acid etching [Kulkarni, 2003]. Germanium oxides are readily soluble in water [Liu, 2002], therefore the observation of an etch rate close to zero for pure germanium is likely to be due to the inability of CrO_3 to oxidise germanium. It can therefore be assumed that only silicon will undergo oxidation in the etch process.

If the oxide removal rate is constant once it has formed (provided the concentra-

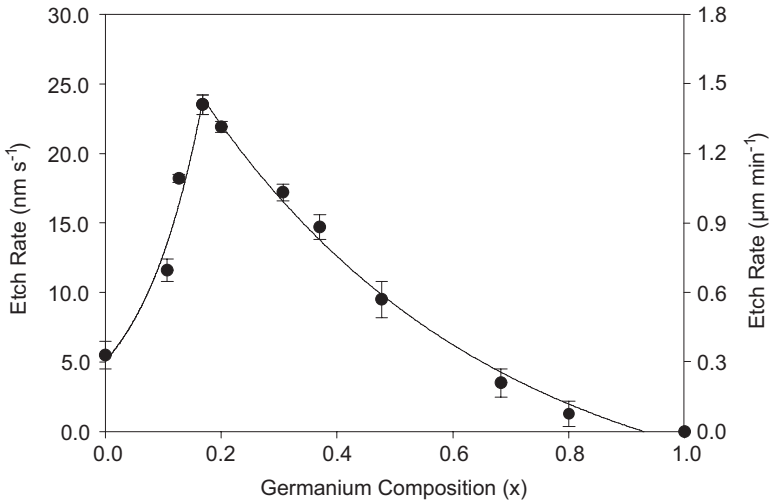

Figure 4.2: Graph to show the etch rate of $Si_{1-x}Ge_x$ in dilute Schimmel etchant.

tion of H^+ ions in solution remains constant), the oxidation of the surface becomes the rate limiting step. The decrease in etch rate with increasing germanium composition is consistent with this view, as the surface contains less silicon to be oxidised. Germanium is presumed to be removed as the silicon oxides dissolve.

At lower compositions, the increase in etch rate with composition indicates an enhancement to the oxidation of silicon due to the presence of small amounts of germanium, a type of behaviour normally associated with other oxidation methods [Hellberg et al., 1997]. However, these processes are performed with dry oxygen at temperatures in excess of 800°C, where the formation of germanium oxides are believed to reduce back into germanium by oxidising local silicon atoms. A similar process may explain the observed shape of the curve in figure 4.2 during oxidation with CrO_3, but such experiments are beyond the scope of this work.

4.1.2 Etch Rates of Bulk and Strained Silicon

To determine how strain affects the etch rate of silicon, a comparison was made between the etch rate of bulk silicon and an 84.7nm layer of strained silicon on a 20% virtual substrate (sample LG20-12 from section 5.1.1). HRXRD measurements show this layer to be only 1.8% relaxed (0% relaxation refers to a strain of $\epsilon = 0.0084$, as given by equation 2.3, and 100% relaxation denotes the silicon layer has relaxed to the bulk state).

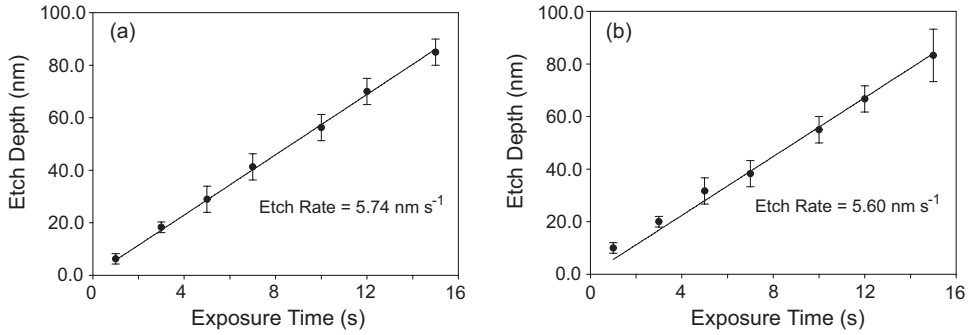

Figure 4.3: Graphs showing mean etch depth with exposure to the dilute Schimmel etchant for (a) bulk silicon and (b) strained silicon on a 20% virtual substrate.

The measured etch rate of bulk and strained silicon presented in figure 4.3 are 5.7$\pm$0.1nm s^{-1} and 5.6$\pm$0.3nm s^{-1} respectively. The application of strain from a 20% virtual substrate therefore has no appreciable effect on the etch rate of silicon. Higher degrees of strain could not be satisfactorily tested due to the difficulty in producing thick enough layers with a low enough density of dislocations for accurate step height measurement (see section 6.5).

4.2 Defect Etching of Strained Silicon

Defect etching is a useful technique for revealing misfit dislocations and stacking faults in strained silicon. The technique is rarely used in this capacity, so it is important to determine the extent of its applicability, particularly for silicon layers on 20% and 50% virtual substrates, which are the basis of this work.

4.2.1 Misfit Dislocations and Stacking Faults

Revealing misfit dislocations at the strained silicon interface requires the silicon to be etched away entirely. An appropriate exposure to the etchant based on the etch rates of silicon and the underlying material can be estimated from figure 4.2, for any known thickness of strained silicon. Figure 4.4 shows an image obtained with the DIC microscope from a 22.0nm strained silicon layer on a 20% virtual substrate which has a 2μm thick constant composition layer (sample TG20-5 in section 5.1.2) after a 10s exposure. Such an exposure is estimated to remove around 150nm of material from the structure, so revealed linear features are located at the strained silicon misfit interface, and not from deeper in the virtual substrate.

Fine lines are clearly seen on the surface which are attributed to 60° misfit dislocations. Each misfit dislocation terminates at one end with a threading dislocation etch pit, which is identified as the gliding threading component in the strained silicon layer. No pits are formed at the threading dislocation component from the virtual substrate (this property becomes particularly important in section 5.6, when studying the interaction of dislocations).

Broader etch trenches are also evident in figure 4.4, which are attributed to extended stacking faults in the strained silicon layer. Stacking faults can be located with PVTEM by using two orthogonal {220} diffraction conditions. Table 4.1 considers

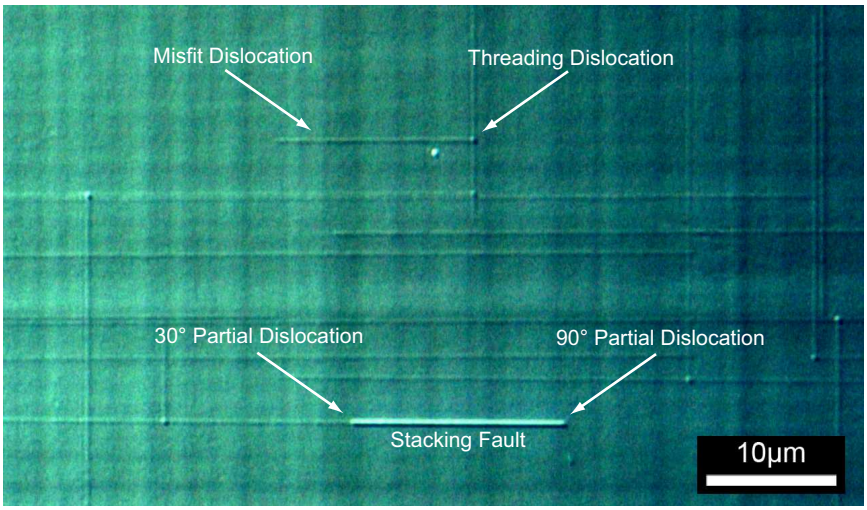

Figure 4.4: Image of a 22.0nm strained silicon layer on a 20% virtual substrate obtained with the DIC microscope after a 10s exposure to the dilute Schimmel etchant.

the invisibility criteria for two orthogonal 90° partial dislocations (which bound an extended stacking fault, see section 2.5.2) and 60° perfect dislocations, under diffraction conditions of $\mathbf{g} = (220)$ and $(2\bar{2}0)$.

		$\mathbf{b} = \frac{1}{2}[\bar{1}01]$		$\mathbf{b} = \frac{1}{6}[\bar{1}12]$	
$\mathbf{g}$	Criterion	$\mathbf{u} = [110]$	$\mathbf{u} = [\bar{1}10]$	$\mathbf{u} = [110]$	$\mathbf{u} = [\bar{1}10]$
(220)	$\mathbf{g}.\mathbf{b}$	-1	-1	0	0
	$\mathbf{g}.(\mathbf{b} \times \mathbf{u})$	0	-2	0	$-\frac{4}{3}$
$(2\bar{2}0)$	$\mathbf{g}.\mathbf{b}$	-1	-1	0	0
	$\mathbf{g}.(\mathbf{b} \times \mathbf{u})$	-2	0	$\frac{4}{3}$	0

Table 4.1: Table of invisibility criteria for two orthogonal 60° perfect ($\mathbf{b} = \frac{1}{2}[\bar{1}01]$) and 90° partial ($\mathbf{b} = \frac{1}{6}[\bar{1}12]$) dislocations along the [110] and $[\bar{1}10]$ directions, under orthogonal diffraction conditions $\mathbf{g} = (220)$ and $(2\bar{2}0)$.

The invisibility criterion for 60° and 90° dislocations requires that both $\mathbf{g}.\mathbf{b}$ and $\mathbf{g}.(\mathbf{b} \times \mathbf{u})$ are zero (see section 3.1.1). For the two orthogonal 60° dislocations

this will not occur with either of the two diffraction conditions considered in table 4.1. 60° dislocations will therefore always be visible for any {220} diffraction condition. Orthogonal 90° partial dislocations, however, each become invisible under orthogonal diffraction conditions. This is illustrated in figure 4.5, confirming the features shown are 90° dislocations. The fringing pattern also shows they are stacking faults (see section 3.1.1) and therefore the bounding 90° dislocations are partial.

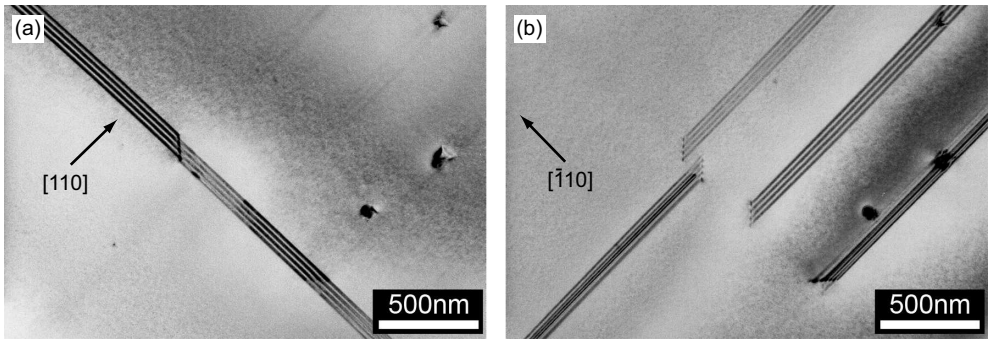

Figure 4.5: PVTEM images obtained from a 184.5nm strained silicon layer grown on a 20% linear graded virtual substrate (sample LG20-12 from section 5.1.1) of the same area using two orthogonal {220} diffraction conditions.

Defect etching reveals stacking faults as broader features because they are 2-dimensional dislocations on {111} planes, and so present an approximate width of $h\cos(45°)$ in plan-view, as noted in previous works [Bedell et al., 2004a]. In figure 4.4 the fine line of the 60° dislocation which underwent the dissociation reaction to form the extended stacking fault can clearly be seen, and no etch pits are observed at the bounding partial threading dislocations. Stacking faults and microtwins in strained silicon are discussed further in sections 5.3.2 and 5.4.

4.2.2 Threading Dislocations

20% Virtual Substrates

Figure 4.6 shows a series of images taken from a 20% linearly graded virtual substrate with a 2μm constant composition cap. Each image is of the same area with increasing exposure to the Schimmel etchant (sample LG20-0 from section 5.1.1). From figure 4.2 the etch rate of $Si_{0.8}Ge_{0.2}$ is estimated to be around 22nm s^{-1}, which gives an exposure time of about 90s before the constant composition capping layer is removed.

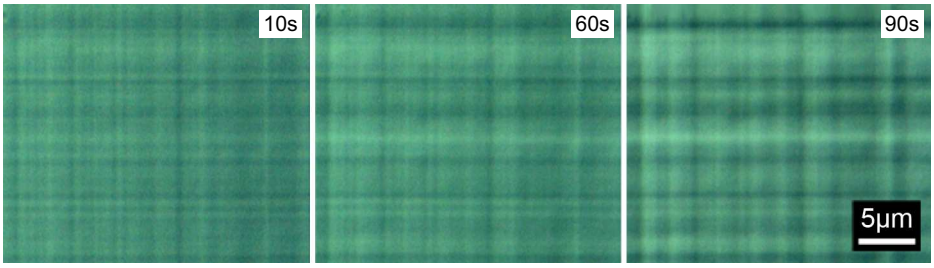

Figure 4.6: Series of images obtained using the DIC microscope for an uncapped linearly graded 20% virtual substrate (LG20-0) etched for increasing lengths of time.

No threading dislocations are revealed in these images even after 90s, and their density across the etched sample was estimated to be $8\pm1\times10^3 cm^{-2}$. This is lower than expected [Dutarte et al., 1994], and is indicative of a very poor selectivity to dislocations in 20% material.

50% Virtual Substrates

Figure 4.7 shows a similar sequence of images from a 50% virtual substrate with a 1μm constant cap (sample TG50-A, as described in section 6.1.2) after increasing exposure to the dilute Schimmel etchant.

An exposure of 120s reaches a depth of around 1100nm, which is inside the

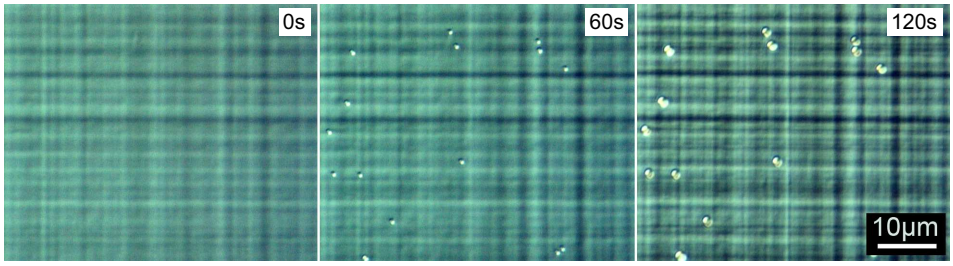

Figure 4.7: Series of images obtained using the DIC microscope for a terrace graded 50% virtual substrate (sample TG50-A) etched for increasing lengths of time.

final compositional grading region of the structure. The threading dislocation density is measured to be $2.0\pm0.6\times10^5\text{cm}^{-2}$, with no additional features evident from the graded region. Etch pits are observed to increase in size with exposure time for 50% material, indicating a higher selectivity than for 20% material.

Cooling the dilute Schimmel etchant to 2°C (thereby reducing the etch rate), has been shown to maintain high selectivity over a large range of germanium compositions [Marchionna et al., 2006]. However, selectivity for 20% virtual substrates can be increased with the addition of a strained silicon layer.

Adding Strained Silicon Layers

Another sequence of images taken for the same 20% virtual substrate structure as shown in figure 4.6, with the addition of a 10.2nm strained silicon layer (sample LG20-1 from section 5.1.1) is presented in figure 4.8. After etching for 10s (reaching a depth of around 190nm), misfit and threading dislocations are clearly revealed, and the threading dislocation density is measured to be $2\pm1\times10^5\text{cm}^{-2}$. An additional 20s exposure (to reach a depth of around 600nm) removes the misfit dislocation features, and etching for another 30s (to a depth of around 1.2μm) begins to eradicate all etch pit features. The

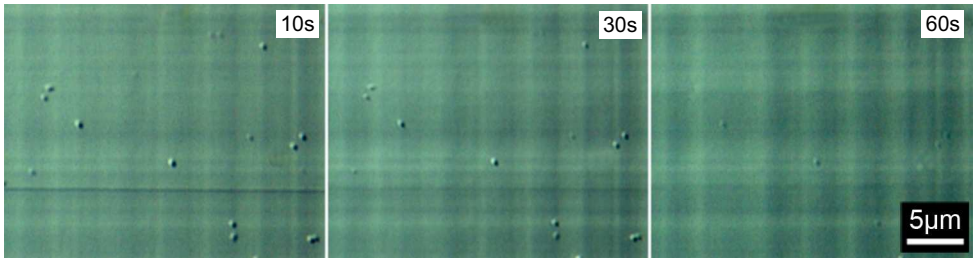

Figure 4.8: Series of images obtained using the DIC microscope for a linearly graded 20% virtual substrate capped with 10.2nm of strained silicon (LG20-1) etched for increasing lengths of time.

increase in threading dislocation density in the strained silicon capped sample clearly demonstrates that strained silicon has a profound effect on the selectivity to threading dislocations in 20% material. The addition of a 10nm strained silicon cap to the 50% virtual substrate on the other hand, yields a measured density of $2.6\pm0.5\times10^5\text{cm}^{-2}$, which agrees to within error with the uncapped result.

4.2.3 Strained Silicon Reveal Enhancement

Selectivity of a dilute Secco etchant has been shown to be enhanced by the addition of a strained silicon layer to thin $Si_{0.75}Ge_{0.25}/SiO_2$ structures [Bedell et al., 2004b]. Large etch pits were observed in the $Si_{0.75}Ge_{0.25}$ and SiO_2 layers, under where a stacking fault was believed to have been present in the (etched away) strained silicon layer. Further investigation is needed to determine why an enhancement occurs for strained silicon capped 20%, but not 50%, virtual substrates.

Samples from a 20% virtual substrate capped with 183.6nm of strained silicon (sample LG20-12 in section 5.1.1) were etched for varying lengths of time and prepared for XTEM observation, the results of which are presented in figure 4.9. An estimated exposure time of 35s is required for full removal of the silicon from figure 4.2. Obser-

vation of threading dislocations using XTEM is very unlikely for densities less than 10^7 (such a density would be considered very high for a 20% linearly graded virtual substrate [Dutarte et al., 1994]). However, stacking faults in the strained silicon layer are linear features and are more likely to cross the viewable area in XTEM (and are also abundant in thicker layers, as observed in section 5.3.2). Like threading dislocations they extend throughout the thickness of the silicon, and so are expected to behave in much the same manner as threading dislocations during etching.

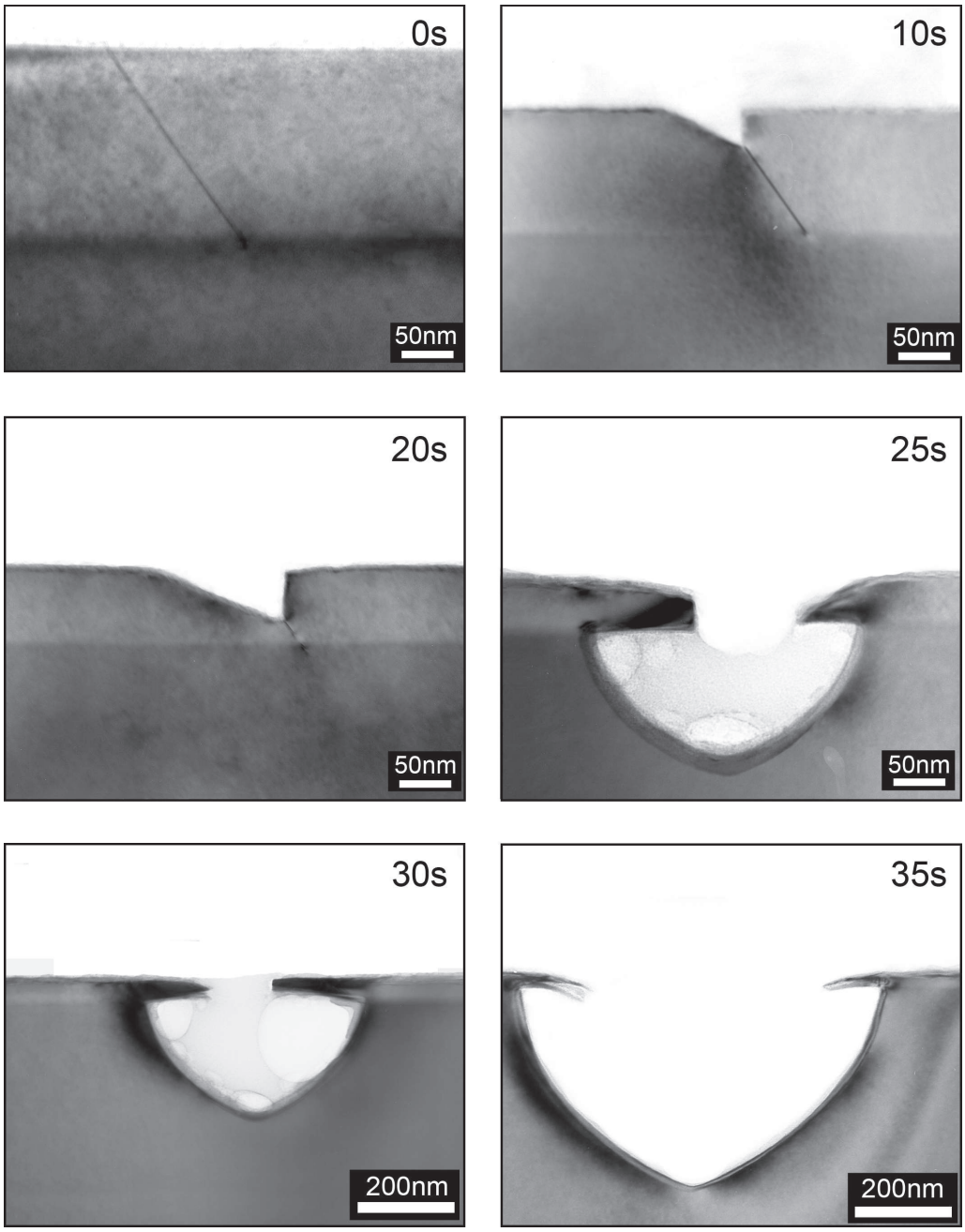

Figure 4.9: Series of XTEM images of etch pits formed around stacking faults obtained in a (220) diffraction condition from a 183.6nm thick strained silicon layer on a 20% linearly graded virtual substrate, after etching for given lengths of time.

During the first 20s of exposure to the etchant, an etch pit forms along the line of the stacking fault in the strained silicon layer, as shown in figures 4.9 (a)-(c). Figure 4.9 (d) shows that once the base of the pit reaches the $Si_{0.8}Ge_{0.2}$ surface, a larger pit begins to undercut the silicon layer, due to the larger etch rate of the $Si_{0.8}Ge_{0.2}$. Increasing exposure widens this pit as the rest of the strained silicon layer is still being removed. Once the strained silicon layer has been completely removed, the etch pit formed in the $Si_{0.8}Ge_{0.2}$ cannot become any larger as undercutting ceases, and additional exposure will eventually remove it (as observed in figure 4.8).

The depth of the etch pit from the misfit interface into the $Si_{0.8}Ge_{0.2}$, d, depends on the length of time during the total exposure, t, that the etchant was in contact with the $Si_{1-x}Ge_x$. This is dictated by the etching rate of the stacking fault, E_{SF}, and the layer thickness, h:

$$d = E_{SiGe}\left(t - \frac{h}{E_{SF}}\right) \tag{4.1}$$

Where E_{SiGe} is the etch rate of $Si_{0.8}Ge_{0.2}$. E_{SF} can be estimated by measuring the depth of the etch pit formed in silicon in figures 4.9 (b) and (c), and by the depth of the etch pit formed in $Si_{0.8}Ge_{0.2}$ in figures 4.9 (d) and (e), using equation 4.1. This is sumarised in table 4.2, together with estimates for the etch rate of strained silicon (E_{S-Si}), based on direct measurement of its remaining thickness.

The mean etch rate of strained silicon is estimated to be 5$\pm$1nm s^{-1}, which rises in the vicinity of a stacking fault (or threading dislocation) to 10$\pm$1nm s^{-1}. These are estimates only, as they based on results obtained from only a few images. Further inaccuracies in thickness measurement arise due to the layer tilting required to achieve the desired diffraction condition.

Dislocations are more clearly revealed in 20% virtual substrates capped with

Exposure (s)	E_{SF} (nm s^{-1})	E_{S-Si} (nm s^{-1})
10	6.8	10.2
20	5.4	8.1
25	5.4	9.3
30	4.2	10.8
35	4.4	11.4

Table 4.2: Calculated etch rates of stacking faults (E_{SF}) and strained silicon (E_{S-Si}) calculated from figure 4.9.

strained silicon due to undercutting arising from the $\sim$15nm s^{-1} etch rate difference between $Si_{0.8}Ge_{0.2}$ and silicon. For 50% virtual substrates the difference is only $\sim$5nm s^{-1}, and so thicker silicon layers are required to create sufficient undercutting to create etch pits which are distinguishable from surface roughness with the DIC microscope (see section 6.5). With the identification of undercutting, the poor selectivity of 20% virtual substrates can be circumvented without the need for cooling when measuring threading dislocation densities with the addition of a strained silicon cap.

Without additional analysis techniques, it is unknown whether a one-to-one correspondence exists between the number of etch pits and the number of threading dislocations at the surface for 50% virtual substrates. One such technique is PVTEM, but it is limited to higher densities of threading dislocations ($>10^7$) due to the smaller viewable area of samples. PVTEM is used in section 6.5 to explore this possibility.

Undercutting also explains why an etch pit is formed around the leading threading dislocation of a misfit dislocation and not the trailing threading dislocation in the virtual substrate. It may also be responsible for the effectiveness of revealing misfit dislocations, assuming the etch rate is increased in their vicinity in a similar fashion to a stacking fault.

4.3 Summary

The etching of $Si_{1-x}Ge_x$ has been shown to have a poor selectivity for $x = 0.2$, where the etch rate is at its highest. The inclusion of a strained silicon cap can lead to undercutting at threading dislocations and stacking faults, which greatly increases selectivity and dislocation reveal. The extent to which this occurs over the germanium composition range cannot be inferred from the present study, but has been shown to be beneficial for 20%, but not for 50% virtual substrates. The etching rate of silicon has been shown to be insensitive to the global strain applied by a virtual substrate, and yields an etch rate similar to that of bulk silicon (5.7 ± 0.1nm s^{-1}).

Other etching chemistries based on Schimmel and Secco etchants exist which give selectivity to dislocations in $Si_{1-x}Ge_x$ over a wider range of germanium compositions [Marchionna et al., 2006]. This study is limited to a dilute Schimmel etchant only, and has been shown to be effective for differentiating misfit dislocations and stacking faults in strained silicon. In the following chapter this will be prove to be especially useful when calculating relaxation (section 5.3), and investigating dislocation interactions (section 5.6) over larger areas than other dislocation imaging techniques such as PVTEM. It is not necessary for the removal of material to be controllable to perform these functions, and so other etch chemistries (which may provide greater selectivity over a wider range of germanium compositions) need not be considered.

Chapter 5

Strained Silicon on 20% Virtual Substrates

The relaxation of strained silicon on 20% virtual substrates is investigated in this chapter using defect etching and HRXRD techniques. Dislocation interactions are also analysed with defect etching, and used to interpret these results.

5.1 Virtual Substrate Designs

Strained silicon layers grown on a basic linear graded and terrace graded virtual substrate design were compared to determine the effect that a lower density of threading dislocations and a smoother misfit interface has on relaxation. The main focus of this chapter is on the strained silicon layers and not the virtual substrates, so no data regarding the optimisation of growth parameters is presented.

5.1.1 Linear Grading

Growth was performed using LPCVD with germane and dichlorosilane as precursor gases to ensure a clean deposition. Hydrogen was used as the carrier gas at a total pressure of 80Torr. The compositional grading was fixed at 10% μm^{-1} which is comparable with other basic linearly graded virtual substrate designs [Dutarte et al., 1994]. A 2μm constant composition layer was added to ensure a high level of relaxation. Details of the structure are shown in figure 5.1.

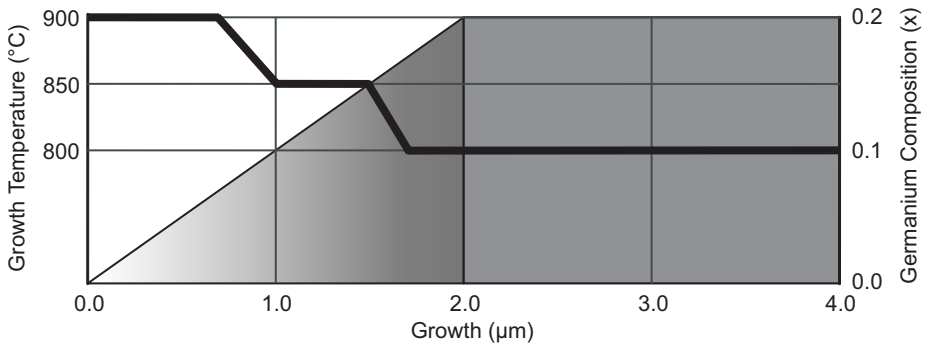

Figure 5.1: Graphical representation of the germanium composition and growth temperature (shown as a black line) of the 20% linearly graded virtual substrate design.

The growth temperature was reduced throughout the deposition process from an initial temperature of 900°C. This maintains a high temperature which promotes relaxation and lower threading dislocation densities [Leitz et al., 2001], whilst not exceeding the melting temperature of the $Si_{1-x}Ge_x$ alloy as the composition increases [Xie et al., 1992]. The melting temperature of $Si_{1-x}Ge_x$ lowers with increasing germanium composition as it varies between the melting temperatures of bulk silicon and germanium, which are 1412°C and 940°C, respectively [Herzog, 1995].

5.1.2 Terrace Grading

A simple 4-tier terrace graded virtual substrate design was selected for this study. Germane and dichlorosilane were again used as precursor gases, at a total pressure of 80Torr. The compositional grading rate of the graded regions was fixed at 10% μm^{-1}, with 500nm constant composition layers grown every 5% germanium composition increase. A final constant composition layer of 2μm was again added. Figure 5.2 shows a graphical representation of this structure.

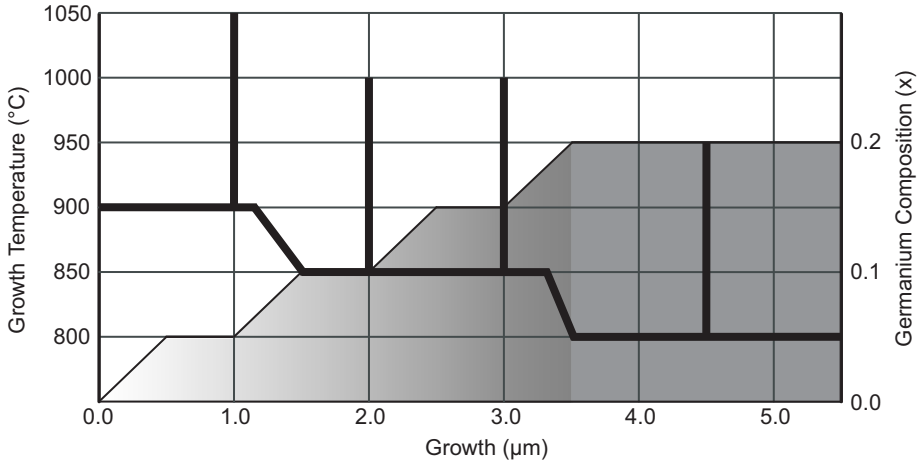

Figure 5.2: Graphical representation of the germanium composition variation and growth temperature (shown as a black line) of the 20% terrace graded virtual substrate design.

Growth temperature was reduced with increasing germanium composition as before, with additional *in situ* annealing stages of 2min duration after the growth of each terrace. This has been shown to enhance the relaxation of the terraces, and promote smoother interfaces [Capewell, 2002].

XTEM images of the final virtual substrate structures are presented in figure 5.3. The confinement of misfit dislocations to the graded regions can clearly be seen, with far fewer observable in the terrace graded design due to the lower misfit between

subsequent terraces. Dislocations injected into the silicon substrate indicate relaxation of the lower compositional layers by the MFR mechanism (see section 2.3.4).

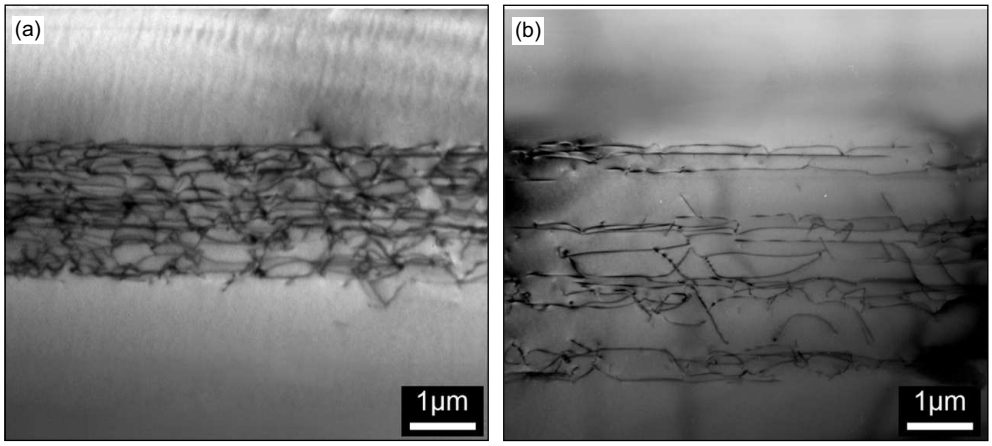

Figure 5.3: XTEM images obtained for 20% virtual substrate of (a) linear graded and (b) terrace graded design, in the (220) diffraction condition.

5.1.3 Strained Silicon

Two sample sets with a variation in the strained silicon cap thickness were constructed using each virtual substrate design. For the growth of each silicon layer, the temperature was lowered to 700°C upon completion of the virtual substrate growth, and the remainder of the precursor gases purged from the growth chamber by the constant flow of hydrogen. Growth was performed at this temperature with a lower total reactor pressure of 20Torr using silane with a deposition rate of 4.50nm min^{-1}.

Strained silicon on 20% germanium content virtual substrates has an approximate critical thickness of 13nm for dislocation glide, and a critical thickness for half-loop nucleation of 130nm (see figure 2.15). Based on these estimates, the thickness range of strained silicon to be investigated was chosen to be between 10nm and 200nm.

Sample	h_{S-Si} ($\pm$0.5nm)	x ($\pm$0.005)	R ($\pm$0.5%)
LG20-0	0.0	0.205	98.5
LG20-1	10.2	0.206	100.3
LG20-2	15.1	0.205	98.7
LG20-3	15.4	0.206	98.9
LG20-4	17.4	0.204	98.5
LG20-5	19.0	0.206	97.7
LG20-6	19.2	0.201	97.3
LG20-7	20.0	0.195	97.1
LG20-8	24.5	0.201	98.3
LG20-9	30.4	0.199	96.7
LG20-10	42.7	0.194	99.7
LG20-11	84.7	0.199	98.8
LG20-12	184.5	0.192	95.7

Table 5.1: Tabulated properties for the 20% linear graded samples of variable strained silicon thickness (h_{S-Si}) as measured by XTEM. Germanium composition (x) and relaxation (R) of the final constant capping layer were measured by HRXRD.

Sample	h_{S-Si} ($\pm$0.5nm)	x ($\pm$0.005)	R ($\pm$0.5%)
TG20-0	0.0	0.192	99.2
TG20-1	11.0	0.187	98.8
TG20-2	13.7	0.188	97.0
TG20-3	17.2	0.186	96.5
TG20-4	19.2	0.193	99.2
TG20-5	22.0	0.189	98.8
TG20-6	26.2	0.190	98.2
TG20-7	44.5	0.190	97.3
TG20-8	95.6	0.190	97.8
TG20-9	183.6	0.189	96.7

Table 5.2: Tabulated properties for the 20% terrace graded samples of variable strained silicon thickness (h_{S-Si}) as measured by XTEM. Germanium composition (x) and relaxation (R) of the final constant capping layer were measured by HRXRD.

A larger number of samples were grown between 15nm and 30nm to accurately determine how relaxation progresses up to twice the critical thickness. The two different sample sets are summarised in tables 5.1 and 5.2, in which the thickness of each layer was measured by XTEM in the (000) diffraction condition to eliminate inaccuracies due to sample tilting. In each sample set, a control virtual substrate was grown without a strained silicon cappng layer, which are labelled LG20-0 and TG20-0.

5.2 Properties of Virtual Substrates

5.2.1 Relaxation and Composition

The germanium composition and relaxation of the constant composition capping layer of each virtual substrate listed in tables 5.1 and 5.2 were determined from RSMs using HRXRD. Figure 5.4 shows RSMs around the (224) reflections for samples LG20-0 and TG20-0. The units Q_x and Q_z are reciprocal lattice units along the x and z directions of the unit cells, respectively.

Peaks associated with the $Si_{0.8}Ge_{0.2}$ layer and silicon substrate do not both line up exactly along each (224) direction (drawn aligned to the silicon substrate peak) due to the relative tilt between the layers, which is compensated for by the software when determining peak positions with a map around the (004) reflection.

Determination of both quantities depends on the ability to determine the peak position of the constant composition layer of a virtual substrate, which is spread to some degree by its dislocation content (see section 3.2.1). For these scans this equates to an error of around $\pm$0.5% in relaxation, and $\pm$0.005 in x, the germanium composition. Tables 5.1 and 5.2 show that all virtual substrates are over 97% relaxed with germanium compositions close to 20%. Together, the relaxation and germanium composition of the

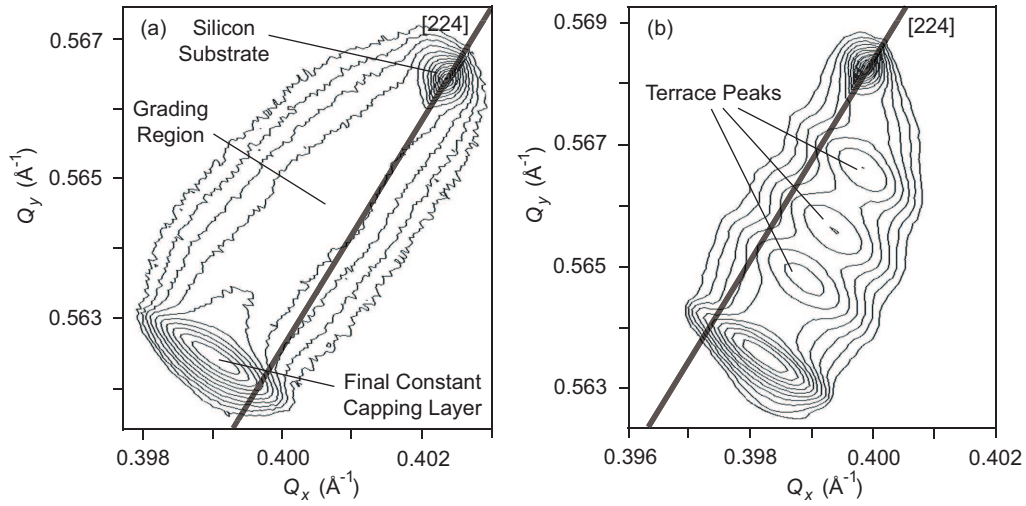

Figure 5.4: RSMs around the (224) reflection for 20% virtual substrates which are (a) linear graded (LG20-0), and (b) terrace graded (TG20-0). Maps have been simplified to aid presentation.

virtual substrate dictate the degree of strain an overgrown layer of silicon is subjected to. This becomes important in section 5.3.2 when calculating the relaxation of the strained silicon layers.

5.2.2 Density of Threading Dislocations and Pile-ups

Each strained silicon layer has threading dislocations grown into it, courtesy of the underlying virtual substrate, which can be revealed with defect etching. A section of approximately 1cm^2 in area was taken from near the centre of each strained silicon capped virtual substrate and etched for 10s, to take advantage of the silicon undercutting to reveal dislocations more clearly (see section 4.2.3). Using the DIC microscope, 50 images were obtained of the etched surface at a $\times$50 magnification, each with a viewable area of 105$\times$78μm (8.19$\times$10^3μm^2). By counting the number of etch pits in each image the mean density of threading dislocations for each sample was calculated, and the

standard deviation between images used as an estimate of the error. The mean density of threading dislocations for each sample set was measured to be $2.2\pm0.7\times10^{5}\,\mathrm{cm}^{-2}$ for the linearly graded samples, and $7.0\pm3.5\times10^{4}\,\mathrm{cm}^{-2}$ for the terrace graded samples.

Strained silicon can complicate the determination of the threading dislocation density originating from only the virtual substrates due to the presence of stacking faults (see figure 4.4). Each stacking fault is bounded by two partial threading dislocations which have originated from the glide of only one 60° dislocation, as depicted in figure 2.24. The true number of threading dislocations at the surface has been increased by one, but the density from the virtual substrate is unchanged. Therefore, if any stacking faults appeared in the 50 images taken from each sample to calculate the density of threading dislocations, only the leading 90° partial threading dislocations were counted. The additional contribution due to stacking faults is considered in section 5.3.2.

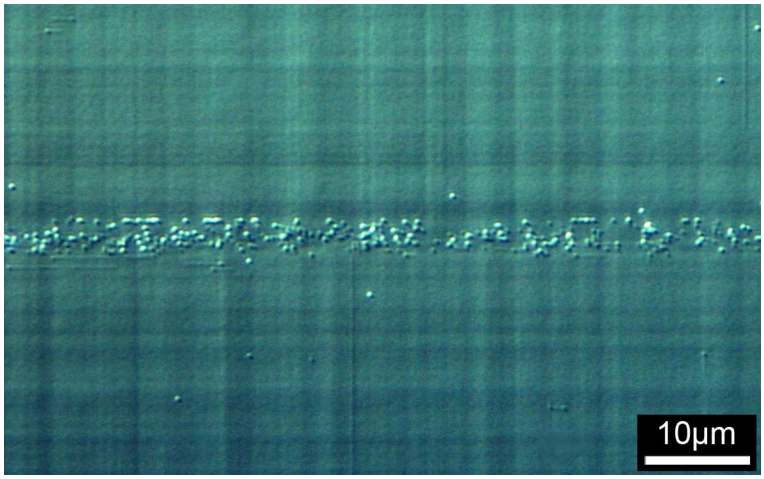

Figure 5.5: DIC microscope image taken from sample LG20-4 (17.4nm of strained silicon) after a 10s etchant exposure, showing pile-up of threading dislocations.

Pile-ups of threading dislocations originating from the virtual substrate can also be revealed by etching, as shown in figure 5.5. To quantify their line density (total length

of pile-ups per unit area), the measurement grid in the eyepiece of the DIC microscope was employed to measure the approximate length of pile-ups whilst scanning the 1cm^2 area of each sample. Mean pile-up densities from all the samples in each sample set were estimated to be 0.5$\pm$0.2cm^{-1} for the linearly graded samples, and $<$0.02cm^{-1} for the terrace graded samples (0.02cm^{-1} was the highest pile-up density measured in the sample set). The effect of pile-ups on the relaxation of strained silicon will be discussed in section 5.5.1.

5.2.3 Surface Roughness

The surface roughness of the uncapped linear and terrace graded virtual substrates (LG20-0 and TG20-0) was measured using AFM to provide an estimate of the roughness of the misfit interface for the silicon capped samples. Scans were conducted over three 20μm^2 areas to determine the mean RMS roughness and Z-range roughness, as shown in table 5.3. Example scans are shown in figure 5.6.

Sample	RMS Roughness (nm)	Z-range (nm)
LG20-0	2.6$\pm$0.4	17$\pm$3
TG20-0	1.5$\pm$0.2	13$\pm$2

Table 5.3: Tabulated AFM results for uncapped 20% linearly graded and terrace graded virtual substrates.

The terrace graded virtual substrate design is possesses a smoother surface than the linear graded design, in addition to its lower densities of threading dislocations and pile-ups at the surface. The relaxation of strained silicon can therefore be studied on two misfit interfaces of differing quality using the two sample sets.

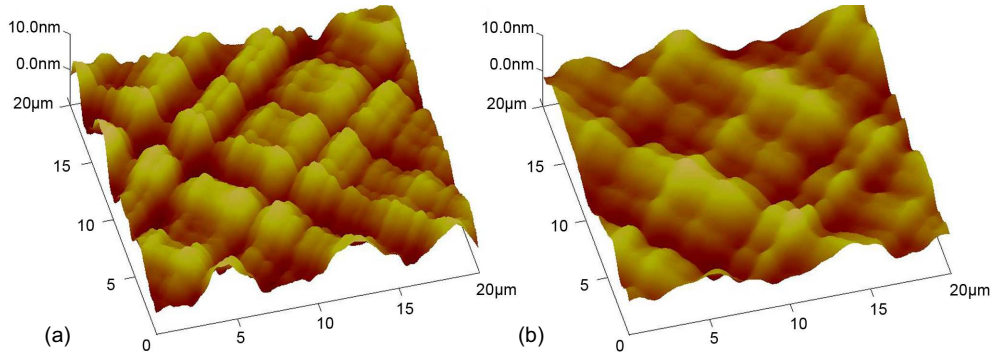

Figure 5.6: AFM images obtained from a $20\mu m^2$ area scan of an uncapped (a) linear graded (LG20-0) and (b) terrace graded (TG20-0) virtual substrate.

5.2.4 Surface Roughness of Strained Silicon

The mean RMS and Z-range roughness for each strained silicon layer was measured with three $20\mu m^2$ area scans. Example scans of samples TG20-4 (19.2nm of strained silicon) and TG20-8 (95.6nm) presented in figure 5.7 show that strained silicon overlayers adopt the same crosshatched pattern as the underlying virtual substrates (see figure 5.6). However, the surface roughness of strained silicon varies with layer thickness, as shown in figure 5.8, such that the surface of all layers are slightly rougher than the bare virtual substrates on which they are grown. In both sample sets, the largest degree of surface roughness is observed in layers which are approximately 20nm thick.

The images presented in figure 5.7 show that increased surface roughness is not due to the onset of 3-dimensional island formations, which can result from highly strained epitaxy (see section 2.2.2). In other works, computer simulations and experimental evidence suggest that it is energetically favourable for increasing degrees of tensile strain in $Si_{1-x}Ge_x$ to smooth a surface, whereas increasing degrees of compressive strain leads to a rougher surface [Xie et al., 1994]. These results offer no explanation as to why

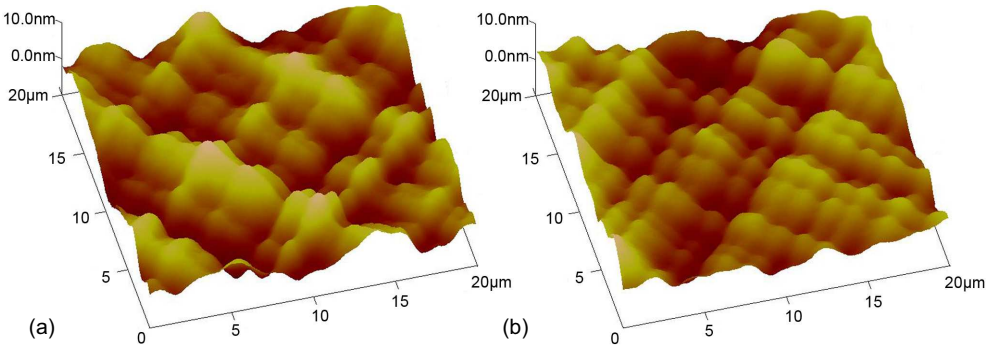

Figure 5.7: AFM images obtained from a $20\mu m^2$ area scan of (a) 19.2nm (TG20-4) and (b) 95.6nm (TG20-8) of strained silicon on 20% terrace graded virtual substrates.

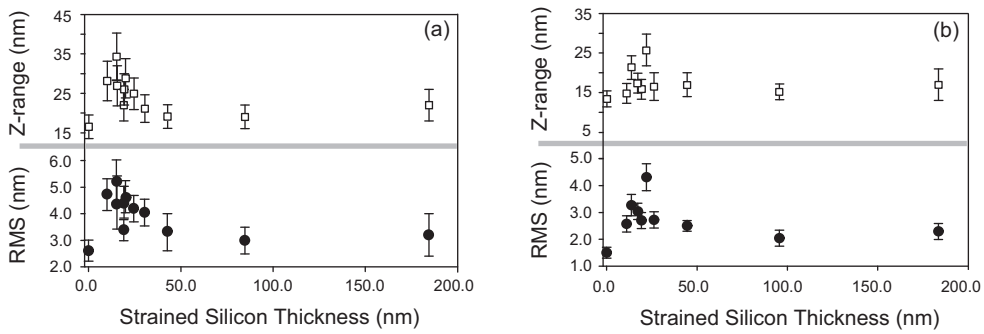

Figure 5.8: RMS and Z-range roughness measured by AFM as a function of strained silicon thickness for (a) linear graded and (b) terrace graded samples.

surface roughness should initially increase with layer thickness before returning to a level comparable to the underlying virtual substrate.

In chapter 2, the theoretical considerations for critical thickness and dislocation pinning assume perfectly flat misfit interfaces and free surfaces for strained layers. Roughness at either interface could can have implications for the validity of their conclusions, as dislocations glide though an undulating layer with local strain variations.

5.3 Measurement of Relaxation with Defect Etching

5.3.1 Annealing Conditions

During electronic device fabrication, substrates may undergo high temperature processing. Strained layers must not undergo excessive relaxation under such conditions, as the associated proliferation of dislocations compromise material quality. Germanium diffusion into the strained silicon layer from the virtual substrate, which reduces the effective thickness of the layer, also becomes a factor at higher temperatures [Sugii, 2001]. The physical processes behind diffusion in silicon and germanium are discussed in detail by Murch and Nowick [1984].

The diffusion of germanium into the strained silicon layer of sample LG20-9 (30.4nm of strained silicon) after annealing was measured by SIMS to determine suitable conditions from which to study relaxation. Annealing was performed in a flowing nitrogen ambient quartz tube furnace for 1hr at a range of temperatures between 750°C and 950°C. Samples were heated in nitrogen in the neck of the furnace for 10min prior to annealing, where they were also allowed to cool for a further 10min after annealing. Comparisons between the different diffusion profiles after annealing and in as-grown state, as shown in figure 5.9, were used to estimate the highest annealing temperature which leads to minimal diffusion.

Annealing at 750°C and 850°C produced diffusion profiles which differ very little from the as-grown state, and display a germanium composition of 1% within 2nm of the misfit interface. At 900°C this is extended to almost 3nm, and at 950°C a germanium composition of 1% is found at approximately 4nm from the interface. Diffusion is more potentially problematic in thinner layers where a significant thickness of the layer becomes compositionally graded $Si_{1-x}Ge_x$. The highest temperature annealing conditions

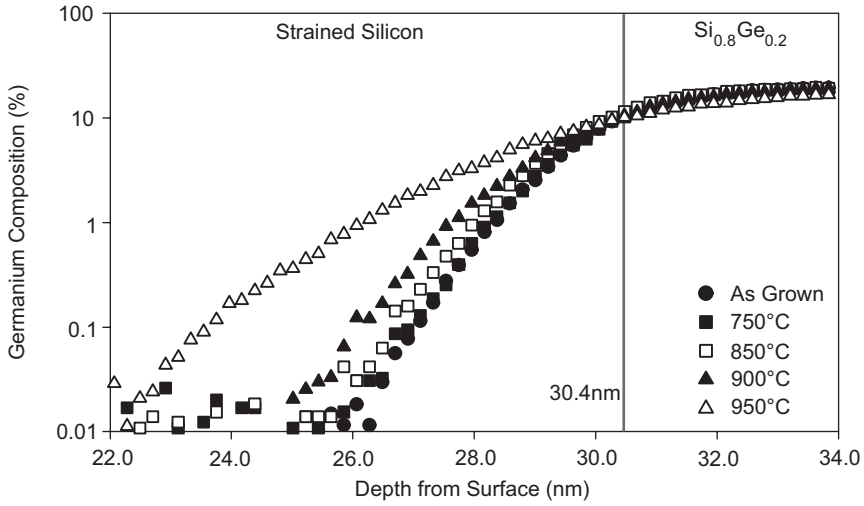

Figure 5.9: SIMS data taken from sample LG20-9 (30.4nm of strained silicon) in the as-grown state and after annealing at 750°C, 850°C, 900°C and 950°C for 1hr. Data obtained by Dr. R. J. H. Morris.

used in the rest of this work was therefore set at 850°C for 1hr, which was assumed to have no effect on the thickness of strained silicon.

5.3.2 Calculating Relaxation

The relaxation of strained silicon can be determined by revealing the presence of dislocations using defect etching. Measurement of the line density of misfit dislocations, ρ_{MD}, and stacking faults, ρ_{SF}, allows their contributions to the total relaxation of the layer, δ, to be calculated using equations 2.10 and 2.20. Relaxation of each layer can then be converted into a percentage of the total strain imparted to it by the underlying virtual substrate with equation 2.3, using HRXRD values in tables 5.1 and 5.2. This can be summarised as:

$$\delta = \frac{(\rho_{MD} b_{eff} + \rho_{SF} b_{SF})}{0.0417 x R} \times 100\% \tag{5.1}$$

Where R is the relaxation, and x the germanium composition of the final constant composition layer of the underlying virtual substrate. In this formulation, 0% relaxation corresponds to a fully strained layer (no dislocations) and 100% relaxation corresponds to bulk silicon.

An exposure time of 10s to the dilute Schimmel etchant was used to reveal dislocation features for the measurement of ρ_{MD} and ρ_{SF} in each sample. Images of misfit dislocations were obtained with the DIC microscope at a $\times$50 magnification (see figure 4.4) and their total length in each image was measured (using UTHSCSA ImageTool v3.0 [ImageTool v3.0, 2007], a freeware image manipulation package), and ρ_{MD} calculated. Stacking faults were imaged at a $\times$10 magnification (with a viewable area of $2.05\times10^5\mu$m^2) and their length measured to calculate ρ_{SF}. Mean values for ρ_{MD} and ρ_{SF} were determined from 10 randomly taken images at each magnification, from which the standard deviation between images served as an estimate of error.

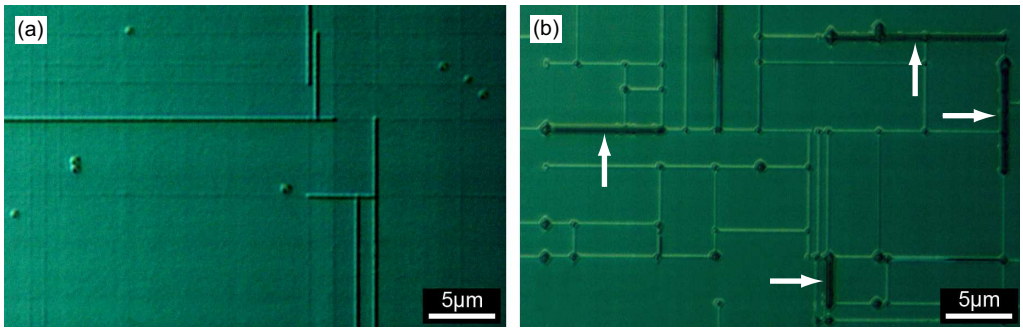

Figure 5.10: Images taken with the DIC microscope showing stacking faults in (a) 30.4nm (LG20-9) (b) 184.5nm (LG20-12) of strained silicon after etching for 10s and 20s, respectively. Possible microtwins are indicated.

The inability to clearly differentiate between stacking faults and misfit dislocations makes any estimate of relaxation in these layers inaccurate, and limits the determination of relaxation by defect etching to a maximum thickness of 45nm. A more

detailed study of the variation in stacking fault density with layer thickness is presented in section 5.3.4.

The relaxation of the linear and terrace graded samples are presented in figures 5.11 and 5.12 as a function of strained silicon thickness. In both sample sets, a low density of misfit dislocations (and a low level of relaxation) is observed below the predicted critical thickness of 13.4nm, as has been noted for strained silicon in other works [Samavedam et al., 1999]. Annealing at 850°C for 1hr increases the level of relaxation observed in layers thinner than 20nm, reaching a maximum of 0.6% for the linearly graded samples and 0.4% for the terrace graded samples. Relaxation of thicker layers appears to be negligibly affected by annealing.

This analysis relies on the ability of defect etching to reveal all the dislocation structures present in strained silicon layers. Unfortunately this technique cannot be applied over the entire thickness range under consideration due to the proliferation of stacking faults in thicker layers. Figure 5.10 (a) is taken from a 30.4nm layer of strained silicon (sample LG20-9), for which the line density of stacking faults is measured to be $350\pm30\text{cm}^{-1}$, and both stacking faults and misfit dislocations can be clearly differentiated. For a 184.5nm layer of strained silicon (sample LG20-12) presented in figure 5.10 (b), the density of stacking faults is $4600\pm320\text{cm}^{-1}$, and no weaker features associated with misfit dislocations are revealed after a 20s exposure to the etchant. Smaller and wider features are present (as indicated) which may be due to two closely spaced stacking faults or nucleated microtwins (the presence of which are discussed in section 5.4).

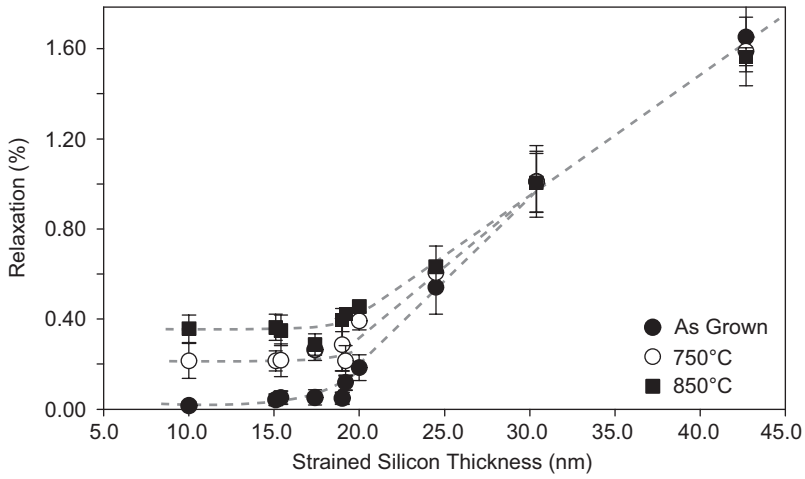

Figure 5.11: Graph to show relaxation as a function of strained silicon thickness for the linearly graded sample set. Lines are for guidance only.

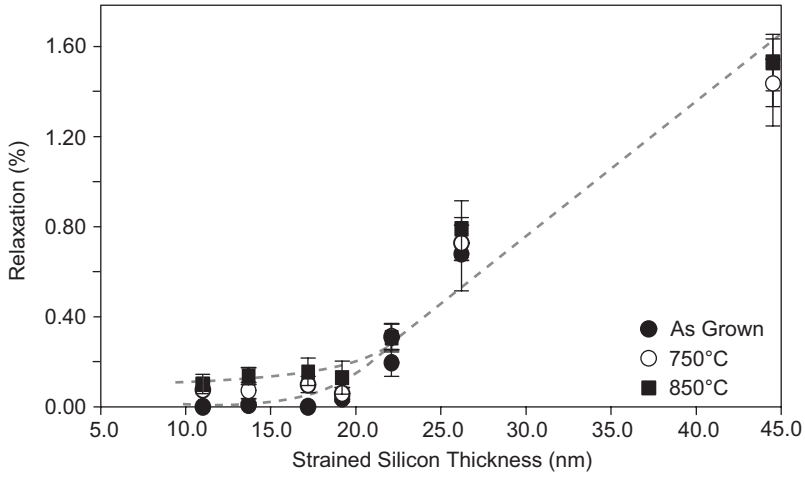

Figure 5.12: Graph to show relaxation as a function of strained silicon thickness for the terrace graded sample set. Lines are for guidance only.

The onset of surface roughness in figure 5.8 cannot be attributed to strain around misfit dislocations (as is believed to be the case with crosshatching [Lutz et al., 1995]) as the densities of dislocations increases with thickness, whereas surface roughness is observed to decrease. The densities observed in thinner layers are also believed to be much too low to create large scale roughness.

5.3.3 Dislocation Motion

Increases in relaxation after annealing are caused either by the lengthening of pre-existing misfit dislocations through glide, or the glide of previously immobile threading dislocations. To measure the percentage of dislocations which have glided in each strained silicon layer, the number of threading dislocations associated with misfit dislocations were counted in 20 images obtained with the DIC microscope. Dividing this quantity by the total number of threading dislocations counted in these images gives the fraction of threading dislocations which have glided to form misfit dislocations, as shown in figure 5.13.

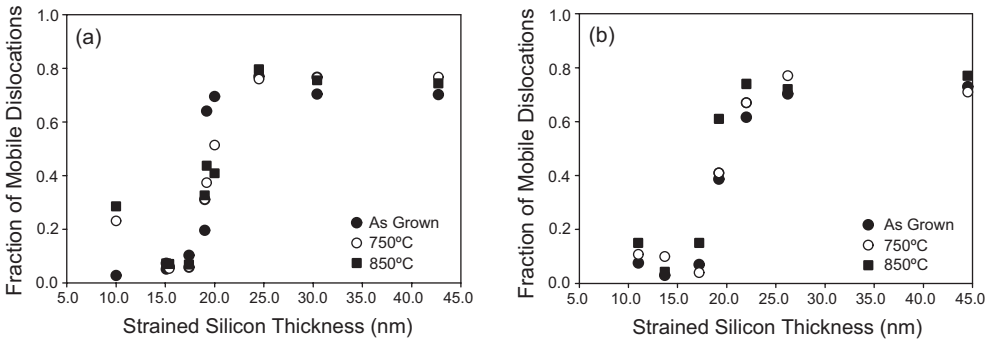

Figure 5.13: Graphs showing the fraction of threading dislocations which have glided to form misfit dislocations for (a) linearly graded and (b) terrace graded samples.

In both sets of samples the percentage of mobile threading dislocations rises from

around 10% to over 70% of the total population as the layer thickness increases. The increase occurs over a narrow thickness range, centred on 20nm, which corresponds to an initial increase in relaxation by a factor of approximately 4 in figures 5.11 and 5.12. Any subsequent variation in the number of mobile threading dislocations is negligible as thickness exceeds 22nm. Relaxation in thicker layers is therefore more likely to be due to increases in the length of misfit dislocations, rather than their number.

To determine the mean misfit dislocation length in each strained silicon layer, the length of 100 randomly chosen misfit dislocations were measured using the scale grid in the microscope eyepiece. Only misfit dislocations which had not undergone a dissociation reaction to form an extended stacking faults were measured, and the results for as-grown samples are presented in figure 5.14.

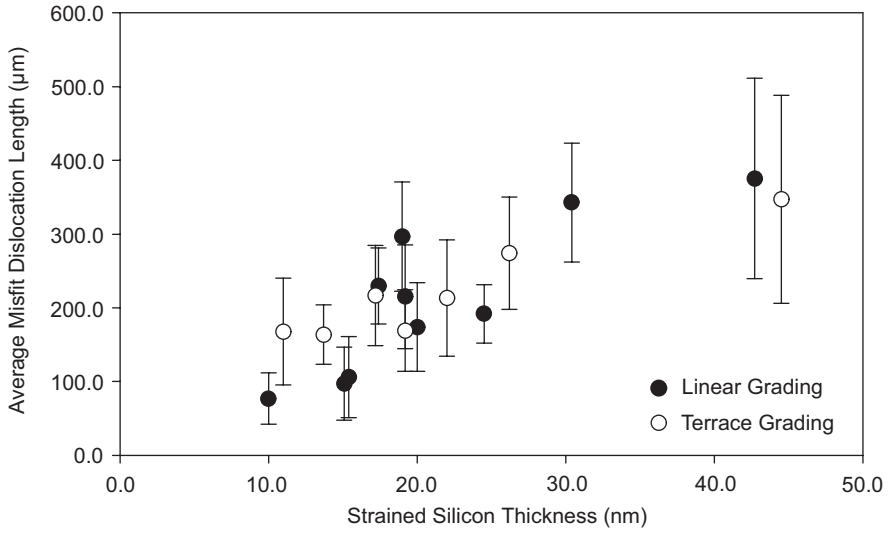

Figure 5.14: Graph to show the mean average length of misfit dislocations for both linear and terrace graded samples in the as-grown state.

The similarity between the fraction of mobile dislocations and the mean average length of misfit dislocation of the linear and terrace graded samples in figures 5.13 and

5.14, infer that the lower misfit interface roughness of the terrace graded samples does not have a significant effect on the gliding behaviour of dislocations. After annealing, a large variation in the length of individual misfit dislocations was observed, making the measurement of mean average lengths prone to large degrees of error. This is believed to be caused by an increased number of dislocation interactions, which are discussed in section 5.6.

Annealing has very little effect on the number of gliding dislocations, the observed increase in relaxation with annealing temperature is therefore predominently caused by the lengthening of pre-existing misfit dislocations formed in the as-grown state. The reluctance for large numbers of threading dislocations to glide, even in thicker layers and during annealing, remains unknown.

5.3.4 Density of Stacking Faults

Extended stacking faults in tensile strained layers are known to increase in density with thickness [Hartmann et al., 2007]. The linear density of stacking faults for the linear and terrace graded samples as determined in section 5.3.2, is presented in figure 5.15.

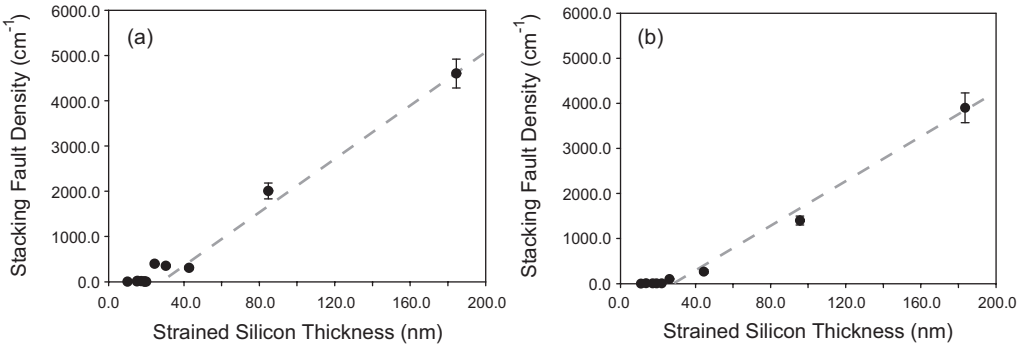

Figure 5.15: Measured line density of stacking faults as a function of strained silicon thickness for (a) linearly graded (b) terrace graded virtual substrates.

The thinnest layer which was observed to contain stacking fault was 13.7nm (sample TG20-2), and relaxation occurs only misfit dislocation formation in thinner layers. In both sample sets, the line density of stacking faults remains initially low and relatively constant at $10\pm5\text{cm}^{-1}$ as the thickness of strained silicon increases. At around 22nm there is a significant increase which continues linearly with thickness. The mean average length of stacking faults (determined from 100 examples in each layer) does not change with thickness, and remains relatively constant at $100\pm30\mu$m for both sample sets. Annealing does not significantly affect the density of stacking faults or their mean average length.

Stacking faults increase the number of threading dislocations at the surface, as described in section 5.2.2. This only becomes significant above 22nm where the density of stacking faults begins to increase. Between 22nm and 50nm, the threading dislocation density rises from $2.2\pm0.7\times10^{5}\text{cm}^{-2}$ to $3.2\pm0.9\times10^{5}\text{cm}^{-2}$ for the linearly graded samples, and from $7.0\pm3.5\times10^{4}\text{cm}^{-2}$ to $8.2\pm3.4\times10^{4}\text{cm}^{-2}$ for the terrace graded samples. The increased threading dislocation densities are within the experimental errors of those recorded whilst neglecting stacking faults, therefore relaxation in the thickness range considered in figures 5.11 and 5.12 does not significantly increase the density of threading dislocations. Layers thicker than 50nm, however, have a much greater stacking fault density, giving an estimated threading dislocation density of $4.5\pm3.1\times10^{6}\text{cm}^{-2}$ for the thickest linearly graded sample (184.5nm, LG20-12) and $2.1\pm2.7\times10^{6}\text{cm}^{-2}$ for the thickest terrace graded sample (183.6nm, TG20-9).

Each stacking fault forms a surface step along its length, as discussed in section 2.5.3. AFM scans over $20\mu\text{m}^2$ areas reveal the presence of such features in the thickest strained silicon layers, where the average separation of stacking faults is roughly comparable to the scan dimensions (see figure 5.10). The AFM height map presented in figure

5.16 (a) shows that the step features are too shallow to be revealed effectively, and only appear in non-quantitative deflection maps, as presented in figure 5.16 (b), from which the step height is estimated to be around 0.3nm. In the thickest layers where the stacking fault density is at its highest, surface steps have no appreciable effect on the surface roughness measured in figure 5.8.

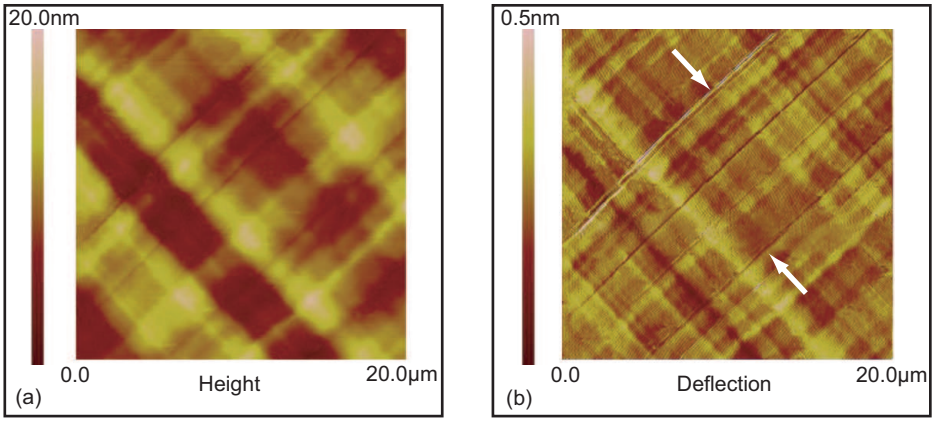

Figure 5.16: AFM 20μm^2 scans obtained from sample LG20-12 (184.5nm of strained silicon) showing (a) height map in plan-view and (b) deflection data of the same area. Two surface steps created by stacking faults are indicated.

Critical Thickness for Stacking Faults

A critical thickness for the formation of stacking faults can be estimated by considering the forces acting on the leading 90° partial dislocation of an extended stacking fault (such as depicted in figure 2.13, for a 60° dislocation). In this case there will be a retarding tensional force from the trailing misfit component (F_d, given by equation 2.12), and an additional retarding force due to the energy required to create a new area of stacking fault during glide, F_{SF}.

The force from the strain in the layer (F_h, given by equation 2.11) must be

greater than the sum of both retarding forces for a stacking fault to be formed ($F_h > F_d + F_{SF}$). Using the approximation $F_{SF} = \gamma h$ [Hull and Bean, 1999], where γ is the areal energy density of a stacking fault (55 - 75mJ m^{-2}, Hull et al. [1992]), the following expression for the stacking fault critical thickness can be obtained when the condition $F_h = F_d + F_{SF}$ is satisfied:

$$h_c \approx \frac{b(1 - \nu \cos^2 \theta)}{4\pi(1+\nu)\epsilon - \gamma} \ln\left(\frac{h_c}{b}\right) \tag{5.2}$$

Where b is the magnitude of the Burgers vector for a 90° partial dislocation (2.25Å), and θ is the angle it forms with the line direction (90°). This equation is plotted in figure 5.17 over the range of γ.

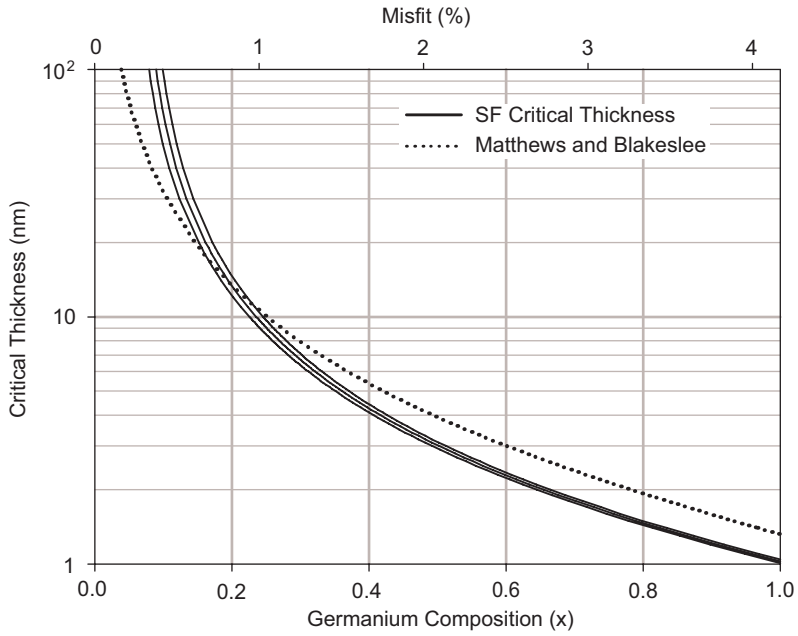

Figure 5.17: Graph to show the critical thickness for stacking fault formation in strained silicon on a 20% virtual substrate (equation 5.2). Also shown is the Matthews and Blakeslee critical thickness for 60° dislocation glide (equation 2.13).

For strained silicon on 20% virtual substrates an estimated critical thickness for stacking fault formation of between 12.2nm and 14.7nm is obtained in the given range of γ. The equations of Matthews and Blakeslee on which this analysis is based, however, have already been shown to yield non-quantitative results for strained silicon. A critical thickness for 60° dislocation glide is predicted at 13nm, but misfit dislocations in this work are observed in layers as thin as 10.2nm (figure 5.11). Qualitatively, equation 5.2 predicts that for strained silicon on 20% virtual substrates, the critical thickness for stacking fault formation should be similar to that of misfit dislocations. This is consistent with the findings of section 5.3.4, in which the thinnest layer in which stacking faults were observed was 13.7nm (sample TG20-2).

5.4 Dislocation Nucleation

XTEM observations of the thickest strained silicon layers (LG20-12 and TG20-9) reveals the presence of misfit dislocations, stacking faults and microtwins. Figure 5.18 (a) shows a microtwin formed along a $\{111\}$ direction by a stack of surface nucleated 90° partial dislocations (as arrowed) aligned along a $\{110\}$ direction (into the plane of the image). Microtwins have the same dependence on $\{220\}$ diffraction conditions as stacking faults (see section 4.2.1), and in figure 5.18 (b) only the microtwins aligned horizontally are revealed, with vertical features out of contrast.

60° dislocations are also revealed in figure 5.18 (b), which confirms such features are still present in thicker layers, and are not revealed in the defect etching image presented in figure 5.10 (b). 60° dislocation half-loops have not been observed in either LG20-12 or TG20-9 with PVTEM, even though both layers exceed the People and Bean critical thickness for nucleation. Both threading dislocations forming a half-loop must be observed to confirm their existence, and so the limited viewable area of PVTEM

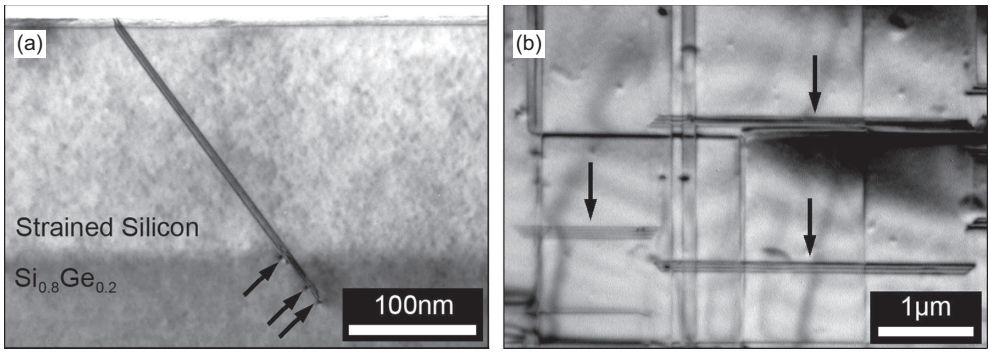

Figure 5.18: TEM images obtained in a (220) diffraction condition of a 183.6nm strained silicon layer (TG20-9) showing microtwin structures in (a) cross-section, with 90° partial dislocations indicated, and (b) plan view, with microtwins indicated.

samples does not entirely rule out their presence.

Estimated Critical Thickness for Microtwins

A lower limit for the critical thickness of microtwin nucleation can be approximated by considering the nucleation and interaction of two 90° partial dislocations on adjacent $\{111\}$ glide-planes (see figure 2.25). The two partial dislocations have equal Burgers vectors, and so their interaction will be repulsive. An expression for the simplified interaction areal energy density between two 90° partial dislocations forming the microtwin is given by [Philips, 2001]:

$$E_{int} = \frac{\mu b^2}{2\pi(1-\nu)r} \tag{5.3}$$

Where μ is the shear modulus of silicon (64GPa) [REF], and r is the distance between the interacting dislocations.

Microtwin formation is approximated to occur when the areal elastic energy density due to the strain in the layer (E_h, given by equation 2.8) exceeds the sum of the

nucleation areal energy density of a 90° partial dislocation (E_n, given by equation 2.8 with b = 2.25Å), the areal energy density of stacking fault formation (γ, as defined in section 5.3.4) and the interaction areal energy density between two 90° partial dislocations. The critical thickness condition is satisfied when $E_h = E_n + E_{int} + E_{SF}$, to give:

$$h_c \approx \frac{(1-\nu)}{2\epsilon^2(1+\nu)}\left[\frac{b^2}{8\pi\sqrt{2}a(x)}\ln\left(\frac{h_c}{b}\right) + \frac{\mu b^2(1+\nu)^2}{2G\pi r(1-\nu)} + \frac{\gamma}{G}\right] \tag{5.4}$$

This equation is plotted in figure 5.19, assuming the distance between the two partial dislocations is equal to the distance between two neighbouring $\{111\}$ glide-planes ($r = \frac{\sqrt{2}a(x)}{2}$). The equation is largely insensitive to the choice of γ, and so is plotted with the average value of 65mJ m^{-2} given in section 5.3.4.

A critical thickness for the nucleation of two 90° partial dislocations on adjacent glide-planes in strained silicon on 20% virtual substrates is predicted to be around 190nm by equation 5.4, which is roughly comparable to that of the People and Bean critical thickness. The existence of microtwins in layers in excess of 180nm suggests that nucleation occurs between 100 - 180nm, which is in reasonable agreement with this prediction. However, all microtwins observed are comprised of three of more 90° partial dislocations (see figure 5.18).

Several simplifications were made in the formulation of equation 5.4, in particular the increase in the surface free energy caused by the formation of a surface step created by the nucleation of the intial 90° partial dislocation was neglected. This makes the nucleation of subsequent 90° partial dislocations on adjacent glide-planes energetically favourable, so that microtwin structures form rather than independent 90° partial dislocation half-loops. It is likely that inclusion of such factors will decrease the estimated critical thickness, as a reduction in nucleation energy will favour nucleation in thinner

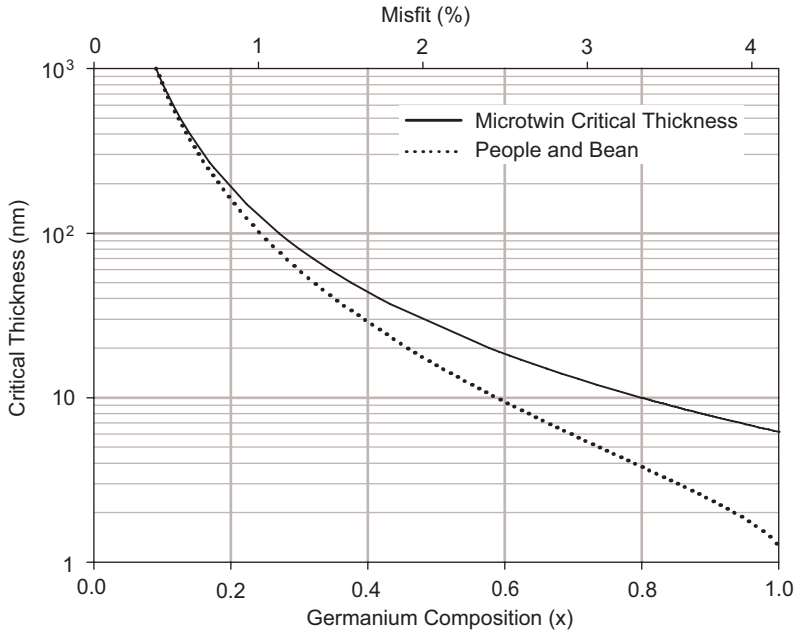

Figure 5.19: Graph showing the critical thickness the nucleation of a simple microtwin (equation 5.4). Also shown is the People and Bean critical thickness for 60° dislocation surface nucleation (equation 2.15).

layers. The addition of more interacting 90° partial dislocations to the mathematical microtwin structure, however, is likely to increase the critical thickness by increasing the interaction energy between the dislocations.

5.5 Measurement of Relaxation using Reciprocal Space Maps

Defect etching cannot be used to accurately measure the relaxation of strained silicon layers thicker than around 50nm, due to the inability to reveal misfit dislocations (see figure 5.18 (b)). Although PVTEM can be used to image dislocations instead, the smaller viewable area and the dependence of image formation on diffraction conditions limit its usefulness. Instead, RSMs of the (224) and (004) reflections with HRXRD

provides a more effective method of measuring relaxation.

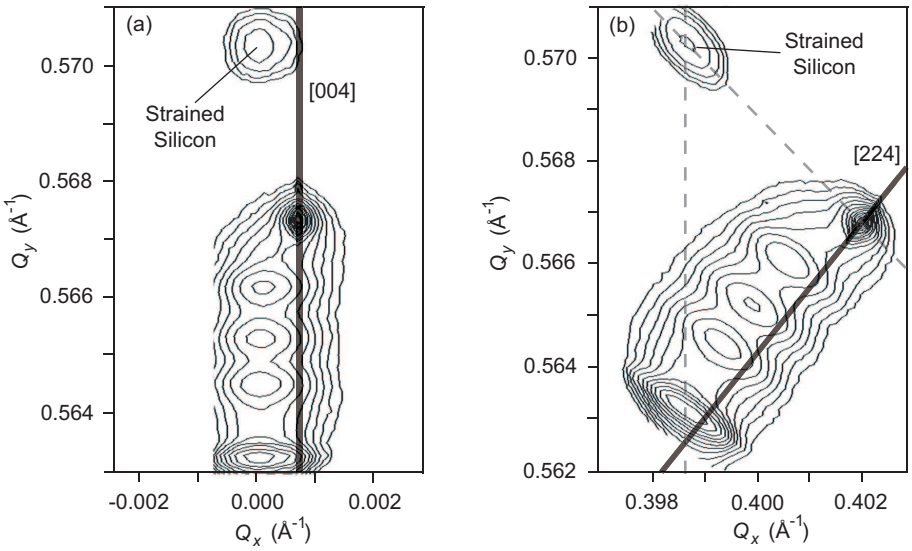

Figure 5.20: RSMs taken from a 20% terrace graded virtual substrates with 95.6nm of strained silicon (TG20-8) around the (a) (004) and (b) (224) reflections (maps have been simplified to aid presentation.)

HRXRD scans were conducted over a minimum of 18hr to increase the X-ray count rate from the relatively thin strained silicon layers and this ensures a suitable signal-to-noise ratio of the strained silicon peaks. This increases the accuracy with which peak positions can be determined in reciprocal space (see section 3.2.1). Example RSMs obtained around both reflections are shown in figure 5.20 for sample TG20-8 (95.6nm of strained silicon).

Strained silicon peak position determination is further complicated by the presence of misfit dislocations which cause peak broadening by enhancing layer mosaicity. In combination with the low intensity of X-rays detected from thin layers, the RSM technique is limited to layers thicker than about 15nm. Together these factors limit measurement of relaxation to around $\pm 0.4\%$.

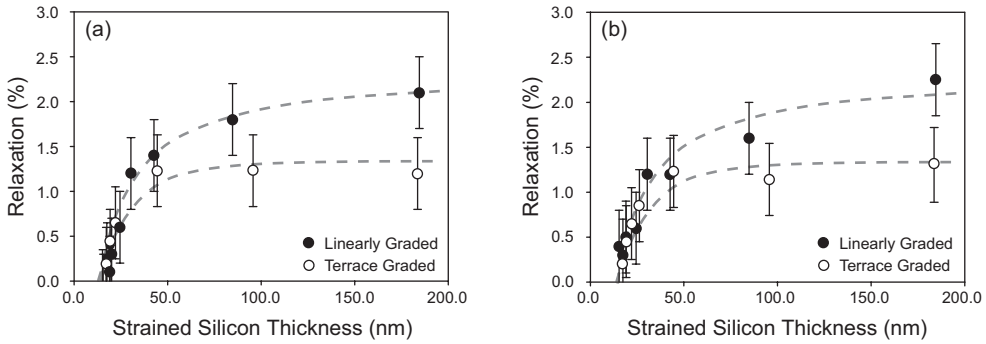

Figure 5.21: Graphs to show the relaxation of strained silicon on 20% linear and terrace graded virtual substrates as measured by HRXRD for (a) as-grown and (b) after annealing at 850°C for 1hr. Lines are for guidance only.

Figure 5.21 (a) shows that the relaxation of both the linear and terrace graded samples begins to saturate as the strained silicon thickness exceeds 50nm. The terrace graded samples reach a lower relaxation of 1.2±0.4% compared to the linearly graded samples, which have a maximum relaxation of 2.1±0.4%. After annealing for 1hr at 850°C, figure 5.21 (b) shows that relaxation appears to remain unchanged within the experimental limitations of the measurements.

Microtwins are only observed in the thickest layers of both sample sets (around 180nm), so it is assumed that the dominant mechanism for relaxation across the entire thickness range is the glide of pre-existing dislocations from the virtual substrate. Nucleated microtwins in the thickest layers of both sample sets are evidently of insufficient density to increase relaxation significantly above that of glide limited layers.

As all layers are relaxed predominantly by glide, the difference between the maximum relaxation of the linearly graded and the terrace graded samples can be explained by the difference in threading dislocation density.

5.5.1 Pile-ups of Threading Dislocations

A strained silicon layer subjects threading dislocations in a pile-up to a misfit strain, which can initiate glide. This can create a region of over-relaxation parallel to the length of a pile-up where the misfit dislocation density is higher than at the rest of the misfit interface. In the example given in figure 5.22 (a), the relaxation of a 20.0nm layer of strained silicon (sample LG20-7) is estimated at 0.2% in a region devoid of pile-ups, compared to roughly 0.9% in figure 5.22 (b).

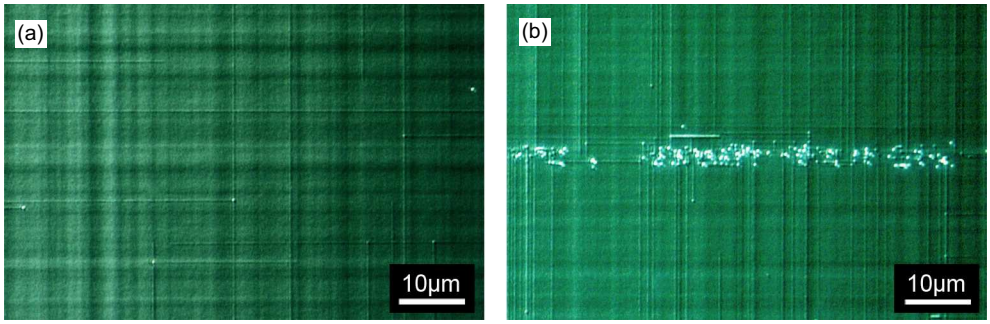

Figure 5.22: DIC microscope images taken from a 20.0nm strained silicon layer on a 20% linearly graded virtual substrate (LG20-7), showing (a) a region devoid of pile-ups, and (b) a pile-up of threading dislocations.

Each pile-up acts as a source for threading dislocation glide, so their density will influence relaxation throughout the layer as well as locally. The lower density of pile-ups and isolated threading dislocations in the terrace graded virtual substrate design provides an explanation for the discrepancy in relaxation as measured by HRXRD between the two sample sets shows in figure 5.21.

Local areas of over-relaxation have been implicated as a major contributory factor in dislocation pinning by locally negating a significant proportion of the misfit strain [Schwarz, 2003]. This possibility will be discussed further in section 5.6.

5.5.2 Comparisons with Compressively Strained $Si_{0.8}Ge_{0.2}$

Comparisons between the relaxation of tensile strained silicon on virtual substrates and compressively strained $Si_{1-x}Ge_x$ on silicon substrates are not straight forward. This is because growth on a silicon substrate is usually initially dislocation free and relaxation only occurs when the layer becomes sufficiently thick for half-loop dislocations to nucleate (around 130nm). However, in other works the growth of $Si_{1-x}Ge_x$ layers of around 20% germanium composition on silicon substrates have still been shown to relax to a much higher degree than the strained silicon layers in this study.

The relaxation of a 100nm thick layer of $Si_{0.86}Ge_{0.14}$ (5 times the Matthews and Blakeslee critical thickness) grown by CVD at 900°C has been measured (by an X-ray technique) to be almost 70% relaxed [Green et al., 1991]. Whilst this strained layer was grown at a higher temperature than in the present work, growth at lower temperatures have also been shown to exhibit a higher degree of relaxation than measured in this chapter. For example, MBE growth of a 160nm thick $Si_{0.85}Ge_{0.15}$ layer (over 8 times the critical thickness) at 550°C, has been measured (also by an X-ray technique) to be 20% relaxed [Bean et al., 1984]. CVD growth of a 70nm layer of $Si_{0.76}Ge_{0.24}$ (7 times the critical thickness) at 500°C has been shown to be 4% relaxed (using another X-ray technique), which increases for a 147nm layer of $Si_{0.73}Ge_{0.27}$ (16 times the critical thickness) to 20% [Jordan-Sweet et al., 1996]. Even after annealing at 850°C for 1hr, strained silicon layers in figure 5.21 still exhibit less than 2% relaxation. In all cases, the relaxation was observed to progress by the onset of MFR multiplication, which is not observed to occur within the thickness range of strained silicon in this study.

Defective silicon substrates and particulate contamination during growth could initiate dislocation nucleation in these layers at a lower thickness than expected, leading to a higher degree of relaxation than under "perfect" conditions. While these param-

eters are unknown, the commercial availability of almost defect-free silicon substrates effectively rules out the first consideration, and the use of CVD reduces the likelihood of the second. The relaxation of tensile strained silicon therefore appears to display an enhanced stability over that of compressively strained $Si_{1-x}Ge_x$. To investigate this fully, dislocation interactions must be considered.

5.6 Impediments to Relaxation

5.6.1 Quantification of Dislocation Pinning

Freund's critical thickness for dislocation pinning (figure 2.17) predicts that pinning events should be readily observed below 42.2nm for strained silicon on 20% virtual substrates. The ability to reveal misfit and threading dislocations by defect etching allows a detailed study of dislocation interactions in *post mortem* to be conducted.

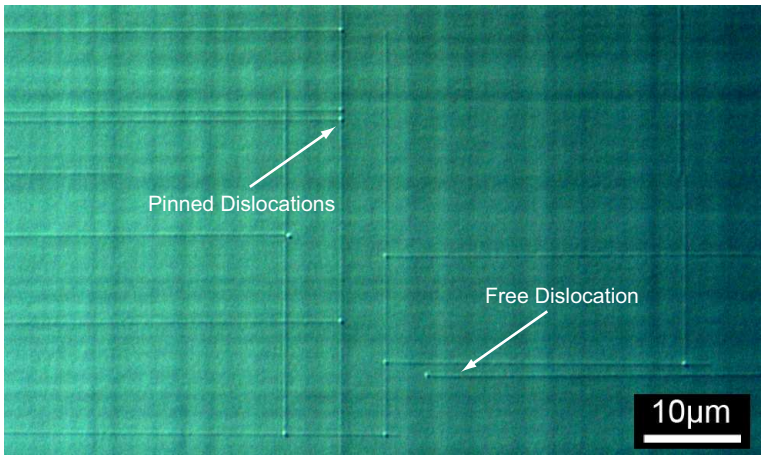

Figure 5.23: Image of the defect etched surface of a 20.0nm strained silicon layer (TG20-5), showing pinned and free dislocations as indicated.

By observing the path of a misfit dislocation along the surface of an etched sam-

ple with the DIC microscope eyepiece, the etch pit formed by the threading dislocation which has glided in the strained silicon can be located. Etch pits are only formed at these threading dislocations due to undercutting and the other threading dislocations, which trail into the virtual substrate, are not evident. If this pit terminates at an orthogonal misfit dislocation or stacking fault, the dislocation is considered to be "pinned". An example image showing pinned and "free" dislocations is shown in figure 5.23 for a 22.0nm layer (TG20-5).

100 randomly chosen dislocations were tracked in this fashion for each sample, and the fraction of pinned dislocations calculated. The error in the measurement was estimated by dividing the 100 dislocations followed in each layer into 5 sets of 20, and calculating the standard deviation between the pinned fraction of each set. This is shown in figure 5.24.

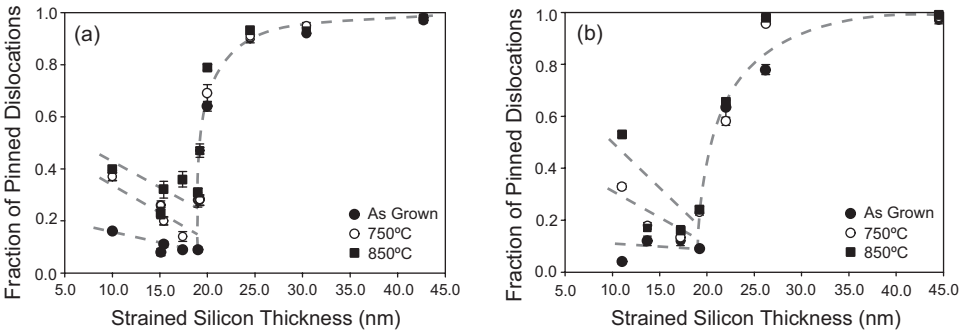

Figure 5.24: Graphs showing the fraction of pinned dislocations for (a) linearly graded and (b) terrace graded samples. Lines are for guidance only.

In Freund's model of dislocation interactions, a reduction in the number of pinning events would be expected from an increased layer thickness due to the corresponding increase in the thickness of the reduced glide channel (h_*, in figure 2.16 and equation 2.17). However, figure 5.24 shows this is evidently not the case for strained silicon, and

only layers thinner than about 20nm display such behaviour. The rapid increase in the pinned fraction at 20nm corresponds to an increase in the density of misfit dislocations (figures 5.11 and 5.12), and the number of mobile threading dislocations (figure 5.13). In these thicker layers there is an increased probability of a gliding dislocation interacting with an orthogonal misfit dislocation and becoming pinned. Existing theory, however, suggests that fewer dislocation should become pinned as layer thickness increases.

Annealing increases the number of pinning events in thinner layers, which can be explained as a direct consequence of the increased misfit dislocation density. Such layers display the predicted decrease in pinned fraction with increasing layer thickness up to 20nm. Figure 5.9 shows that it is unlikely that thinning of the reduced glide channel by germanium diffusion increases pinning after annealing within the chosen annealing temperature range.

The analysis of dislocation interactions by defect etching can only consider perpendicular interactions. A dislocation gliding parallel to a pre-existing misfit dislocation will also experience a reduced strain as it glides through its strain field [Schwarz, 2003]. In the present experimental analysis, it cannot be determined if misfit dislocations which end in the proximity of a parallel misfit dislocation were pinned, or stopped due to the termination of growth or annealing. The roughness of the strained silicon layer may also contribute to dislocation pinning by adding variability to its thickness and subsequently the reduced glide channel. Again this cannot be determined in the present analysis, but it should be noted that the differing misfit interface roughness of the terraced and linearly graded samples (section 5.2.3) does not seem to significantly affect the pinning or gliding behaviour of the dislocations (see also section 5.3.2). The similarities between the fraction of pinned dislocations in both sample sets in figure 5.24 also shows that it is unlikely that this significantly influences pinning.

In compressively strained $Si_{1-x}Ge_x$, it was found that dislocation pinning was absent as the layer thickness exceeded the value of 42.2nm, as predicted by Freund, allowing relaxation to progress to a much higher degree [Stach et al., 2000]. However, figure 5.24 shows that almost all dislocations in strained silicon become pinned up to a thickness of 50nm, which severely limits relaxation measured in figure 5.21, possibly up to 180nm. Further investigation is evidently still required.

5.6.2 Pinning by Stacking Faults

Stacking faults have already been included as sources for pinning in the data presented in figure 5.24. However, the image presented in figure 5.25, shows many threading dislocations terminating at stacking faults, which suggests their contribution to the total number of pinned dislocations may be more significant.

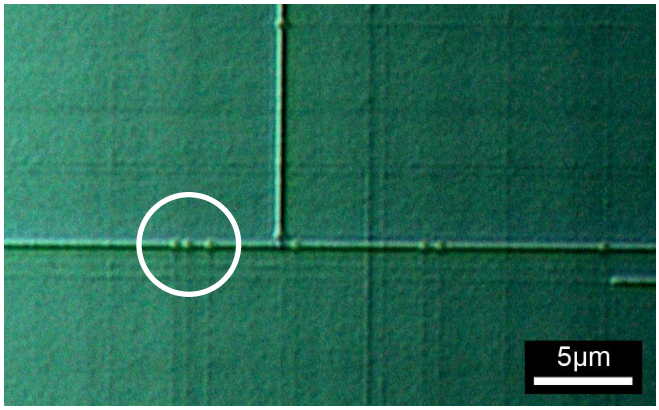

Figure 5.25: Image of the defect etched surface of a 20.0nm strained silicon layer (LG20-7), showing dislocations pinned by stacking faults, three of which are indicated.

To quantify dislocation impediment by stacking faults, the paths of randomly chosen misfit dislocations were followed using the DIC microscope, and it was noted if the chosen dislocation was pinned by an orthogonal stacking fault, misfit dislocation or

remained free. 100 pinned dislocations were located in each sample, and the fraction of dislocations pinned by stacking faults determined the results of which are shown in figure 5.26. A fraction of 1.0 in this formulation corresponds to all dislocations pinned by orthogonal stacking faults, and 0.0 corresponds to all dislocations pinned by orthogonal misfit dislocations.

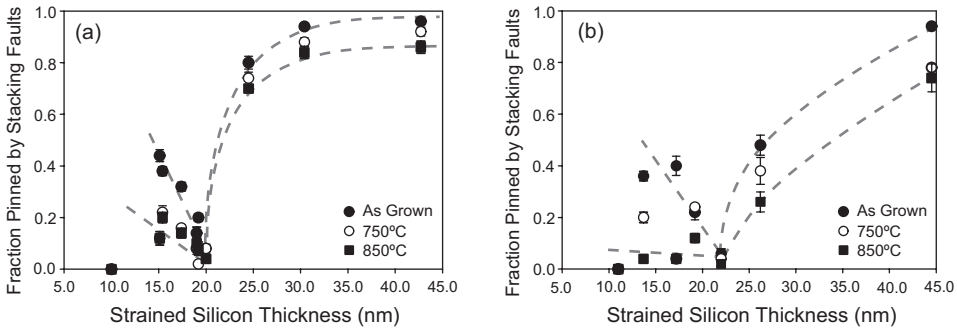

Figure 5.26: Fraction of pinned dislocations which are pinned by orthogonal stacking faults for (a) linearly graded and (b) terrace graded samples. Lines are for guidance only.

Pinning by stacking faults is observed to dominate in thicker layers, and is strongly correlated with the stacking fault line density (figure 5.15). Linearly graded samples display a sharp increase in stacking fault pinning for layers thicker than 20nm, the thickness at which the stacking fault density begins to rise significantly. The steadier increase in stacking fault pinning of the terrace graded samples is a consequence of the lower stacking fault density between 20nm and 50nm.

In the thinnest layers, stacking fault pinning accounts for almost 40% of all pinned dislocations, even though their line density within the layer is much lower than in the thicker layers. A minimum occurs at around 20nm, the thickness at which the fraction of mobile threading dislocations rapidly increases and pinning by misfit dislocations dominates (figure 5.24).

Increased annealing temperatures lead to an overall reduction in the stacking fault pinning fraction by around 10 - 20%, which suggests that annealing leads to an increase in the numbers of dislocations pinned by misfit dislocations. It is possible that pinned threading dislocations may become thermally unpinned from stacking faults more easily than misfit dislocations. Other works have shown theoretically that a dislocation pinned by a misfit dislocation leads to a very stable configuration, requiring a large amount of energy to unpin [Stach et al., 2000], but no such study has been conducted for stacking faults.

These results shown that the critical thickness of 42nm for dislocation pinning at this degree of strain theoretically predicted by Freund, is consistent for strained silicon. As the layer thickness approaches 50nm almost all pinning events are due to stacking faults, which are not considered in Freund's original theory, and pinning by orthogonal misfit dislocations approaches zero.

Stacking faults evidently provide a more effective impediment to dislocation glide than orthogonal misfit dislocations. Unlike misfit dislocations they are not confined to the plane of the misfit interface, and instead present a plane of atoms to the leading threading component of a gliding dislocation which it must displace to pass. No reduced glide channel exists for stacking faults, and so as the layer becomes thicker and the density of stacking faults increases (see figure 5.15), dislocation pinning by stacking faults becomes a significant limitation to relaxation by dislocation glide. The interaction between stacking faults also becomes important in thicker layers where a larger proportion of the total dislocation content are dissociated to form stacking faults. Crossing events between stacking faults were never observed in any of the etched layers up to 180nm, implying that the gliding 90° partial dislocation of a stacking fault is always impeded by an orthogonal stacking fault over this thickness range (see figures 4.5 and 5.10).

The impediment to the glide of both 60° dislocations and 90° partial dislocations by stacking faults therefore provides an explanation for the apparent stability of tensile strained silicon over that of compressively strained $Si_{0.8}Ge_{0.2}$. Significant levels of relaxation may only occur if the tensile strained layers become thick enough for the onset of the MFR multiplication mechanism to become energetically favourable.

5.7 Relaxation of Thicker Strained Silicon Layers

A maximum relaxation of only 2% has been measured up to a thickness of 180nm using HRXRD, with limited nucleation. Thicker layers were grown to determine how relaxation progresses, and which nucleation mechanisms were responsible.

Two strained silicon layers in excess of 350nm were grown on 20% linearly graded virtual substrates, under the same conditions specified in section 5.1.1. XTEM images presented in figure 5.27 (a) show that contamination occured during the growth of the silicon layers, the most likely origin of which being the deposition of silicon on the walls of the CVD chamber falling onto the surface during growth.

Repeat growths using dichlorosilane for the strained silicon layer (which reduces chamber coating [Hull and Bean, 1999]) at a temperature of 700°C and a growth rate of 8.70nm min^{-1}, gave the same results (figure 5.27 (b)).

Sample	Gas	h_{S-Si} (nm)	Relaxation (%)
S1	Silane	387.8	23.2
S2	Silane	742.6	68.5
D1	Dichlorosilane	471.1	—
D2	Dichlorosilane	726.8	—

Table 5.4: Tabulated properties for strained silicon of thickness h_{S-Si}, grown on 20% linearly graded virtual substrates. Relaxation of the silicon was measured by HRXRD.

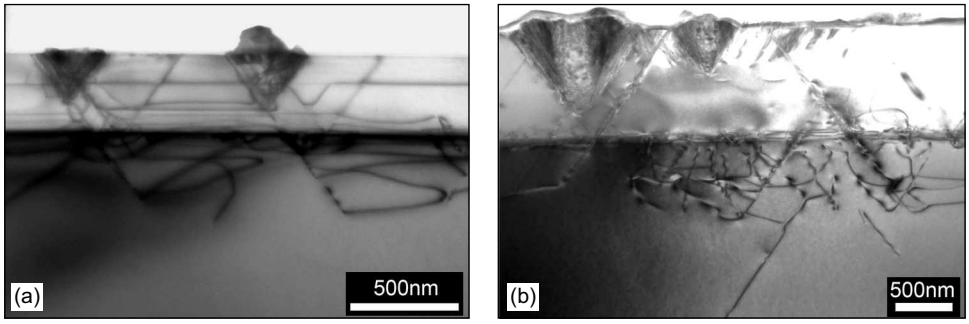

Figure 5.27: XTEM image of strained silicon layers grown using (a) silane (S1) and (b) dichlorosilane (D2), on 20% linearly graded virtual substrates.

Dislocation nucleation is observed in the vicinity of contaminants in both images of figure 5.27, together with dislocation injection below the misfit interface. The dislocation networks display the characteristic shape of the MFR multiplication mechanism (see figure 2.18).

HRXRD measurements in table 5.4 show that relaxation is almost 70% at 740nm. Whilst these layers provide evidence that relaxation increases significantly when the MFR mechanism becomes energetically favourable, the nucleation centres provided by the contaminants prevent these layers from inclusion in this work.

5.8 Summary

The relaxation of strained silicon on linear and terrace graded 20% virtual substrate designs has been quantified up to a thickness of 180nm (approximately 14 times the critical thickness) using HRXRD. The results show 2.1% relaxation of a 180nm thick strained silicon layer on the linearly graded virtual substrate design, while the same layer thickness on the terrace graded virtual substrate design was 1.2% relaxed. The discrepancy has been attributed to the lower density of threading dislocations, both in

isolation and in pile-ups, which the terrace graded design has been shown to possess. Annealing at 850°C for 1hr did not produce any measurable increase in relaxation using this technique.

A defect etching technique was also used to determine relaxation of strained silicon layers, which is more accurate at a thickness of less than 50nm than HRXRD. Misfit dislocations (and low levels of relaxation) were observed in layers thinner than the predicted Matthews and Blakeslee critical thickness, using this technique. Annealing at 850°C for 1hr was shown to increase relaxation in layers thinner than 20nm by 0.4%, while thicker layers remained unaffected. Comparisons between the relaxation of strained silicon obtained by both methods, and the relaxation of compressively strained $Si_{0.8}Ge_{0.2}$ determined in other works, suggests that strained silicon is more stable.

Examination of dislocation structures using defect etching revealed that relaxation is achieved through the glide of pre-existing threading dislocations from the virtual substrate up to a strained silicon thickness of 180nm. Dislocation nucleation in the form of microtwins was observed in the thickest layers, but were of insufficient density to yield an increase in relaxation above that achieved through glide alone. Up to a layer thickness of 22nm, dislocation glide predominantly forms 60° misfit dislocations, with few extended stacking faults resulting from dissociation. As the layer thickness exceeds 22nm, dissociation events become more frequent until extended stacking faults comprise a significant proportion of the total dislocation population at 180nm. While relaxation remains low up to a thickness of 180nm, the increased density of stacking faults and their associated threading components make such layers unsuitable for the fabrication of electronic devices.

Dislocation interactions which lead to pinning have been shown by Freund to enhance strained layer stability by inhibiting dislocation glide. Using the ability to dis-

tinguish the leading threading dislocation of a misfit dislocation afforded by defect etching (covered in the previous chapter), dislocation pinning was quantified for strained silicon layers below 50nm in thickness. Determination of the percentage of dislocations which terminate their leading threading dislocation on an orthogonal misfit dislocation or stacking fault (i.e. were pinned) led to an unexpected result. Almost all dislocations were observed to be pinned as the thickness of strained silicon increased to 50nm, which is contrary to the model proposed by Freund in which fewer pinning events are expected as the thickness of the strained layer exceeds 50nm.

Measurement of the contribution to dislocation pinning by stacking faults showed that a greater percentage of dislocations terminate at stacking faults as the strained silicon thickness increases (stacking faults are therefore more effective at pinning dislocations), until all pinned dislocations at 50nm are pinned by stacking faults (this is not accounted for in the model proposed by Freund). It was also observed that the interaction of orthogonal stacking faults always leads to pinning. As extended stacking faults do not form in compressively strained $Si_{1-x}Ge_x$, the enhanced stability (and limited degree of relaxation) of strained silicon is due to the increasing density of extended stacking faults with layer thickness. Significant levels of relaxation are have not been observed in this work, but are expected at a thickness where dislocation nucleation or multiplication becomes energetically favourable.

Chapter 6

Strained Silicon on 50% Virtual Substrates

In this chapter, the relaxation of strained silicon on 50% virtual substrates is investigated. The effect of using linear and terrace grading designs for virtual substrates is again considered.

6.1 Virtual Substrate Designs

Strained silicon was grown on two different virtual substrate designs, making up two sample sets within the same thickness range. Linear and terrace graded designs were again used to ascertain the effect the improved terrace graded design has on the relaxation of strained silicon. Three different terrace grading designs were considered.

6.1.1 Linear Grading

The 50% linear graded virtual substrate design used was a simple extension of that used in the previous chapter (see section 5.1.1). Growth was performed by LPCVD, using

germane and dichlorosilane with hydrogen as a carrier gas, at a total pressure of 80 Torr. Grading was fixed at 10% μm^{-1}, with a 2μm constant capping layer, making a 7μm thick structure. Unlike the 20% virtual substrates, growth temperature remained relatively constant and high throughout and was reduced only once from 900°C to 850°C at a germanium composition of 7%. This is represented in figure 6.1.

Intermediate *in situ* annealing stages of a 2min duration up to 20% were introduced in the same fashion as the terrace graded structures detailed in section 5.1.2. This provides energy for dislocation glide, and enhances relaxation in the lower regions of the virtual substrate. Also shown in figure 6.1 are the HRXRD results for relaxation and germanium composition of the final constant capping layer, which indicate that LG50-0 is highly relaxed.

6.1.2 Terrace Grading

Terrace graded virtual substrates have a large number of adjustable design parameters. In this study a design is desired which has a lower density of threading dislocations and pile-ups, and a smoother surface than the 50% linear graded design. A simple study was conducted to find a design by varying the compositional grading rate, and the thickness and number of terraces used.

Three designs were considered which were all based on the original design for the 20% terrace graded virtual substrates (see section 5.1.2), in which the grading rate was fixed at 10% μm^{-1}, with 500nm constant composition layers grown every 5% compositional increase (section 5.1.2). Variations between samples were implemented between 20% and 50% to determine if any properties are adversely affected when compared to the original design.

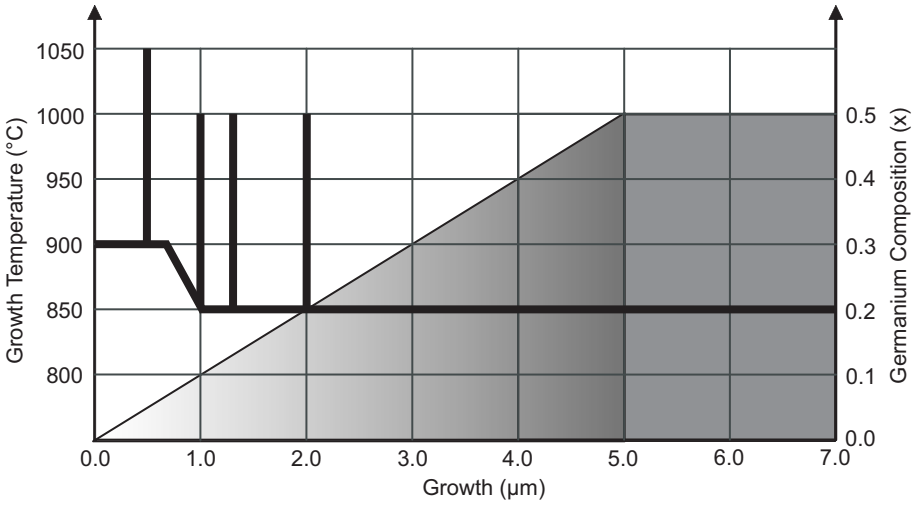

Figure 6.1: Graphical representation of the germanium composition and growth temperature (shown as a black line) for sample LG50-0, a 50% linearly graded virtual substrate.

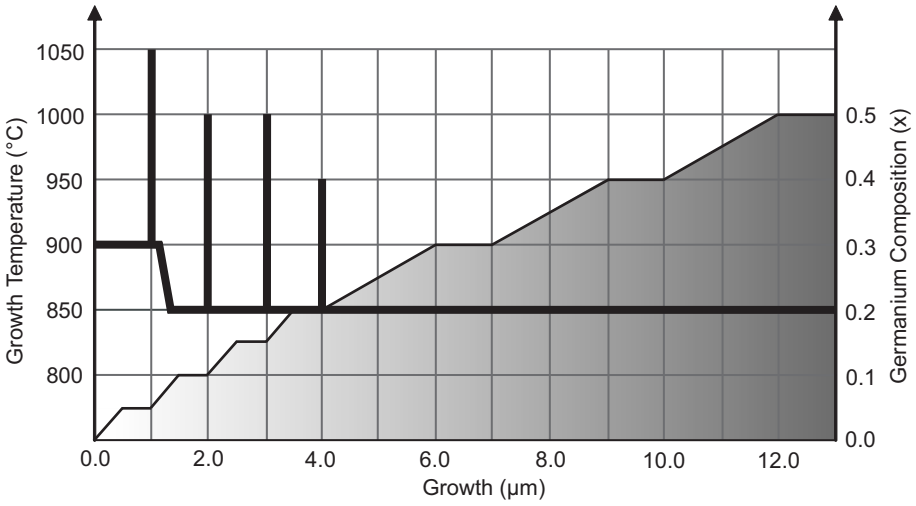

Figure 6.2: Graphical representation of the germanium composition and growth temperature (shown as a black line) for sample TG50-A, a 50% terrace graded virtual substrate. Also shown are HRXRD results for relaxation and germanium composition at each terrace.

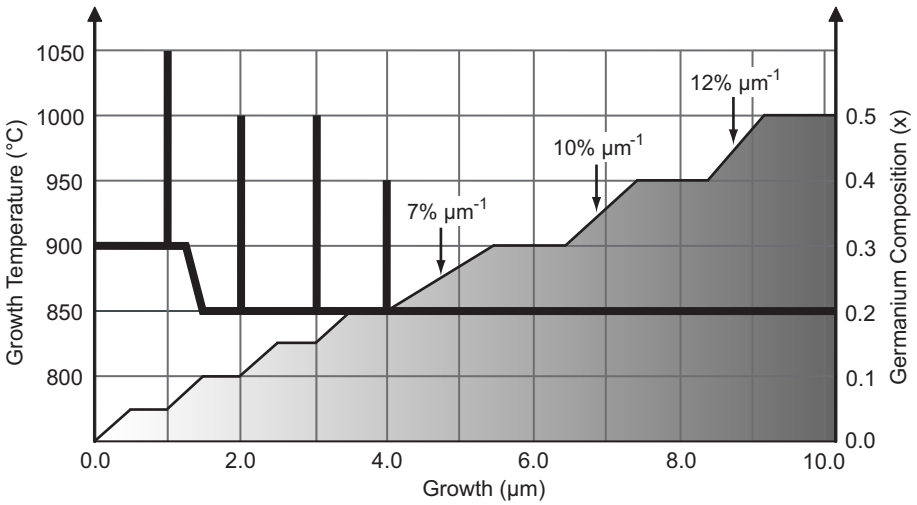

Figure 6.3: Graphical representation of the germanium composition and growth temperature (shown as a black line) for sample TG50-B, a 50% terrace graded virtual substrate. Also shown are HRXRD results for relaxation and germanium composition at each terrace.

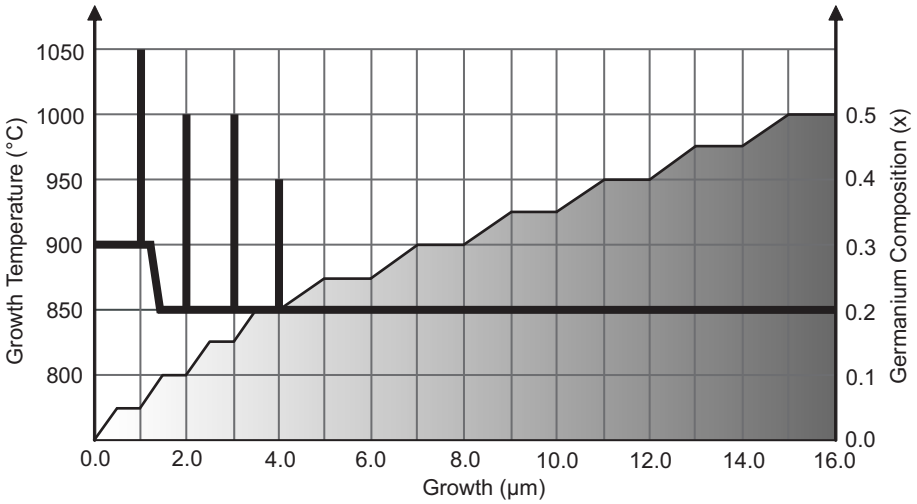

Figure 6.4: Graphical representation of the germanium composition and growth temperature (shown as a black line) for sample TG50-C, a 50% terrace graded virtual substrate. Also shown are HRXRD results for relaxation and germanium composition at each terrace.

In the first sample, TG50-A, the grading rate was reduced to 5% μm^{-1}, with 1μm thick constant composition layers grown at every 10% composition increase between 20% and 50%. Sample TG50-B had the same grading rate as sample TG50-A, but with 1μm thick terraces added every 5% composition increase. Together these two samples determine the effect additional terraces has on the properties of the virtual substrate and are shown in figures 6.2 and 6.3.

For sample TG50-C, the grading rate was increased with composition as shown in figure 6.4. TG50-C was designed to determine how such an increase affects the properties of the virtual substrate when compared to TG50-A. Other works suggest that increasing the grading rate at high composition will have an adverse effect on the threading dislocation density and surface roughness [Bogumilowicz et al., 2006].

The relaxation of each terrace presented in figures 6.2, 6.3 and 6.4 show over-relax in the intermediate layers which indicates the possibility that some degree of tensile strain is present. The final constant composition layer is highly relaxed in all cases. XTEM images of the structure of each virtual substrate design obtained in a (220) diffraction condition, is shown in figure 6.5.

Figure 6.5: XTEM images of (a) LG50-0, (b) TG50-A, (c) TG50-B, and (d) TG50-C, all obtained in a (220) diffraction condition.

6.2 Properties of Virtual Substrates

6.2.1 Density of Threading Dislocations and Pile-ups

Etching of $Si_{0.5}Ge_{0.5}$ in dilute Schimmel etchant displays some degree of selectivity to threading dislocations, as evidenced in section 4.2.2. Threading dislocation and pile-up

densities were measured in the uncapped linear and terrace graded virtual substrates after exposure of approximately 1cm^2 samples to the etchant for 60s. Three samples from each virtual substrate were used to estimate linear pile-up densities. The results are shown in table 6.1.

Sample	TDD ($\times 10^5$cm^{-2})	PUD (cm^{-1})
LG50-0	3.4±0.7	0.4±0.1
TG50-A	2.0±0.6	∼0.01
TG50-B	3.2±0.8	∼0.01
TG50-C	2.3±0.7	∼0.01

Table 6.1: Tabulated defect etch results for 50% virtual substrates, showing threading dislocation density (TDD) and linear pile-up density (PUD).

The variation in the threading dislocation density between the linear and terrace graded virtual substrates is around 1.4×10^5cm^{-2}. Sample TG50-B has the highest threading dislocation density of all four designs, which suggests that increasing the number of terraces has an adverse effect on the final threading dislocation density.

No pile-ups were found in any of the terrace graded virtual substrates, and so maximum densities were determined based on the area of each sample viewed during the measurement. Pile-ups were generally found to contain more threading dislocations than in 20% virtual substrates, as shown by comparing the image presented in figure 6.6 with that of figure 5.5. This is due to the requirement for more dislocations to relax the higher composition structure. The density of pile-ups within the 50% structure, however, is comparable to that of the 20% structure.

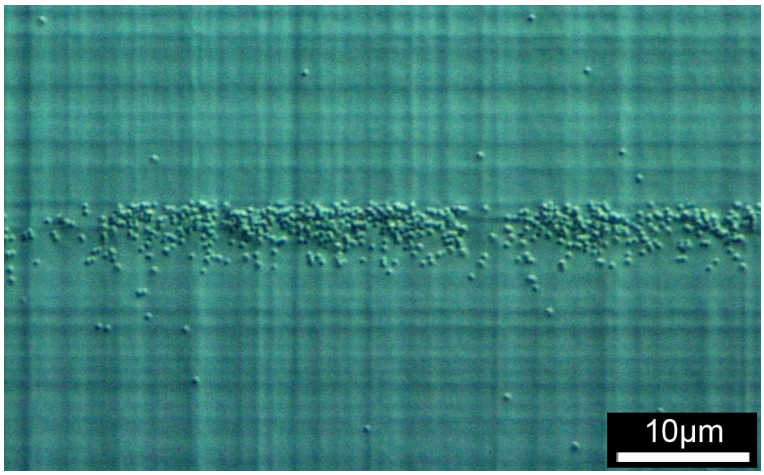

Figure 6.6: DIC microscope image taken from sample LG20-0 (50% linear graded virtual substrate) after a 60s etchant exposure, showing a dense pile-up of threading dislocations.

6.2.2 Surface Roughness

The mean RMS and Z-range surface roughness of the uncapped virtual substrates was measured using AFM from three $20\times20\mu m^2$ area scans, which are shown in figure 6.7. The results are presented in table 6.2.

Sample	RMS (nm)	Z-range (nm)
LG50-0	9.50±0.9	63±9
TG50-A	6.98±0.6	54±8
TG50-B	6.89±0.7	40±6
TG50-C	6.96±0.6	55±8

Table 6.2: Tabulated AFM results for 50% uncapped virtual substrates.

All three of the terrace graded samples have a reduced surface roughness compared to LG50-0, which is believed to be as a result of reducing the number of pile-ups formed in the graded regions of the structure (section 2.4.1). RMS roughness is compa-

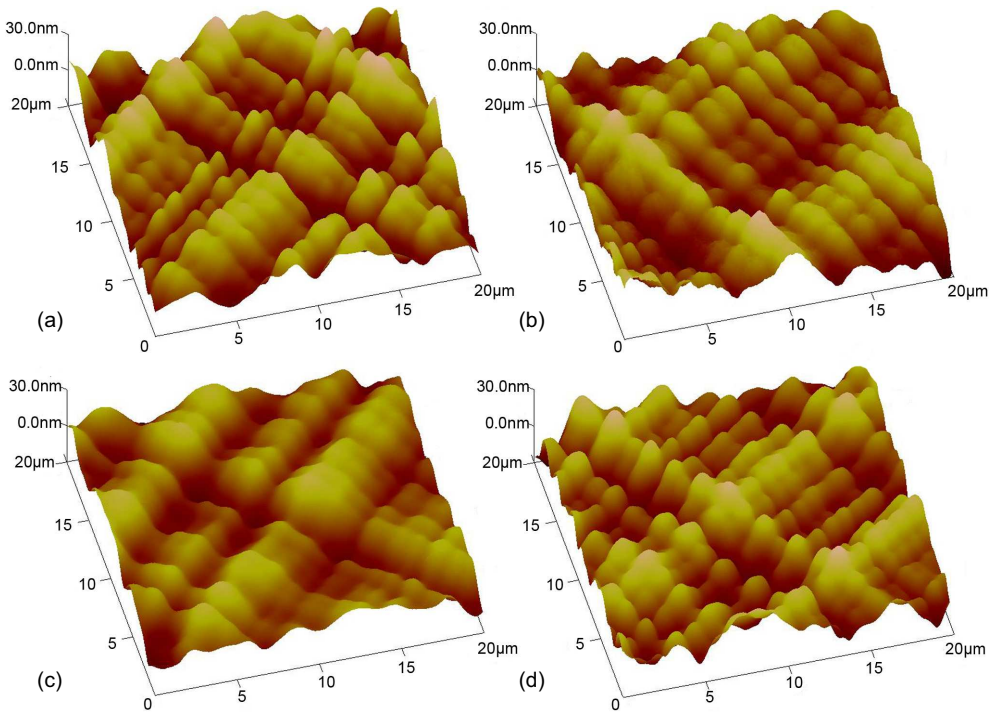

Figure 6.7: AFM 20μm^2 scans of samples (a) LG50-0, (b) TG50-A, (c) TG50-B and (b) TG50-C.

rable between the terrace graded samples, but the Z-range roughness of sample TG50-B is significantly lower. The increased number of terraces therefore has the effect of reducing the height range of the crosshatching, but the apparent increased width of the striations (figure 6.7 (c)) gives an RMS roughness close to that of the other terrace graded designs where the crosshatching is narrower.

The properties of samples TG50-A and TG50-C are very similar, which implies that increasing the grading rate as the composition increases has no appreciable effect on the the properties of the virtual substrate, within the chosen conditions of growth. Sample TG50-B displays a smoother surface, but an increased density of threading dislocations when compared to sample TG50-A, which is a result of increasing the

number of terraces. Sample TG50-C was chosen as the design for the strained silicon capped terrace graded virtual substrate sample set, purely on the basis that it is thinner and therefore easier to grow.

6.3 Strained Silicon

The same conditions were used to grow strained silicon as in the previous chapter, with silane at a temperature of 700°C and pressure of 20 Torr. The deposition rate was assumed to remain at 4.50nm min^{-1}.

From figure 2.15, the critical thickness of strained silicon on 50% virtual substrates is estimated to be 3.9nm for relaxation by glide, and 15.8nm for 60° half-loop nucleation (in the absence of significant glide induced relaxation). The range of strained silicon to be investigated was chosen to be between 5nm and 100nm, and the thickness of each layer was measured using XTEM in the (000) diffraction condition. All samples are listed in tables 6.3 and 6.4, together with relaxation and germanium compositions as measured by HRXRD.

Sample	h_{S-Si} (nm)	Ge Content (x)	Relaxation (%)
LG50-0	0.0	0.467	99.7
LG50-1	5.5	0.471	99.9
LG50-2	8.2	0.467	99.3
LG50-3	10.7	0.469	100.4
LG50-4	15.9	0.472	101.0
LG50-5	27.0	0.462	99.5
LG50-6	33.2	0.461	100.7
LG50-7	70.7	0.460	100.7

Table 6.3: Tabulated properties for the 50% linear graded samples of variable strained silicon thickness (h_{S-Si}) as measured by XTEM. Germanium composition and relaxation of the final constant capping layer were measured by HRXRD.

Threading dislocation densities of the two sample sets were measured and compared to the values obtained in table 6.1 for the uncapped virtual substrates LG50-0 and TG50-C (on which these samples are based). Increases in dislocation content limited the evaluation to samples thinner than 27nm (samples LG50-5 and TG50-3), which will be discussed further in section 6.5.2. The average threading dislocation density was measured to be $3.7\pm0.9\times10^5\text{cm}^{-2}$ for the linear graded samples, and $2.4\pm0.8\times10^5\text{cm}^{-2}$ for the terrace graded samples. Both results show a slight increase when compared to their uncapped counterparts in table 6.1, which may indicate an increase in selectivity afforded by the undercutting of the strained silicon layer (see section 4.2.3).

Sample	h_{S-Si} (nm)	Ge Content (x)	Relaxation (%)
TG50-0	0.0	0.473	98.5
TG50-1	9.4	0.474	100.3
TG50-2	18.5	0.474	98.8
TG50-3	21.6	0.474	100.5
TG50-4	34.6	0.468	99.1
TG50-5	39.3	0.488	100.3
TG50-6	68.8	0.470	99.4

Table 6.4: Tabulated properties for the 50% terrace graded samples of variable strained silicon thickness (h_{S-Si}) as measured by XTEM. Germanium composition and relaxation of the final constant capping layer were measured by HRXRD.

6.3.1 Surface Roughness of Strained Silicon

Mean RMS and Z-range roughness values were determined for each of the strained silicon layers using AFM, by averaging over three $20\mu\text{m}^2$ area scans, example scans of which are shown in figure 6.8. All layers were observed to adopt the crosshatching of their underlying virtual substrates, with no evidence of 3-dimensional island formations.

The measured surface roughness of strained silicon was observed to vary with

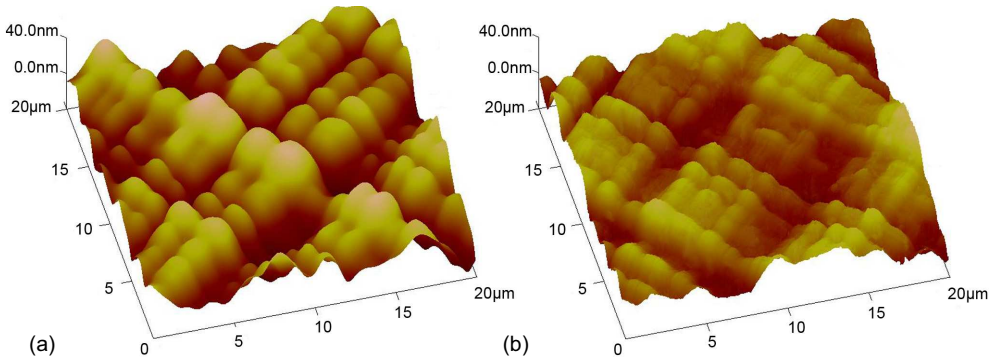

Figure 6.8: AFM images obtained from a 20μm^2 area scan of (a) LG50-4 (15.9nm of strained silicon) and (b) LG50-7 (70.7nm) of strained silicon on 50% linearly graded virtual substrates.

layer thickness, as shown in figure 6.9, in a similar fashion to that of the 20% virtual substrate samples (see figure 5.8). The roughest layers are again observed around 20nm in thickness, and so it is more likely that the additional roughness is a product of the chosen growth conditions rather than an affect of strain. Further work is required to determine if this is indeed the case, and suitable conditions under which it can be minimised.

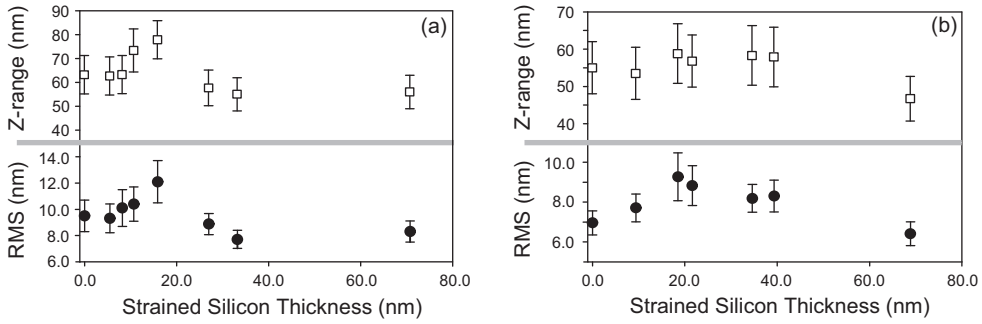

Figure 6.9: RMS and Z-range roughness measured by AFM as a function of strained silicon thickness for (a) linear graded and (b) terrace graded samples.

6.4 Measurement of Relaxation using Reciprocal Space Maps

6.4.1 Annealing Conditions

In the previous chapter, the maximum annealing temperature was determined to be 850°C for strained silicon on the 20% virtual substrates (see section 5.3.1). The relaxation of strained silicon in this chapter is also to be considered as a function of annealing temperature, so diffusion from the higher germanium composition virtual substrates must be considered. Figure 6.10 shows SIMS depth profiles of sample TG50-4 (34.6nm of strained silicon) in the as-grown state and after annealing for 1hr at temperatures between 750°C and 950°C. The same conditions were used during annealing as before, with 10min heat-up and cool-down times in a nitrogen ambient (see section 5.3.1).

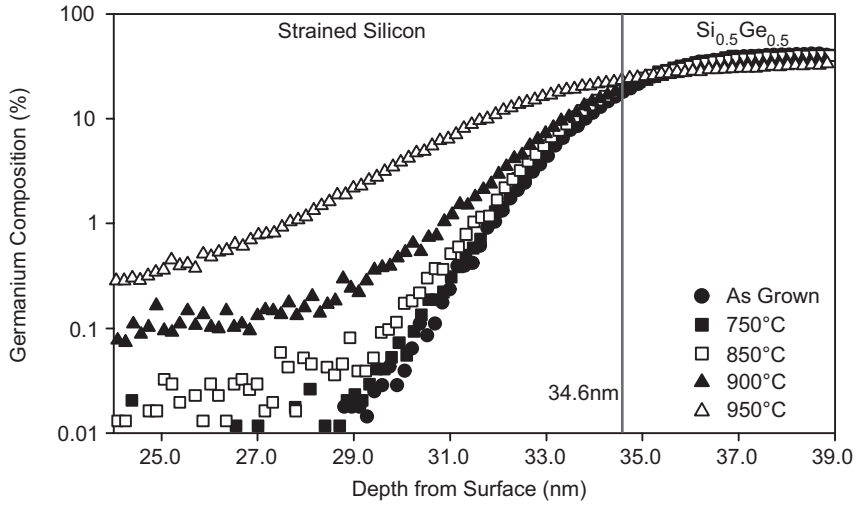

Figure 6.10: SIMS data taken from sample TG50-4 (34.6nm of strained silicon) in the as-grown state and after annealing at 750°C, 850°C, 900°C and 950°C for 1hr. Data obtained by Dr. R. J. H. Morris.

Annealing at 750°C and 850°C yield depth profiles which differ very little from the as-grown state, and all show a germanium composition of 1% within 4.0nm of the

misfit interface. This range is extended to 5.0nm at 900°C, and 8.0nm at 950°C. The highest temperature annealing conditions therefore remains at 850°C for 1hr.

6.4.2 Reciprocal Space Mapping

HRXRD scans were conducted over an 18hr period for obtaining RSMs to maximise the signal from thin (compared to the virtual substrate) strained silicon layer, thereby improving the accuracy of peak position determination and the measured relaxation. Under these conditions, the strained silicon peak for layers thinner than around 15nm do not have sufficient intensity from which to determine peak position, and can only be measured with much longer scan times. RSMs of samples TG50-3 (21.6nm) and TG50-6 (68.8nm) presented in figure 6.11 show significant mosaic peak broadening which indicates a high dislocation content. The higher surface roughness of the 50% virtual substrates also reduces the intensity of the strained silicon peak in comparison to the 20% virtual substrates, shown in figure 5.20. Both effects limits the accuracy relaxation measurement to approximately $\pm 0.5\%$.

In the previous chaper, annealing was shown to have minimal effect on the relaxation of strained silicon on 20% virtual substrates within the accuracy of the HRXRD scans (see figure 5.21). For the case of 50% virtual substrates, annealing is observed to significantly shift strained silicon peak positions of the thicker layers in reciprocal space. This is shown in figure 6.12, by comparing the RSMs of sample LG50-7 (70.7nm) in the as-grown state and after annealing at 850°C for 1hr. The diffuse nature of the strained silicon peak after annealing suggests a greatly increased dislocation content, which creates further inaccuracies in peak position determination, and increases the error in relaxation to around $\pm 2\%$.

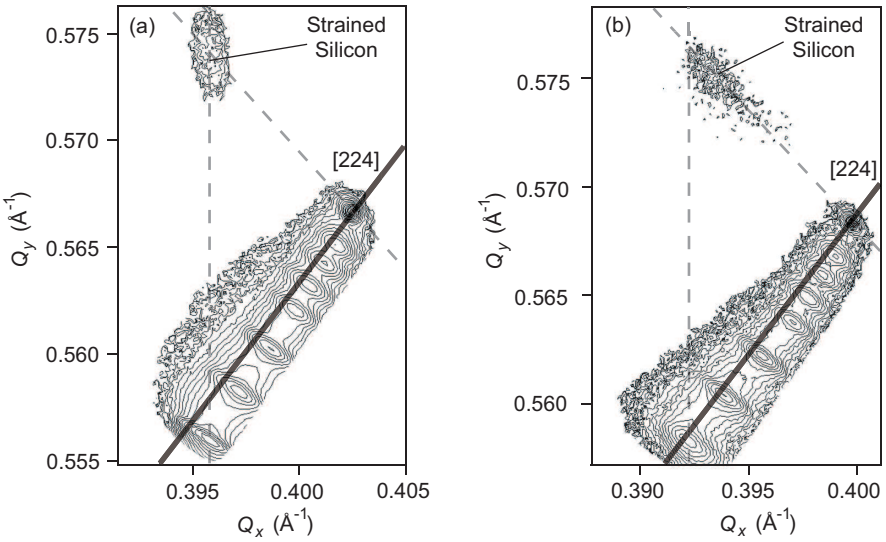

Figure 6.11: Simplified RSMs around the (224) reflection for (a) TG50-2 (18.5nm) of strained silicon and (b) TG50-6 (68.8nm), with the marked approximate position expected for a fully strained layer.

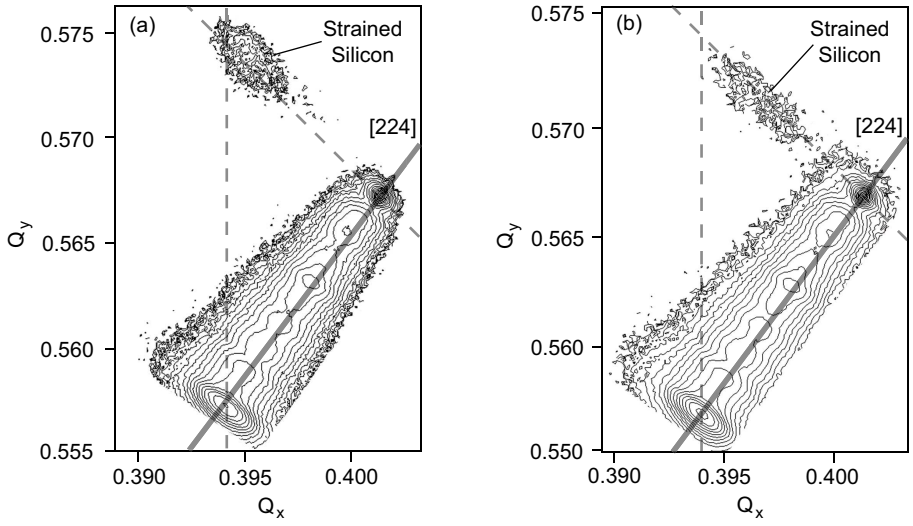

Figure 6.12: Simplified RSMs around the (224) reflection for sample LG50-7 (70.7nm) of strained silicon (a) in the as-grown state and (b) after annealing for 1hr at 850°C.

The relaxation of the linearly graded and terrace graded samples obtained by reciprocal space mapping are presented in figure 6.13. For the as-grown samples of both sets, relaxation remains at less than 2% up to a layer thickness of around 35nm (approximately 9 times the Matthews and Blakeslee critical thickness). In the previous chapter, a lower degree of relaxation was observed for the terrace graded samples, which was inferred to be due to their lower threading dislocation density and the dominance of glide in the relaxation process (see section 5.5). The measurement error associated with relaxation in figure 6.13, however, is larger than (or comparable to) any difference that may exist between the two sample sets.

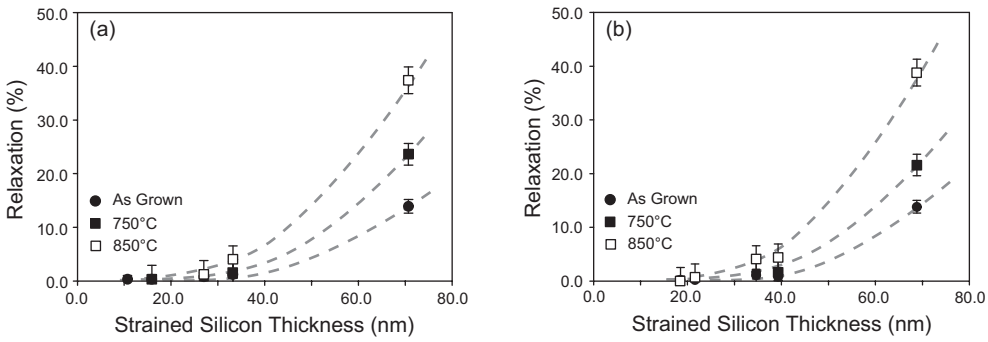

Figure 6.13: Graphs to show the relaxation of strained silicon on 50% virtual substrates which are (a) linearly graded and (b) terrace graded, as measured by HRXRD.

As the layer thickness increases to around 70nm, relaxation increases significantly to 14±1%. Annealing at 750°C and 850°C for 1hr increases the relaxation of these layers to 22±2% and 37±2%, respectively, whilst the thinner layers seem to remain unaffected. Between 30nm and 40nm, there is some indication that annealing induces a small increase in relaxation of around 3%, but the results for these layers are close to the error limits of the corresponding as-grown layers, limiting their validity.

6.4.3 Comparisons with Compressively Strained $Si_{0.5}Ge_{0.5}$

Tensile strained silicon layers on 20% virtual substrates were shown in the last chapter to be more stable to relaxation than compressively strained $Si_{0.8}Ge_{0.2}$ layers in other published works (see section 5.5.2). A similar comparison between the relaxation of strained silicon on 50% virtual substrates in figure 6.13 and the relaxation of $Si_{0.5}Ge_{0.5}$ suggests this is also true at higher degrees of strain.

At a growth temperature of 550°C using MBE, a 50nm thick $Si_{0.5}Ge_{0.5}$ layer was measured by an X-ray technique to be around 60% relaxed. This increased in a 120nm layer to over 95%, and at 250nm was almost 100% relaxed [Bean et al., 1984]. Using a different X-ray technique, a 45nm thick CVD grown layer of $Si_{0.41}Ge_{0.59}$ at an unknown temperature produced the comparable result of 71% relaxation [Bugiel and Zaumseil, 1993]. Relaxation was observed to occur in these two example cases by a combination of MFR multiplication and surface roughening in the form of 3-dimensional island formation (see section 2.2.2). 3-dimensional island formations have not been observed for strained silicon within the range of layer thickness used in this study (see figure 6.9).

The relaxation of strained silicon on 50% virtual substrates up to a thickness of 35nm behaves in a similar fashion to that of the 20% virtual substrates up to 180nm (see figure 5.21), in which relaxation increases to a maximum which is less than 2%. Exceeding 35nm, however, leads to a significant increase in relaxation to around 14%, which is increases to approximately 37% after annealing at 850°C for 1hr. To understand what causes relaxation to remain low up to 35nm, and how it subsequently increase up to 70nm, the type of dislocations formed in the layers must be considered.

6.5 Dislocation Structures

6.5.1 Critical Thickness

It is important to obtain an empirical estimate of the critical thickness of each dislocation type in order to determine which types are predominant in the relaxation process as the layer thickness increases. TEM was used to detect the presence of each dislocation type across the thickness range of strained silicon, and the thinnest layer in which a given type was observed used as an estimate of critical thickness. Unfortunately the use of defect etching, which provides a much larger scale view, is limited. It does, however, provide a useful qualitative view of dislocation interactions, and will be considered in section 6.5.2.

Critical Thickness of 60° Misfit Dislocations and Stacking Faults

The thinnest layers of either sample set in which dislocations are observed using PVTEM and XTEM are the 8.2nm (LG50-2) and 9.4nm (TG50-1) layers, which suggests that the critical thickness for the glide of pre-existing dislocations lies between approximately 6nm and 8nm. Stacking faults are also observed in these layers, as shown in figure 6.14, and so the estimated critical thickness for their formation is comparable to that at which dislocation glide is initiated.

For strained silicon on 50% virtual substrates, theoretical predictions based on the Matthews and Blakeslee equations predict a critical thickness for 60° dislocation glide of approximately 4nm (see figure 2.15), and a critical thickness for stacking fault formation of approximately 3nm (see figure 5.17). Both predictions are lower than the estimates obtained using TEM, but are comparable in thickness, which shows (together with the analysis for 20% virtual substrates in section 5.3.4) that calculations based on

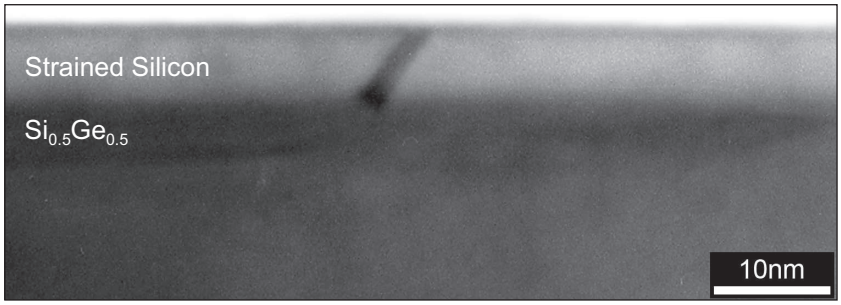

Figure 6.14: XTEM image of a 8.2nm strained silicon layer (LG50-2), showing the presence of a stacking fault.

the equations of Matthews and Blakeslee serve only as qualitative approximations.

It should also be noted, however, that TEM is generally a small scale technique in which dislocation structures must be of sufficient density to be observable. This can lead to overestimations when used in this way to determine critical thickness. Further work, employing more sensitive techniques across samples which are more continuous in strained silicon layer thickness is needed to determine more accurate values.

Critical Thickness of Microtwins

Microtwins are first observed in the two sample sets at a thickness of 33.2nm (LG50-6) and 34.6nm (TG50-4), as shown in figure 6.15. This gives an approximate critical thickness of between 27nm and 35nm. A simplified theoretical estimate for the critical thickness at which microtwin nucleation is expected to occur (see figure 5.19) predicts a value of 28nm for strained silicon on a 50% virtual substrate.

Whilst the predicted and experimentally determined values are consistent, the thickness of strained silicon in both sample sets are not sufficiently continuous, and accuracy is limited to around 6nm. Again the estimated critical thickness using TEM may be higher than if a more sensitive technique were employed.

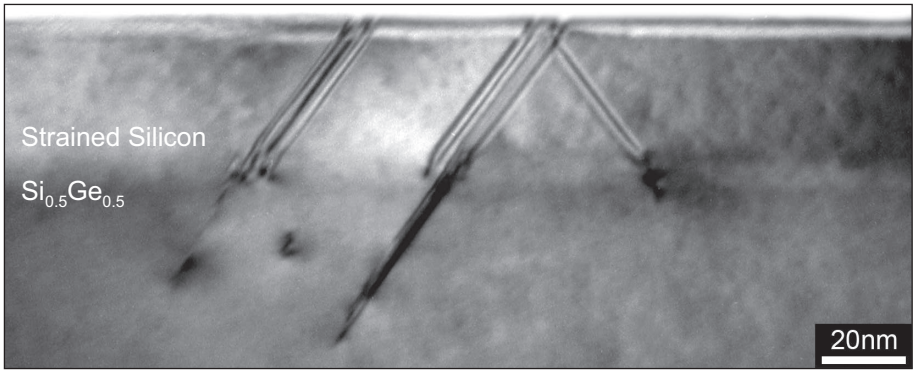

Figure 6.15: XTEM image of a 33.2nm strained silicon layer (LG50-6), showing the presence of a microtwin.

6.5.2 Dislocation Interactions

In the previous chapter, defect etching was used to show that relaxation is dictated by the predominant dislocation types and their interaction at a given thickness (see section 5.6). Unfortunately, the use of defect etching is limited for strained silicon on 50% virtual substrates due to reduced undercutting (discussed in section 4.2.3) and increased surface roughness compared to 20% virtual substrates. However, defect etching still provides a useful large scale view of dislocation formations and their interactions in the as-grown samples which is non-quantitative.

Relaxation of As-Grown Samples

The thinnest layer for which dislocations are revealed is 21.6nm (TG50-3), as shown in figure 6.16 (a) after a 10s exposure to the etchant. Thinner layers do not reveal dislocations even with shorter exposures, and it is assumed that etch pits formed with thinner layers are not deep enough to produce sufficient contrast in the DIC microscope. The line features revealed in figure 6.16 (a) are only faintly observable (two of which are

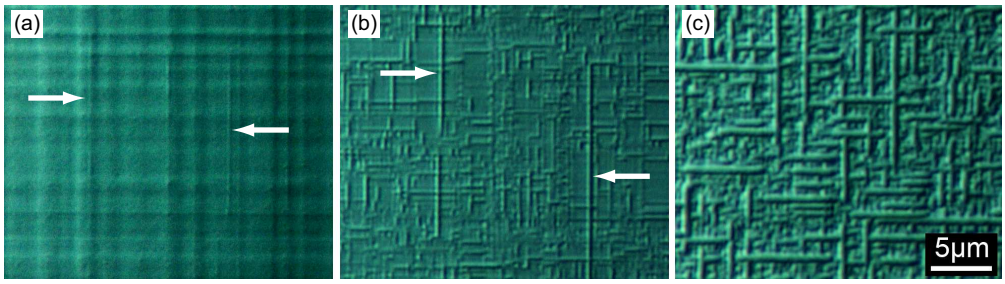

Figure 6.16: Images obtained after exposure to dilute Schimmel etchant using the DIC microscope, for (a) 21.6nm of strained silicon (TG50-3), with two faint dislocation features indicated, (b) 34.6nm (TG50-4), with two possible microtwins indicated, and (c) 68.8nm (TG50-6).

indicated), and there is no distinction between dislocation types, even though critical thickness estimates using TEM suggest that both misfit dislocations and stacking faults should be present. Accurate determination of relaxation therefore cannot be otained using defect etching, but an upper limit of 0.34±0.02% can be estimated by assuming all features are 60° misfit dislocations (using equation 5.1). This figure is consistent with the HRXRD results given in figure 6.13. Observation of etch pits formed at only the leading edge of dislocations suggest that 60° half-loop nucleation has not occurred, which is predicted at around 16nm.

Figure 6.16 (b) shows an increased density of line features in 34.6nm of strained silicon (TG50-4), such that individual line separation is of the order of hundreds of nanometers. The majority of features display stacking fault characteristics, as they appear unable to cross each other (see figure 5.10 (b)). A lower density of broader line features are also evident, which are possibly attributable to microtwins (two of which are indicated). Using the assumption that all the finer linear features revealed are stacking faults, relaxation is estimated using equation 5.1 to be around 1.8±0.1%.

At a thickness of 68.8nm (TG50-6), defect etching reveals the density of broader

features (which are assumed to be microtwins) to be greatly increased, as shown in figure 6.16 (c). TEM images, an example of which is presented in figure 6.17, confirm that large numbers of microtwin features are present in the thickest layers of both sample sets. Unlike stacking faults, the microtwin features in figure 6.16 (c) appear to be capable of crossing existing features to form much longer segments.

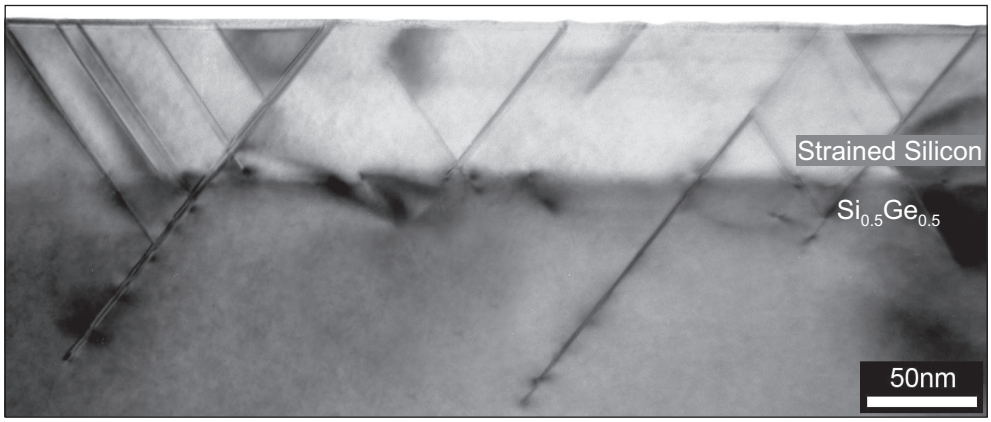

Figure 6.17: TEM image of a 70.7nm layer (LG50-7) obtained in the (220) diffraction condition.

The images presented in figure 6.16 cannot be used for the quantitative analysis of dislocation interactions, which was undertaken in the section 5.6. Individual dislocations cannot be resolved and tracked sufficiently, and there is limited distinction between dislocation types. However, such images can be used to qualitatively explain why relaxation is less than 2% in layers thinner than 35nm, as shown in figure figure 6.13, and how it increases to around 14% at 70nm in the as-grown state.

The low density of microtwins revealed for the 34.6nm strained silicon layer in figure 6.16 (b) infers that all layers thinner than 35nm are relaxed predominantly by glide. Therefore, relaxation in these layers is limited due to dislocation pinning, and the effectiveness with which extended stacking faults inhibit glide. Dislocation line segments

revealed in figure 6.16 (b) appear (on average) to be much shorter than those of the 21.6nm layer in figure 6.16 (a). This is a consequence of the inability of extended stacking faults to cross each other, which was noted in section 5.6, so their high density within the layer limits glide and relaxation does not exceed 2%. This is similar to the behaviour of 180nm layers of strained silicon on 20% virtual substrates, in which the predominant dislocation structures were impeded stacking faults, and microtwin nucleation was limited (see figure 5.10).

In the 68.8nm layer shown 6.16 (c), dislocation glide is supplanted by nucleation in the form of large densities of deeply-penetrating microtwins, which are also shown by XTEM in figure 6.17. Relaxation in these layers is no longer limited by dislocation pinning and the glide of pre-existing dislocations. Microtwins appear able to form in long segments which cross existing stacking faults, and relaxation is increased significantly to around 14%.

Subsequent increases in relaxation with annealing cannot be studied by using defect etching, as the associated increase in dislocation density produces DIC images which are not interpretable. Examination of the dislocation structures using XTEM provides a clearer picture of how such relaxation is achieved.

Relaxation Induced by Annealing

HRXRD measurements in figure 6.13 show that annealing has a significant effect on the relaxation of only the thickest layers (around 70nm) in both sample sets. An example XTEM image of a 70.7nm strained silicon layer (LG50-7) after annealing for 1hr at 850°C, presented in figure 6.18, shows that microtwins and stacking faults have formed in the strained silicon layer in the same fashion as the as-grown layer in figure 6.17. The dark features present at the misfit interface, which did not appear in the as-grown

images, are due to a large number of dislocations running into the plane of the image. Additional dislocations are also observed to be injected into the virtual substrate.

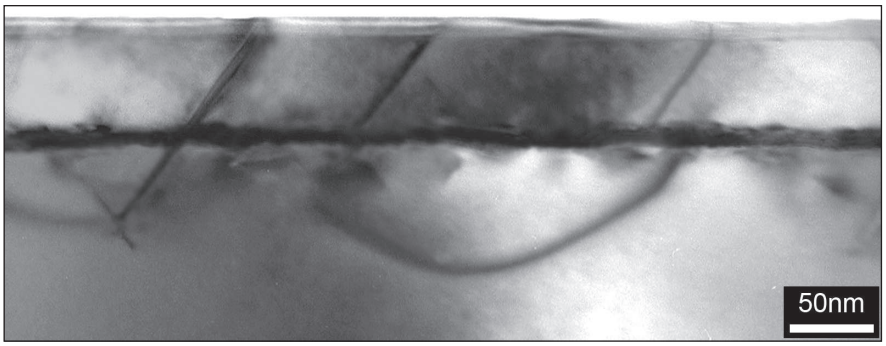

Figure 6.18: TEM image of a 70.7nm layer (LG50-7) obtained in the (220) diffraction condition after annealing for 1hr at 850°C.

Dislocations injection into the substrate of $Si_{1-x}Ge_x$ strained layer epitaxy is generally associated with multiplication of 60° dislocations through the MFR mechanism (shown schematically in figure 2.18, and by example in figure 5.27). The dislocation features in figure 6.18 do not display the fringing patterns associated with partial dislocations, or the dependence on orthogonal $\{220\}$ diffraction conditions which are indicative of 90° dislocations. This suggest they are 60° dislocations, and such features are most likely produced by the early stages of the MFR mechanism.

The increased level of relaxation due to annealing also has an effect on the surface morphology of the thickest layers. This is shown by the two $5\mu m^2$ deflection maps presented in figure 6.19, which are taken from sample LG50-7 (70.7nm of strained silicon) before and after annealing at 850°C for 1hr. The small surface step striations formed in the as-grown state are due to stacking faults and microtwins. Before annealing the RMS and Z-range surface roughness are measured to be 8.3±0.8nm and 56±7nm, respectively (see figure 6.9), and are 8.6±0.7nm and 55±8nm after annealing.

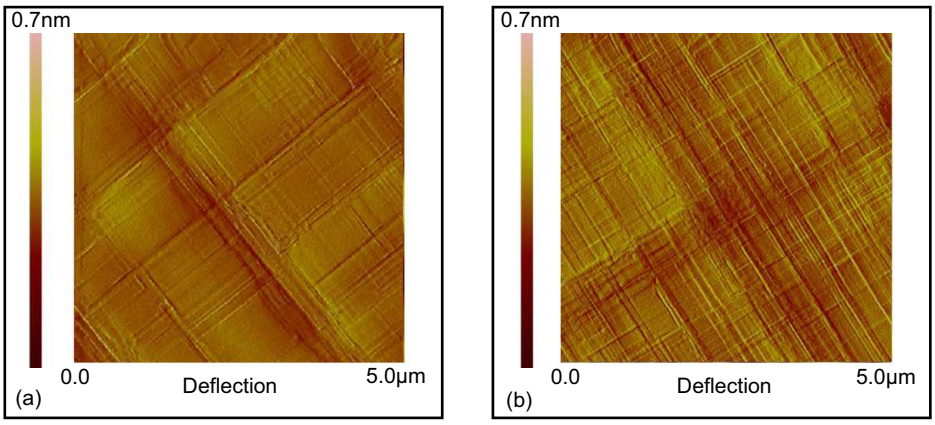

Figure 6.19: AFM deflection map images obtained from a 5μm^2 area scan of sample LG50-7 (70.7nm of strained silicon) (a) before annealing and (b) after annealing at 850°C for 1hr.

Additional striations formed in figure 6.19 after annealing are due to the possible onset of multiplication observed in figure 6.18. Comparison between XTEM images taken before and after annealing at 850°C for 1hr of this layer (such as those of figures 6.17 and 6.18), do not typically show an increase in the number of microtwins or stacking faults after annealing. The presence of multiplication sources rather than increased nucleation therefore may be responsible for the increase in relaxation observed after annealing in the thickest layers. Relaxation of compressively strained $Si_{0.5}Ge_{0.5}$ favours the MFR multiplication mechanism, through which much higher degrees of relaxation are achieved (see section 6.4.3).

The apparent appearance of multiplication may not be due solely to the addition of thermal energy during annealing. Both bulk silicon and germanium experience expansions of their lattice constants at high temperatures, but bulk germanium generally expands by a larger degree. Additional strain can therefore be induced into a layer of strained silicon due to the mismatch in linear thermal expansions between silicon and

the underlying $Si_{1-z}Ge_x$ of the virtual substrate.

Thermal Expansion

The linear thermal expansion coefficients of bulk silicon, α_{Si}, and germanium, α_{Ge}, are shown in figure 6.20. As α_{Ge} is larger than α_{Si}, all $Si_{1-x}Ge_x$ alloys will also have a larger thermal expansion coefficient than α_{Si}, which can be estimated by interpolation. At high temperatures the lattice constant at the surface of a virtual substrate will expand more than a strained silicon overlayer, inducing more strain than at room temperature.

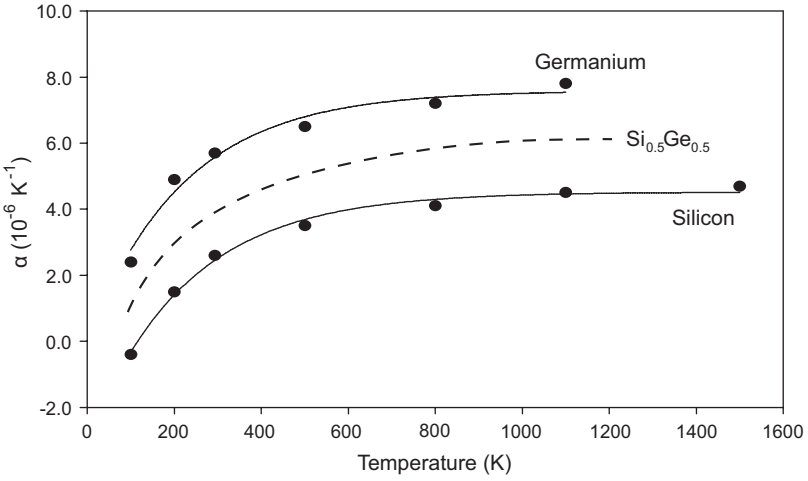

Figure 6.20: Graph to show the variation of thermal expansion coefficients with temperature for bulk silicon and germanium, taken from Kaye and Laby [1995]. Also shown are interpolated expansion coefficients for $Si_{0.5}Ge_{0.5}$.

If L is any lattice constant, its expansion, δL, along one dimension due to a change in temperature, δT, can be approximated by:

$$\delta L = \alpha L(\delta T) \tag{6.1}$$

The difference in the expansion of the lattice constants of $Si_{1-x}Ge_x$ (a_{SiGe}) and

silicon (a_{Si}), ΔL, will cause an additional strain to be imposed on the silicon layer. This strain can reinterpreted as an effective increase in the germanium composition of the virtual substrate, Δx, which would be required to achieve the same level of strain in a silicon overlayer. This can be determined by substituting equaton 6.1 into equation 2.1:

$$\Delta x = \left(\frac{(a_{SiGe} + \Delta L) - a_{Si}}{a_{Ge} - a_{Si}} \right) - x \tag{6.2}$$

Values for Δx over a range of temperatures presented in table 6.5 shows that 20% virtual substrates induce an effective strain increase of only 2.1% germanium at the growth temperature of 700°C, which increases to 2.5% at 850°C. This was neglected in the previous chapter, as the germanium composition variation between samples in tables 5.1 and 5.2 is comparable at 1.9%.

Temperature (°C)	Δx for $Si_{0.8}Ge_{0.2}$ (%)	Δx for $Si_{0.5}Ge_{0.5}$ (%)
700	2.07	5.21
750	2.22	5.59
850	2.53	6.35
950	2.83	7.12

Table 6.5: Strain increase in strained silicon due to thermal expansion, presented as an effective germanium increase (Δx) of the virtual substrate.

More detailed works have cited thermal expansion of 20% virtual substrates as a possible explanation for slight variations in strain measured in silicon at higher temperatures, where its effect becomes more significant [Samavedam et al., 1999]. Additional strain may also result from sample heating and cooling rates before and after annealing, due to the differing thermal conductivities of silicon and germanium [Kaye and Laby, 1995]. To minimise such effects, samples were heated prior to entry into the furnace for 10min, and cooled upon exit for a further 10min (see sections 5.3.1 and 6.4.1).

50% virtual substrates increase the strain in a silicon overlayer equivalent to an additional 5.2% germanium at the growth temperature of 700°C, and 6.4% at 850°C. The difference between the growth and annealing temperatures is only around 1% effective germanium increase, but strained silicon layers are maintained at an elevated strain for much longer during annealing than during growth (at a growth rate of 4.50nm min^{-1} for silane, 70nm of strained silicon spends just over 15min at 700°C, while during annealing it spends 60min at 750°C or 850°C).

Annealing could therefore be responsible for increasing relaxation through the MFR multiplication mechanism not by an increased thermal energy, but by the associated increase in strain due to expansion.

6.6 Summary

A linear graded and terrace graded 50% virtual substrate design were used to determine how the relaxation of overgrown strained silicon depends on surface roughness, and the densities of threading dislocations and pile-ups. Three terrace graded designs were considered, which varied the number of terraces and their intermediate grading rates. Within the range of variation of these designs it was found that increasing the number of terraces produced an increase in the threading dislocation density, but also a smoother surface. Increasing the grading rate between the higher germanium composition layers was observed to have no appreciable effect on the threading dislocation density, for the chosen rates. In comparison with the basic linearly graded design, all three terrace graded designs possessed a lower degree of surface roughness, and a comparable or lower threading dislocation density. Pile-ups of threading dislocations were not observed on any of the terrace graded samples, which indicates that terrace grading up to 50% has the ability to lower the density of pile-ups (as it did at 20%) within the range of variation

imposed by this study.

Strained silicon layers of variable thickness up 70nm (around 18 times the critical thickness) were grown on the linearly graded and chosen terrace graded virtual substrate designs, making two different sample sets. Relaxation of the strained silicon was quantified using HRXRD, the results of which showed no measurable difference in the relaxation of strained silicon between the two sets. For the 20% virtual substrate designs of the previous chapter, lower relaxation was measured for the terrace graded design, and attributed to the lower threading dislocation density providing less threading dislocations for glide. For the 50% virtual substrates, however, increased surface roughness and misfit dislocation content led to a higher measurement error which was greater than any measurable differences.

Relaxation was observed to remain at less than 2% up to a thickness of about 35nm. Examination of the dislocation structures using TEM and defect etching showed these layers to be relaxed predominantly by dislocations formed by glide (60° misfit dislocations and stacking faults). In the previous chapter it was shown that strained silicon layers on 20% virtual substrates which are relaxed by glide display a limited degree of relaxation due to dislocation pinning, particularly by extended stacking faults. For 50% virtual substrates, stacking faults were observed to form in strained silicon layers of around 8nm in thickness, and defect etching showed their density to become the predominant dislocation type in layers thicker than 22nm (with a low density of nucleated microtwins). It was concluded therefore that relaxation was limited in layers thinner than 35nm by the impediment to dislocation glide provided by stacking faults, enhancing stability above that of compressively strained $Si_{0.5}Ge_{0.5}$ observed in other works. Even though relaxation is low, the density of stacking faults within the strained silicon makes such layers unsuitable for the fabrication of electronic devices.

At 70nm, relaxation was measured to increase significantly to around 14% due to the nucleation of microtwins, which were shown to comprise a significant proportion of the total dislocation population. Annealing at 750°C and 850°C for 1hr further increased the degree of relaxation to approximately 22% and 37%, respectively, and had almost no observable effect (within experimental limitations) on the relaxation of thinner layers. TEM and AFM observations suggested that additional relaxation is achieved mostly through dislocation multiplication in these thicker layers, rather than purely increased microtwin nucleation events. The possible onset of multiplication may not be simply due to the increased thermal energy available to dislocations during annealing, as it was shown that annealing can lead to increased strain due the differing thermal expansion coefficients of silicon and the underlying virtual substrate.

Chapter 7

Conclusion and Further Work

In this work, the relaxation of silicon subjected to strain imparted by 20% and 50% virtual substrates has been quantified, and the results interpreted by examination of dislocation interactions. A defect etching technique was employed for the observation of dislocations and their interactions over large areas. The extent of applicability of a dilute Schimmel etchant for this purpose was extensively studied, and its etch rate determined as a function of germanium composition. It was found that strained silicon enhances the ability to reveal threading dislocations from a 20% virtual substrate due to undercutting, which is consequence of the different etch rates of silicon and $Si_{0.8}Ge_{0.2}$. Unfortunately, this ability is limited for 50% virtual substrates as the difference between the etch rates of silicon and $Si_{0.5}Ge_{0.5}$ is smaller. The range of germanium compositions of the virtual substrate for which undercutting occurs has not been fully explored, and remains open for the possibility of further research.

The enhancement to revealing dislocations afforded by strained silicon proved to be useful in the rest of the work for studying relaxation and dislocation interactions. However, a number of questions surrounding defect etching remain unanswered. The

exact mechanisms behind the etching process are not well understood, and the observed dependence of etch rate on germanium composition highlights the need for a clearer understanding. This work is also limited to the use of a particular dilute Schimmel etchant at room temperature, and further work would be required to determine the suitability of other etchants, or cooling of the existing process, to provide greater selectivity over a wider range of compositions.

The relaxation of strained silicon layers many times the critical thickness on 20% and 50% virtual substrates have been measured using HRXRD. These results show relaxation to be less than 2% for both virtual substrates compositions when dislocation glide is the predominant relaxation mechanism. Such layers maintain a high degree of stability, even during annealing at 850°C for 1hr. Comparisons were made between the relaxation of strained silicon on linearly graded and terrace graded virtual substrate designs. For the 20% virtual substrates, the thickest strained silicon layers (180nm) displayed a lower level of relaxation on the terrace graded design than a comparable layer on the linearly graded design. This was suggested to be a consequence of the lower threading dislocation density of the terrace graded design, both in isolation and in pile-ups. No such differences were observed between the 50% linearly graded and terrace graded designs, but this was attributable to the lower accuracy of the HRXRD technique due to surface roughness and dislocation content.

The relaxation of tensile strained silicon at the levels of strain imposed by 20% and 50% virtual substrates is much lower than previously published works for compressively strained $Si_{1-x}Ge_x$ under the same degree of strain. Examination of dislocation interactions in *post mortem* using defect etching has shown that in glide-limited layers, the low level of relaxation is due dislocation interactions which impede glide. For strained silicon on 20% virtual substrates, quantification of dislocation pinning suggested

that extended stacking faults (which form with a higher density in thicker layers) are more effective at impeding glide than misfit dislocations, and so were implicated as the primary source of stability. As extended stacking faults only occur when the strain is tensile, and not when it is compressive, their presence results in a low level of relaxation ($<$2%). This reasoning was extended to glide-limited layers on 50% virtual substrates, but it could not be studied in detail due to the limitations of defect etching.

The increased probability of pinning arrising from the interaction between stacking faults and gliding dislocations has not been shown on a theoretical basis. Formulation of such a model (conducted as additional work) could be used in addition to the Freund model for 60° pinning interactions to obtain a fuller understanding of dislocation pinning, and ultimately a quantifiable model for the relaxation of tensile strained layers. Future studies could also determine whether these general conclusions apply to tensile strained $Si_{1-x}Ge_x$, and strained silicon on insulator platforms.

Increased levels of relaxation were observed in strained silicon layers that are thick enough for dislocation nucleation or multiplication to occur. This was achieved for strained silicon layers on 50% virtual substrates, in which a high density of microtwins nucleated at a thickness of around 70nm (18 times the critical thickness) and increased relaxation to 14%. Subsequent annealing of these layers at 850°C for 1hr indicated the possible onset of MFR multiplication, although this may be due to additional strain during annealing arising from different the thermal expansions of strained silicon and $Si_{1-x}Ge_x$. For the 20% virtual substrates only limited microtwin nucleation events were observed at 180nm (14 times the critical thickness) which were of too low a density to increase relaxation above that achieved by glide alone. Annealing was observed to have no effect on the relaxation of these layers.

Two mathematical models were formulated in this work for the estimation of

the thickness at which extended stacking faults and microtwins form. The critical thickness for extended stacking faults was obtained from the equations of Matthews and Blakeslee, and the critical thickness for microtwins was based on the equations of People and Bean. Both models are simplified cases, and do not incorporate several physical properties which effect how either dislocation types is physically formed. The possibility for further refinement to these models remains, as does the investigation of their predictive ability over a wider range of degrees of strain than presented here.

All virtual substrate designs and strained silicon layers were grown with the same precursor gases, and within the same temperature range. This allowed meaningful comparisons to be drawn between results obtained at both levels of strain, but it leaves a large amount of scope for future investigations concerning the dependence of relaxation on growth temperature. Of particular interest would be the pursuit of low temperature growths for the silicon layers, and how they relax under annealing conditions. Different growth conditions may also allow thicker strained silicon layers than considered in this work to be grown and studied, with the possible elimination of particulate contamination. With careful selection of growth conditions, it may be possible to resolve the issue raised in this work over the dependence of the surface roughness roughness of strained silicon on the layer thickness, and whether it is due to initial growth conditions. Designs considered for the 50% terrace graded virtual substrates also leave a large number of parameters unexplored. It was shown that increasing the number of terraces can be detrimental to various qualities, and that increases in grading rate had a negligible effect on such qualities. However, these studies were limited, as their purpose was to find a virtual substrate design which was improved over that of the simple linearly graded design, and the possibility of further investigation remains.

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