Silicon-based Nanodevices

European Network of Excellence
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SINANO NEWSLETTER

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EDITORIAL

The SINANO Network of Excellence aims to strengthen European scientific and technological excellence in the field of electronics, Si-based nanodevices for terascale integrated circuits (ICs). Over the next quarter century considerable challenges exist to push the limits of silicon integration down to nanometric dimensions. These are addressed by integration, at the European level, of the individually excellent research capabilities already existing in main universities and national research centers.
SINANO has also carried out a structuration of a network of small-scale, highly flexible fabrication and characterization platforms open to the partners, which is complementary to the pre-industrial or industrial ones. These platforms are used for rapid prototyping, test and validation of very innovative material and device ideas for long term nanoelectronics applications.

SINANO's activities, with long-term and multidisciplinary objectives, could herald a revolution in IC technology, involving integration of nanoscale CMOS and emerging post-CMOS logic and memory devices (single electron and quantum nanodevices).
Within SINANO, researchers work to enhance device performance and integration, to meet the ever increasing demands of communications and computing. The network includes partners with expertise required in developing these advanced devices, from basic materials science through design and nanofabrication to characterisation and device physics and modelling.

Launched in January 2004, SINANO gathers 44 partners with about 300 researchers and PhDs coming form 16 European countries. This represents an unprecedented collaboration in the field of Nanoelectronics devices in Europe.
SINANO has established a strong collaborative partnership between the scientific and the industrial communities. These co-operations lead to a strong European structuring and will allow speeding up technological innovation in the Nanoelectronics area in order to underpin the European economy over the coming decades.

Although it is a young Network, started 18 months ago, SINANO has already produced significant results. All the following activities will lead to a lasting association of the Network.

SCIENTIFIC RESULTS

In SINANO, many new materials and innovating architectures are studied for Si-based CMOS and beyond-CMOS nanodevices integration. A strong effort is also devoted to the understanding and modelling of the physical and electrical properties of these nanoscale structures.

Research undertaken within SINANO has already produced significant results

Several joint projects have led to many very interesting results. Exploitable knowledge has been notably produced in the following areas:

New materials:

- New high-k gate insulator (HfO2, ZrO2, AL2O3…) and gate electrode (Ni, TiN, Al, Mo, NiAlN, W, NiSi…) materials
- Method for producing strain relaxed layers and strained silicon layers using ion implantation
- New virtual substrates with ultrathin highly relaxed SiGe buffers
- Tuning of Schottky barrier height by ion implantation

New fabrication processes:

- Development of step&repeat nanoimprint technique at low-pressure and room temperature
- New process for fabrication of SOI nanowires and nanodots
- Fabrication process for tunneling FETs

Development of new models and codes:

- Development of Monte-Carlo codes for the simulation of transport in NanoMOSFETs
- Simulation package for quantum mechanical description of NanoMOSFETS, SETs and QCAs
- Compact models for nanoscale devices

A strong partnership with the European industry

SINANO has established a strong partnership with industrial partners. In particular, a strong co-operation has been developed with the Integrated Project NanoCMOS, coordinated by STMicroelectronics.
Long term research activities, based on the expertise and excellence of the SINANO scientific community, are needed for proposing innovating materials and devices for the end of the International Technology Roadmap for Semiconductors. These results are transferred to the main European semiconductor companies, which will allow speeding up technological innovation in Nanoelectronics preparing the path for future industrial applications.

TRAINING ACTIVITIES

The training of researchers and students from partners of the network or outside is an important task of SINANO. More than a hundred weeks of exchange and training have been realized so far between the different partners.

Many SINANO members are also involved in the organization of summer schools. Thus, SINANO supports each year the International summer school on advanced microelectronics (MIGAS) and the European school on nanoscience/nanotechnology (ESONN) that are organized by the CNRS and the CEA in Grenoble and its surroundings.

1st SINANO modelling school

Besides, the 1st SINANO Device Modelling Summer School took place in Glasgow in August 2005. The aim of the Summer School was to further the knowledge of PhD students and postdoctoral researchers in the advanced modelling and simulation techniques amenable to conventional and novel nano-CMOS devices. It included discussion of device physics, and corresponding models, numerical techniques, programming and simulation tools. Each of the 5 days of the School was dedicated to one of the following topics:

- Classical (continuum) simulations with quantum corrections.
- Monte Carlo simulations.
- Quantum transport and simulations.
- Novel devices, device physics and their industrial prospects.
- Atomic scale device simulation and intrinsic parameter fluctuations.

Lecturers included Wolfgang Fichtner, Mark Lundstrom, Mario Ancona, Supriyo Datta, M. P. Anantram, John Barker, Carlo Jacoboni, Umberto Ravaioli, Enrico Sangiorgi, Bernd Meinerzhagen, Simon Deleonibus, Thomas Skotnicki, Ken Rim, Asen Asenov, Masami Hane, Phillipe Dollfus and Alex Schluger.
The school was organised by Asen asenov and Enrico Sangiorgi acting as co-director and Scot Roy acting as a Chairman of the local organising committee. It was sponsored by SINANO, but also EPSRC (UK), AMD and Scottish Enterprise. The School gathered more than 95 students from academia and industry from all over the world.
The 2nd edition will be hold in Bologna in August 2006.

DISSEMINATION

SINANO supports also other dissemination activities within its research fields. Since the beginning of the project more than 100 papers have been published in high level international Journals and many SINANO results have also been presented in the best international Conferences in this field (IEDM, ESSDERC …).

European events organized by SINANO Partners

SINANO contributes to the organisation of European and international events. Since January 2004, SINANO supported the following conferences and workshops:

- **5th and 6th European Workshop on ULtimate Integration of Silicon** (ULIS), Leuven, March 2004 (organized by IMEC) and Bologna, April 2005 (organized by ARCES)
- **Conference on Microelectronics, Microsystems and Nanotechnology** (MMN), Athens, November 2004 (organized by IMEL)
- **Workshop « Frontier of Nanoelectronics »**, Jülich, February 2005 (organized by Forschungszentrum Jülich)
- **15th edition of the Workshop « Modeling and simulation of electron devices »** (MSED), Pisa, June 2005 (organized by the University of Pisa)

In the framework of SINANO research activities, two workshops were also organized this year by IMEP-CNRS in Grenoble, France: the **1st Common Workshop between NANOCMOS Integrated Project and SINANO** (January 27-28 2005) and the **SINANO Workshop 2005 "Nanoscale CMOS and emerging post-CMOS logic and memory nanodevices"** (September 16 2005). About a hundred persons attended each one. The SINANO workshop took place just after the ESSDERC conference. The objective was to present the status and trends of CMOS and post-CMOS nanodevices for terascale ICs. The talks focused notably on the latest advances in strained silicon and SOI structures, carrier transport in ultra-thin SOI and FinFETs devices, as well as recent prospects in tunneling FETs, hybrid CMOS-nanowires, nanodots and carbon nanotube devices. The

following presentations were hold and can be downloaded from the SINANO website:

- "Transport in ultra-thin SOI devices", Ken Uchida (Toshiba)
- "Modeling approaches for Decananometer MOSFETs within SINANO", Luca Selmi (University of Udine)
- "Advancing Strained Silicon", Anthony O'Niell et al. (Newcastle University, KTH, Stuttgart University)
- "Novel Virtual Substrates for Strained SOI", Siegfried Mantl (Forschungszentrum Juelich)
- "FinFET: a mature multi-gate MOS technology? A wideband transistor simulation and characterization approach", Jean-Pierre Raskin et al. (UCL, IMEC, ISP Kiev)
- "Recent advances in metallic source/drain engineering", J. Knoch et al. (Forschungszentrum Juelich, IEMN, UCL)
- "Current Status and Trends of Nanoelectronic Devices", Yoshio Nishi (Stanford University)
- "Molecular/carbon nanotube electronics", Jimmy Xu (Brown University)
- "Hybrid CMOS-Nanowire circuit architectures for digital and analog applications", Adrian Ionescu (EPFL)
- "Complementary Tunneling-Transistors (TFET): Fabrication and Application down to the 65nm CMOS-node", M. Sterkel et al. (Technical University Munich)
- "Post-CMOS generation: the different modeling approaches developed within SINANO for nanotubes, nanodots and resonant tunneling devices", Philippe Dollfus (IEF)

FORTHCOMING EVENTS

- **ULIS 2006**, Minatec, Grenoble, April 2006 (organized by CEA-Leti)
- **7th Symposium Diagnostics and Yield**: Advanced Silicon Devices and Technologies for ULSI era, Warsaw, June 2006 (organized by WUT in Warsaw)
- **MIGAS 2006**, Grenoble, June 2006 (organized by CNRS)
- **ESONN 2006**, Grenoble, August-September 2006 (organized by CNRS)
- **SINANO Modelling School**, Bologna, August 2006 (organized by ARCES)
- **Workshop on Nanoscaled semiconductor-on-insulator technologies and devices**, Kiev, October 2006 (organized by the Institute of Semiconductor Physics in Kiev)

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